GETTING TO 32 Gb/S

A TUTORIAL ON VERY HIGH SPEED DIFFERENTIAL SIGNALING

Presented by: Speeding Edge

At

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Santa Clara, California

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ACKNOWLEDGEMENTS

- **This presentation would not be possible without the help of the following:**

- **John Zasio for skew measurements and loss validation**

- **Tom Dagostino for precisely measurements**

- **Scott McMorrow for data analysis and loss derivations**

- **Isola Laminates for making test board fabrication possible**

- **MEI for fabricating the test PCBs with great care**
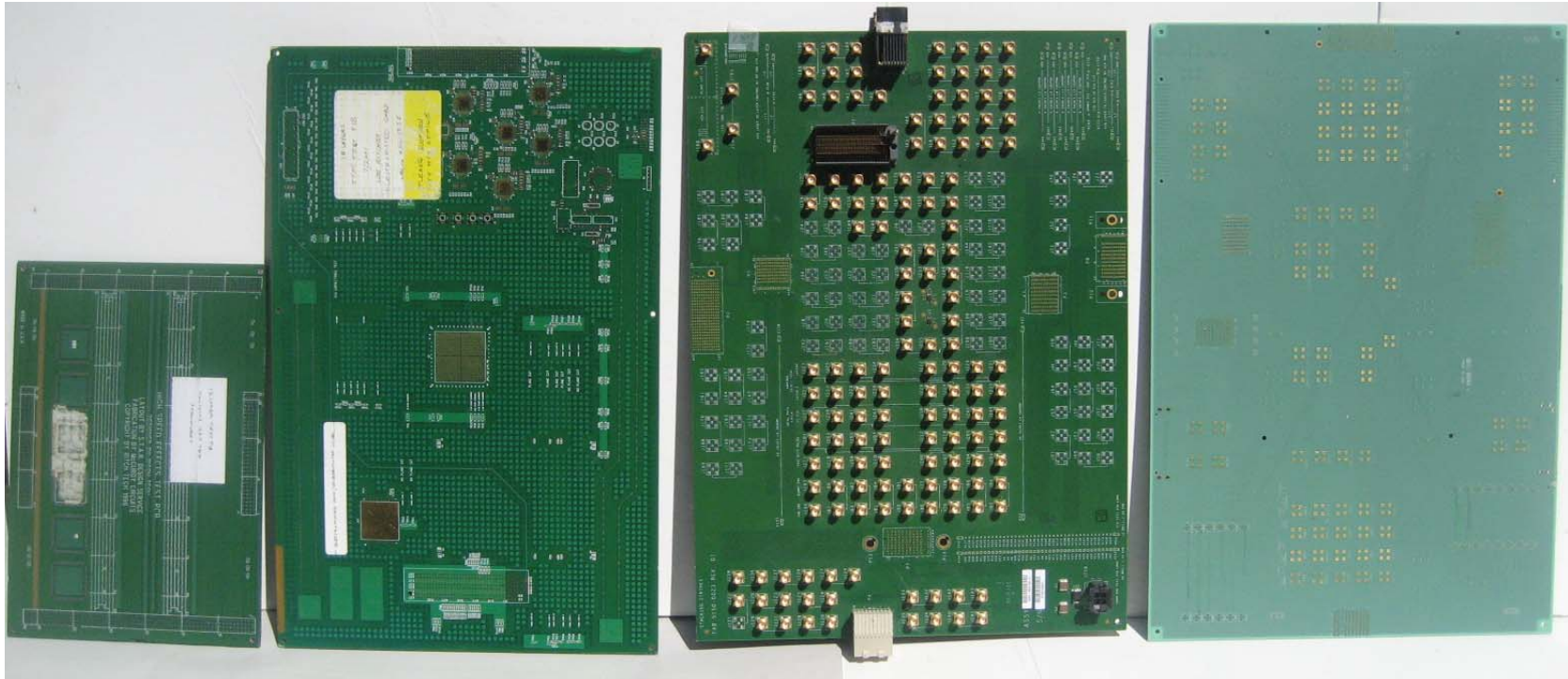
COURSE OBJECTIVES

- **Examine how differential pairs operate.**

- **Determine channel bandwidth needed by differential pairs and discuss power delivery system (PDS) requirements.**

- **Examine sources of degradation in differential pair channels.**

- **Examine materials available to fabricate differential pair channels.**

- **Examine connectors available for differential pair channels.**

- **Construct a set of design rules for high speed differential pairs.**

- **Determine documentation required to properly specify high performance PCBs.**

VALIDATING RULES AND MEASUREMENTS

- A common problem facing design engineers is finding a way to validate rules and simulations prior to creating a final set of design rules.

- Often, design requirements force engineers to make decisions based on   claims made by others who represent themselves as experts whose advice should be followed without proof that it is accurate or needed for a particular situation.

- In order to minimize the uncertainty that the above cases represent, we have constructed more than 30 test PCBs to determine materials properties and the effects of structures such as vias and right angle bends.

- The test PCB set on the next slide is an example of test PCBs used in this course.

SOME TEST PCBs USED TO VALIDATE RULES

1996	1999	2003	2005
100 MHz	2.4 Gb/S	4.8 Gb/S	5.2 Gb/S
14 Layers	18 Layers	16 Layers	20 Layers
"FR4"	Nelco 4000-13SI	Nelco 4000-13SI	FR408

RITCHEY'S SIMULATION RULE

UNVALIDATED SIMULATIONS ARE WORTH THE PAPER THEY ARE WRITTEN ON

DIFFERENTIAL PAIRS

DEFINITION - A differential pair is two transmission lines that have equal and opposite polarity signals traveling on them. These signals are tightly timed to each other. This is all they have in common.

Differential pairs terminate on differential receivers designed to ignore common mode signals. Receivers and transmitters may be a transformers.

Differential signaling has emerged as the best method for transmitting data at very high rates, such as OC48 and GBEN.

The Ethernet as we know it would not exist without differential signaling.

NOTE: All differential circuits exploit the <u>voltage difference</u> between the two wires. That is the reason for the description differential, not the differential impedance between them or the absolute magnitude of either signal.

TYPES OF DIFFERENTIAL PAIRS

- **ECL long line drivers and receivers**

- **Biphase clock distribution systems (TTL)**

- **LVDS (Low Voltage Differential Signals)**

- **Infiniband**

- **PCI Express**

- **10BT and 100BT Ethernet phone lines (Transformer coupled)**

- **All of the new high speed data links.**

Ritchey, Lee W, "A Treatment of Differential Signaling and Its Design Requirements" Speeding Edge, May 29, 2008.

PROPERTIES OF DIFFERENTIAL PAIRS THAT WARRANT USING THEM:

- **Capable of dealing with ground offsets between boxes or signal path ends. *****

- **Capable of dealing with signal degradation over long lines. Some new transceivers can tolerate 38 db of attenuation along the path!*****

- **In PCBs, side by side routing can result in increased crosstalk, not common mode rejection as is often conjectured. This is a misconception about diff pairs.**

*** Principal reasons for use

A TYPICAL ECL DIFFERENTIAL PAIR CIRCUIT
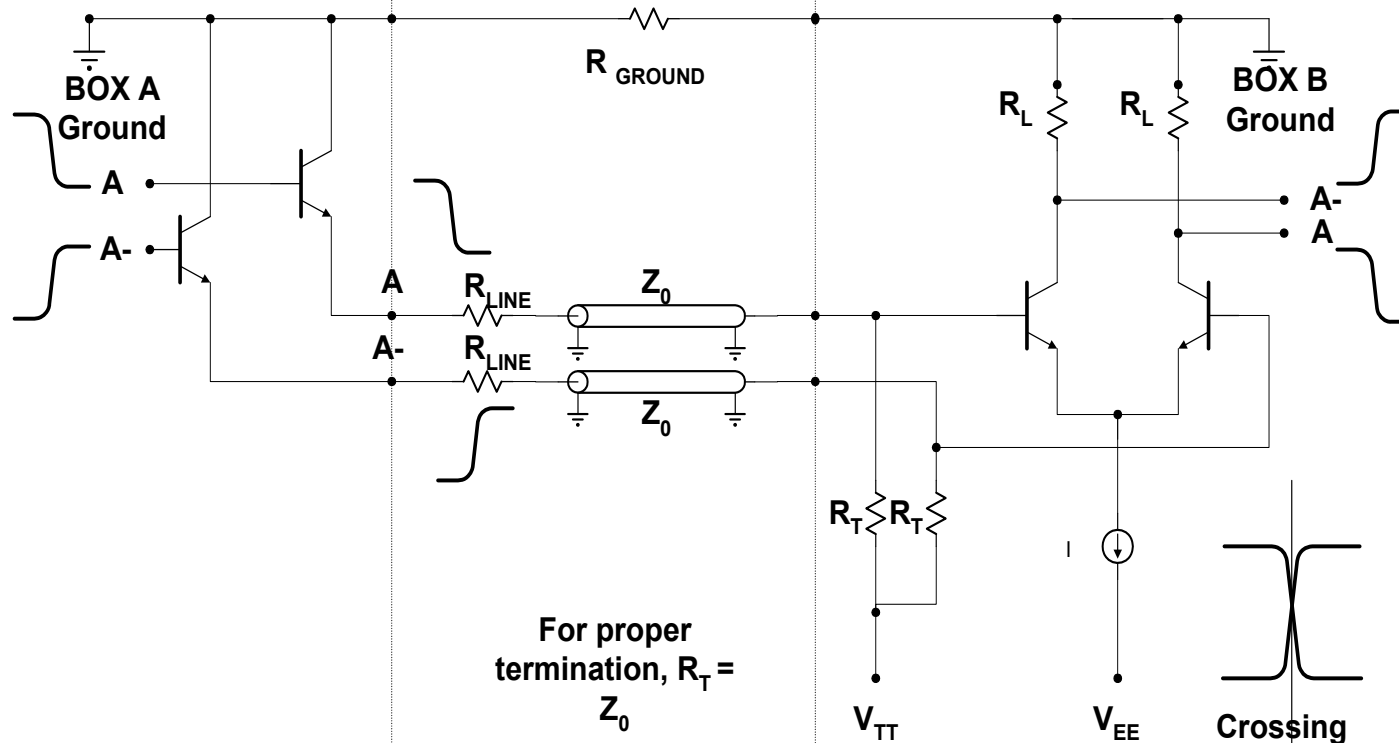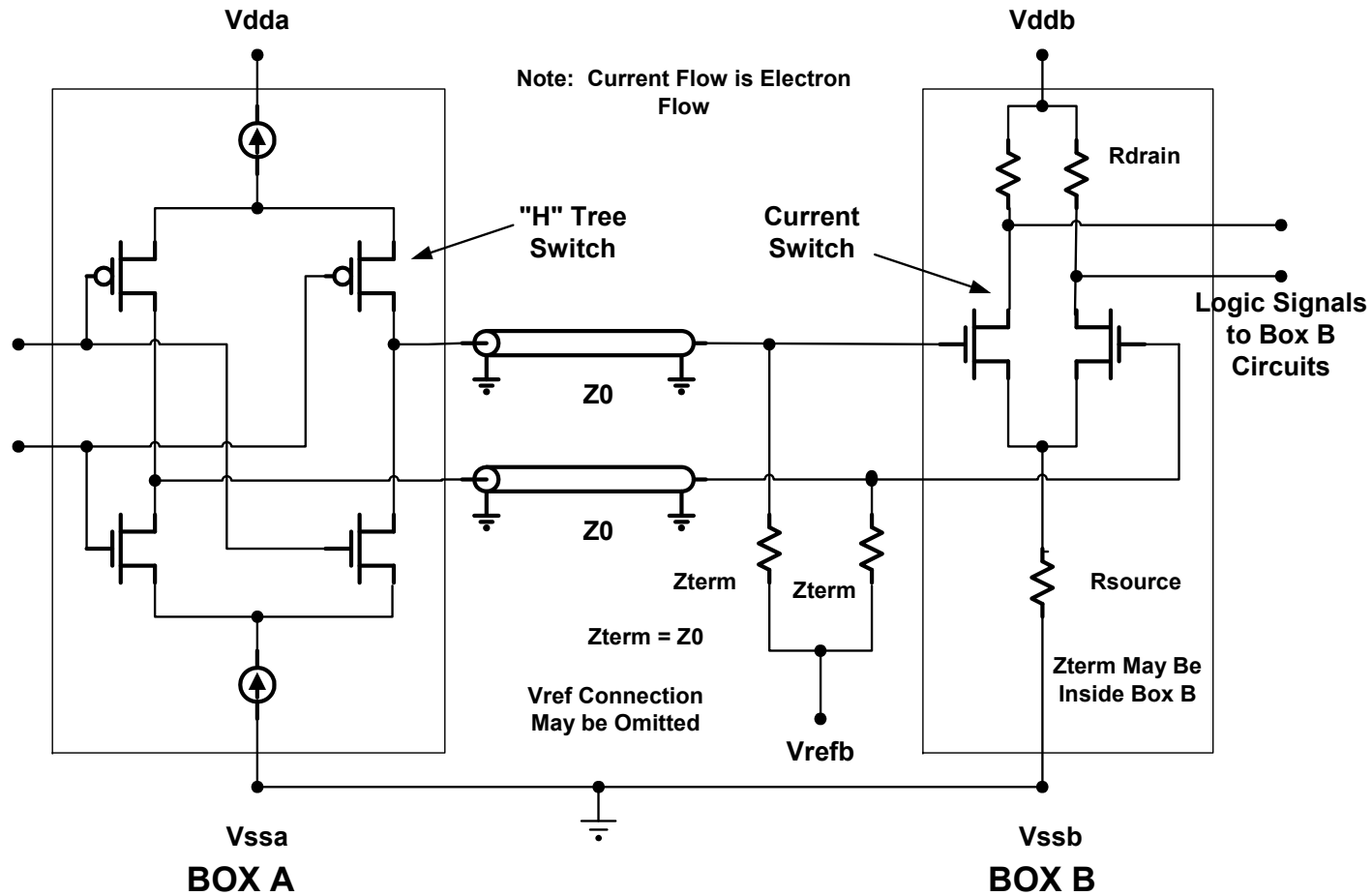

For proper termination, $R_T = Z_0$
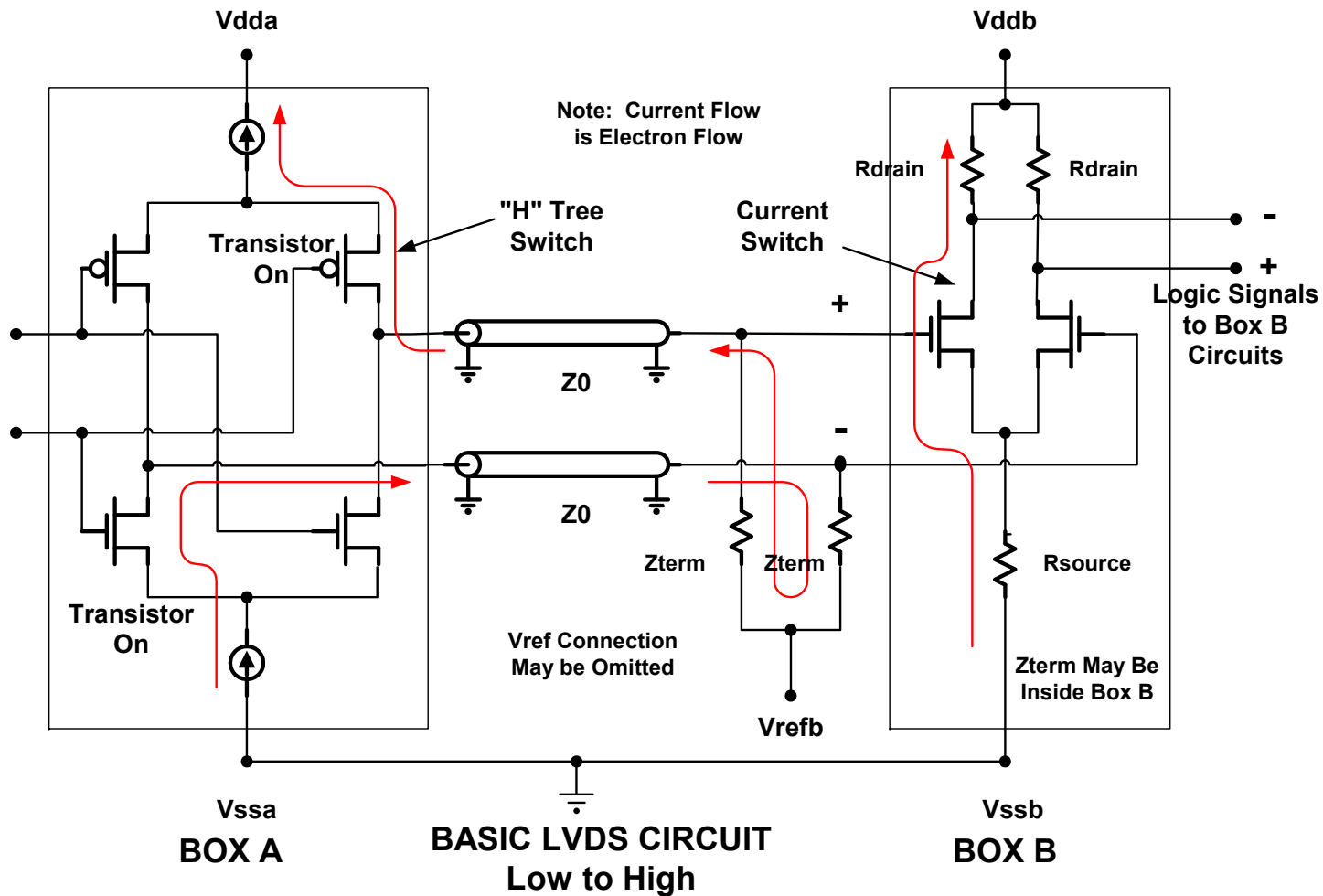
BOX A

Interconnecting Circuitry

BOX B

There are three choices of how to terminate this ECL Diff pair.
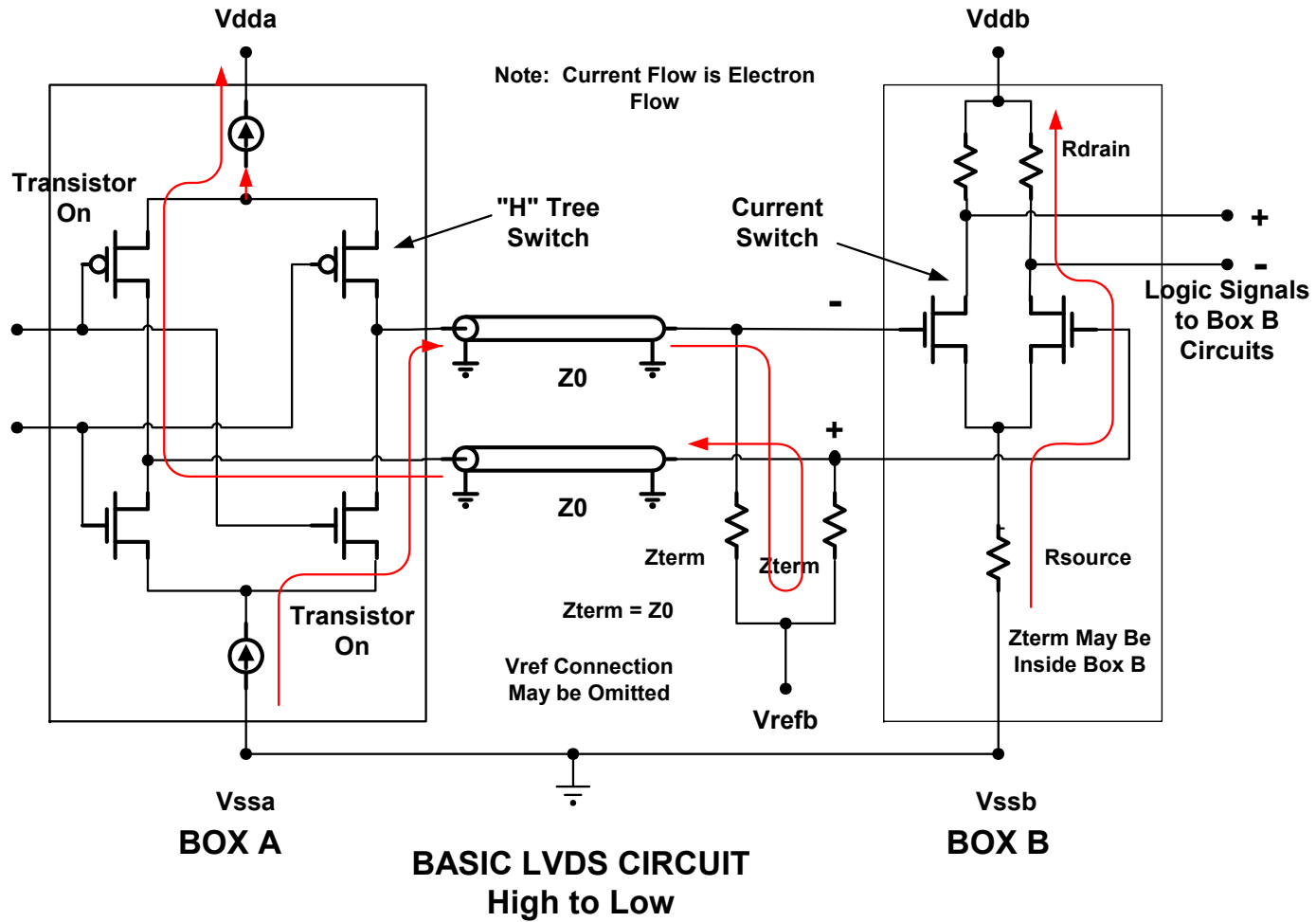
LVDS DIFFERENTIAL INTERFACE

BASIC LVDS CIRCUIT

LVDS CIRCUIT LOW TO HIGH

BASIC LVDS CIRCUIT
Low to High

LVDS CIRCUIT HIGH TO LOW

BASIC LVDS CIRCUIT
High to Low

OBSERVATIONS ABOUT DIFFERENTIAL PAIRS

- **Current drain from the PDS can be constant resulting in very low potential ripple and simple PDS design. Current is merely switched from one side to the other.**

- **Caution: Virtually all modern differential driver receiver pairs have complex adaptive circuitry that does not have constant current drain requiring good PDS design.**

- **Each side of a differential pair is independent of the other. Their only relationship to each other is tight timing.**

- **Primary design concerns are; length matching, managing reflections, and discontinuities, managing loss, managing cross talk, managing DC offset between the ends of a path.**

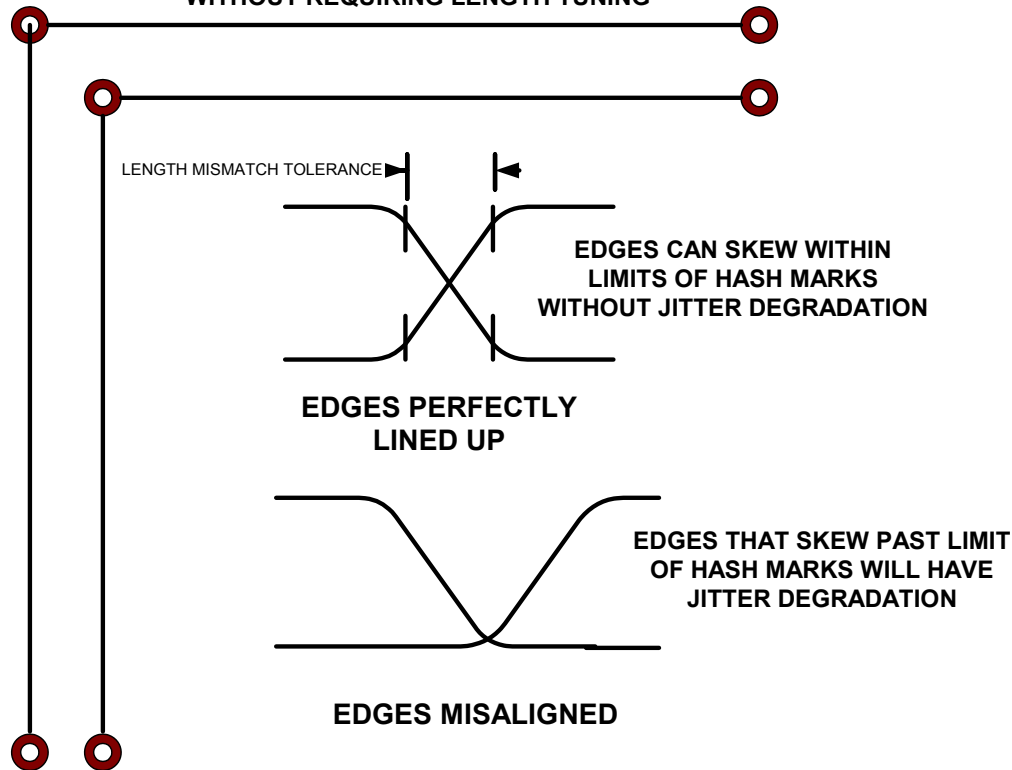# SIX TYPES OF DIFFERENTIAL CIRCUITS USED IN LOGIC SYSTEMS ARE:

- **ECL differential signal sets**

- **Biphase clock distribution systems (old TTL)**

- **LVDS data distribution systems**

- **Infiniband**

- **PCI Express**

- **All high speed serial data links**

- **All six circuit types detect the time that the two oppositely changing signals cross and produce a single-ended logic voltage change.**

- **Preserving the accuracy of the crossing is critical.**

- **Differential impedance has no role in their operation.**

DIFFERENTIAL PAIRS DESIGN CONSIDERATIONS

- Each side of the pair should be engineered to be a good 50 ohm line parallel terminated in 50 ohms.

- Both wires must be exactly the same length, within system timing tolerances. (Preserves crossing timing.)

- Lay out each line as a separate, stand alone transmission line using the same rules that apply to all other transmission lines. It is not necessary to route wires side by side, although it is often convenient to do so.

- No need to specify "differential" impedance between two lines.

- Routing wires side by side does not guarantee noise immunity from common mode noise. On the contrary, noise from an adjacent line will couple more into one side of the pair than the other.

- Usually not needed unless paths are long or grounds have offsets or excessive ground bounce.

DIFFERENTIAL PAIR LENGTH MATCHING

LENGTH MATCHING TOLEARANCE SHOULD ALLOW FOR THIS TYPE OF ROUTING WITHOUT REQUIRING LENGTH TUNING
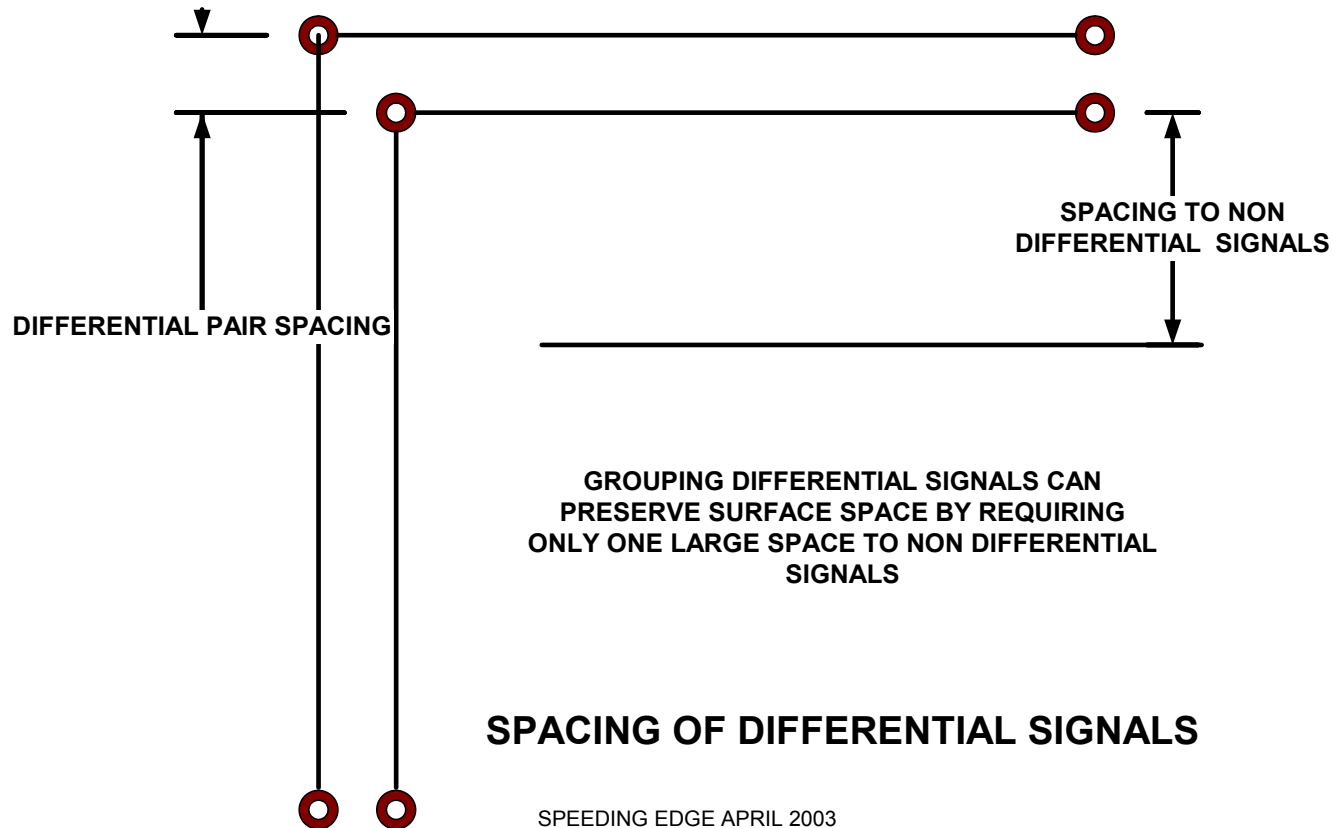
LENGTH MISMATCH TOLERANCE

EDGES CAN SKEW WITHIN LIMITS OF HASH MARKS WITHOUT JITTER DEGRADATION

EDGES PERFECTLY LINED UP

EDGES THAT SKEW PAST LIMIT OF HASH MARKS WILL HAVE JITTER DEGRADATION

EDGES MISALIGNED

DIFFERENTIAL PAIR LENGTH MATCHING STUDY

For minimum jitter, edges need to cross in the "straight" portions of the rise and fall times. Edges can misalign as long as they cross in this portion of each waveform.

Calculate the fastest rise and fall times at the receiver and convert to distance. Divide distance in half to get the ± length matching tolerance.

If this time is 400 pSEC, that is approximately 2.4" or 6 cm. Length mismatch can be as much as ±2.4" and jitter will be minimized.
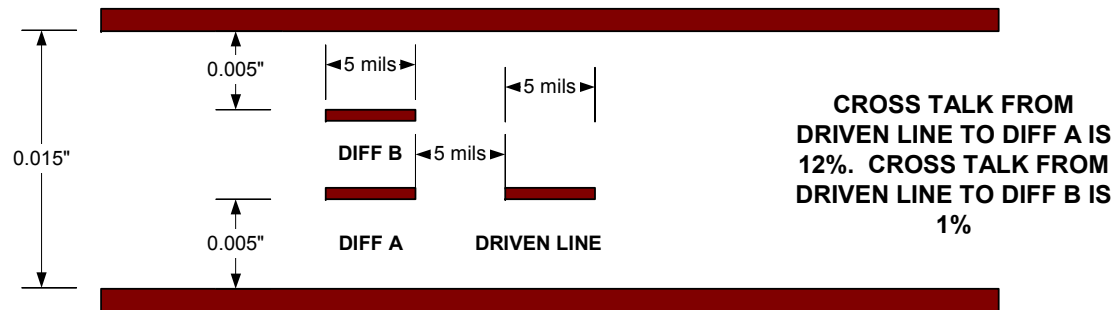
For 2.4 Gb/S the tolerance is 60 nS or ±150 mils (63.5 microns).

DIFFERENTIAL PAIR SPACING FOR CROSS TALK CONTROL

DIFFERENTIAL PAIR SPACING

SPACING TO NON DIFFERENTIAL SIGNALS

GROUPING DIFFERENTIAL SIGNALS CAN PRESERVE SURFACE SPACE BY REQUIRING ONLY ONE LARGE SPACE TO NON DIFFERENTIAL SIGNALS

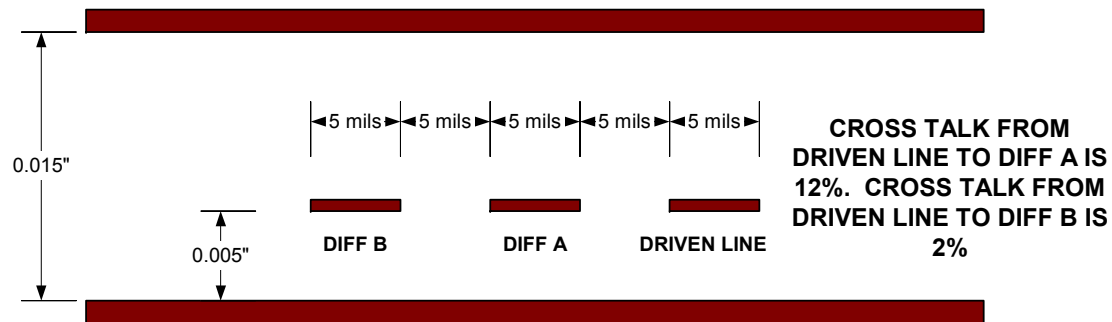## SPACING OF DIFFERENTIAL SIGNALS

SPEEDING EDGE APRIL 2003

POSSIBLE ROUTING CHOICES FOR DIFFERENTIAL PAIRS

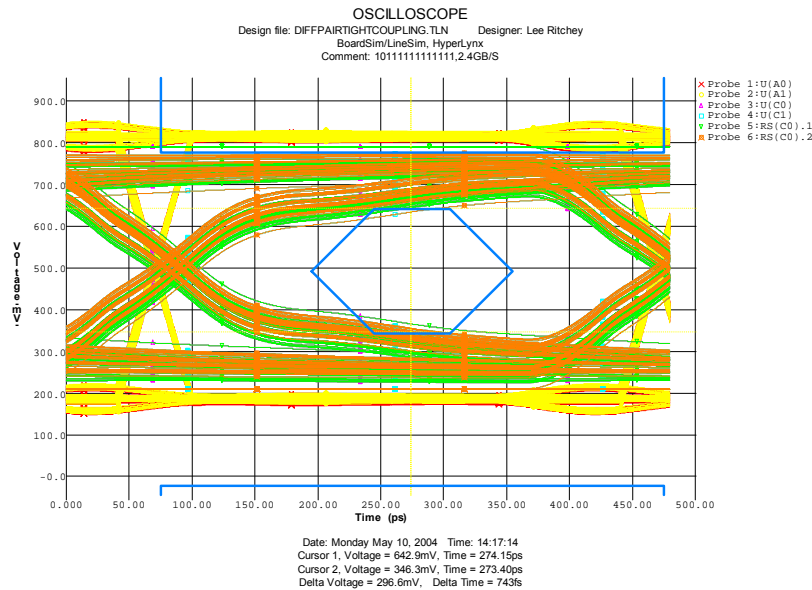**NEITHER SIDE BY SIDE ROUTING OR ABOVE AND BELOW ROUTING PRODUCES COMMON MODE NOISE REJECTION IN A DIFFERENTIAL PAIR**

CROSS TALK FROM DRIVEN LINE TO DIFF A IS 12%. CROSS TALK FROM DRIVEN LINE TO DIFF B IS 1%

0.015"   0.005"   5 mils   5 mils   5 mils   DIFF B   DIFF A   DRIVEN LINE

BROADSIDE DIFFERENTIAL PAIR CROSS TALK

CROSS TALK FROM DRIVEN LINE TO DIFF A IS 12%. CROSS TALK FROM DRIVEN LINE TO DIFF B IS 2%

0.015"   0.005"   5 mils   5 mils   5 mils   5 mils   5 mils   DIFF B   DIFF A   DRIVEN LINE

COPLANAR DIFFERENTIAL PAIR CROSS TALK

Speeding Edge

WHO SAID "EVERYBODY KNOWS TIGHT COUPLING BETWEEN MEMBERS OF A DIFFERENTIAL PAIR IS A GOOD THING?"

- **Is this really true? If so, there must be some proof.**

EXAMPLE OF TIGHT VS. LOOSE SPACING
3.125 Gb/S LINK

OSCILLOSCOPE
Design file: DIFFPAIRTIGHTCOUPLING.TLN   Designer: Lee Ritchey
BoardSim/LineSim, HyperLynx
Comment: 10111111111111,2.4GB/S

Date: Monday May 10, 2004   Time: 14:17:14
Cursor 1, Voltage = 642.9mV, Time = 274.15ps
Cursor 2, Voltage = 346.3mV, Time = 273.40ps
Delta Voltage = 296.6mV,   Delta Time = 743fs

TIGHT COUPLING

Figure 1. 5 mil lines, 5 mil spacing, 10 mil height, 100 ohm differential impedance, 70.7 ohm single ended, 30 inch long lines, 2.4 GB/S, on layer 3

OSCILLOSCOPE
Design file: DIFFPAIRTIGHTCOUPLING.TLN   Designer: Lee Ritchey
BoardSim/LineSim, HyperLynx
Comment: 10111111111111,2.4GB/S

Date: Monday May 10, 2004   Time: 14:19:05
Cursor 1, Voltage = 698.9mV, Time = 274.15ps
Cursor 2, Voltage = 319.2mV, Time = 274.15ps
Delta Voltage = 379.7mV,   Delta Time = 0.000s
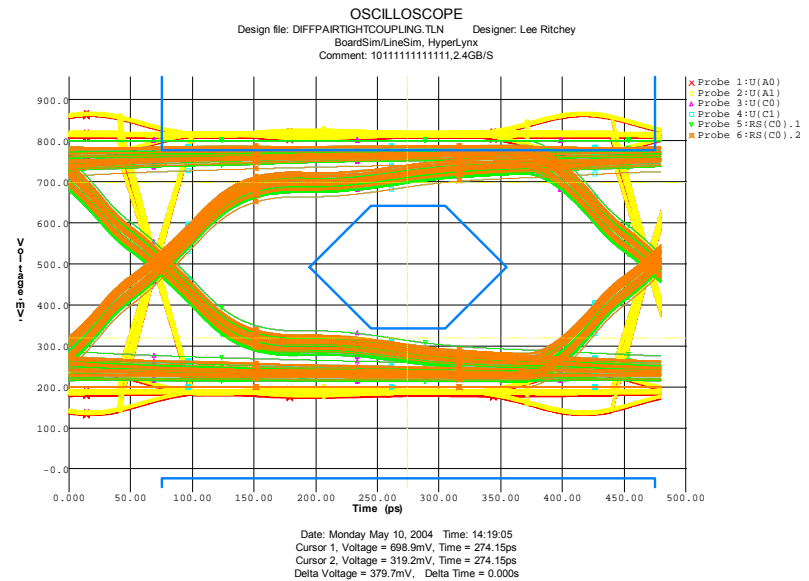
LOOSE COUPLING

Figure 2. 10 mil lines, 15 mil spacing, , 10 mil height 100 ohm differential impedance, 54.4 ohm single ended, 30 inch long lines, 2.4 GB/S on layer 3

The principal reason for the higher loss is the need to narrow the traces in order to maintain the 100 ohm differential impedance.

REASON TIGHTLY COUPLED TRACES MUST BE NARROWED

- When any metallic object, including another trace, is placed near a transmission line, this object drives the impedance of the trace down.

- In order to get back to the original target impedance it is necessary to narrow the trace.

- As a result, the surface area of the trace is reduced driving up skin effect loss.

- Note: This impedance problem occurs with single ended signals as well when tight routing rules are used.

POTENTIAL TIGHTLY COUPLED DIFFERENTIAL PAIR ROUTING PROBLEM

70 ohms SE

50 ohms SE   Zdiff = 100 OHMS

Zdiff = 140 OHMS

50 ohms SE   TRACE WIDTH 5 MILS
SPACING 5 MILS

70 ohms SE

TIGHTLY COUPLED CASE

54 ohms SE

50 ohms SE   Zdiff = 100 OHMS

Zdiff = 109 OHMS

50 ohms SE   TRACE WIDTH 10 MILS
SPACING 10 MILS

54 ohms SE

SPEEDING EDGE 2011
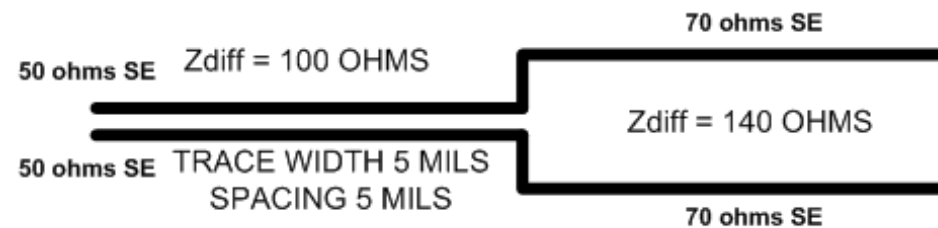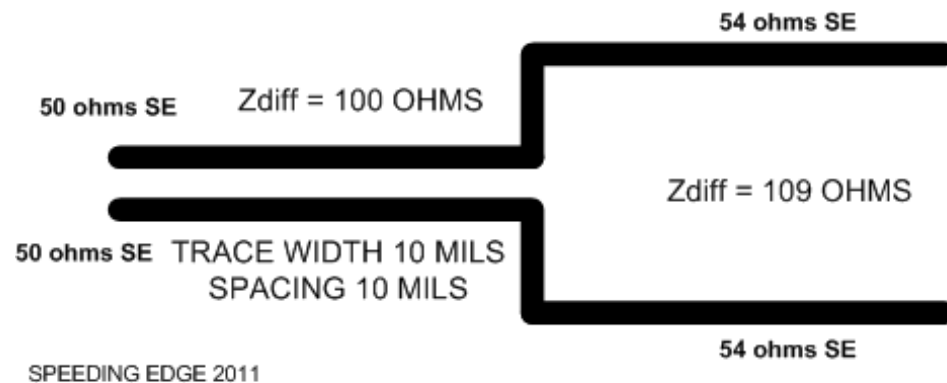
LOOSELY COUPLED CASE

CONSEQUENCES OF TIGHT vs. LOOSE COUPLING

It is better to specify a "not closer than" spacing rule for differential pairs to avoid this problem when forced to spread out a diff pair to route through arrays of holes such as in a 1 mm pitch BGA.

DIFFERENTIAL AND SINGLE ENDED IMPEDANCE vs. SPACING
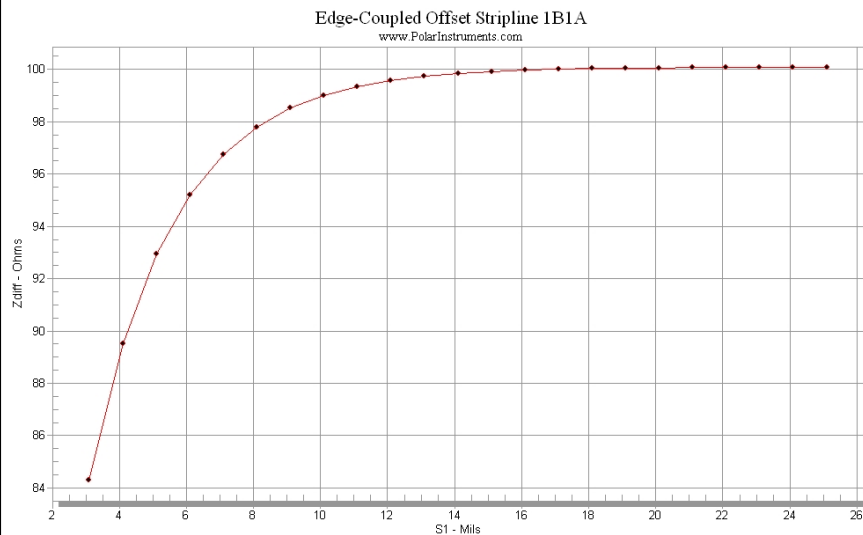
Differential Impedance vs. Trace Separation   Single Ended Impedance vs. Trace Separation
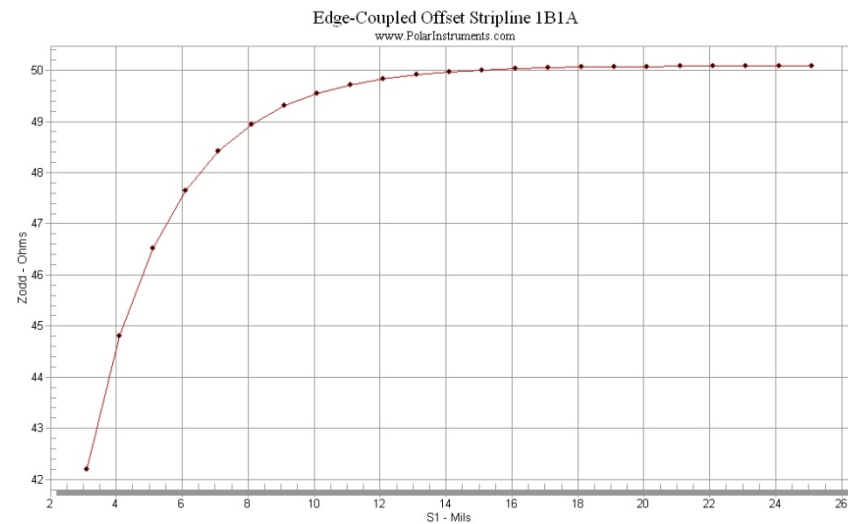
Transmission line geometry is centered stripline with height to nearest plane of 4 mils.   A "not closer than" rule of 10 mils guarantees minimal impedance change when traces must be separated to route through an array or pins or vias.

CONSERVATIVE DESIGN RULE FOR DIFFERENTIAL PAIRS

- From previous slides it can be seen that tightly coupling members of a differential pair has a few down sides.

- Tight coupling forces each trace to be narrowed in order to preserve 100 ohm differential (50 ohm single ended) impedance and this drives up skin effect loss.

- Tight coupling narrows each member of the differential pair such that when they must be separated, their individual impedance, instead of being 50 ohms, will be much higher, resulting in a differential impedance that is too high and large reflections.

- **The best rule for routing differential pairs is keep them far enough apart that they don't adversely affect each other. This makes routing rules much easier to follow.**

- **This rule should apply for single ended signal as well.**

POWER DELIVERY SYSTEMS FOR DIFFERENTIAL SIGNALING

- As noted in one of early slides in this section, basic differential signaling has a constant current drain from the power delivery system (PDS).

- Unfortunately, all modern differential driver/receiver pairs have compensation added at both ends to deal with path loss and discontinuities. Encoding and clock recovery systems also are included in most systems.

- These additional circuits are not constant current. The frequencies demanded from the PDS can range from DC to hundreds of megahertz. Therefore the PDS must be capable of providing all of those frequencies.

- What happens if ferrite beads are placed in the power leads of circuits as many applications notes recommend?

EFFECT OF USING FERRITE BEADS IN POWER LEADS OF A HIGH SPEED DEVICE
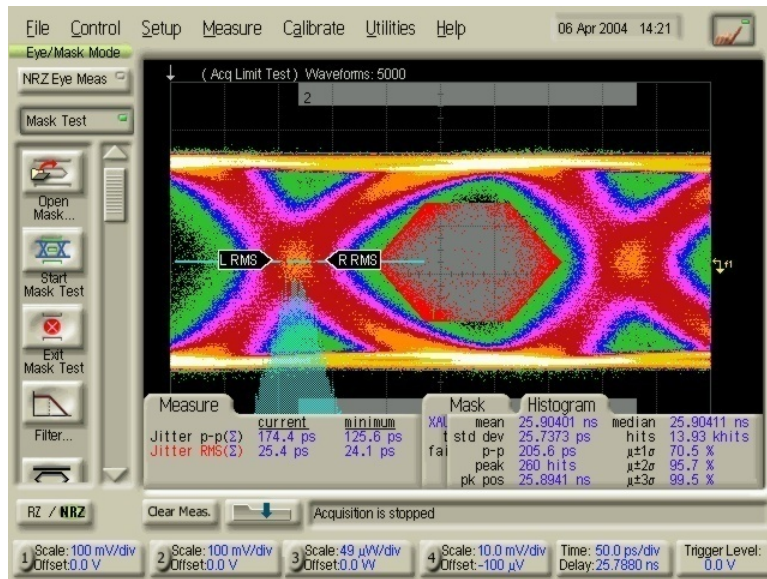
Eye diagram for a 3.125 GB/S serial link with recommended ferrite bead in power lead.
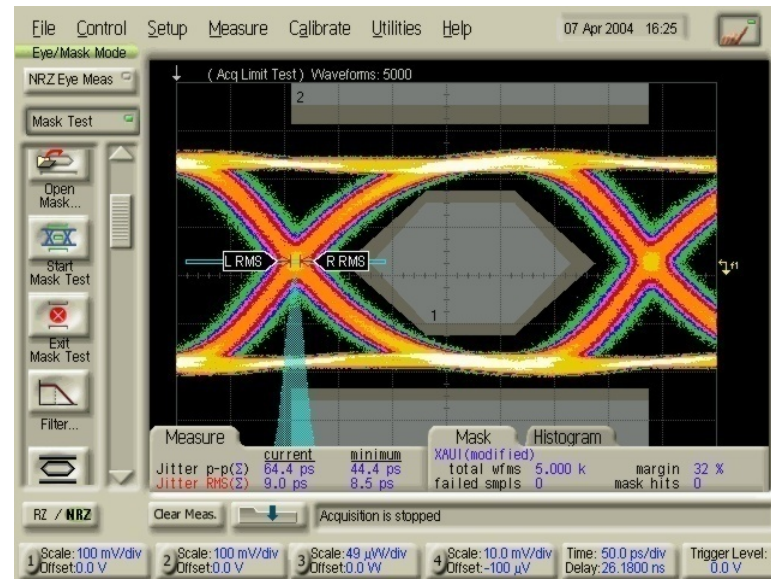
Eye diagram for a 3.125 GB/S serial link with recommended ferrite bead removed from power lead.

This is another case of an IC vendor preparing an applications note by just copying what was done on the last applications note, instead of performing analysis and testing to insure a design recommendation is appropriate to use.

PDS CONSIDERATIONS FOR DIFFERENTIAL SIGNALING

- As was shown on the previous slide, most differential signaling protocols are very complex require a well engineered PDS to insure proper operation.

- Any application note that recommends placing ferrite beads in the power leads of these circuits should be considered invalid and not followed, no matter what the applications engineer demands.

- If such a recommendation is demanded, insist on seeing successful circuit designs that follow such advice.

🚫 FERRITE BEADS

🚫 FERRITE BEADS

HOW MUCH BANDWIDTH DOES A HIGH SPEED DIFFERENTIAL SIGNAL PATH REQUIRE?

(Requiring a design to have more bandwidth than is actually needed by a signaling protocol increases cost without the accompanying benefit.)

BANDWIDTH REQUIREMENTS OF VARIOUS SIGNALING PROTOCOLS

- **There are two basic logic signaling protocols. These are:**

1. **Single-ended logic paths that have a driver at one end and one or more receivers at the other end with a single connection from drivers to receivers.**

2. **Differential signaling paths that have two outputs from a driver and two inputs on each receiver. Each logic path has two connections.**

A TYPICAL DIFFERENTIAL DATA PATH
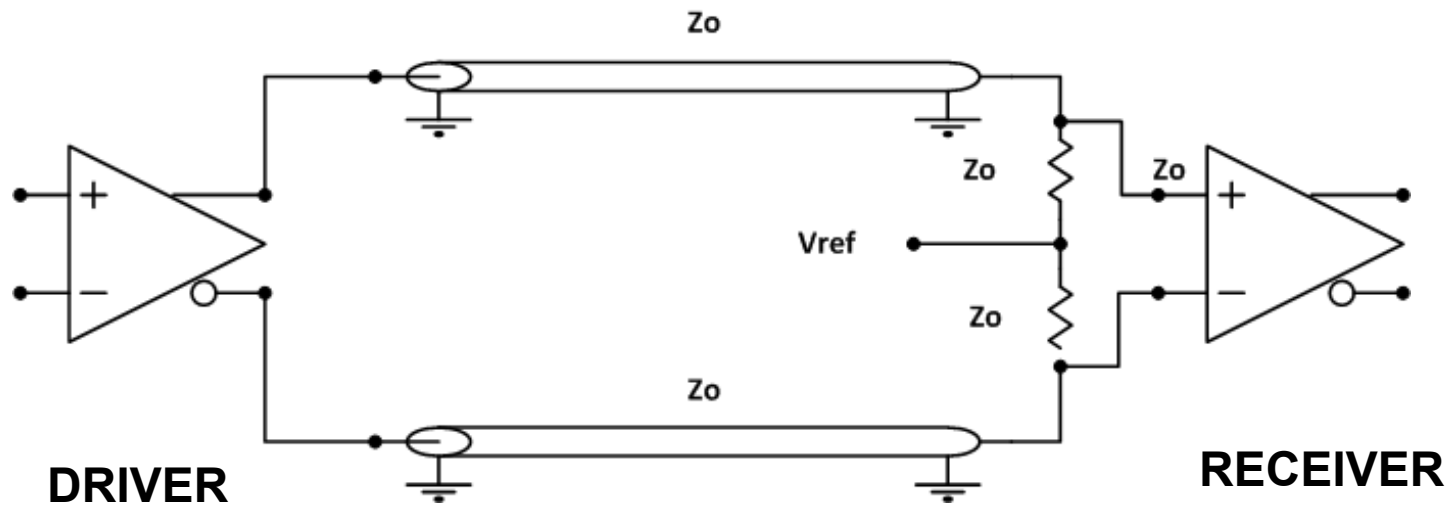
DRIVER

RECEIVER

IDEAL LOGIC SIGNALS

- Ideal logic signals are perfect square waves.

- Perfect square waves are made up of all the odd harmonics of the clock frequency out to infinity.

- To pass a perfect square wave from a driver to a receiver two conditions are required. These are:

1. The drivers must produce signals with infinite bandwidth.

2. The signal path must have flat bandwidth from DC to infinity.

REAL LOGIC SIGNALS

- **Real logic signal are not perfect square waves.**

- **Real drivers have limited ability to generate higher harmonics of the clock frequency resulting in rounded edges as seen on the left below.**

- **Slower drivers produce slower edges as seen on the graphic on the right hand side.**
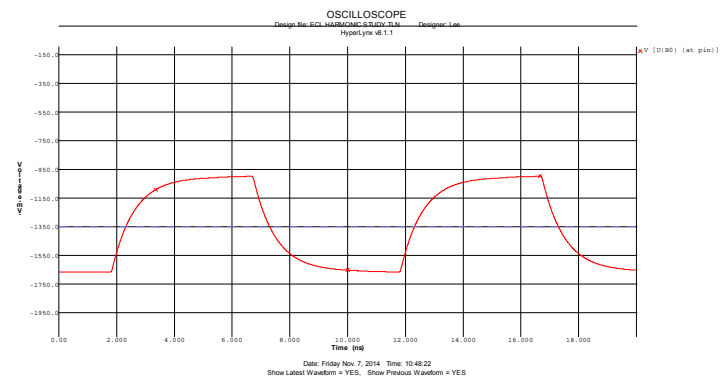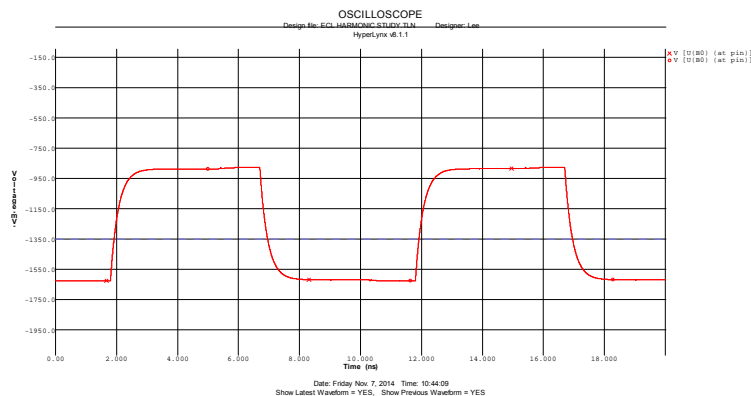
SINGLE ENDED LOGIC PATHS

- Single-ended logic paths have inputs that respond to the rising and falling edges of the logic signals.

- When a rising or falling edge passes through a threshold voltage (usually midway between a logic 1 level and a logic 0 level), a logic change is detected.

- How precisely the timing of the logic change is depends on how fast or sharp that edge is.

- Slower edges result in less precise detection of when a logic state changes.

- In order to preserve logic precision, the signal path must pass several higher harmonics of the clock frequency.

SIGNAL HARMONICS VS. RISE TIME

- **Fourier transformation of a waveform produces the harmonics present in the waveforms as well as their amplitudes.**

- **The diagram on the left below shows the frequency content of a logic path whose clock frequency is 100 MHz with a slow rise time. The main components are odd harmonics of this frequency.**

- **The diagram on the right below is the same waveform with faster rise and fall times. Note that the higher frequency harmonics are much larger.**

- **A signal path with a low bandwidth would cause this slowing down of the edges as shown on the left below, resulting in less reliable operation of single-ended data path.**

Spectrum Analyzer
Design file: 33VPARTERM.TLN   Designer: Lee
HyperLynx v8.1.1

20mA
13mA
6mA
0 ns   30 ns

+50dBuV/m

+30dBuV/m

+10dBuV/m
0   500.000 MHz   1.000 GHz

Date: Friday Nov. 7,2014   Time: 9:18:25

Spectrum Analyzer
Design file: 33VPARTERM.TLN   Designer: Lee
HyperLynx v8.1.1

23mA
14mA
6mA
0 ns   30 ns

+50dBuV/m

+30dBuV/m

+10dBuV/m
0   500.000 MHz   1.000 GHz

Date: Friday Nov. 7,2014   Time: 9:19:20
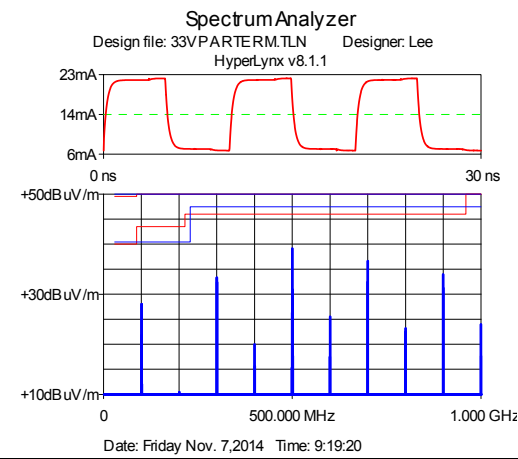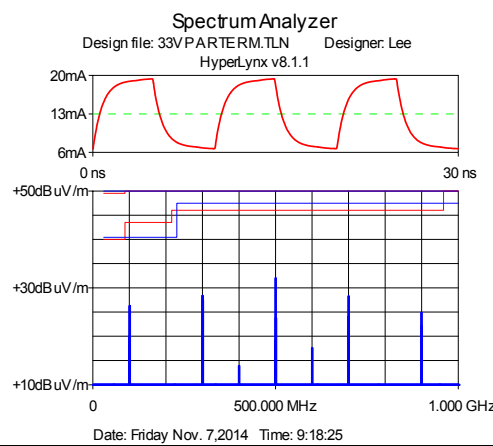
SPECTRUMS OF SLOW AND FAST EDGES

Spectrum Analyzer
Design file: 33VPARTERM.TLN   Designer: Lee
HyperLynx v8.1.1
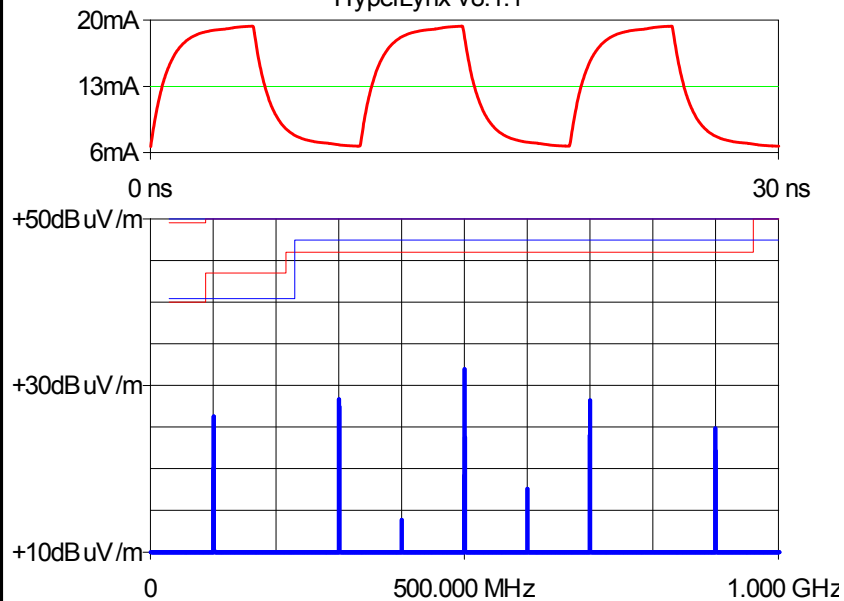
Date: Friday Nov. 7,2014   Time: 9:18:25

SLOW RISE TIME

Spectrum Analyzer
Design file: 33VPARTERM.TLN   Designer: Lee
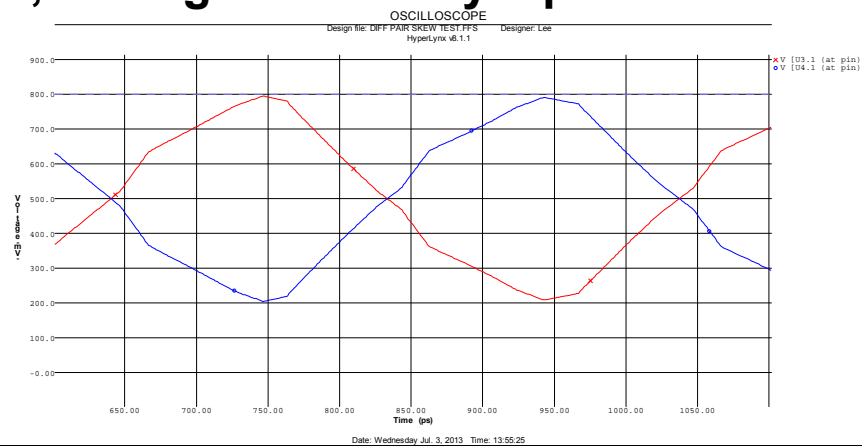HyperLynx v8.1.1
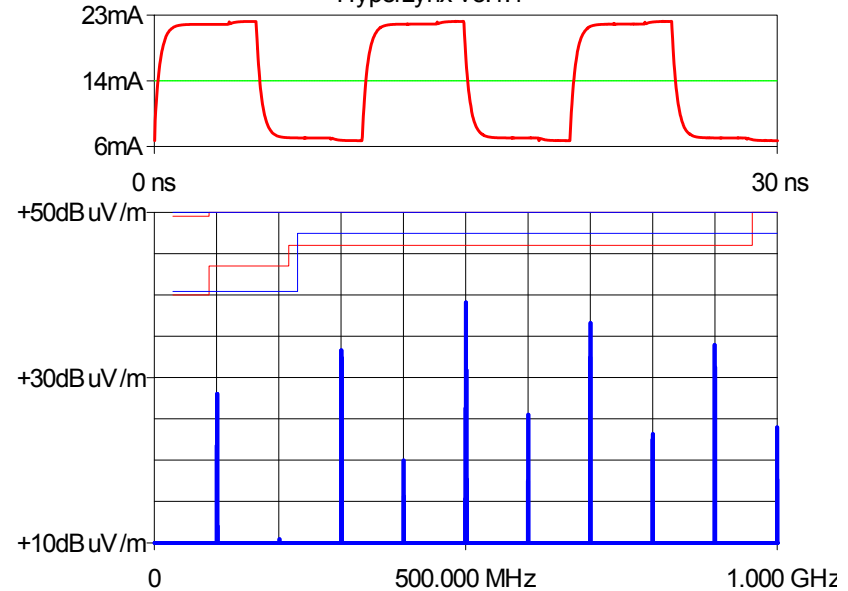
Date: Friday Nov. 7,2014   Time: 9:19:20

FAST RISE TIME

Note amount of very high frequency content needed to create fast rise time signal. This means the data path will need a very high bandwidth compared to the clock frequency, as much as 10X the clock frequency.

DIFFERENTIAL DATA PATHS

- **Differential data paths operate quite differently from single-ended logic paths.**

- **Differential data paths decide when a logic state change takes place by detecting when the two equal and opposite signals cross as shown in the "eye" diagram below.**

- **The differential data path has a different requirement than does a single-ended path. Focus is on the precision of the crossing which does not depend on rise time of the signal.**

- **As an be seen below, the signal is nearly a perfect sine wave.**

OSCILLOSCOPE
Design file: DIFF PAIR SKEW TEST.FFS   Designer: Lee
HyperLynx v8.1.1

Date: Wednesday Jul. 3, 2013 Time: 13:55:25

COMMENTS ON THE SIGNAL ON THE PREVIOUS SLIDE

- The differential signal on the previous slide has the appearance of an "eye". In fact, our industry describes this as an eye diagram.

- Two conditions are necessary for a differential signal path to operate properly. These are:

1. The "eye" must be sufficiently open to allow the receiver to accurately detect the logic state. (Some receivers need only 4 or 5 millivolts to do this.)

2. The place where the signals cross is when a logic state change is detected. This must not move back and forth in time (jitter) too much.

- These conditions are met when the signal is little more than a sine wave or the first harmonic of the clock frequency.

BANDWIDTH NEEDED BY A DIFFERENTIAL DATA PATH

- **From the discussion on the previous slides it can be seen that the bandwidth requirements of a differential signaling path are much less demanding than for a similar frequency single-ended data path.**

- **Successful signaling with a differential data path requires a path bandwidth that is little more than the clock frequency.**

    - **For example, a 6.125 Gb/S data path has a clock frequency of 3.0625 GHz. A data path with a bandwidth of little more than 3 GHz will perform properly at this data rate.**

    - **A similar data rate single-ended data path would require a bandwidth of about 40 GHz to operate properly.**

TYPES OF PLATED THROUGH HOLES THAT CONNECT TO TRANSMISSION LINES

- There are two types of plated through holes that connect to transmission lines. These are vias that connect signal pins to transmission lines and connector holes. Both have inductance along their length as well as capacitance. Capacitance is a function of drill diameter and hole length. Inductance is a function of length and is approximately 35 pH per mil (25 microns) of length.

- Vias tend to be drilled with a 10 mil (254 micron) or 12 mil (305 micron) drills and are usually no longer than 120 mils (3.05 mm). A 12 mil drilled via 100 mils (2.54 mm) long averages about 0.3 pF.

- Connector plated through holes are usually drilled 22 mils (.56 mm) in diameter and are often as long as 250 mils (6.35 mm). A connector plated through hole 30 mils (.76 mm) in diameter and 100 mils long averages about 0.6 pF.

INDUCTANCE OF CONNECTING VIAS

VIA INDUCTANCE VS. LENGTH
(12 mil drill diameter)
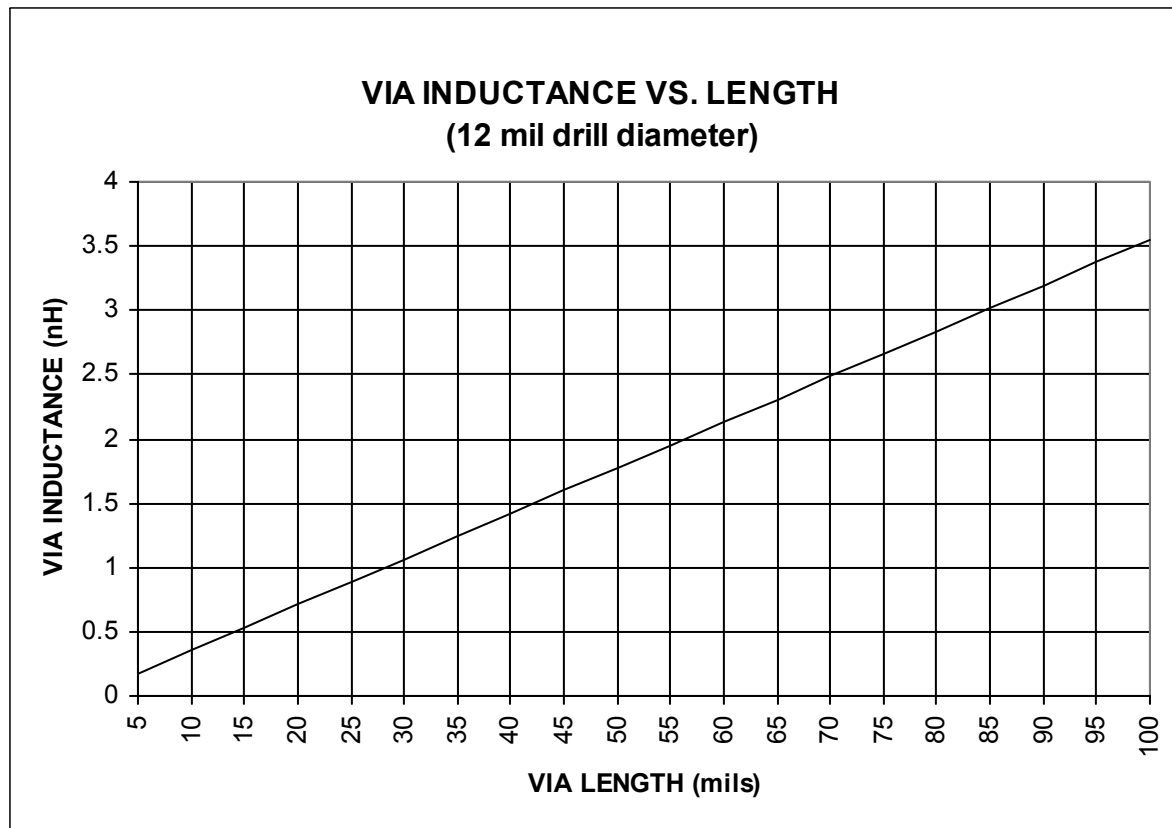
This inductance is also in series with power pins attempting to draw power from the planes. This is the inductance of one via.

WHAT HAPPENS WHEN SIGNAL GET VERY FAST

- **Introduction**

- **A 5.2 GB/S Data Path**

- **Signal Quality From 100 MB/S to 4.8 GB/S**

- **Sources of Degradation**

- **Making Design Tradeoffs for Optimum Price Performance**

•Volume 2 Chapter 8

INTRODUCTION

- A real data path will be driven by ever faster signals and the changes in signal quality observed.

- The sources of degradation will be removed from the model one by one to illustrate where the degradation originates.

- The simulation model was verified for accuracy by constructing the real network in hardware and characterizing it using a network analyzer.

- The objective is to determine which design rules are most important to achieving a good data path with the least effort.

- A method called "eye diagram" analysis will be used to assess path quality.

A TYPICAL CIRCUIT TRAVELLING BETWEEN DAUGHTER CARDS ACROSS A 4 METER CABLE

PCB A   **CABLE**   **PCB B**

DRIVER   **CABLE**   **CABLE**   **RECEIVER**
OUTPUT   **INPUT**   **OUTPUT**   **INPUT**

L = 8"   L = 4 meters   **L = 8"**
Stripline   (157.5")   **Stripline**
TW = 5 mils   Infiniband   **TW = 5 mils**
T = 0.6 mils Cable   **T = 0.6 mils**
S = 15 mils   Loss = .0005   **S = 15 mils**
er = 3.8   er = 1.8   **er = 3.8**
Loss = .015   **Loss = .015**
FR408   **FR408**
Z0 = 50 ohms   **Z0 = 50 ohms**
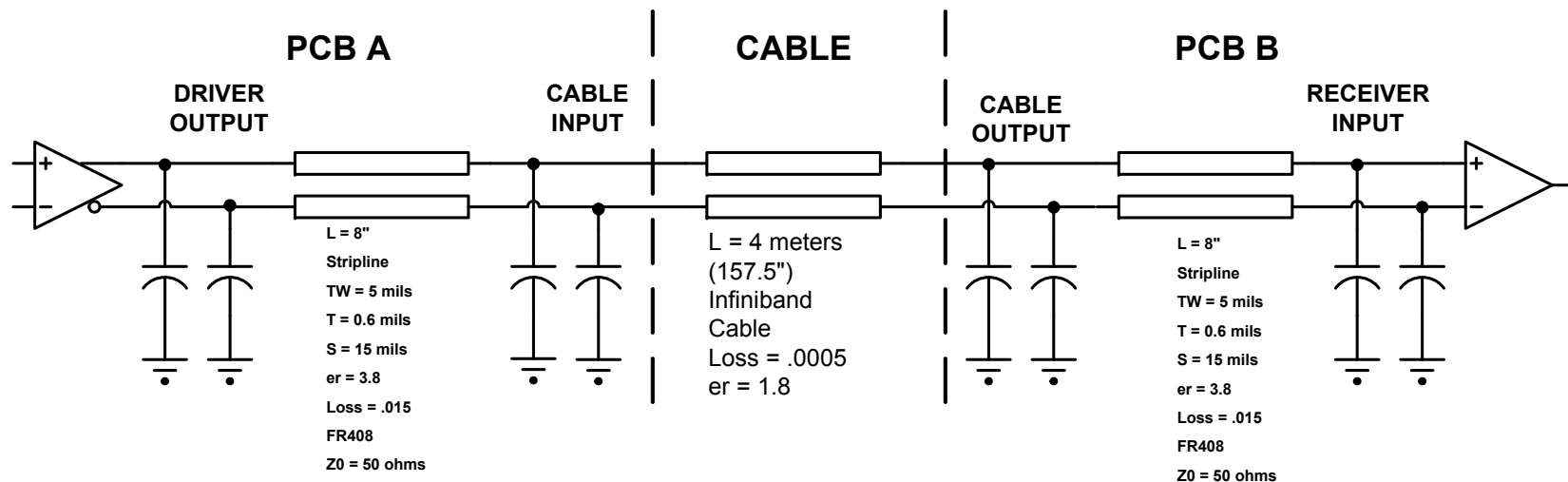
Capacitors are parasitic capacitance of plated through holes (vias) used to enter and leave PCB traces. Value = 0.65 pF

Driver and receiver models taken from latest SPICE models provided by IBM and include pad transfers.

SPEEDING EDGE 2004

SIMULATION MODEL FOR 5.2 GB/S SERIAL LINKS

•Note that there are 4 each 12 mil drilled vias on each of the signal paths. Each PCB is 110 mils (2.79 mm) thick.

ADVANTAGES OF MODELS

- **Models allow rapid changes in various conditions to examine how changes affect performance.**

- **Models allow endless "what if" questions to be asked without incurring the costs and time delays of prototypes.**

Caution- Models must be validated using real hardware to insure they accurately represent the real thing.

HARDWARE MODEL USED FOR TESTS
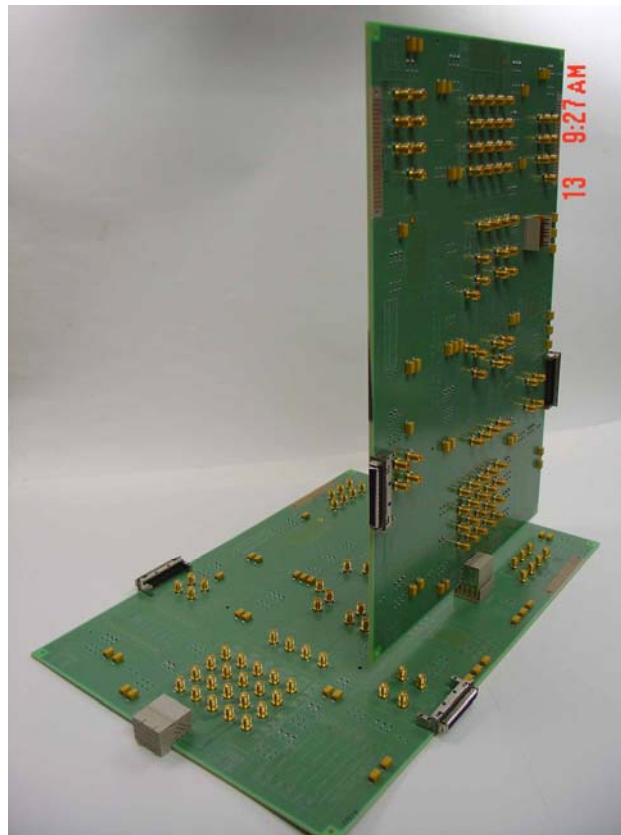
SIMULATOR MODEL VS. ACTUAL CIRCUIT
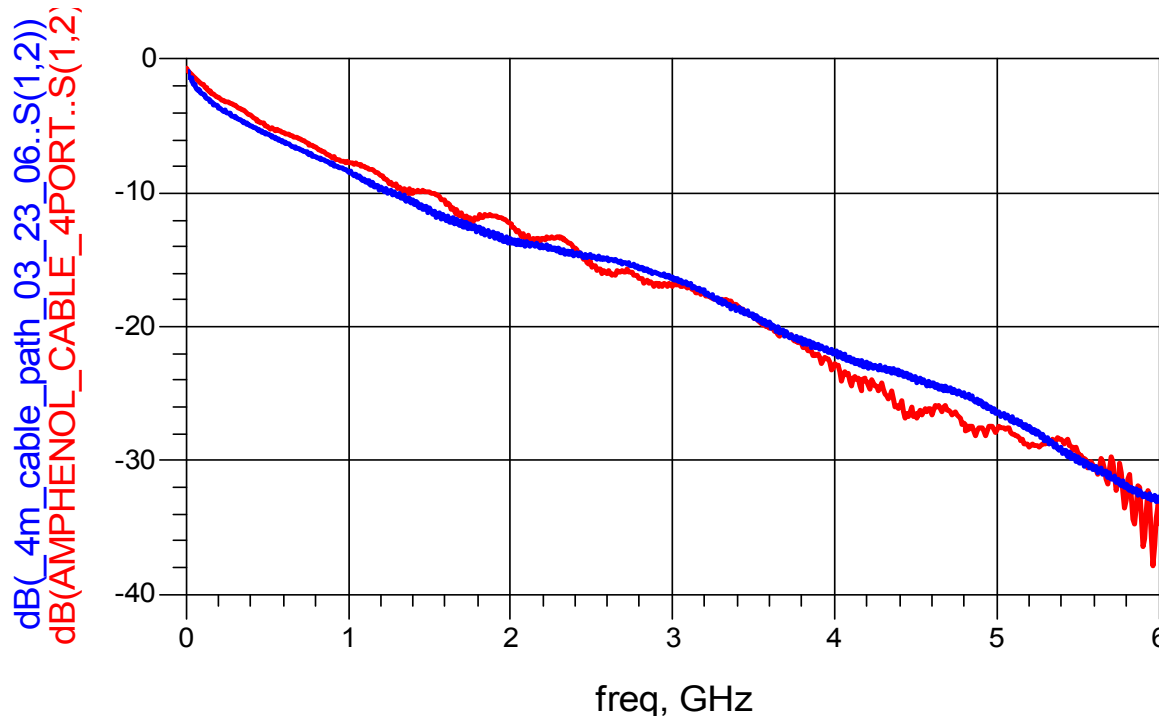
- Blue curve is loss vs. frequency for the simulation model. Red curve is measured loss vs. frequency for the actual circuit being analyzed. There is very good agreement between model and hardware, so simulations should be representative of what will be seen in final product.

SIGNAL QUALITY AT 100 MB/S AT DRIVER
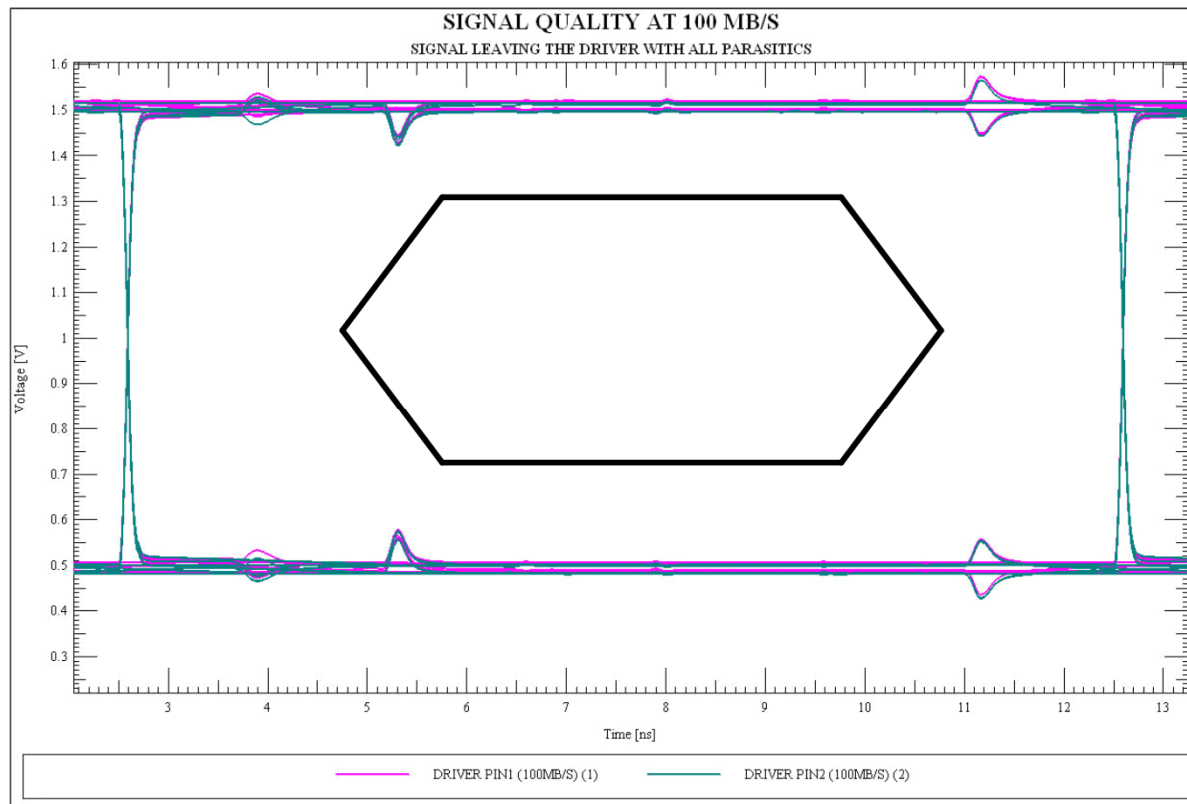
SIGNAL LEAVING THE DRIVERS

TIME SCALE- 1 nSec/Division

This is an eye diagram which is a single bit period displayed on a storage oscilloscope with a very long pseudorandom data pattern with a very long length, expecting to find the worst case signal that will occur.

RECEIVER SIGNAL QUALITY AT 100 MB/S
(Vias and losses in model)
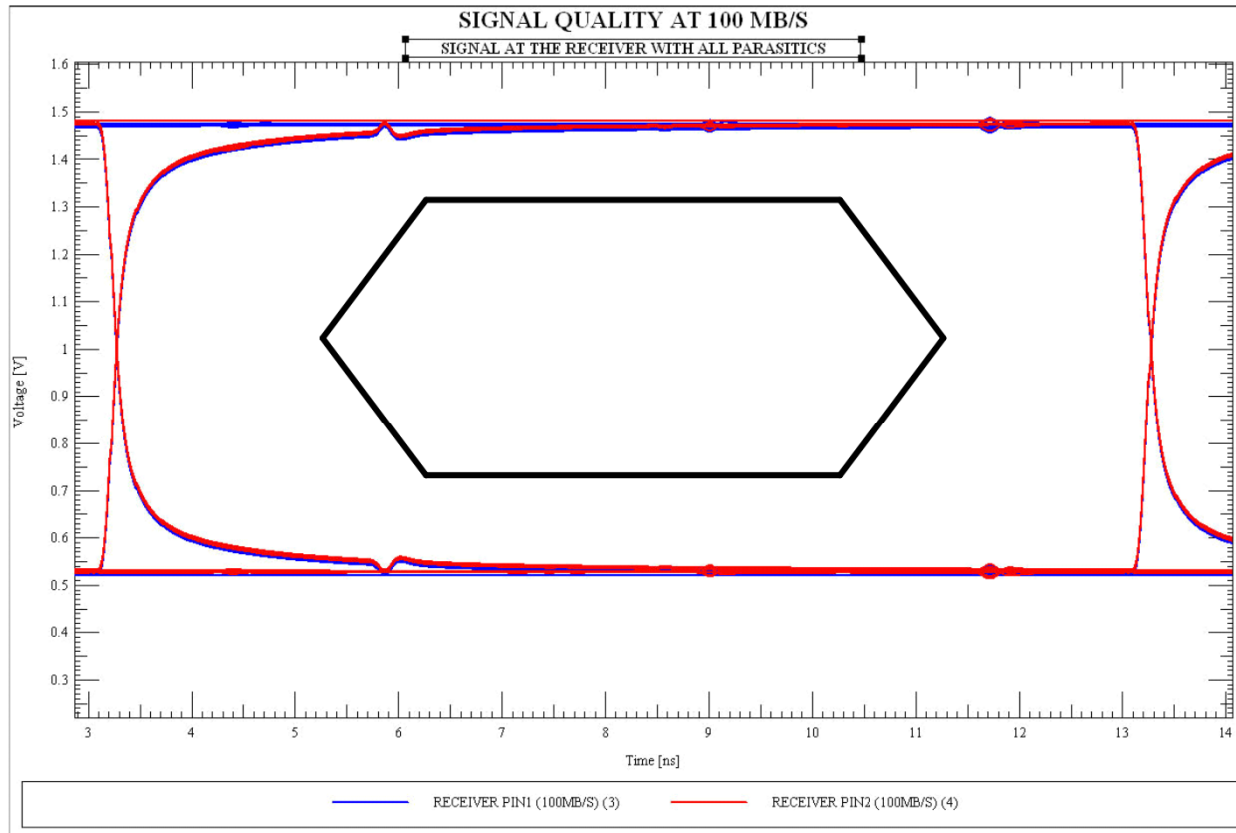
SIGNAL ARRIVING AT THE RECEIVERS WITH ALL LOSSES IN MODEL

RECEIVER SIGNAL QUALITY AT 100 MB/S
(Losses removed, vias present)
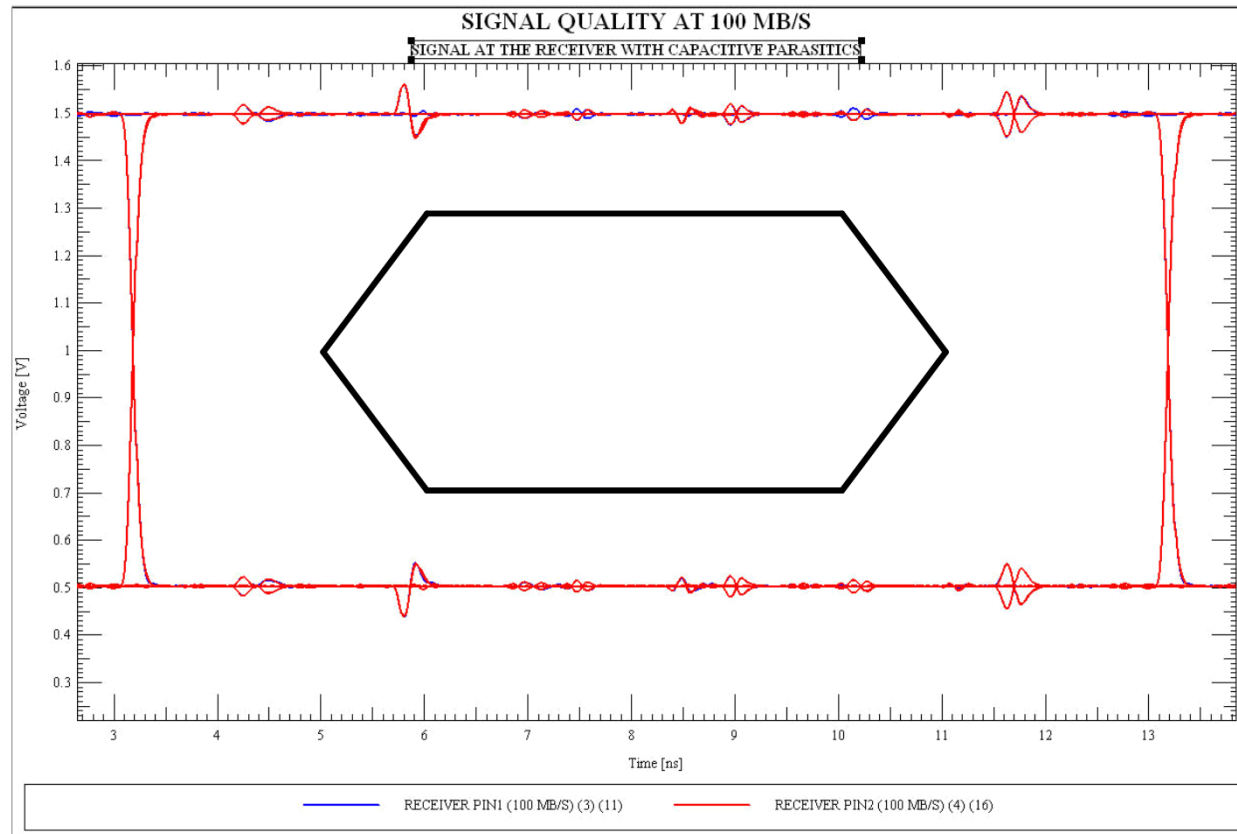
SIGNAL ARRIVING AT THE RECEIVERS WITH NO TRANSMISSION LINE LOSSES

(EITHER COPPER OR DIELECTRIC) IN MODEL

RECEIVER SIGNAL QUALITY AT 100 MB/S
(No losses, no vias)

SIGNAL QUALITY AT 100 MB/S
SIGNAL AT THE RECEIVER WITH NO LOSSES

RECEIVER PIN1 (100 MB/S) (3)   RECEIVER PIN2 (100 MB/S) (4)
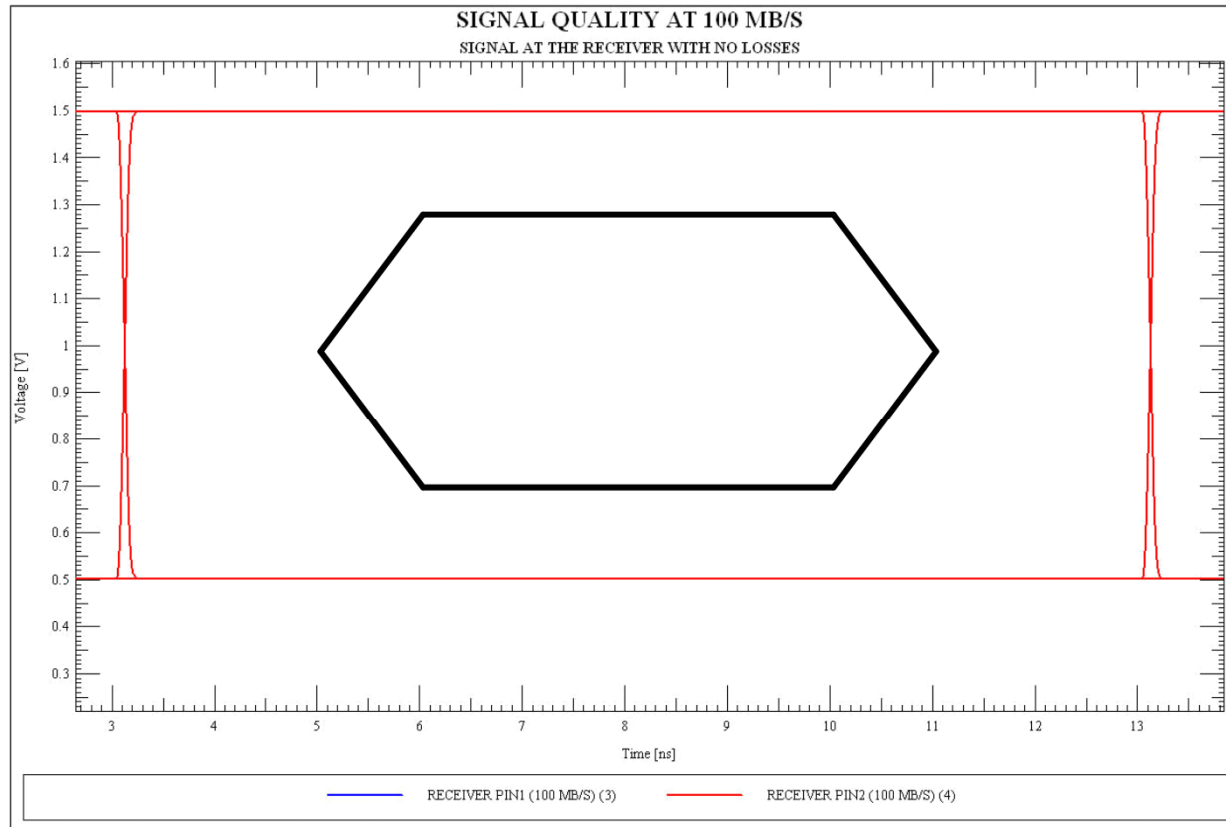
SIGNAL ARRIVING AT THE RECEIVERS WITH NO TRANSMISSION LINE LOSSES AND

NO PARASITIC CAPACITANCES IN MODEL

SIGNAL QUALITY AT 1 GB/S AT DRIVER

SIGNAL QUALITY AT 1 GB/S
SIGNAL AT THE DRIVER WITH ALL PARASITICS

DRIVER PIN1 (1GB/S) (5)　　　DRIVER PIN2 (1GB/S) (6)
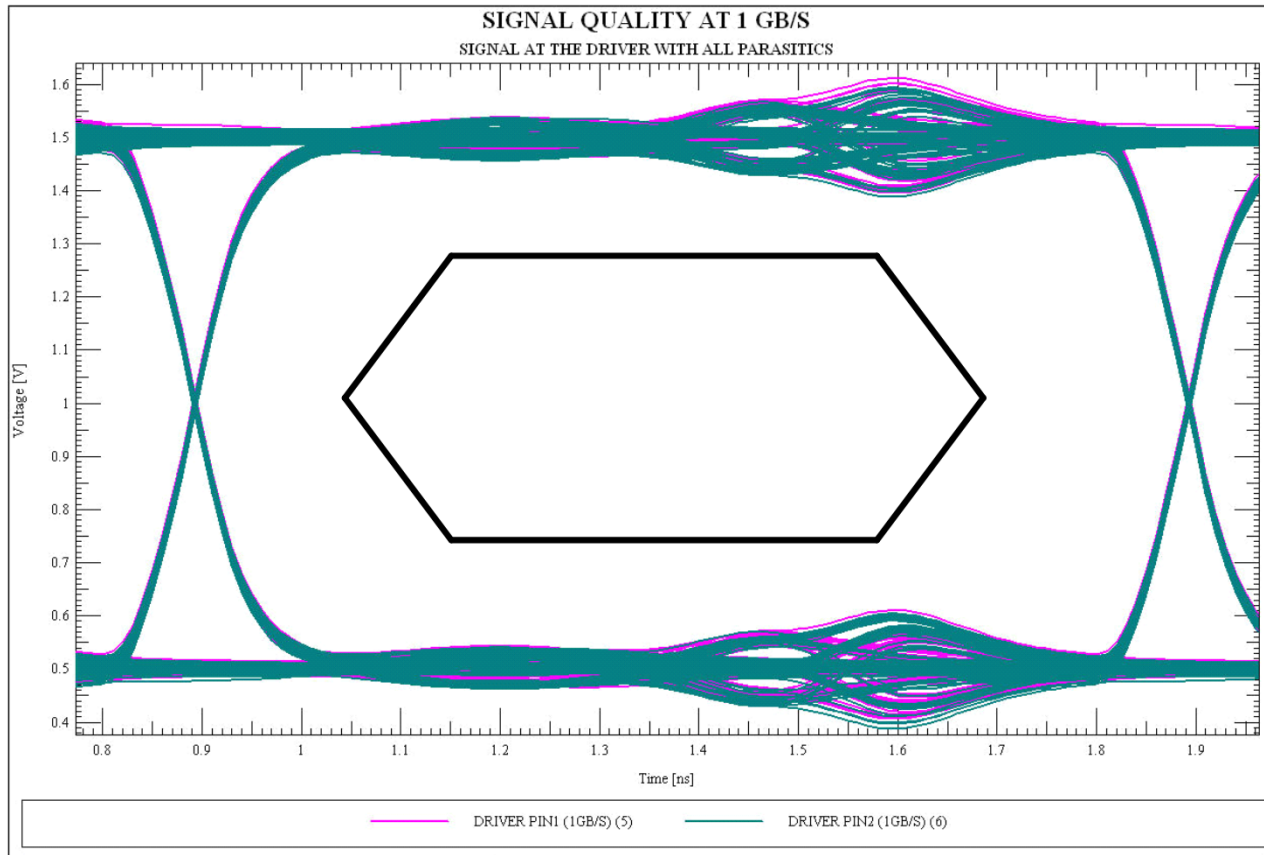
SIGNAL LEAVING DRIVER WITH ALL PARASITICS

TIME SCALE- 100 PSec/Division

RECIEVER SIGNAL QUALITY AT 1 GB/S
(All losses and vias present)

SIGNAL QUALITY AT 1 GB/S

SIGNAL AT THE RECEIVER WITH ALL PARASITICS

RECEIVER PIN1 (1GB/S) (7)   RECEIVER PIN2 (1GB/S) (8)
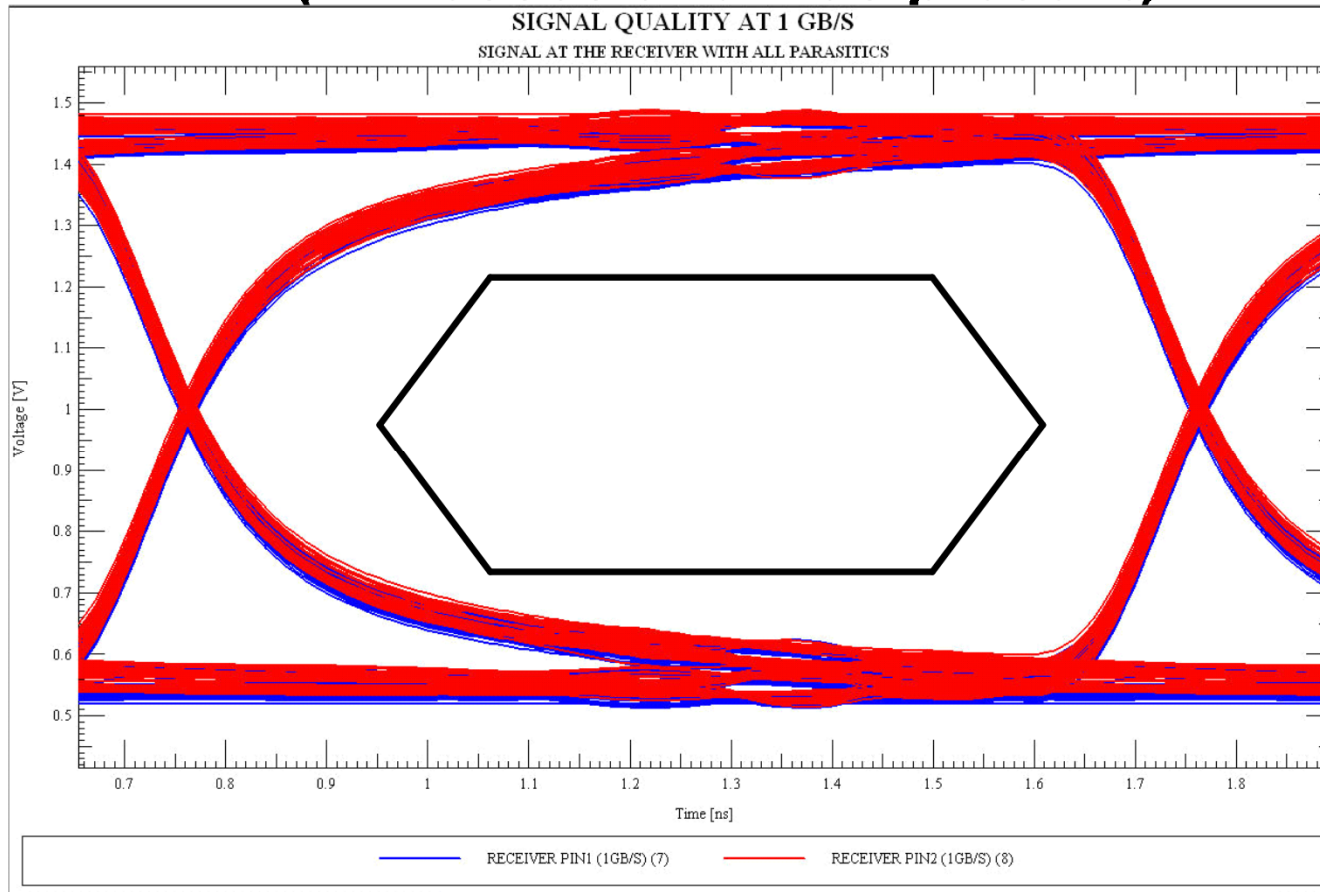
TIME SCALE- 100 PSec/Division

DRIVER SIGNAL QUALITY AT 2.4 GB/S
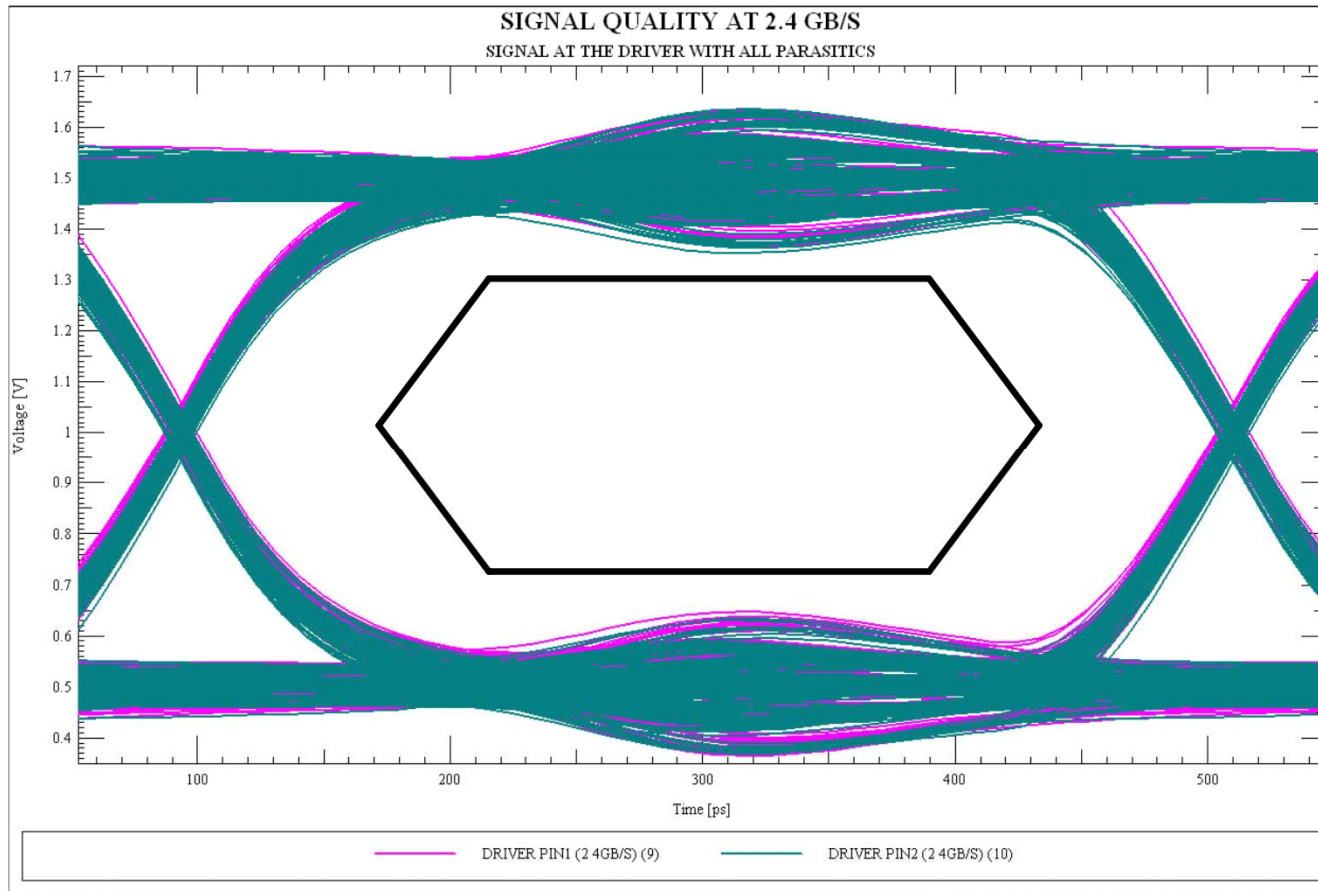
SIGNAL AT DRIVER WITH ALL PARASITICS

TIME SCALE- 100 PSec/Division

RECEIVER SIGNAL QUALITY AT 2.4 GB/S
(All losses and vias present)

SIGNAL QUALITY AT 2.4 GB/S
SIGNAL AT THE RECEIVER WITH ALL PARASITICS

RECEIVER PIN1 (2.4GB/S) (11)   RECEIVER PIN2 (2.4GB/S) (12)
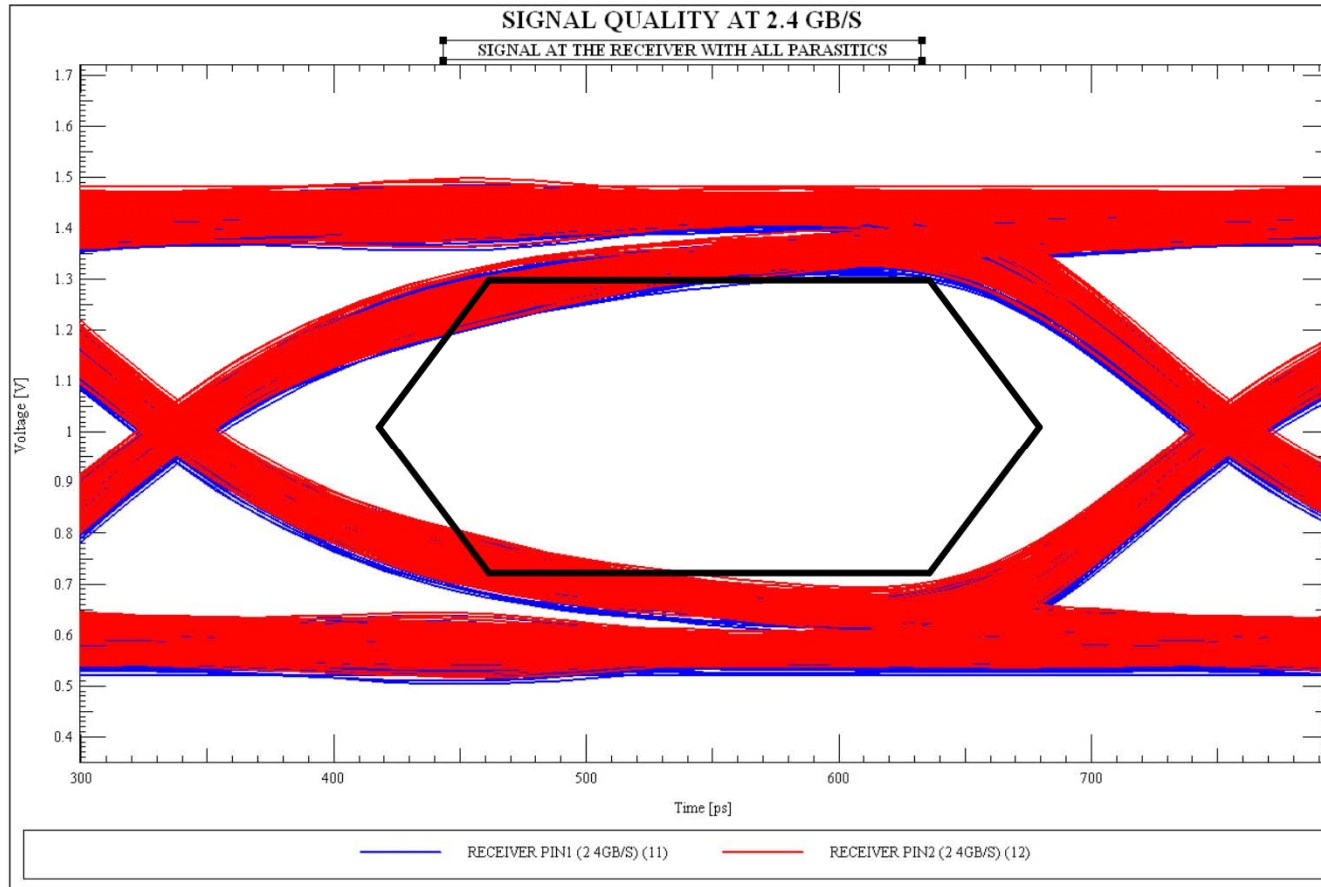
SIGNAL AT RECEIVER WITH ALL PARASITICS

SIGNAL QUALITY AT 2.4 GB/S
(Losses removed, vias present)

SIGNAL QUALITY AT 2.4 GB/S
SIGNAL AT THE RECEIVER WITH CAPACITIVE PARASITICS

RECEIVER PIN1 (2 4 GB/S) (11) (10)   RECEIVER PIN2 (2 4 GB/S) (12) (13)
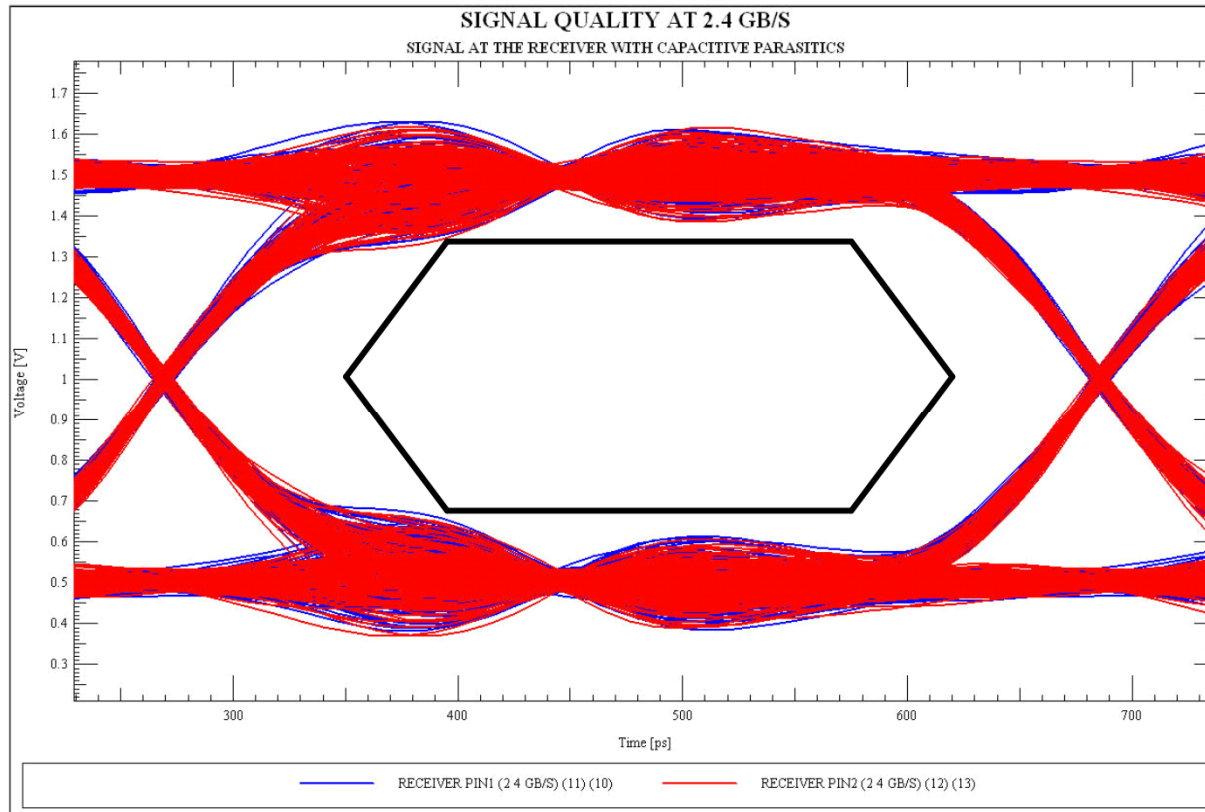
SIGNAL AT RECEIVER WITH NO TRANSMISSION LOSSES

SIGNAL QUALITY AT 2.4 GB/S
(Losses and vias removed)
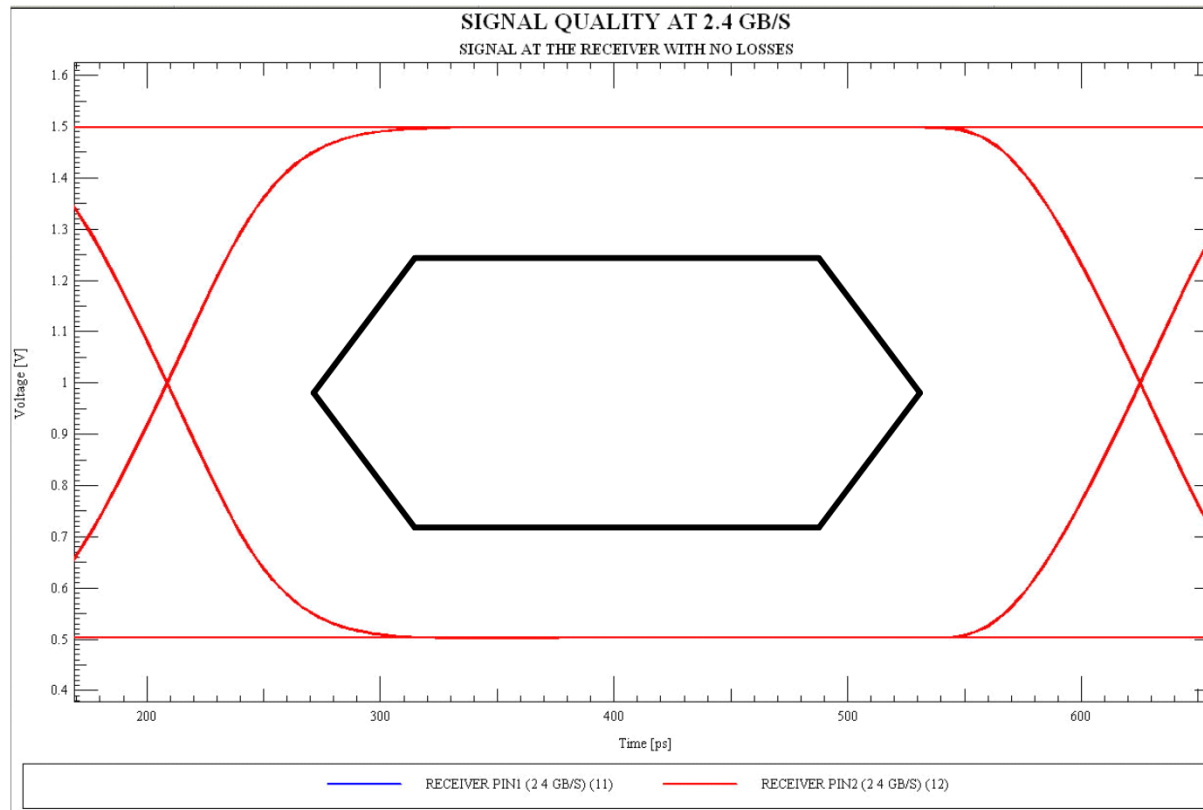
SIGNAL AT RECEIVER WITH NO TRANSMISSION LOSSES OR PARASITIC C (vias)

RECEIVER SIGNAL QUALITY AT 2.4 GB/S WITH 2 pF VIAS

SIGNAL QUALITY AT 2.4 GB/S
SIGNAL AT THE RECEIVER WITH CAPACITIVE PARASITICS
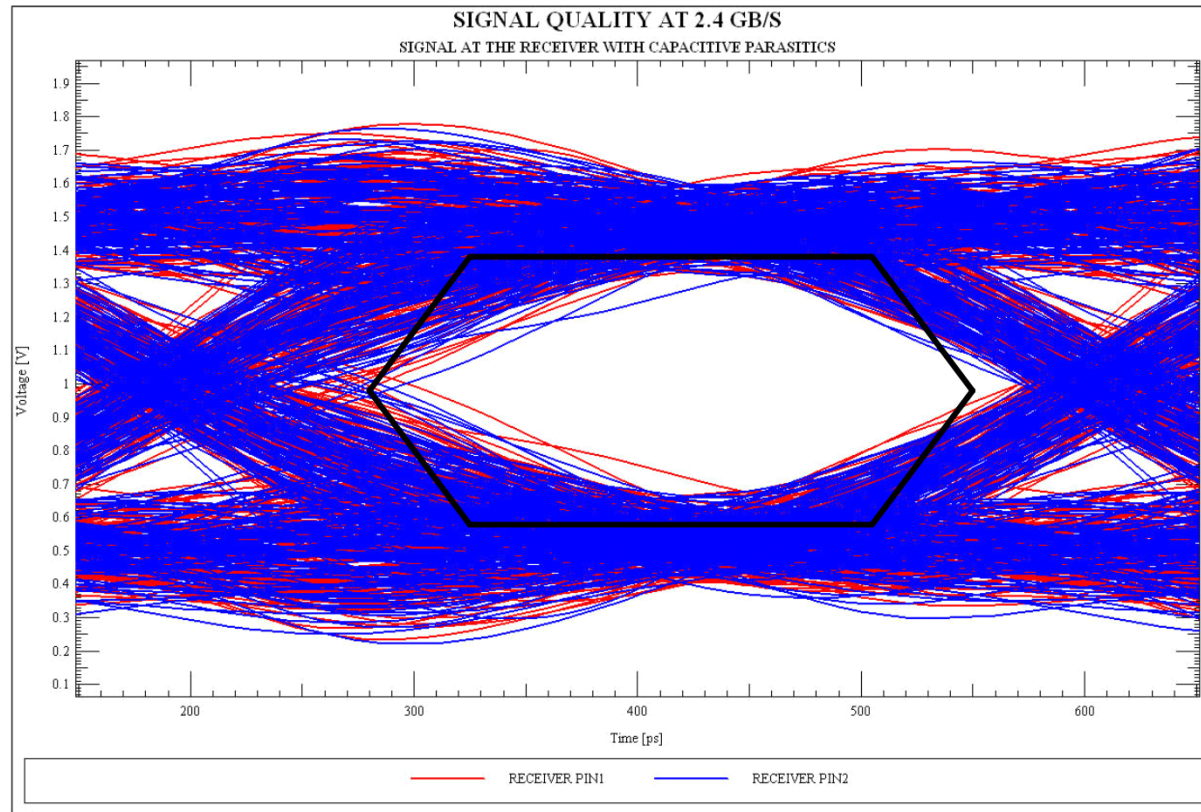
SIGNAL AT RECEIVER WITH 2 pF VIA CAPACITANCE AS FOUND IN BACKPLANES

LARGE DIAMETER, LONG PLATED THROUGH HOLES ARE REQUIRED BY PRESFIT CONNECTORS. MITIGATING THIS PROBLEM GAVE RISE TO BACKDRILLING.

SOURCES OF PARASITIC CAPACITANCE AND THEIR EFFECTS

- Parasitic capacitance comes from device inputs and from the barrels of plated through holes.

- Plated through holes, such as those required for press fit connectors, are often called stubs by mistake.

- The parasitic capacitance lowers the impedance locally resulting in reflections.

- These reflections, if large enough, can result in signal loss and jitter. As noted in this analysis, when there is a large amount of loss in the signal path, the effects of the vias is minimized.

- Irregular weave in the glass reinforcement can cause the same problem.

- In some cases, back drilling can remove this excess capacitance from plated through holes such as vias and connector pin holes.

RECEIVER SIGNAL QUALITY AT 4.8 GB/S
(Vias and losses present)
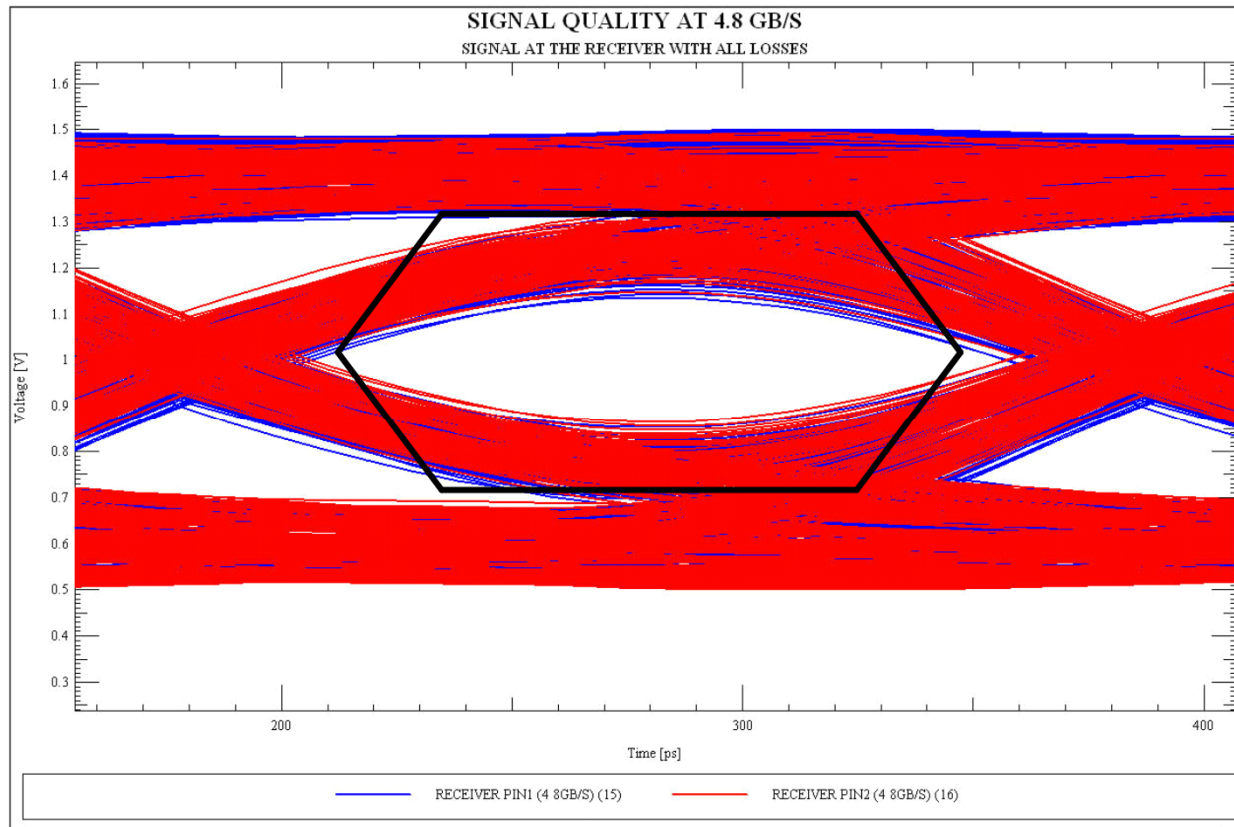
SIGNAL AT RECEIVER WITH TRANSMISSION LOSSES AND PARASITICS

TIME SCALE- 100 PSec/Division

WHAT TO DO WHEN SIGNAL IS STILL TOO SMALL

1. Select a lower loss material.

2. Use pre-emphasis to compensate for losses at high frequencies.

3. Use post emphasis to amplify high frequencies more than low frequencies.

4. Redesign receiver to require less signal amplitude.

    2 and 3 are known as adaptive techniques and are often found together in newer transceiver sets.

    (Increasing trace width to reduce skin effect losses results in PCBs that can grow too thick for ease of manufacture. This is my last choice.)

RECEIVER SIGNAL QUALITY AT 4.8 GB/S
(Vias and losses present, reduced amplitude requirement)

SIGNAL QUALITY AT 4.8 GB/S
SIGNAL AT THE RECEIVER WITH ALL LOSSES

RECEIVER PIN1 (4 8GB/S) (15)   RECEIVER PIN2 (4 8GB/S) (16)
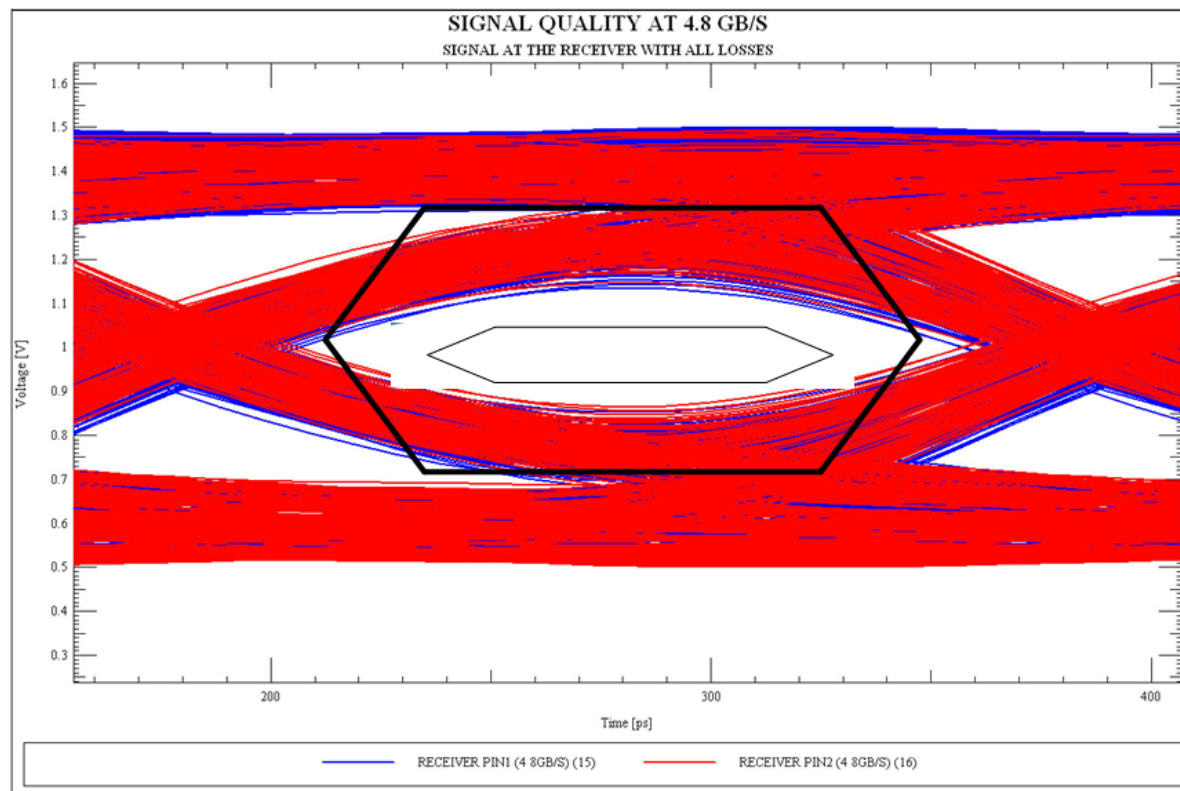
Original minimum amplitude requirement was 550 millivolts. New amplitude requirement is 150 millivolts. Latest Xilinx receiver requires only 5 millivolts.

POSSIBLE LOWER LOSS LAMINATES

- **There are two types of lower loss laminates**

  - **A. Glass reinforced**
  - **B. Non glass reinforced**

- **Glass reinforced laminates of choice**

  - **Isola I-TERA, I-SPEED, TACHYON, TERAGREEN, CHRONON,**
  - **Nelco 4000-13SI**
  - **Rogers 4350**
  - **Megtron 6**
  - **Doosan DS-7409DV**

- **Non glass reinforced laminates**

  - **For high layer count PCBs, none work well**
  - **For low layer count PCBs various Rogers materials work**

WHEN LOWER LOSS LAMINATES ARE NOT ENOUGH WHAT NEXT?

- When the lowest possible loss laminate is used and the signal is still too small use:

- Pre-emphasis

- De-emphasis (Same as pre-emphasis, different supplier)

- Post-emphasis

- Use adaptive transceivers- these use a combination of pre and post emphasis to compensate for path losses. Some newer transceivers can compensate for 38 db of path loss!

AN EXAMPLE WHERE LOSS AND JITTER IS TOO HIGH

Eqn eye_rx=eye((T6-T5), 2G, 2, 0ps)
Eqn eye_drv_out=eye((T8-T9), 2G, 2, 0ps)
Eqn eye_brd1_out=eye((T10-T11), 2G, 2, 0ps)
Eqn eye_cable_out=eye((T12-T13), 2G, 2, 0ps)
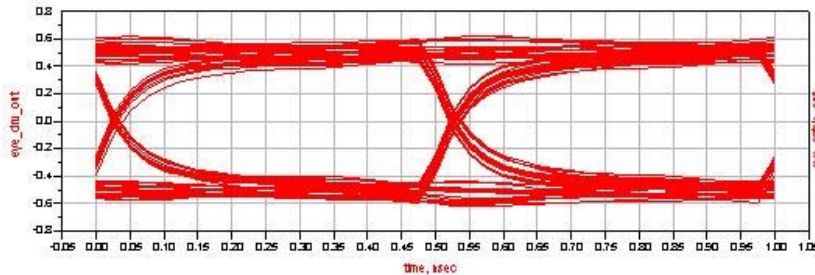
DRIVER OUTPUT   **INPUT TO CABLE**
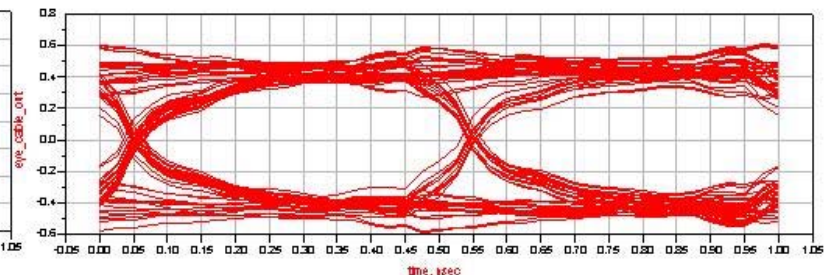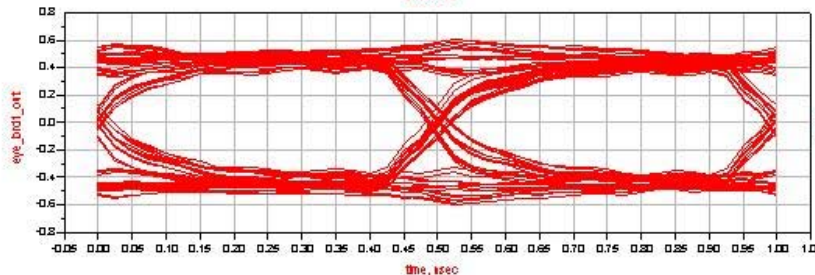
OUTPUT OF CABLE   **RECEIVER INPUT**
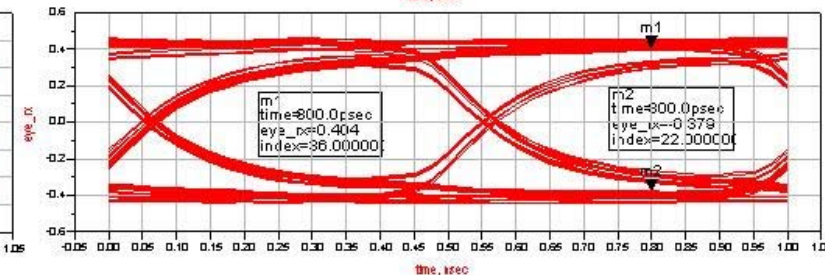
•DATA RATE 5.2 GB//S, NO PRE-EMPHASIS

TIME SCALE- 5 PSec/Division

SIGNAL PATH WITH PRE-EMPHASIS ADDED

Eqn eye_rx=eye((T6-T5), 2G, 2, 0ps)
Eqn eye_drv_out=eye((T8-T9), 2G, 2, 0ps)
Eqn eye_brd1_out=eye((T10-T11), 2G, 2, 0ps)
Eqn eye_cable_out=eye((T12-T13), 2G, 2, 0ps)
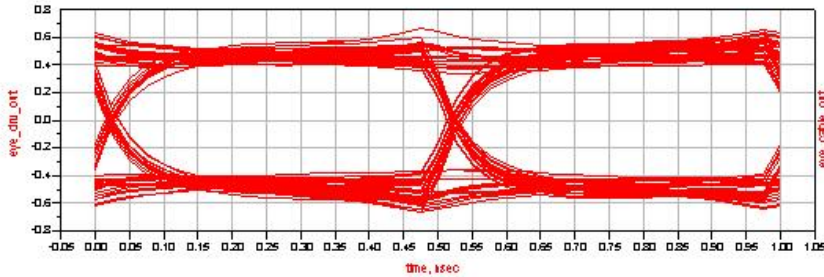
DRIVER OUTPUT   **INPUT TO CABLE**
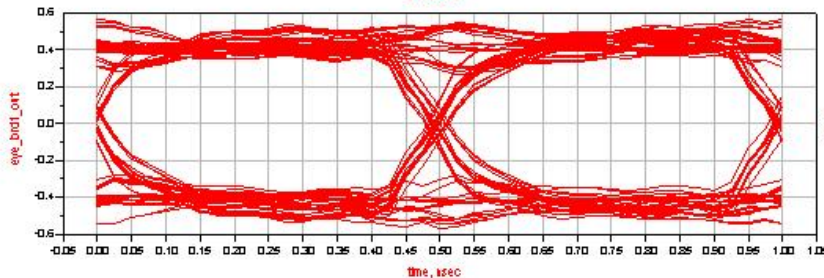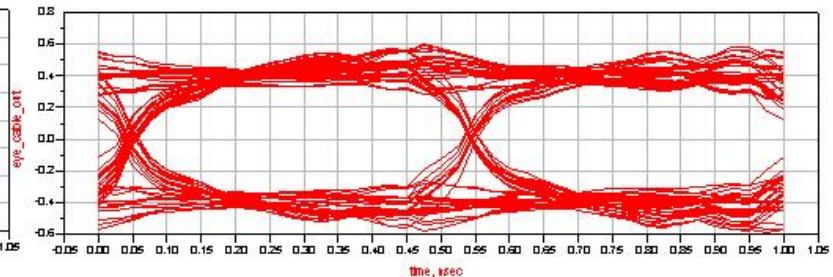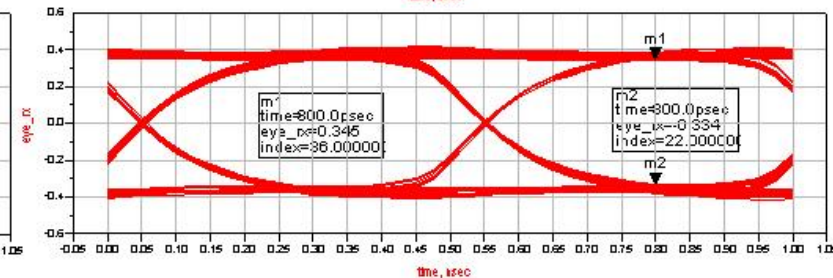
OUTPUT OF CABLE   **RECEIVER INPUT**

•DATA RATE 5.2 GB//S- WITH PRE-EMPHASIS

TIME SCALE- 5 PSec/Division

WHAT PRE-EMPHASIS LOOKS LIKE
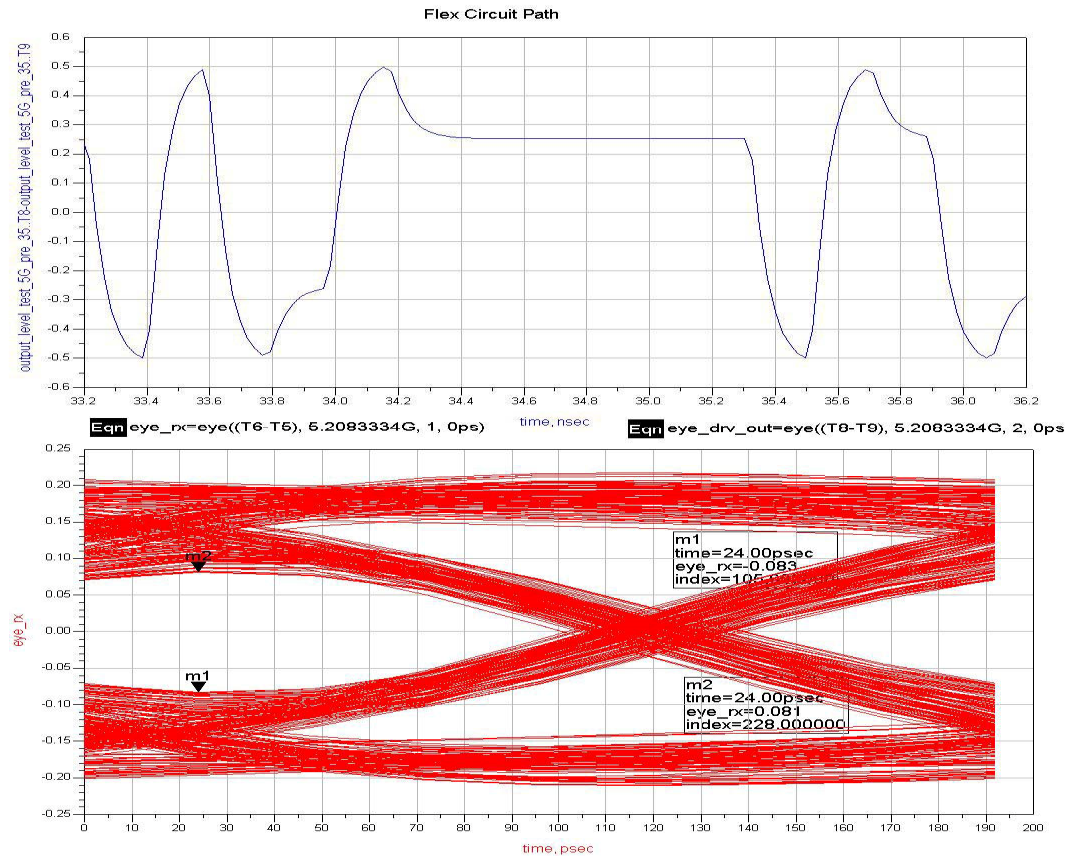
When the data changes polarity, the first bit is made larger than those that follow. This adds back some of the high frequency energy lost in the data path, improving the signal amplitude at the receiver.

SOURCES OF SIGNAL DEGRADATION IN HIGH SPEED DIFFERENTIAL SIGNALING

- There are number of potential sources of signal degradation in high speed data paths. Among these are:

- Copper losses

- Dielectric losses

- Skew

- Cross talk

- Vias and plated through holes

  Right angle bends are not sources of degradation as has been demonstrated many time in tests performed on actual hardware, including tests PCBs used in this course.

DEALING WITH COPPER LOSSES IN THE DATA PATH

- Copper loss can be affected by basic copper conductivity, surface roughness and surface area of the conductor.

- All copper foils used in PCB laminates are plated on a drum rather than rolled and annealed. Therefore, there is not much one can do to change this.

- Copper surface roughness as manufactured can vary in roughness. From very smooth to quite rough.

- The process a fabricator uses to treat the exposed copper can affect loss by increasing the surface roughness.

- Surface area affects loss. Wider traces result in lower loss by increasing the surface area. Thicker copper does not result in lower loss due to skin depth issues.

THE CONCEPT OF SKIN DEPTH

- **As the frequency of a signal traveling on a conductor increases, the depth to which the current flows decreases.**

- **As soon as the thickness of a trace exceeds two times the skin depth of the current at the frequency of interest, adding more copper or increasing the thickness of the conductor does not reduce copper loss.**

- **If the roughness of the copper exceeds the skin depth, surface roughness becomes a significant player in the path loss.**

SKIN DEPTH VS. FREQUENCY

Skin Depth Microns vs Frequency GHz Copper
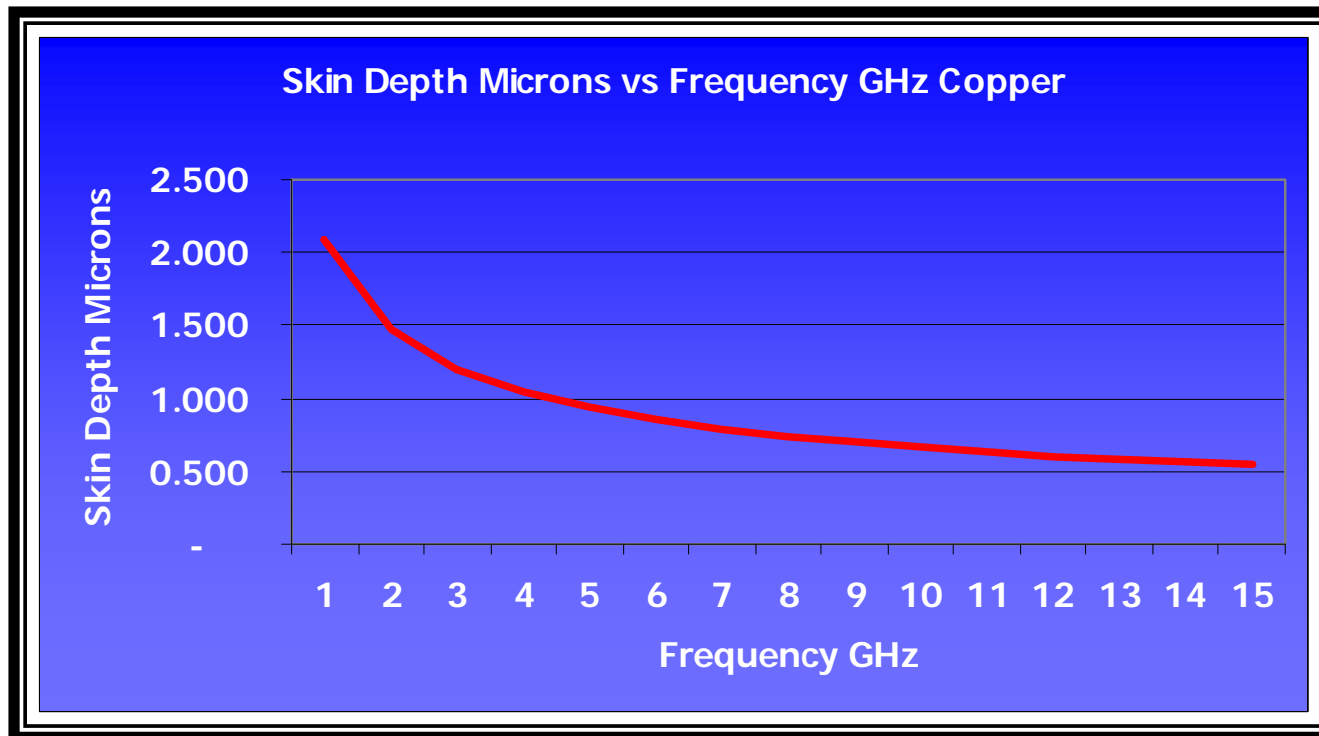
Notice that at 1 GHz, skin depth is 2 microns or 80 micro inches. Trace layers thicker than ½ ounce copper do not help above this frequency. (All high speed serial links are 2.4 Gb/S or higher.)

Therefore, ½ ounce signal layers (700 micro inches) are 'good enough" for all high speed serial links found in modern electronic systems.

REDUCING LOSS BY INCREASING TRACE WIDTH

- Reducing loss by increasing trace width and, therefore, surface area seems tempting.

- Increasing trace width reduces impedance.

- To maintain the 50 ohm impedance required by differential pairs, the dielectric thickness must increase, increasing the overall thickness of the PCB.

- Increasing the PCB thickness also increases its cost due to the need for more material.

- Increasing the PCB thickness also increases the parasitic capacitance of the plated through holes.

- The next slide shows effect of increasing trace width on loss improvement.

AN EXAMPLE OF SKIN EFFECT AND DIELECTRIC LOSS IN A SIGNAL PATH

•.127, .152, .178, .203, .229, & .254 mm wide traces, 84 cm long

Skin Effect Loss, 5, 6, 7, 8, 9 10 mil wide, 33" long trace

Dielectric Loss, TanD .009, .014, .020; 33" long trace
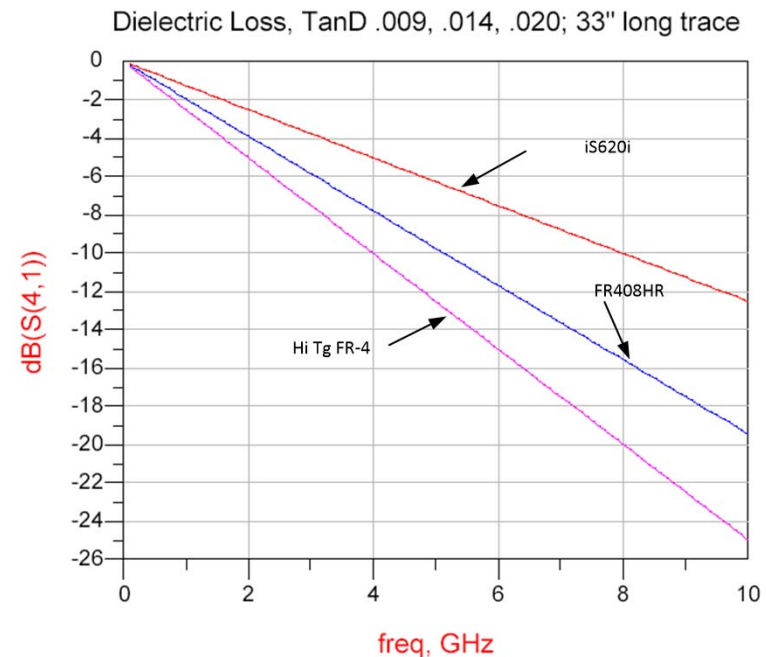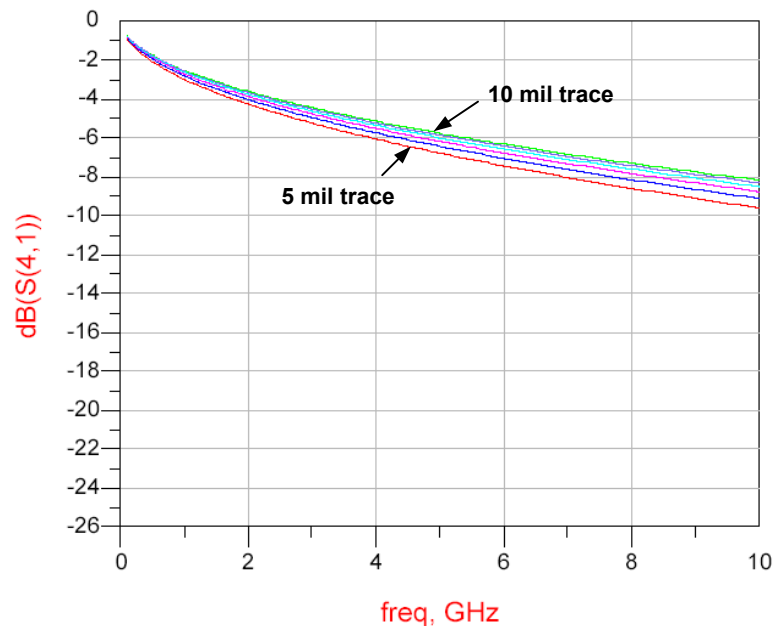
Dielectric loss dominates the loss problem for most common laminates used to fabricate PCBs. Changing to a lower loss dielectric is much better than using wider traces to reduce skin effect losses as wider traces result in thicker PCBs, higher crosstalk and larger via capacitance.

TRACE WIDTH CONCLUSIONS

- From the previous slide, varying trace width from 5 mils (127 microns) to 10 mils (254 microns) reduces skin effect loss at 2.5 GHz (5 Gb/S) approximately 1 db for 33" (84 cm) long trace.

- Changing trace width from 5 mils to 10 mils results in a PCB that is often as much as twice as thick. (This makes cost go up and plating more difficult.)

- Changing from a lossy dielectric to a less lossy dielectric has a much bigger impact on overall loss.

- To minimize overall loss and maximize manufacturability, it is wise to use lower loss laminate and minimize trace width. (My standard trace width is 4 mils (81 microns) even at 10 Gb/S.

COPPER FOIL FINISHES

- There are several types of surface finish available on copper foils as purchased by laminate manufactures for use in creating laminates.

- The two most common are reverse treat (RTF) and very low profile (HVLP).

- If the surface finish is not specifically called out on a fabrication drawing, the copper will be reverse treat (RTF).

- Reverse treat has a rough finish to promote adhesion during lamination. This rough finish is much larger than the skin depth at frequencies above 2 GHz resulting in higher than expected losses.

- The next slide shows the difference in loss for two traces of the same width and length using the two copper finishes.

LOSS DIFFERENCE BY CHANGING FROM STANDARD REVERSE TREAT COPPER TO VLP COPPER

GigaSync dB Loss vs. Freq for 8" Trace

—— Cu=VLP —— Cu=RTF
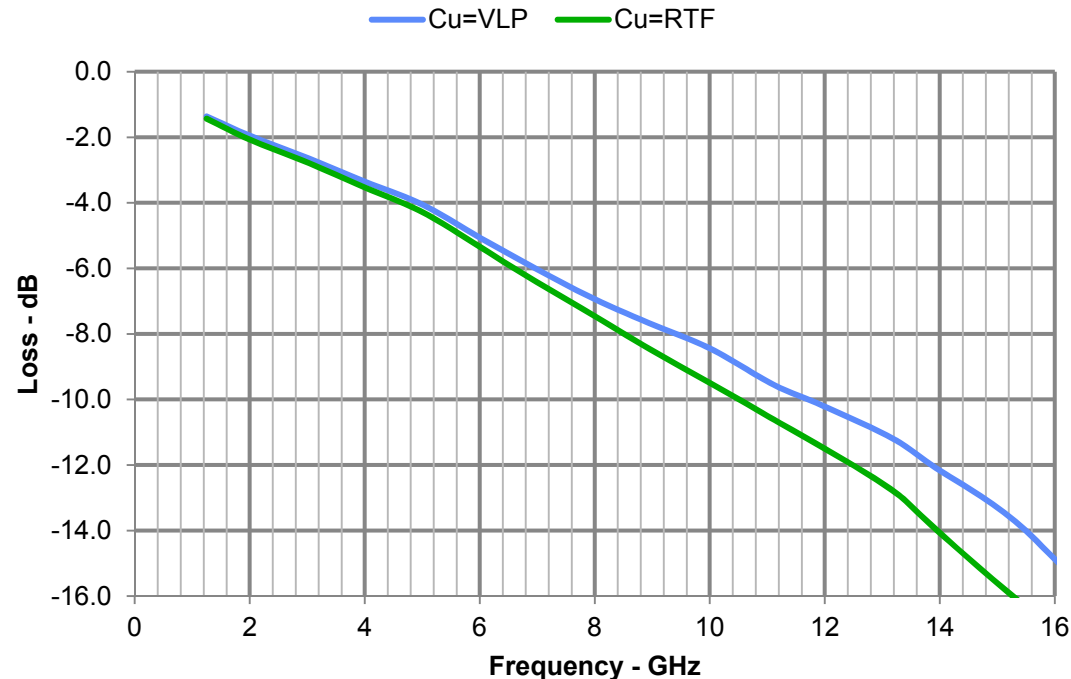
Reverse treat copper is the standard copper foil finish supplied by nearly all laminate suppliers. VLP (very low profile) copper is a foil that can be specified for very high frequency applications to reduce skin effect loss at high data rates. It is necessary when data rates exceed 10 Gb/S with long signal paths.

Cross Sections of Traces on Previous Slide

HVLP FOIL

REVERSE TREAT FOIL

HVLP copper has a surface roughness of 2 microns. RTF copper has a surface roughness of 7 microns.

Copper Loss Due to Fabricator Treatment
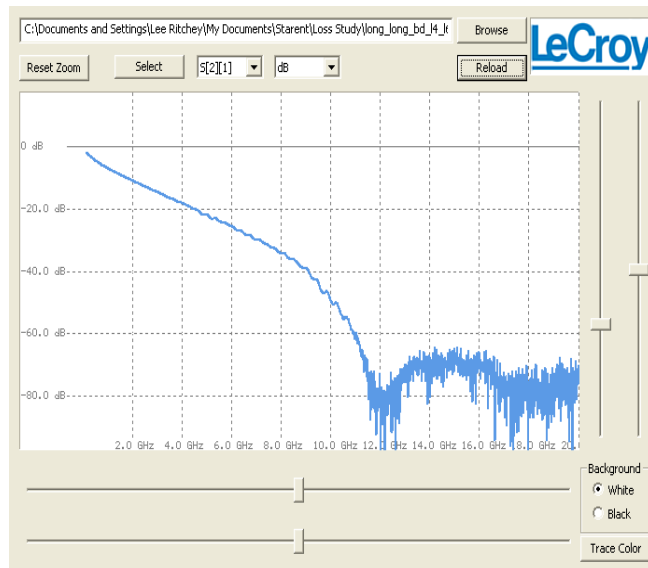
35 db at 8 GHz
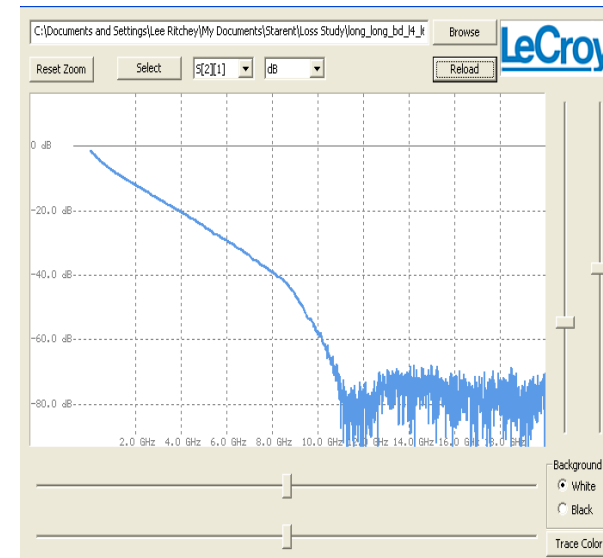
40 db at 8 GHz

Two PCBs built at two different fabricators using the same materials and the same stackup yield different losses due to differing surface roughness done during processing. Copper roughness has been left to each fabricator. With the advent of 10 Gb/S and higher signal paths, this is no longer allowable. Test structure is 7" Daughterboard made from FR408HR, 13" backplane made from Megtron 6 and 7" daughter board made from FR408HR. Only daughter boards were from different fabricators.

CROSS SECTION OF TWO PCBS ON PREVIOUS SLIDE

Supplier # 1 No Oxide

Supplier # 2 Oxide

Good Loss

Poor Loss

Slide
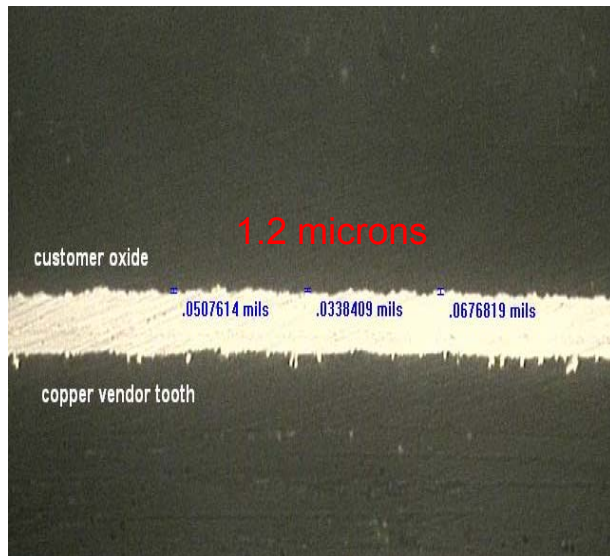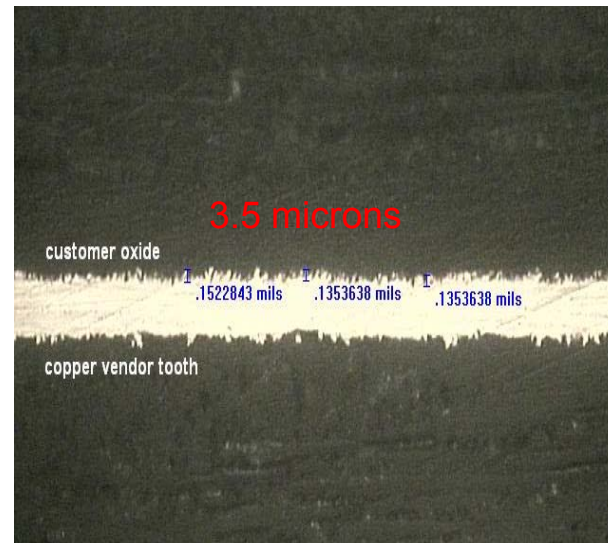
DEALING WITH DIELECTRIC LOSSES IN THE DATA PATH

- Dielectrics used in multilayer PCBs are made of two components. These are:

- Woven glass cloth for mechanical strength.

- Organic resin systems that provide the adhesive strength to hold the layers together.

- Each of these has its own dielectric constant and dielectric loss.

- Laminate manufactures combine these two to create laminate.

- Either the glass or the resin system or both may be modified to reduce loss.

GLASS CLOTH CHOICES

- There are two basic glass choices available for weaving the cloth used in laminate. All glasses are alloys of silicon dioxide and other minerals. These choices are:

  E glass- The most common glass used to make fiber glass cloth. This glass style is formulated to produce glass fibers at a low cost that adhere well to resins.

  S glass- This is a formulation that has been designed to minimize loss. It is more difficult to spin and does not adhere to resins as well as does E glass. It is more expensive and is single sourced around the world. The primary laminate system using this glass style is Nelco 4000-13SI and its derivatives.

RESIN SYSTEM CHOICES FOR LOW LOSS

- There are a number of resin systems formulated to reduce loss in the data path. The primary players in the low loss laminate market for high layer count PCBs are:

- Isola- I-TERA, TACHYON, CHRONON

- NELCO- 4000-13SI and derivatives

- PANASONIC- MEGTRON 6

- DOOSAN- DS-7409DV

- Other laminate suppliers, such as Rogers, are not considered candidates because their products are not appropriate for high layer count PCBs.

COMMON DIELECTRIC LOSS TEST METHODS

- There are two common test methods used by the laminate industry to measure loss tangent, or dissipation factor, Df. These are:

- Split Post Cavity Method

- Bereskin Method

- We have done many tests to see which method yields results that are most accurate in order to provide good data to our simulation tools.

- The Split post cavity method yields loss tangents that are as much as 30% lower than the actual value.

- The Bereskin method yields loss tangents that are within 5% of the actual value we measure.

COMPARISON OF TWO COMMON LAMINATE TEST METHODS

Test Method	Frequency (GHz)	GETEK	FR408	IS415	IS620
Split Post Cavity Dissipation Factor (Df)	2 GHz	0.0099	0.0084	0.0095	0.0044
	5 GHz	0.0102	0.0089	0.0096	0.0050
	10 GHz	0.0110	0.0089	0.0096	0.0053
Bereskin Stripline Dissipation Factor (Df)	2 GHz	0.0140	0.0120	0.0129	0.0060
	5 GHz	0.0141	0.0127	0.0130	0.0066
	10 GHz	0.0141	0.0125	0.0130	0.0071

If a laminate data sheet lists Df using the split post cavity method, increase that value by 25% when comparing the material to one using the Bereskin method. Do the same when performing simulations.

LOSS vs. FREQUENCY FOR SEVERAL LAMINATES
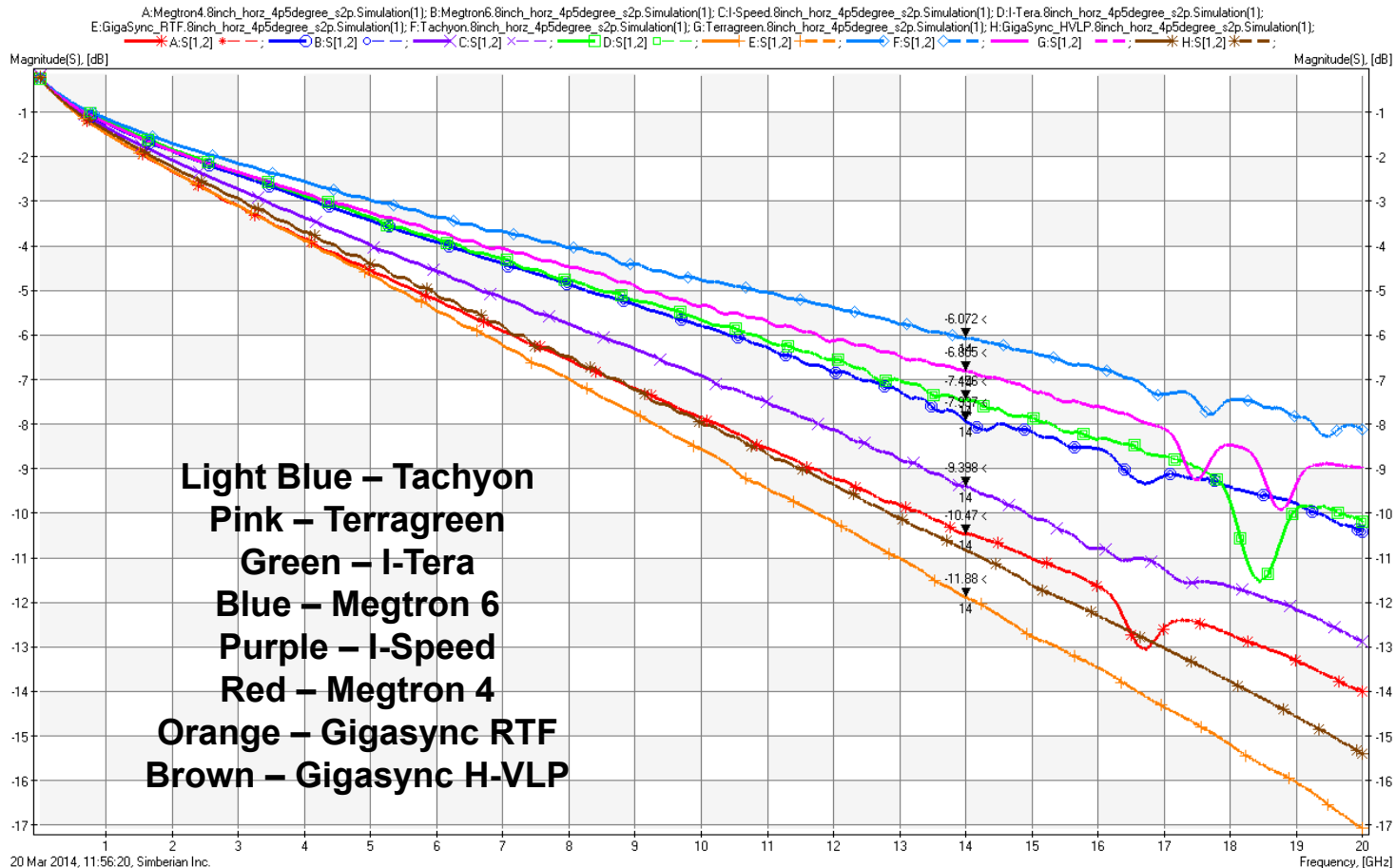
Data taken from Speeding Edge test PCBs.

THE MERITS AND DRAWBACKS OF USING LOW DK LAMINATES IN HIGH SPEED PCBs

- **There are those who advocate using low loss laminates for a variety of reasons.**

- **This section will examine those reasons for this and their merits and drawbacks.**

REASONS LOW DK LAMINATES ARE USED

- Low DK (dielectric constant or e_r) laminates can provide some advantages when designing PCBs that are used for very high data rate paths. Among these are:

1. For a given trace width selected to produce a given impedance, the laminate used between the trace and its adjacent plane can be thinner resulting in an overall thinner PCB.

2. For a given thickness of laminate selected to produce a given impedance, the trace width can be wider resulting in lower signal loss due to skin effect loss in the trace.

- Each of these choices has some undesirable side effects that will be discussed in this presentation.

AN IMPEDANCE EQUATION SHOWING HOW DK (DIELECTRIC CONSTANT) AFFECTS IMPEDANCE

- The equation shown below has often been used to calculate the impedance of a surface microstrip transmission line. It has been shown to be inaccurate with the dimensions used in modern PCBs but it illustrates how DK or e_r affects impedance.

- The variables are: H = height above plane, W = trace width, T = trace thickness, e_r = relative dielectric constant or DK, Zo = impedance in ohms

- Notice that lowering er results in higher impedance and raising e_r results in a lower impedance.

$$Z_0 = \frac{79}{\sqrt{e_r + 1.41}} \ln\left(\frac{5.98\,H}{0.8W + T}\right)$$

ON USING LOW DK LAMINATES TO REDUCE OVERALL PCB THICKNESS

- The larger, high layer count backplanes used in products such as Internet core routers and switches can be as thick as 400 mils (10 mm). This thickness presents several problems among them are:

  – Drilling and plating of the through holes may be difficult.

  – The parasitic capacitance of these long, large holes may adversely affect signal quality at very high data rates necessitating "back drilling" to remove most of the unwanted copper in the holes.

- A lower DK laminate would reduce the thickness of the laminate needed to achieve the desired impedance, reducing the overall thickness of the PCB and hole capacitance.

- The down side of using a lower DK laminate is higher cost and limited flexibility on materials choices, usually single source.

ON USING LOWER DK LAMINATES TO ACHIEVE WIDER TRACES

- From the equation on a previous slide it can be seen that for a given height above the plane, a lower DK laminate allows the use of a wider trace for a given target impedance.

- The motivation for using wider traces is to reduce the signal loss resulting from the "skin effect" phenomenon by increasing the surface area of the trace.

- As with the attempt to reduce thickness by using low DK laminates, this will result in a more expensive PCB as well as a limited set of source for the materials.

- Is the added cost and limited materials availability worth it?

AN ANALYSIS OF LOSS vs. TRACE WIDTH

- **The curves below show the reduction in loss vs. change in trace width of a 33" (84 cm) stripline signal path when the trace width is varied from 5 mils (127 microns) to 10 mils (254 microns) on the left side.**

- **On the right hand side is the reduction in loss by using a lower loss laminate.**

Skin Effect Loss, 5, 6, 7, 8, 9 10 mil wide, 33" long trace

10 mil trace

5 mil trace

Dielectric Loss, TanD .009, .014, .020; 33" long trace

iS620i

FR408HR

Hi Tg FR-4
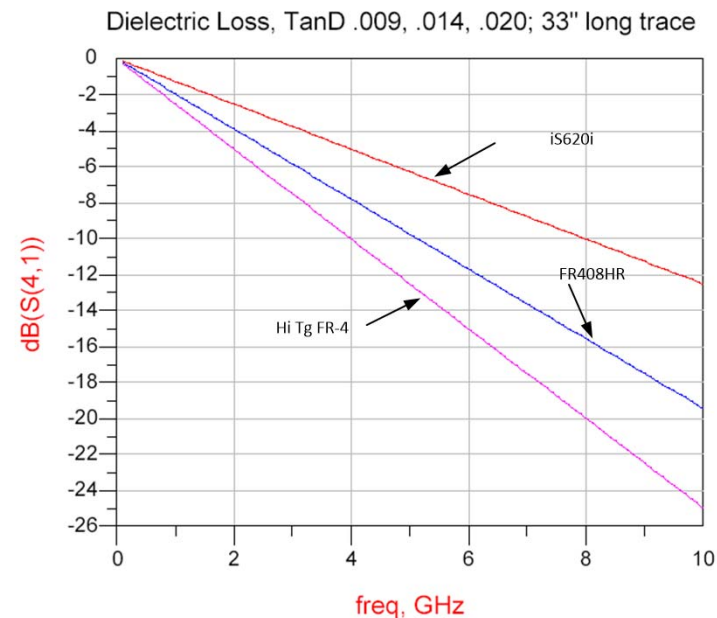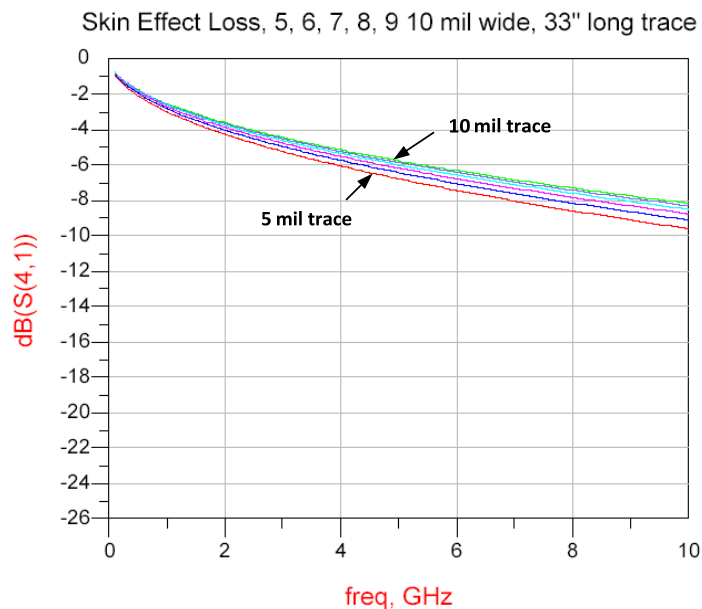
22 LAYER STACKUP USING 4 MIL (101 MICRON) WIDE STRIPLINE TRACES – 106 MILS (2.65 MM) THICK

	Layer #	Material Name	Material Type	Material Construction	Material Unpressed Er (at ~2 GHz)	Material Pressed Er (at ~2 GHz)	Material Unpressed Thickness (mils)	Material Pressed Thickness (mils)	Picture	Copper Thickness (mils)	Copper Thickness (oz)	Single Ended Trace Width (mils)	Single Ended Imped. (ohms)
GENERIC 22 LAYER SWITCH FABRIC PCB STACKUP 09/03/09													
								0.7	Solder Mask				
Top	1								1	2.2	1.5		
		FR-408	Prepreg	1 x 3313 RC = 53.8%	3.7		4	3.4	Prepreg				
S1	2								2	0.6	0.5	4.5	50.0
		FR-408	Core	1 x 2113 RC = 44%	4.2			3	Core				
Ground	3								3	0.6	0.5		
		FR-408	Prepreg	1 x 2113 RC = 57%	4		4	3	Prepreg				
V1	4								4	0.6	0.5		
		FR-408	Core	1 x 3313 RC = 53.8%	3.7			4	Core				
S2	5								5	0.6	0.5	4	51.0
		FR-408	Prepreg	1 X 3313 RC + 1 X 106 = 56%	3.7		6.5	6	Prepreg				
Ground	6								6	0.6	0.5		
		FR-408	Core	1 x 3313 RC = 53.8%	3.7			4	Core				
S3	7								7	0.6	0.5	4	51.0
		FR-408	Prepreg	1 X 3313 RC + 1 X 106 = 56%	3.7		6.5	6	Prepreg				
Ground	8								8	0.6	0.5		
		FR-408	Core	1 x 3313 RC = 53.8%	3.7			4	Core				
S4	9								9	0.6	0.5	4	51.0
		FR-408	Prepreg	1 X 3313 RC + 1 X 106 = 56%	3.7		6.5	6	Prepreg				
Ground	10								10	0.6	0.5		
		FR-408	Core	1 x 2113 RC = 44%	4.2			3	Core				
V2	11								11	0.6	0.5		
		FR-408	Prepreg	2 x 106 RC = 63.3%	3.7		4	3.4	Prepreg				
Ground	12								12	0.6	0.5		
		FR-408	Core	1 x 2113 RC = 44%	4.2			3	Core				
V3	13								13	0.6	0.5		
		FR-408	Prepreg	1 X 3313 RC + 1 X 106 = 56%	3.7		6.5	6	Prepreg				
S7	14								14	0.6	0.5	4	51.0
		FR-408	Core	1 x 3313 RC = 53.8%	3.7			4	Core				
Ground	15								15	0.6	0.5		
		FR-408	Prepreg	1 X 3313 RC + 1 X 106 = 56%	3.7		6.5	6	Prepreg				
S8	16								16	0.6	0.5	4	51.0
		FR-408	Core	1 x 3313 RC = 53.8%	3.7			4	Core				
Ground	17								17	0.6	0.5		
		FR-408	Prepreg	1 X 3313 RC + 1 X 106 = 56%	3.7		6.5	6	Prepreg <-				
S9	18								18	0.6	0.5	4	51.0
		FR-408	Core	1 x 3313 RC = 53.8%	3.7			4	Core				
V6	19								19	0.6	0.5		
		FR-408	Prepreg	2 x 106 RC = 63.3%	4		4	3	Prepreg				
Ground	20								20	0.6	0.5		
		FR-408	Core	1 x 2113 RC = 44%	4.2			3	Core				
S10	21								21	0.6	0.5	4.5	50.0
		FR-408	Prepreg	1 x 3313 RC = 53.8%	3.7		4	3.4	Prepreg				
Bottom	22								22	2.2	1.5		
								0.7	Solder Mask				
							89.6	106.0		16.4			
							Material Thickness	Total Thickness		Copper Thickness			

Speeding Edge, SPRING 2018

22 LAYER STACKUP USING 8 MIL (203 MICRON) WIDE STRIPLINE TRACES – 160 MILS (4 MM) THICK

GENERIC 22 LAYER SWITCH FABRIC PCB STACKUP 09/03/09

	Layer #	Material Name	Material Type	Material Construction	Material Unpressed Er (at ~2 GHz)	Material Pressed Er (at ~2 GHz)	Material Unpressed Thickness (mils)	Material Pressed Thickness (mils)	Picture	Copper Thickness (mils)	Copper Thickness (oz)	Single Ended Trace Width (mils)	Single Ended Imped. (ohms)
								0.7	Solder Mask				
Top	1									2.2	1.5		
		FR-408	Prepreg	1 x 3313 RC = 53.8%	3.7	4		3.4	Prepreg				
S1	2									0.6	0.5	8	50.0
		FR-408	Core	1 x 2113 RC = 44%	4.2			9	Core				
Ground	3									0.6	0.5		
		FR-408	Prepreg	1 x 2113 RC = 57%	4	4		3	Prepreg				
V1	4									0.6	0.5		
		FR-408	Core	1 x 3313 RC = 53.8%	3.7			9	Core				
S2	5									0.6	0.5	8	50.0
		FR-408	Prepreg	1 X 3313 RC + 1 X 106 = 56%	3.7		6.5	8	Prepreg				
Ground	6									0.6	0.5		
		FR-408	Core	1 x 3313 RC = 53.8%	3.7			9	Core				
S3	7									0.6	0.5	8	50.0
		FR-408	Prepreg	1 X 3313 RC + 1 X 106 = 56%	3.7		6.5	8	Prepreg				
Ground	8									0.6	0.5		
		FR-408	Core	1 x 3313 RC = 53.8%	3.7			9	Core				
S4	9									0.6	0.5	8	50.0
		FR-408	Prepreg	1 X 3313 RC + 1 X 106 = 56%	3.7		6.5	8	Prepreg				
Ground	10									0.6	0.5		
		FR-408	Core	1 x 2113 RC = 44%	4.2			3	Core				
V2	11									0.6	0.5		
		FR-408	Prepreg	2 x 106 RC = 63.3%	3.7	4		3.4	Prepreg				
Ground	12									0.6	0.5		
		FR-408	Core	1 x 2113 RC = 44%	4.2			3	Core				
V3	13									0.6	0.5		
		FR-408	Prepreg	1 X 3313 RC + 1 X 106 = 56%	3.7		6.5	8	Prepreg				
S7	14									0.6	0.5	8	50.0
		FR-408	Core	1 x 3313 RC = 53.8%	3.7			9	Core				
Ground	15									0.6	0.5		
		FR-408	Prepreg	1 X 3313 RC + 1 X 106 = 56%	3.7		6.5	8	Prepreg				
S8	16									0.6	0.5	8	50.0
		FR-408	Core	1 x 3313 RC = 53.8%	3.7			9	Core				
Ground	17									0.6	0.5		
		FR-408	Prepreg	1 X 3313 RC + 1 X 106 = 56%	3.7		6.5	8	Prepreg <-				
S9	18									0.6	0.5	8	50.0
		FR-408	Core	1 x 3313 RC = 53.8%	3.7			9	Core				
V6	19									0.6	0.5		
		FR-408	Prepreg	2 x 106 RC = 63.3%	4	4		3	Prepreg				
Ground	20									0.6	0.5		
		FR-408	Core	1 x 2113 RC = 44%	4.2			9	Core				
S10	21									0.6	0.5	8	50.0
		FR-408	Prepreg	1 x 3313 RC = 53.8%	3.7	4		3.4	Prepreg				
Bottom	22									2.2	1.5		
								0.7	Solder Mask				
								143.6	160.0	16.4			
								Material Thickness	Total Thickness	Copper Thickness			

CONCLUSIONS FROM ANALYSIS OF PREVIOUS SLIDES

- On a previous slide if one examines the loss change at 2.5 GHz, roughly 5 Gb/S by changing the trace width from 5 mils to 10 mils (possible only by reducing DK by more than half, it is only 1 db improvement over a path that is 33" (84 cm) long. This is not a very big gain.

- If one examines the loss change at the same frequency by using a moderately lower loss laminate, the reduction in loss is 2 db.

- If one of the newer ultra low loss laminates is used, the improvement at 2.5 GHz is more than 6 db.

- From previous two slides it can be seen that increasing the trace width from 4 mils to 8 mils increased the thickness of a 22 layer PCB by 60%.

- Clearly, using a lower loss laminate system yields a much bigger improvement in loss than does using a low DK laminate. In the bargain 60% less material is use which could pay for the added cost of the lower loss laminate.

WHAT IS SKEW?

Skew is the misalignment of the two signal edges of a differential pair as they arrive at the terminals of the differential receiver.

To understand how skew causes problems it is useful to review how a differential pair operates.

WHERE DOES SKEW CAUSE PROBLEMS?

- Differential signaling has evolved into the principal way electronic components are connected in the 21st century.

- The part of the Internet that runs in copper traces or wires relies on differential signaling to move data from place to place. Without this protocol, the Internet along with all of the computers and cell phones we rely on to do our daily business would not be possible.

- The latest versions of ICs have made it possible to send data over differential pairs in PCBs at rates as high as 32 Gb/S. At these speeds, very small variations in the laminates used to fabricate PCBs can destroy a data path if care is not taken in how these paths are designed and manufactured. One of the primary variations that destroys data links is skew in a data path.

WHERE DOES SKEW COME FROM?

- Skew or misalignment of the two edges in a differential pair can come from one or more of three places.

- The three places are:

  1. Lack of alignment coming out of the transmitter or going into the receiver due to errors in the length of the connections in the IC packages.
  2. Different path lengths on the PCB and in the connectors.
  3. Differences in flight time on the two paths due to different speeds in the laminate.

1. Modern IC technology is capable of maintaining alignment at the package level to as little as 1 pSec.

2. Modern PCB layout tools and connector manufacturing are capable of matching lengths to as little as 1 pSec.

3. As will be shown in later slides differences of path length as large as 61.5 pSec can be created by the lack of uniformity of the glass weave in the laminate used to fabricate the PCB.

HOW DOES SKEW AFFECT DIFFERENTIAL PAIRS?

- When the two signals of a differential pair arrive at the receiver at different times the receiver can misinterpret what data bits are being sent.

- This results in lost data or data that has errors in it.

- If the error rate exceeds the ability of the data path to correct for errors the link fails which can cause serious problems.

DIFFERENTIAL PAIR USED IN THIS PRESENTATION

U1.1

TDR

TL1

49.8 ohms
527.070 ps
3.000 in
Stripline

U3.1

TDR

R1

100.0 ohms

U2.1

TDR

TL2

49.8 ohms
527.070 ps
3.000 in
Stripline

U4.1

TDR
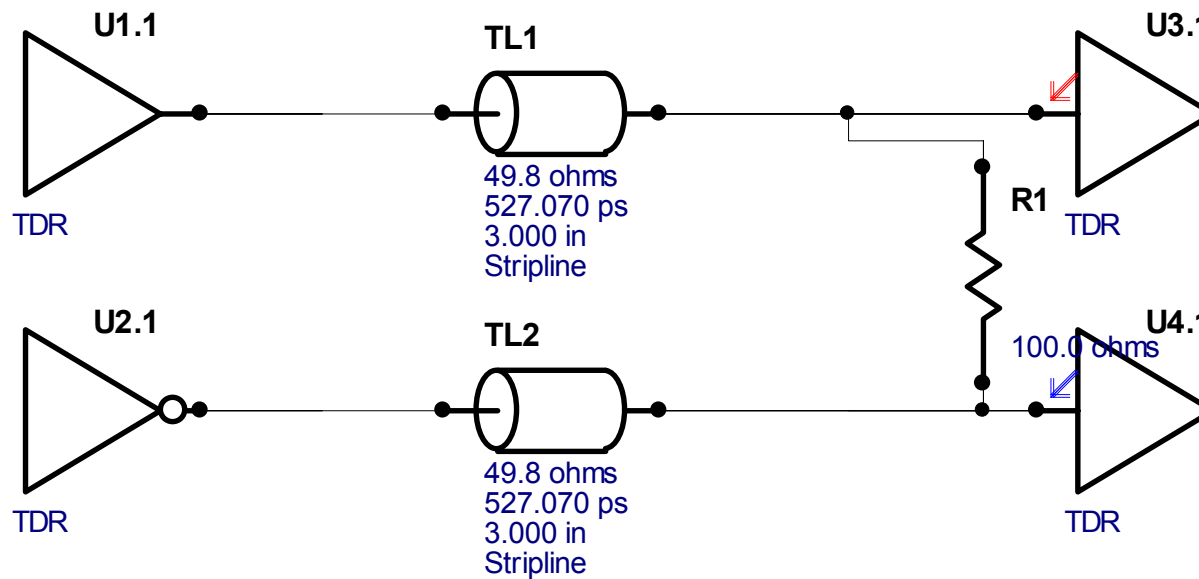
Note: Differential impedance has nothing to do with proper operation of this data path. There are two "good" 50 ohm transmission lines here, each terminated in 50 ohms. In this case, the "ground" connection of the two 50 ohm resistors was not needed, so a single 100 ohm terminating resistor was used.

A PERFECTLY ALIGNED 2.5 Gb/S DIFFERENTIAL PAIR SIGNAL. (TWO DATA BITS SHOWN)
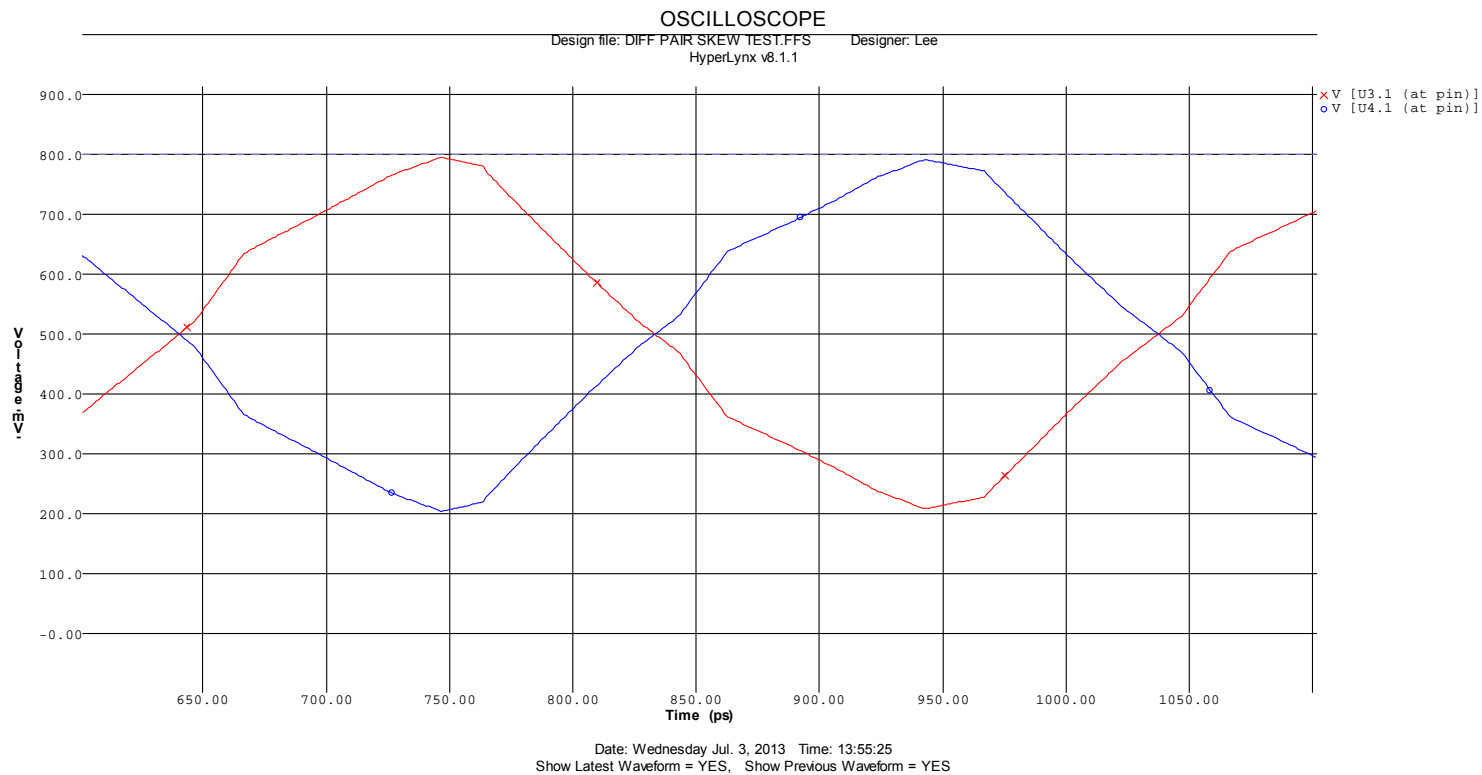
Note how the eye is fully open with a perfectly aligned signal pair and the crossing is centered.

2.5 Gb/S, 2 each 3" Lines

A 2.5 Gb/S DIFFERENTIAL PAIR WITH ONE SIGNAL ARRIVING 40 pSEC BEFORE THE OTHER
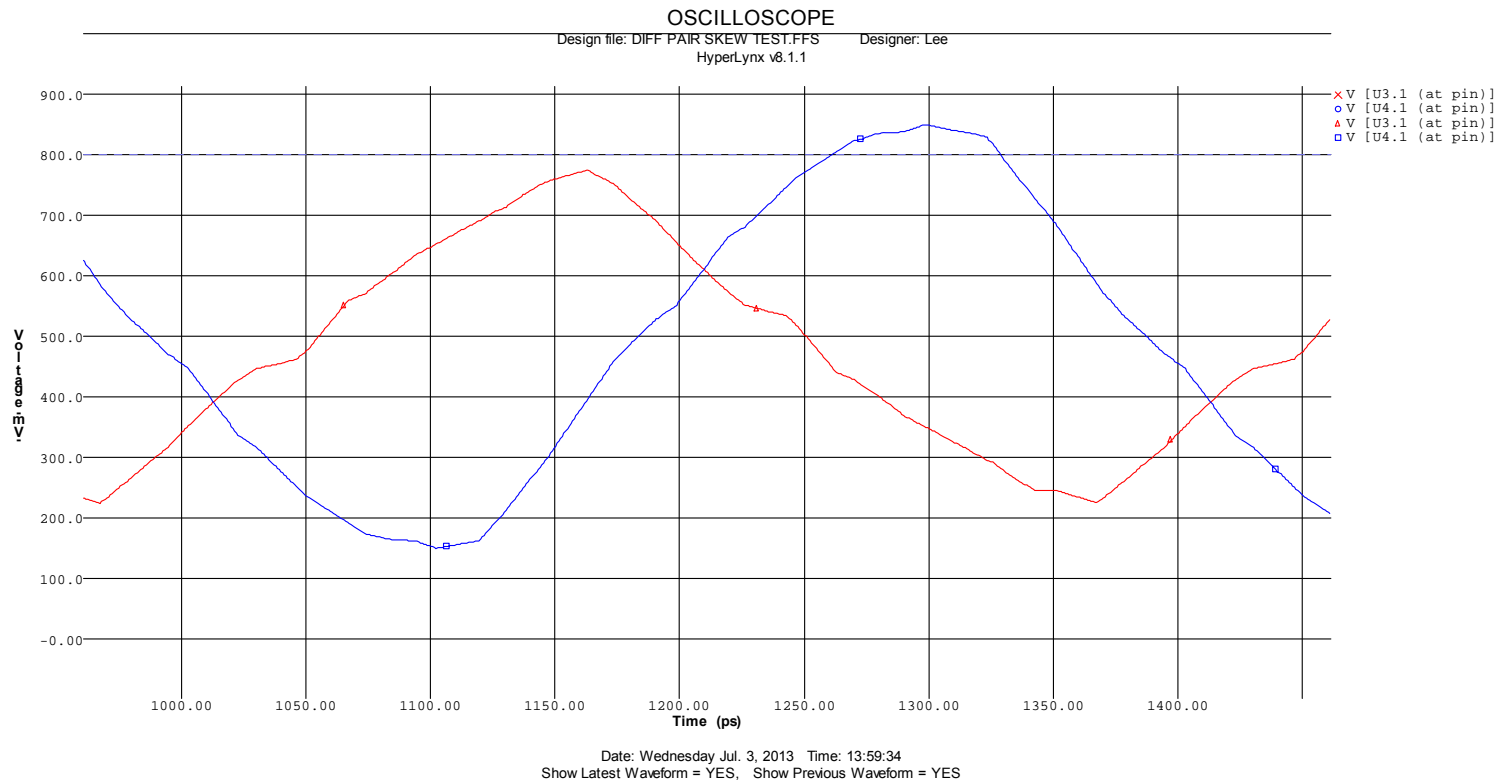
Note how eye is not as open as the perfectly aligned signal pair and the crossing is no longer centered.

2.5 Gb/s, 1- 3" Line, 1-2.75" Line, Delta = 40 pSec

A 2.5 Gb/S DIFFERENTIAL PAIR WITH ONE SIGNAL ARRIVING 80 pSEC BEFORE THE OTHER
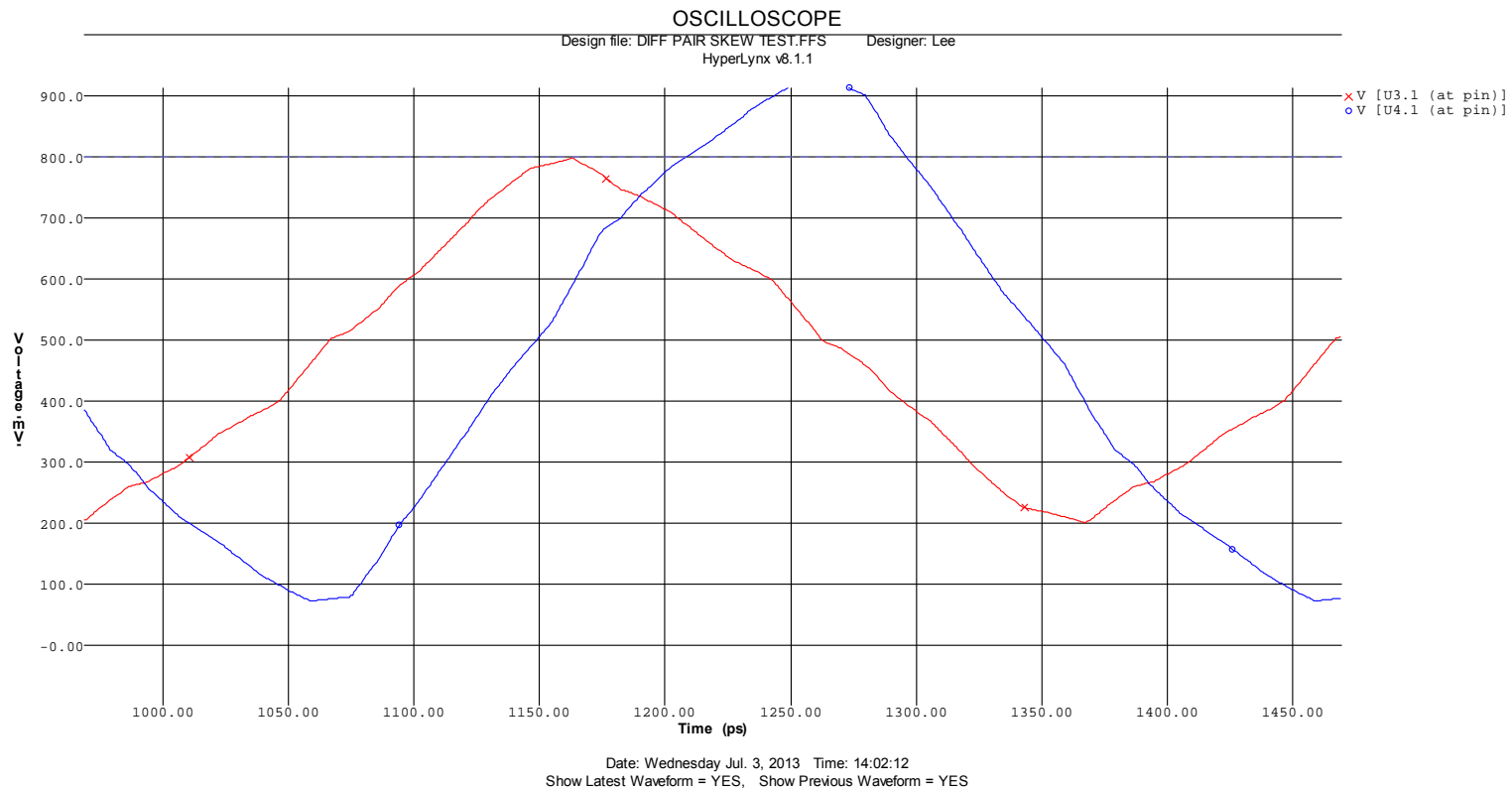
Note how eye is almost closed and crossing is far away from centered.

2.5 GHz, 1- 3" Line, 1-2.50" Line, Delta = 80 pSec

SOME COMMON DATA RATES AND THEIR UNIT INTERVALS.

DATA RATES Gb/S	UNIT INTERVAL (pSec)	QUARTER UNIT INTERVAL (pSec)
1	1000	250
2.4	416	104
3.125	320	80
5	200	50
6.125	180	45
10	100	25
13.5	74	18.8
27	37	9.25
40	25	6.25
100	10	2.5

A UI is a unit interval or one data bit in length.

While there is no standard amount of skew that a differential link can tolerate, the generally accepted amount is one quarter UI before signal quality degrades and data is lost.

TEST PCB USED TO COLLECT SKEW DATA
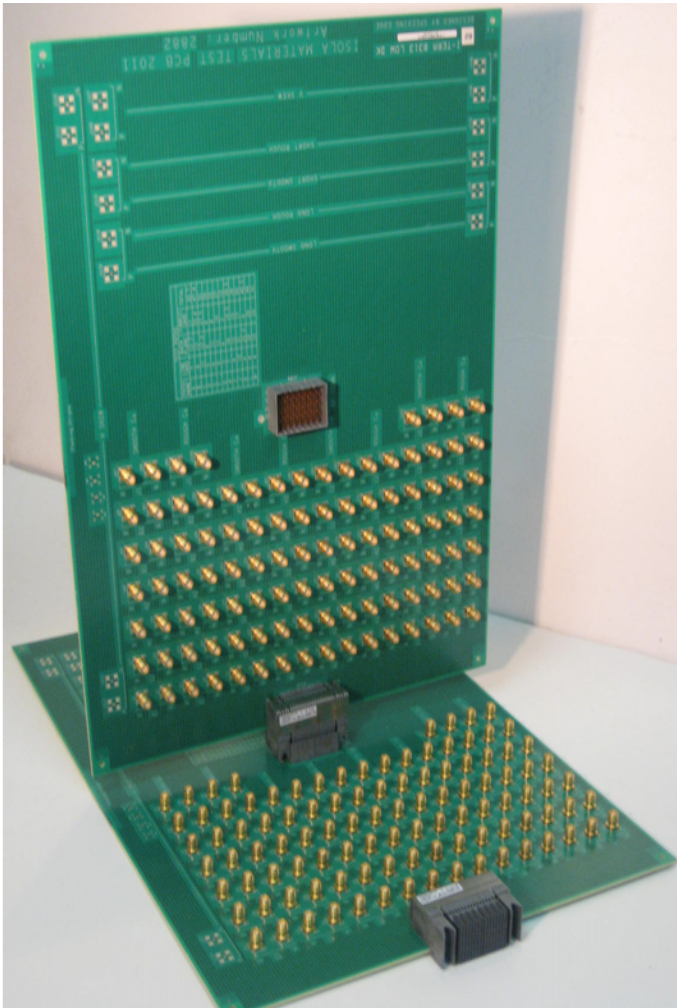
Test PCBs are designed to allow mating them in a daughter card-backplane-daughter card configuration.

Each test PCB was designed with differential pair paths that vary from 9" to 60".

This allows plugging any combination of laminates together to measure actual losses in proposed signal paths.

Both horizontal and vertical differential pairs are routed on each PCB.

SKEW IN A TEST PCB THAT HAS STANDARD 3313 AND 8313 GLASS WEAVE CLOTH

TEST PCB SKEW DATA, pSec 6 SAMPLES								
			VERTICAL (fill) 9"			HORIZONTAL (grain) 14"		
MATERIAL	WEAVE	MINIMUM	MAXIMUM	AVERAGE		MINIMUM	MAXIMUM	AVERAGE
IS415	3313	0	4	2.5		15	61.5	44
FR408HR	3313	0.5	4	2.5		1.5	21.5	10
FR408HRIS	8313	0	3.5	2.3		3	10	5.9
I-SPEED	3313	1.5	5	2.25		0.5	29.5	9
I-SPEED LOW DK	8313	0.5	2	1.15		2.5	6	3.75
I-TERA	3313	0.5	6	3		0.5	6.5	4.75
I-TERA LOW DK	8313	0.5	2	1.25		2	29.5	12.3

This data was taken from identical test PCBs made with two glass cloth weaves, 3313 and 8313, neither of which was uniformly spread in both directions and made from five different resin systems. Notice skews as large as 61.5 pSec on a 14" (35.56 cm) horizontal differential pair while vertical skew on the 9" line is much smaller.

SKEW IN A TEST PCB THAT WAS FABRICATED WITH A LAMINATE SYSTEM DESIGNED TO MINIMIZE SKEW

Horiz	14"					
J110	43.883	43.923	43.907	43.910	43.883	43.906
J111	43.897	43.930	43.927	43.921	43.889	43.919
Skew	0.014	0.007	0.020	0.011	0.006	0.013
Vert	9"					
J106	42.480	42.473	42.479	42.479	42.474	42.477
J107	42.476	42.466	42.472	42.475	42.474	42.471
Skew	0.004	0.007	0.007	0.004	0.000	0.006

These data were taken from six test PCBs made with the same artwork as those on the previous slide. Notice how much lower the skew is. (The nature of the glass weave is not known.)

The author has recently fabricated PCBs using 2 ply 1067 mechanically spread glass which resulted in skews over two 9" (22.86 cm) paths no greater than 2 pSec.

GLASS WEAVE STYLES AND THEIR EFFECT ON SKEW

- Glass cloth woven for use in the fabrication of PCBs comes in many styles. The most commonly used glass cloth styles are shown in the following slides.

- Glass cloth styles are known by numerical designations such as 106, 1035, 1067, 1080, 1086, 2116, 3313 and so on.

- There are standards that define how many threads per inch and the size of the threads for each of these styles.

- However, there are no standards for how each bundle of glass is formed.

- Each bundle may be tightly twisted or spread out and still satisfy the standard. As will be shown, how the bundles are formed can have a large effect on the quality of a high speed differential pair.

EXPLANATION GLASS SPREADING TERMINOLOGY

Standard

Expanded

Spread (MS)
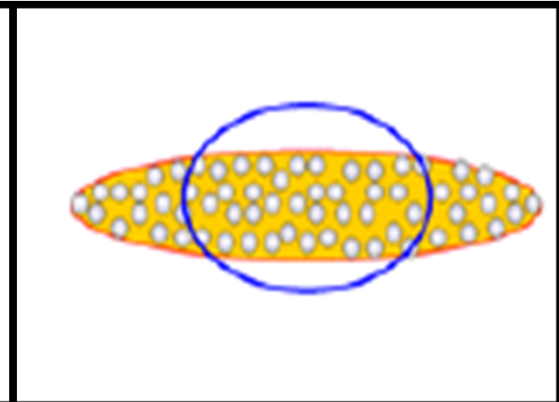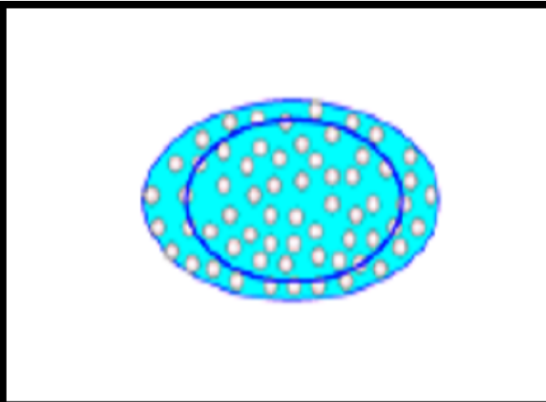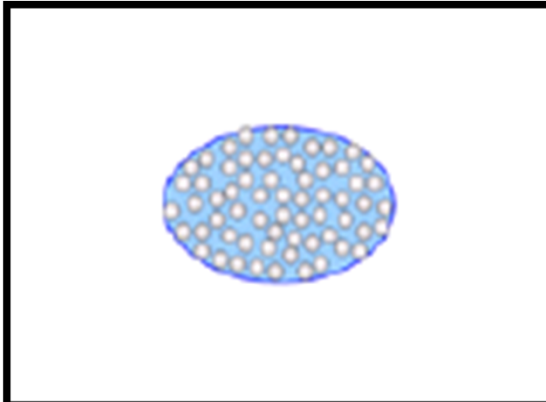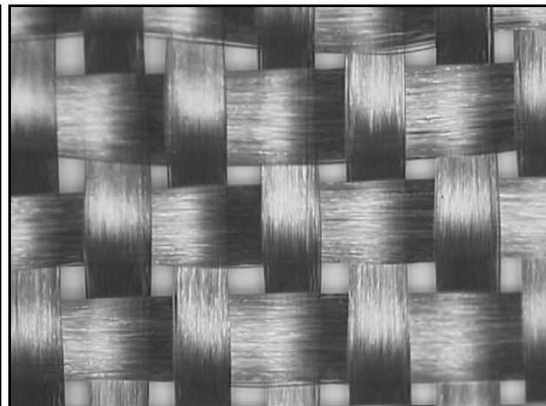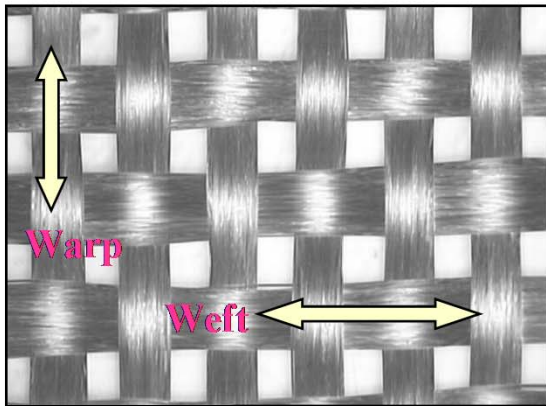
SOME REPRESENTATIVE GLASS STYLES
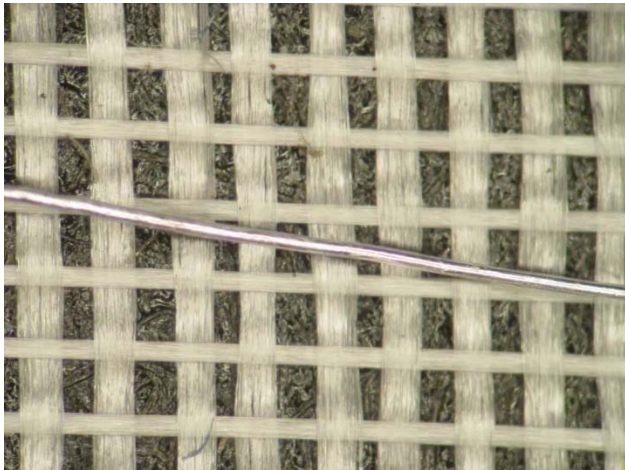
106

WIRE IS 3.5 MILS IN DIAMETER
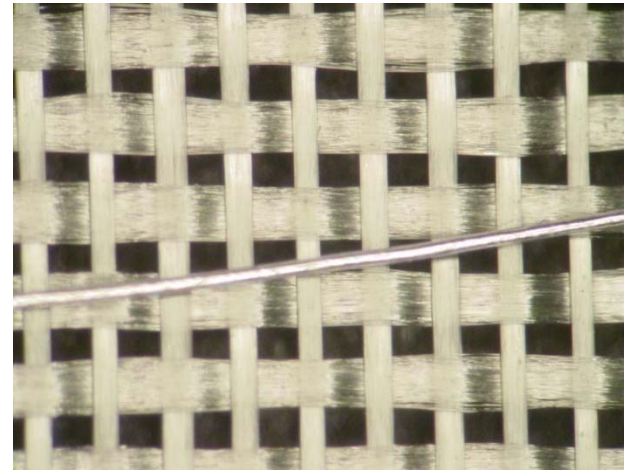
1080
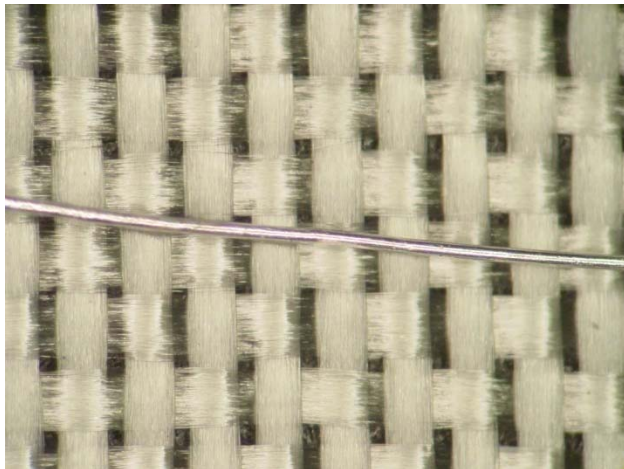
2113
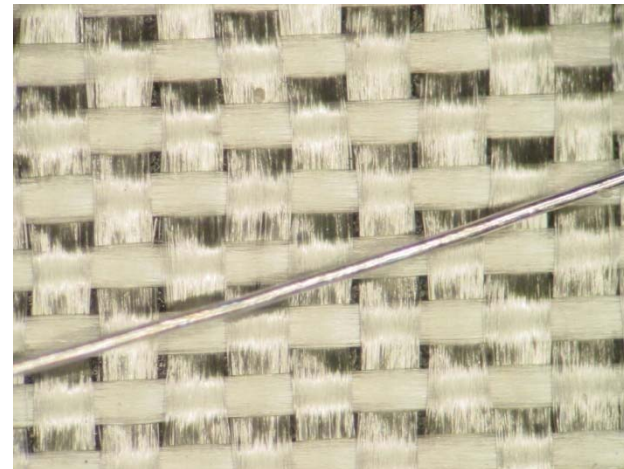
3313

IMPEDANCE VARIATION OVER 1080 GLASS

+10%

-10%
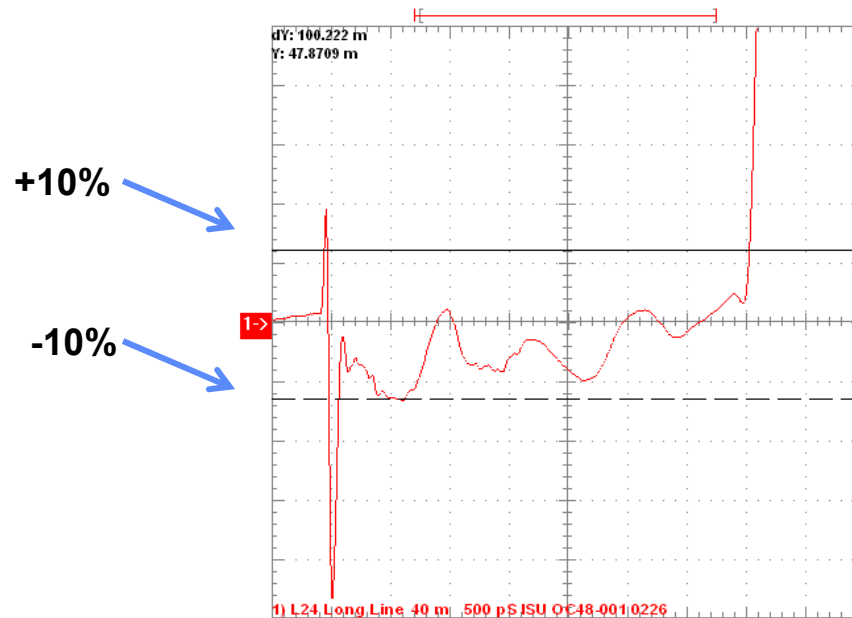
1080 glass cloth has been the most commonly used weave to create a 4 mil core.

The centerline is 50 ohms. The upper line is plus 10% and the lower line is minus 10%. This wide impedance variation can result in severe skew with high speed differential pairs and should not be used in PCBs with this class of signals.

IMPEDANCE VARIATION OVER 3313MS GLASS

+10%

-10%
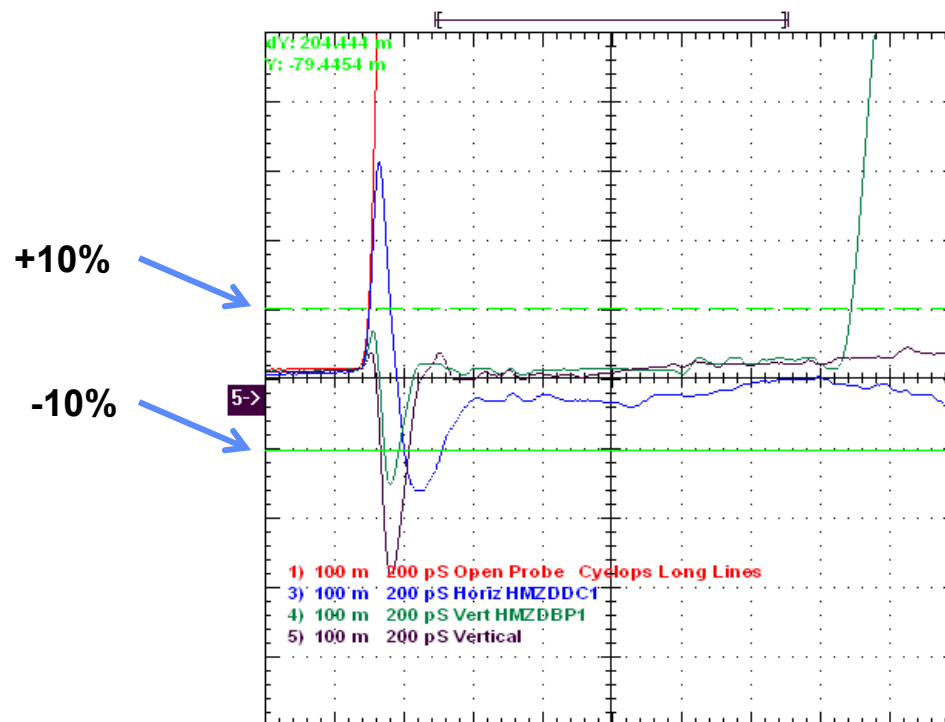
Notice how much more uniform the impedance is as it travels across the glass weave in both horizontal and vertical directions as compared to 1080 glass. This results in very low skew. Weaves known to cause skew in differential pairs- 106, 1080, 2116, 7628.

FIVE PROPOSED METHODS FOR CONTROLLING WEAVE INDUCED SKEW

Several methods have been proposed to minimize weave-induced skew. Reference 8 at the end of this presentation is a study of ways to control skew. The proposed methods include:

1. Route differential pairs at an angle (15º) to the weave. Ref 7. A paper presented at DesignCon 2018 suggests that 3º rotation is adequate.

2. Build each PCB at the fabrication shop with the artwork rotated at an angle to the glass weave.(Traces routed X and Y in artwork.)

3. Route each member of the pair at the same pitch as the glass fibers.

4. Use glass that has a lower dielectric constant (similar to the resin).

5. Use a glass weave style that has the glass mechanically spread in a uniform manner, such as 1035MS, 1067MS, 1086MS, and some versions of 3313.

1. ROUTING SIGNALS AT AN ANGLE TO THE WEAVE

- **This solution has been imposed by some OEMs on their layout teams.**

- **It has been shown to minimize skew by causing traces to, more or less, uniformly travel on and off the glass bundles.**

- **Clearly, this complicates the layout operation and may make it more costly.**

- **In many cases, such as backplanes, there is not mechanically enough room to allow this "off angle" routing.**

- **It would be desirable to solve the skew problem another way.**

2. FABRICATE PCBS AT AN ANGLE TO THE PANEL

This solution requires the fabricator to orient the PCB artwork at an angle to the laminate panel as shown.

The differential pairs (assuming they were routed only in X and Y in the artwork) would travel at an angle to the weave.

As can be seen, significant material is wasted increasing board cost (the red areas).

Again, it would be good to find a better solution.

PCB ROTATED IN PRODUCTION PANEL

RED IS WASTED MATERIAL
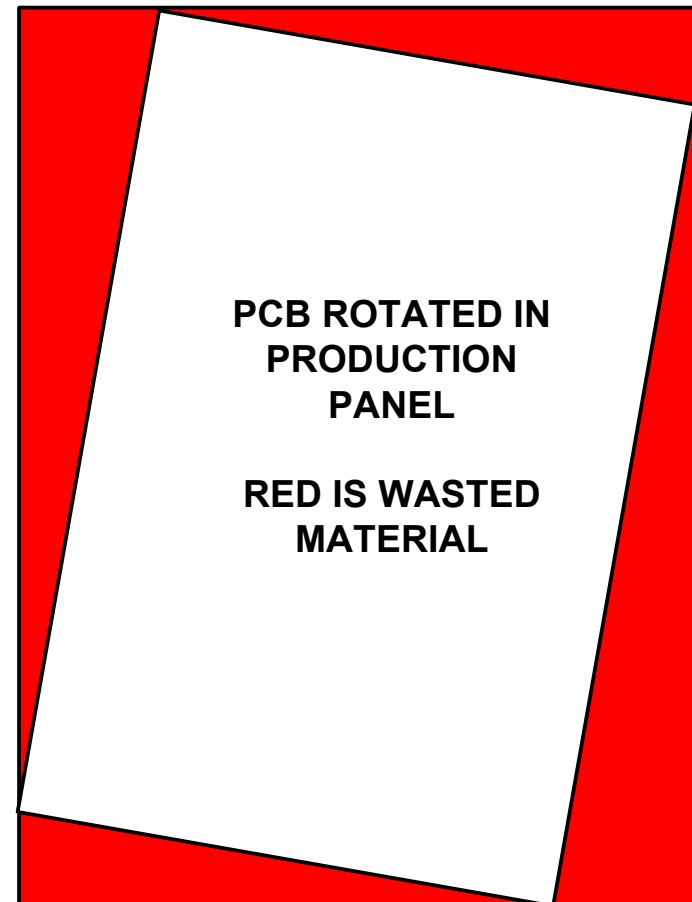
3. ROUTE SIGNALS ON WEAVE PITCH

- This approach is based on the idea that if the traces of a differential pair are spread out to the same pitch as the glass bundles both will see the same variations and skew will be minimized.

- The differential pairs on the test PCB shown earlier were routed in this manner and did not result in minimum skew.

- The next slide is a chart that shows the weave pitch of several commonly used glass styles.

- The pitch ranges from 14 mils to 22 mils.

- Assuming this method controls skew, the wide spacing can be difficult to achieve on dense PCBs.

- It would be good to find an alternative solution that does not impose this constraint on the routing of the PCB.

WOVEN GLASS FIBER DIMENSIONS
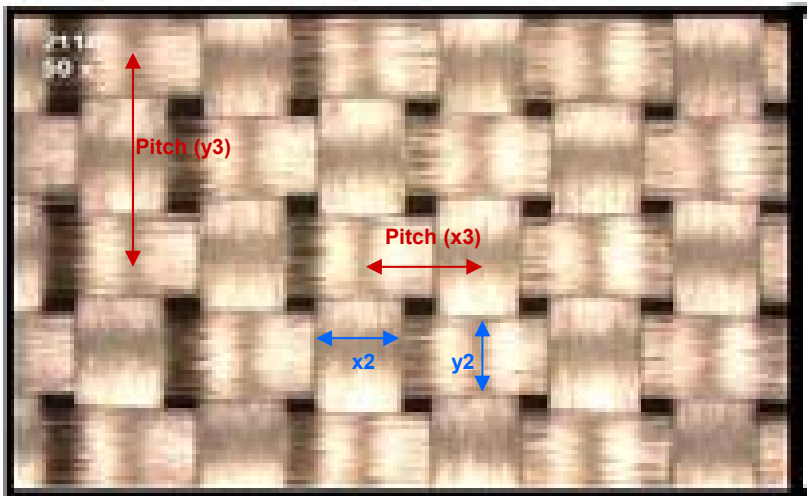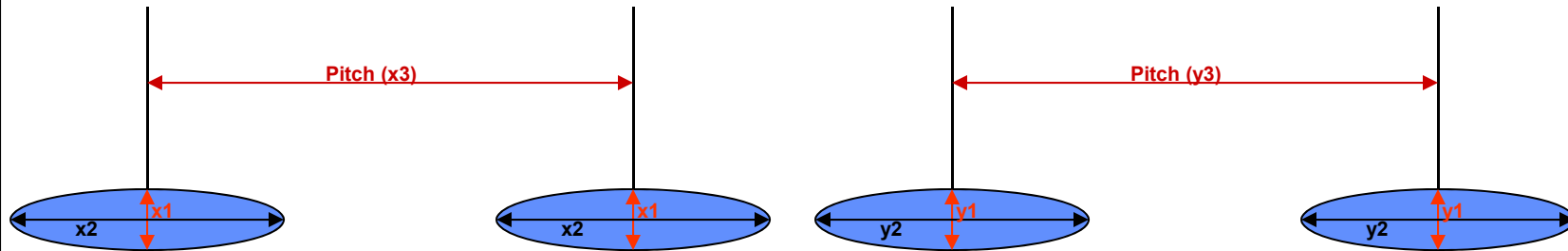
Glass Fabric	Measurement Results (mils)					
	X1	X2	X3	Y1	Y2	Y3
106	1.00	4.80	18.50	0.60	10.20	20.60
1067	0.82	8.85	14.30	0.78	12.40	13.70
1080	1.60	8.20	17.00	1.10	12.10	22.40
1086	1.44	10.80	16.60	1.00	14.70	17.10
2113 / 2313	2.40	10.50	17.00	1.00	15.30	18.20
3313	1.90	13.10	16.20	1.50	11.00	16.30
3070	1.70	12.70	14.80	1.70	12.60	14.20
2116	2.20	14.10	17.20	2.00	14.50	17.30
1652	2.40	15.30	17.50	2.90	15.90	18.80

Courtesy of
Isola Corp.

4. USE LOW DK GLASS WEAVE
(DK OR e_r IS DIELECTRIC CONSTANT)

- **Differential skew is caused by the large difference in dielectric constant of the glass and the resin in laminates. E glass has a DK around 6 and resins have a DK below 3.**

- **Using a lower dielectric constant glass should help ease the skew problem.**

- **Several of the test PCBs were built with low DK glass (8313 DK ≈ 4).**

- **Test results show that this method does not work well.**

5. USE MECHANICALLY SPREAD GLASS

- Mechanically spreading the fibers in each glass bundle has the effect of reducing the variations in dielectric constant seen by transmission lines as they traverse a PCB.

- Examples of this are: 1035MS, 1067MS, 1086MS, 1078MS and some varieties of 3313 glass.

- The test PCBs in this study were fabricated from 3313 glass spread in only the vertical or fill direction. This direction had very low skew.

- Test results clearly show that mechanically spreading the glass results in very low skew at little or no cost penalty.

- A problem with relying on mechanically spread glass is there are no standards that define when the glass has been properly spread and each supplier does it differently.

EXAMPLES OF MECHANICALLY SPREAD GLASS
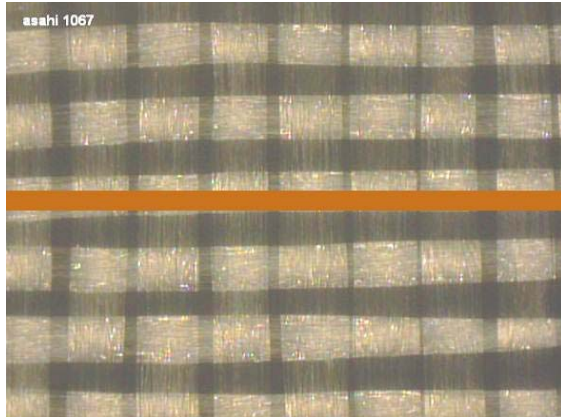
1067MS WEAVE
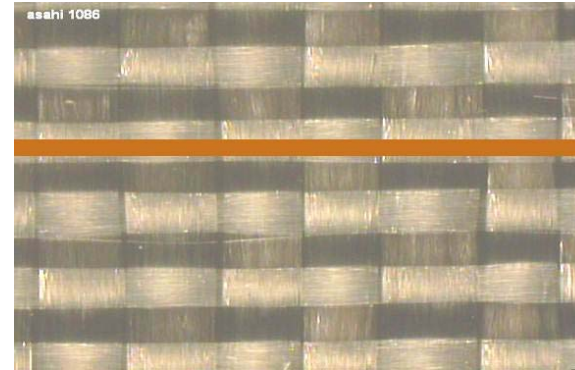
1086MS WEAVE
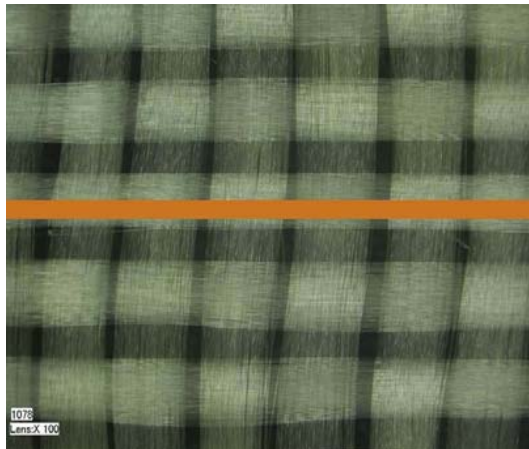
1078MS WEAVE
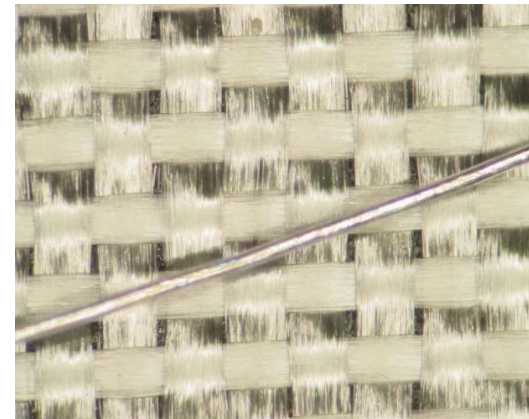
3313MS WEAVE

SKEW TEST RESULTS WITH MECHANICALLY SPREAD GLASS

- The test results below used 1067MS glass weave which is mechanically spread in both horizontal and vertical (warp and fill) directions. (Warp spread not as good as fill spread.)

- Clearly, spreading the glass is a safer, less expensive way to reduce differential skew than the other four methods.

- As already mentioned, spreading methods differ by glass suppler.

PCB #	1	2	3	4	5	6
HORZONTAL SKEW (pSec) (Warp)- 14" TRACES						
I-SPEED	17	2	12	2	2	8
VERTICAL SKEW (pSec) (Fill)- 9" TRACES						
I-SPEED	2	3	2	1	2	2

POTENTIAL PROBLEMS WITH RELYING ON GLASS WEAVE UNIFORMITY

- Currently, the woven glass industry spreads the glass weave in order to provide a more uniform laser drilled blind via for build up PCBs used in cell phones and tablets.

- There is no standard in place that insures that every weaver of glass cloth spreads the glass the same way.

- As an example, the 3313 and 8313 glass used in the test PCBs in this study did not have the glass spread in both directions while previous test PCBs built with 3313 glass from another weaver produced excellent skew results because the glass was spread uniformly in both horizontal and vertical directions.

- Yet another potential problem stems from a fabricator changing the glass style to one that is not spread resulting in skew in excess of what the data links can tolerate.

SOLVING THE SKEW PROBLEM WITH ISOLA'S Chronon® AND GIGASYNC®

- Isola has developed two laminate systems engineered to minimize skew in differential pairs that are not affected by glass weave.

- These laminate systems are GigaSync® and Chronon®.

- GigaSync® is an ultra low skew, moderate loss laminate system intended for the server blade market. Its loss tangent is .006.

- Chronon® is an ultra low skew, very low loss laminate system intended for systems containing large backplanes with long data paths and very high data rates. It has a loss tangent of .003.

SKEW TEST RESULTS FOR GIGASYNC® AND Chronon®

- **This data is taken from test PCBs fabricated from the same artwork used to fabricate all of the test PCBs on the previous slides. Notice how tightly grouped and small the skew is with this new material set.**

- **The skew results are independent of glass style used making it far less likely that a fabricator can compromise a design by changing glass styles. (Note: Chronon® is ISE-41 below.)**

- **The small skew from both of these material systems satisfies the skew needs of data links to at least 40 Gb/S without the need for special design or fabrication methods.**

PCB #	1	2	3	4	5	6
HORZONTAL SKEW (pSec) (Warp)- 14" TRACES						
GigaSync	0	2	2	2	4	2
ISE-41	5	1	3	1	5	3
VERTICAL SKEW (pSec) (Fill)- 9" TRACES						
GigaSync	0	1	0	0	1	1
ISE-41	1	0	1	2	1	0

REFERENCES

1.Zasio, John, "Rogers Test Board TDR Analysis", December 11, 2008.

2.McMorrow, Scott etal, "Impact of PCB Laminate Weave on Electrical Performance", DesignCon, Fall 2005.

3.Ritchey, Lee W. "A Way to Address the Problem of Jitter and Skew in Gigabit and Faster Signals Caused by Laminate Weaves," Current Source, June 2007

4.Bogatin, Eric, "Skewering Skew, Laminate Weave Induces Skew", Printed Circuit Design, April 2005.

5.Horn, Allan, etal, "Effect of Conductor Profile on Insertion Loss," DesignCon January 2010.

6. Ritchey, Lee W, "Designing a PCB Stackup," Current Source, Volume 3, Issue 3, September 2009.

7.Loyer, Jeff, etal, "Fiber Weave Effect: Practical Impact Analysis and Mitigating Strategies", DesignCon 2007

8. Ritchey. Lee W, etal, 5-TP5 High Speed Signal Path Losses as Related to PCB Laminate Type and Copper Roughness, DesignCon 2013

MANAGING CROSSTALK

- There are two places that cross talk can take place in a high speed system. These are:

  - Trace to Trace
  - Line to line in connectors

- Trace to trace crosstalk takes two forms. Side by side routed traces and over an under traces.

- Side by side cross talk is minimized by spacing constraints and can be readily calculated using most SI tools. Special care must be taken with the receive ends of paths that have been degraded by large amounts of path loss.

- Over and under cross talk stems from traces routed in adjacent signal layers. This form of cross talk is severe. Over under routing must be prohibited by the design rules (X Y routing) and checked after routing is completed.

MANAGING CONNECTOR CROSSTALK

- Cross talk in connectors occurs because most connectors do not have any form of isolation between signal pins.

- As a result, it is necessary to carefully assign differential pairs so that those paths with very low signal levels, such as the receive ends of signal paths with high loss, are not adjacent to drive ends of signal paths where the signal amplitude is large.

- Connector manufacturers who serve the high speed market have mechanically spaced the signal paths in the connectors to minimize cross talk and provide the user with pinout patterns that minimize this problem.

- Some connector manufacturers have placed baffles between rows to improve isolation.

WHEN VIAS CAUSE PROBLEMS

- In the section on what happens when things get fast we saw that the effects of vias on high speed signals are minimized when the data path has large amounts of loss.

- When nets are short and the loss is small, the capacitance associated with a via or plated through hole attached to traces can cause severe signal degradation.

- The circuit effect that is observed is as though a low pass filter in the form of a pi network has been created.

- As observed earlier, the capacitance of a signal via in a 100 mil thick (2.54 mm) board is approximately 0.3 pF and the capacitance of   30 mil (.78 mm) diameter,   is approximately 0.6 pF.

POTENTIAL PROBLEMS WITH SHORT, FAST PATHS

- On earlier slides, it was shown that the effects of vias are minimized with lossy paths.

- When paths are short and loss is small, the parasitic capacitance of a via or pair of vias can cause a resonance to be set up that results in very high loss at selected frequencies, because two vias and the low loss line segment between them create a PI filter which is lossy at high frequencies.

- The graph on the next slide is the loss vs. frequency of 2 8" (20.32 cm) lines in the same PCB. The blue line was routed on L14 of a 16 layer, 100 mil (2.54 mm thick) PCB and the green line was routed on L3 of the same 16 layer PCB.

- As can be seen, the green line has a severe loss above 5 GHz. This is what is expected when a low pass filter is inserted in a signal path.

LOSS vs. FREQUENCY, 8" LINES
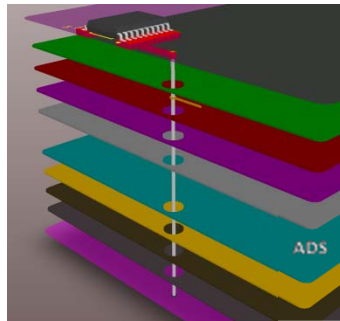
This data was taken from two SET2DIL test traces.
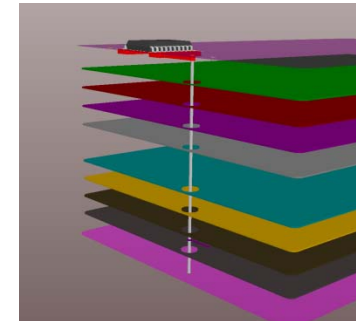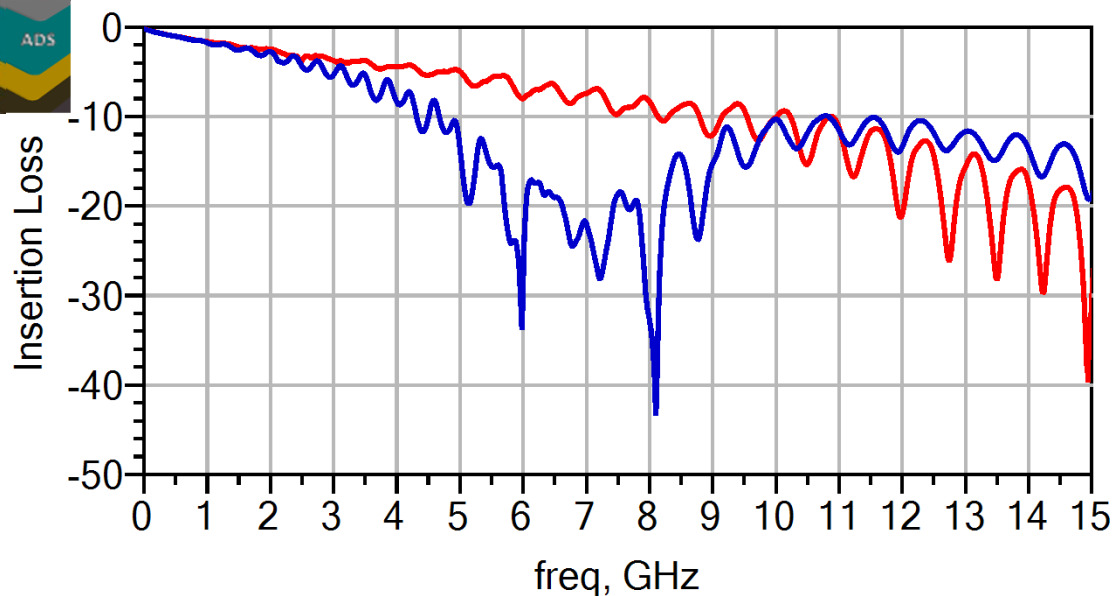
L1 to L3

L1 to L14

Red loss curve is for a 8" trace on L14 of a 16 layer PCB with the signal injected and measured on L1. Blue curve is for a trace on L3 with signal injected and measured on L1. Laminate is I-SPEED from Isola.

REASON FOR DIFFERENCES IN LOSS vs. FREQUENCY ON PREVIOUS SLIDE

- As observed earlier vias have inductance along their length. Vias also have capacitance along their length. A via in a multilayer PCB made with a 12 mil (0.305 mm) drill that is 100 mils (2.54 mm) long has about 0.3 pF of capacitance and 3.5 nH of inductance much like any transmission line.

- When the signal travels the length of the via the capacitance is distributed along the signal path as is the inductance, resulting in behaviour like a transmission line.

- When the signal travels over only part of the via, the capacitance that is not included in the path, forms a low pass filter along with other similar vias blocking high frequencies.

EQUIVALENT CIRCUIT OF VIAS IN TRANSMISSION LINE

50 ohm   50 ohm   50 ohm

0.5 pF   0.5 pF

EQUIVALENT CIRCUIT OF VIAS IN TRANMSISSION LINE

This circuit constitutes a low pass filter as very high frequencies when the signal does not travel the length of the via. When the middle transmission has very low loss, the network is said to be high "Q" and frequency dependent attenuation results.

The 0.5 pF capacitor has a capacitive reactance of about 8 ohms at 10 GHz!

TWO LAYER CHANGING VIAS
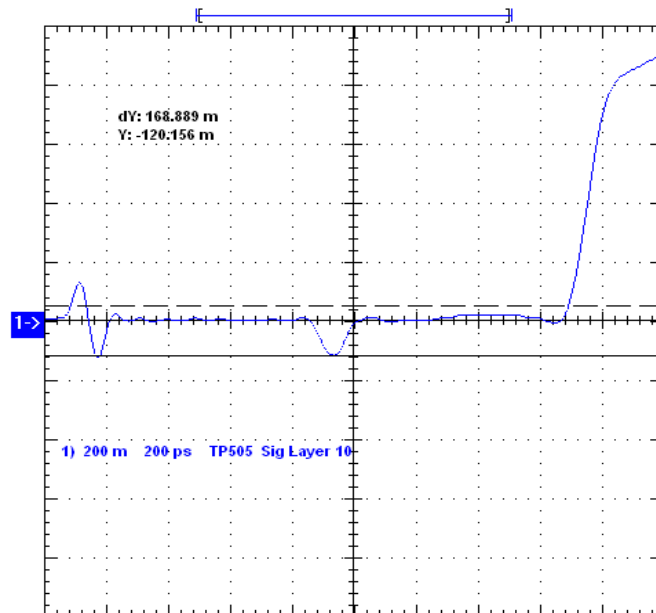
TDR result for trace travelling from L9 to L10 in a 22 layer PCB .
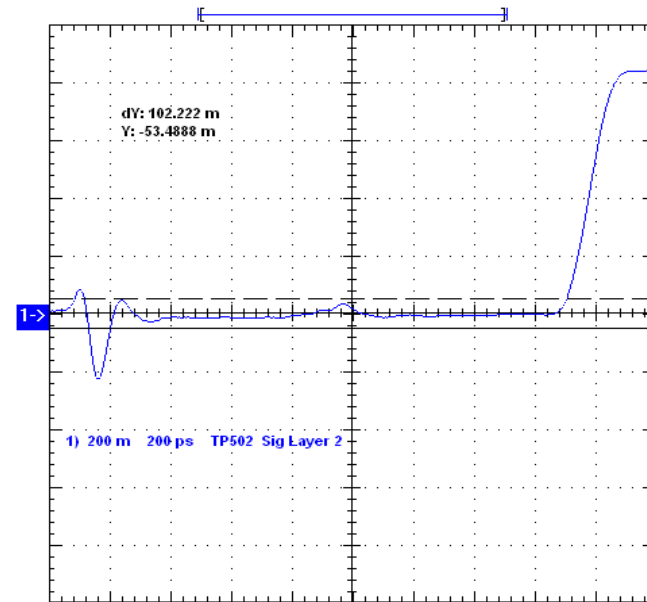
TDR result for trace travelling from L2 to L21 in a 22 layer PCB.

No "ground" vias nearby. Notice that when layer change travels the length of the via, its parasitic capacitance is spread along its length (inductance) making its effect negligible. This is the way to handle very high speed signals.

A 3.6 Gb/S DIFFERENTIAL PAIR

Design File: Sandia 36 GbS W OCAPS Stripline.ffs
HyperLynx LineSim v8.1.1
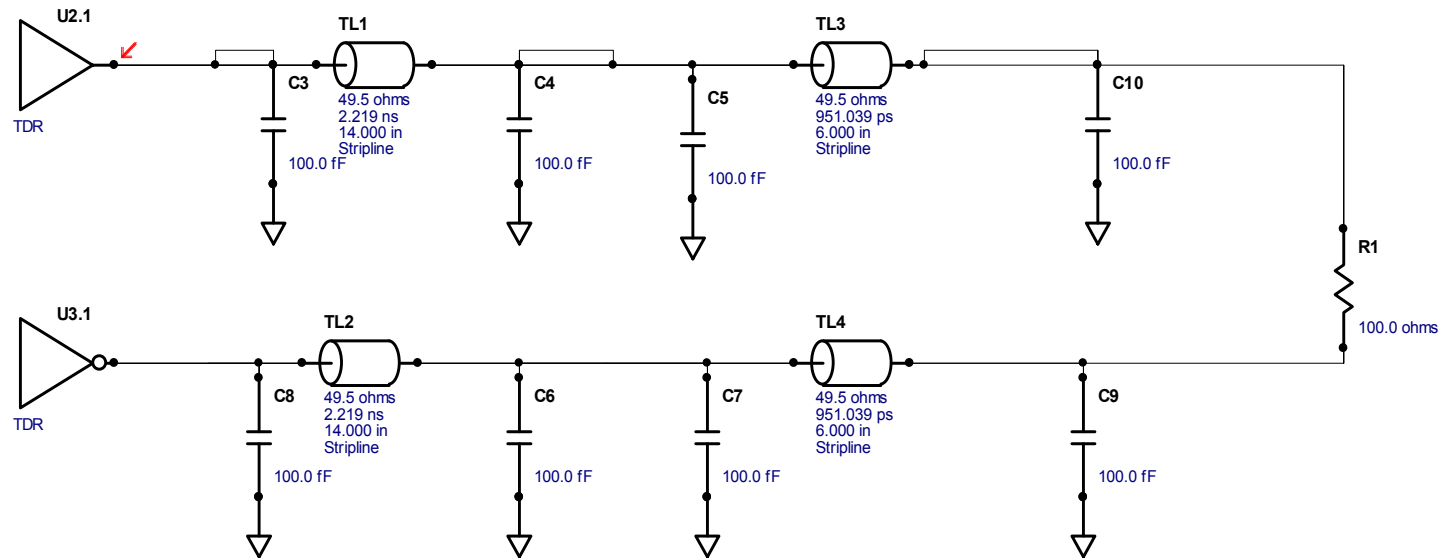
This differential pair will be used to simulate 30 mil (.762 mm) vlas 250 mils (6.35 mm) long as can be found in some backplanes. Simulation will be done with and without back drilling.

This is the interface to a wafer probe IC tester.

3.6 Gb/S SIMULATION WITH BACK DRILLED VIAS
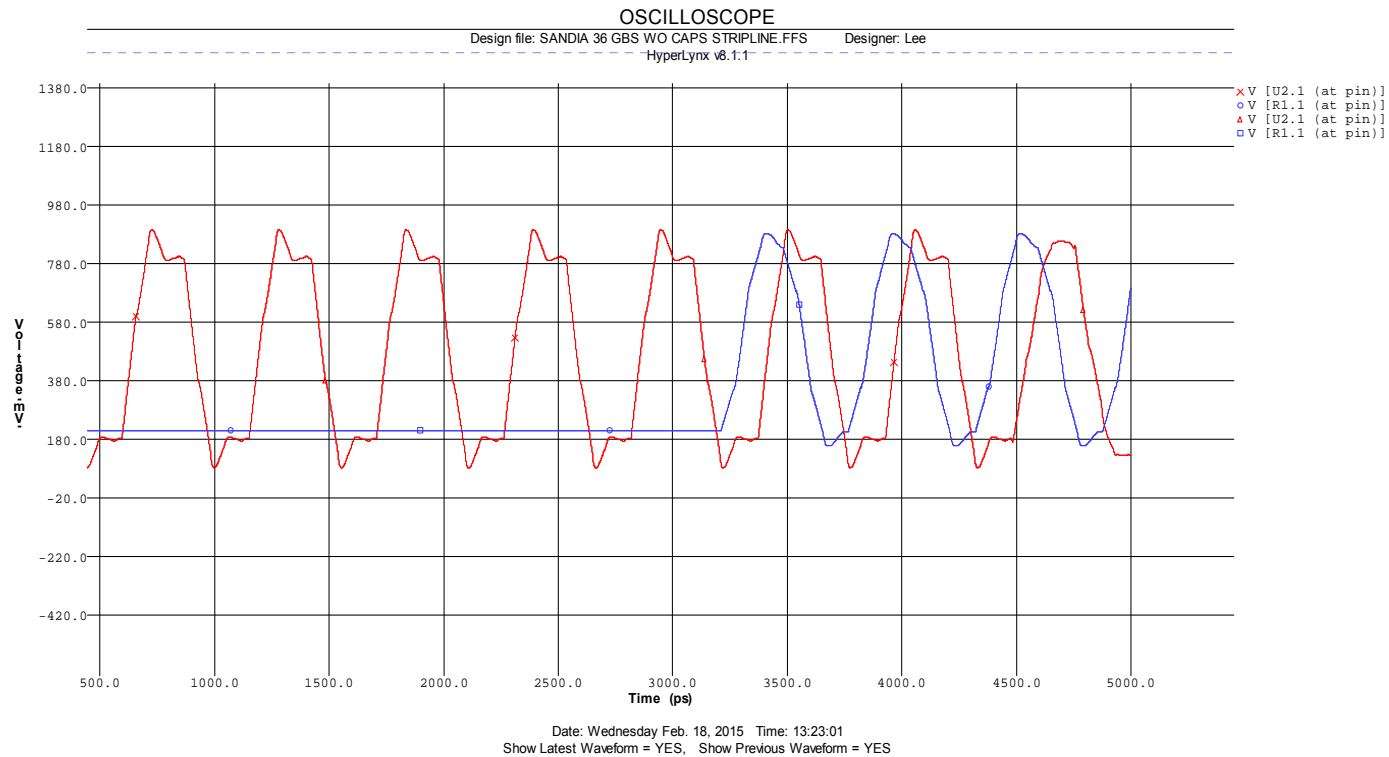
Red waveform is driver output. Blue waveform is receiver input.

3.6 Gb/S SIGNAL WITHOUT BACK DRILLED VIAS
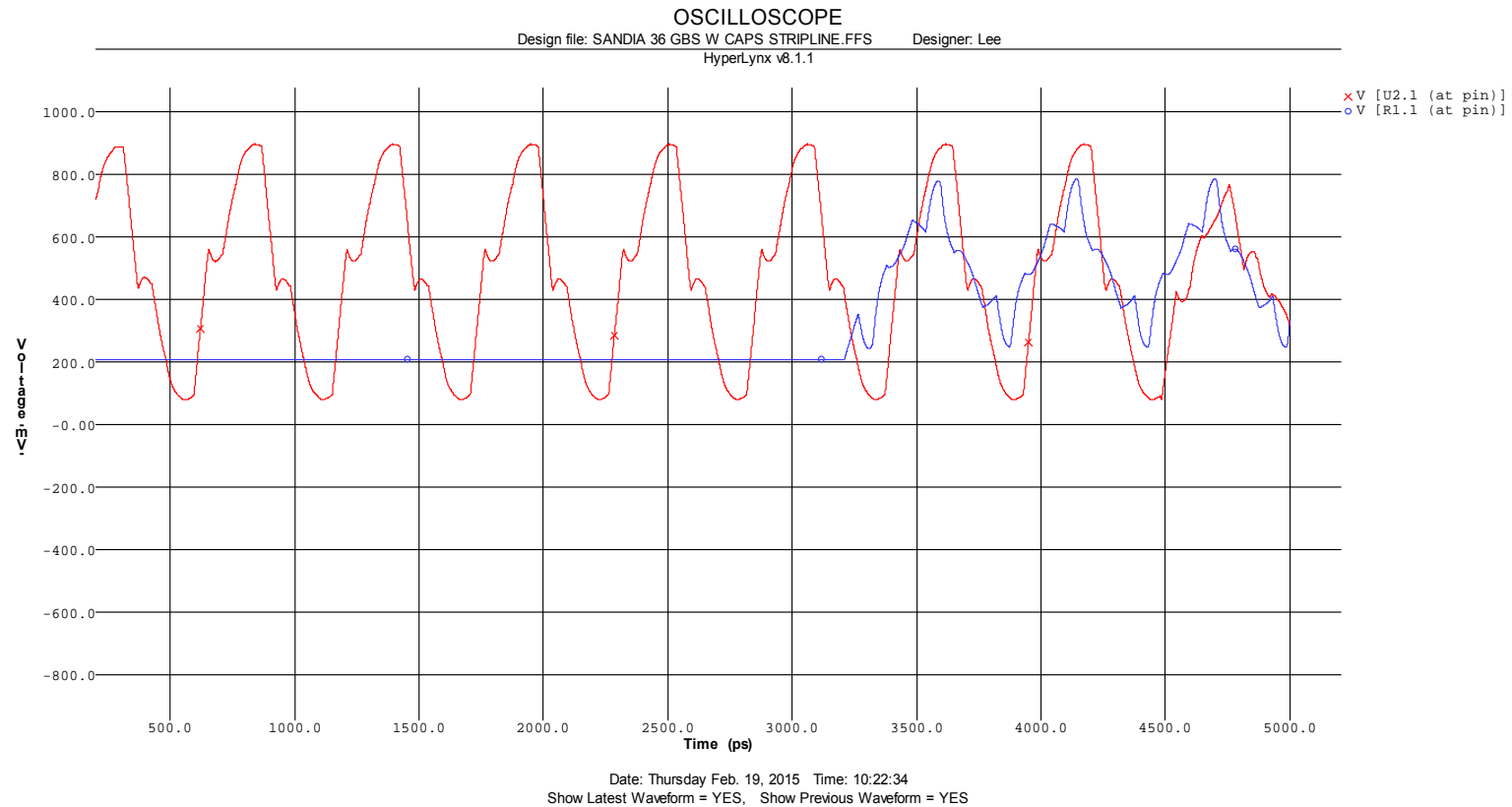
Red waveform is driver output. Blue waveform is receiver input.

MEASURED WAVEFORM FOR PROBE CARD
3.6 Gb/S
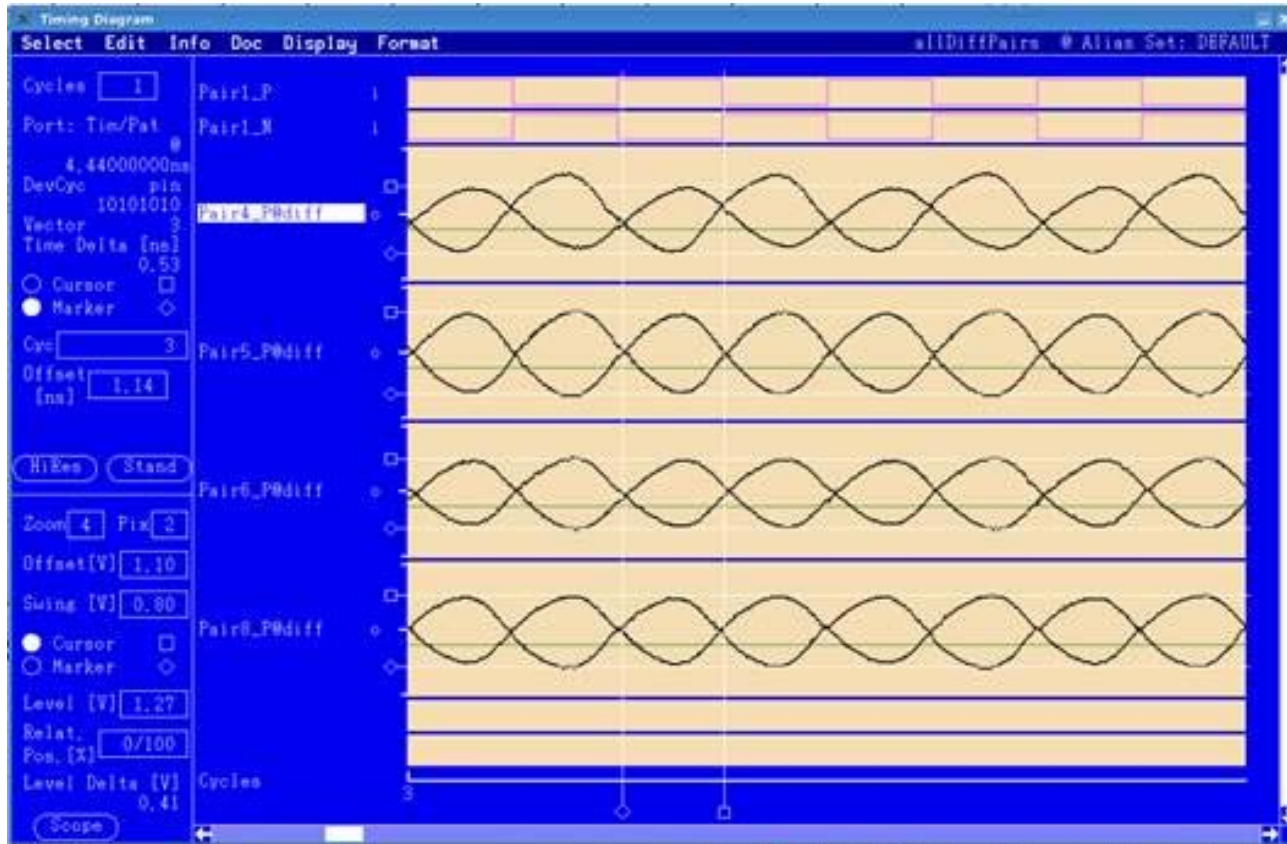
HOW TO MINIMIZE VIA EFFECTS IN HIGH SPEED SIGNALS

The parasitic capacitance of the via can cause a problem. Some refer to this as a via stub. Ways to minimize this problem are:

1. Make sure signals travel the whole length of the via by placing signal on a bottom layer of the PCB.

2. Begin and end the signal on layer 1 and use no vias.

3. Use vias at both ends of the signal when routed on layers near the top of the PCB and back drill away the portion of the via that extends below the trace layer.

4. Route signal on Layer 2 and enter and exit the trace using a laser drilled blind via.

COMMENTS ON METHODS LISTED IN LAST SLIDE

As with most things, there are likely to be drawbacks to chosen routing methods. This is true for the four methods listed on the previous slide. They are:

1. Route signals only on bottom layers. This works only if the number of signals to be routed will fit on these layers.

2. Route signals on L1 with no vias. Works if all signals will fit in the available space. Outer layers have poorest impedance accuracy. Plating these signals with ENIG results in much higher loss than anticipated due to ferromagnetic properties of nickel.

3. Back drill away unwanted portion of via that extends below the trace layer. Back drilling is an extra process step and adds cost. There is a risk of drilling too deep and breaking connection to trace.

4. Route signals on L2 and use blind vias to connect. Results in the best signal quality. Blind via drilling is an extra process step.

USING A BLIND VIA TO ACCESS LAYER 2
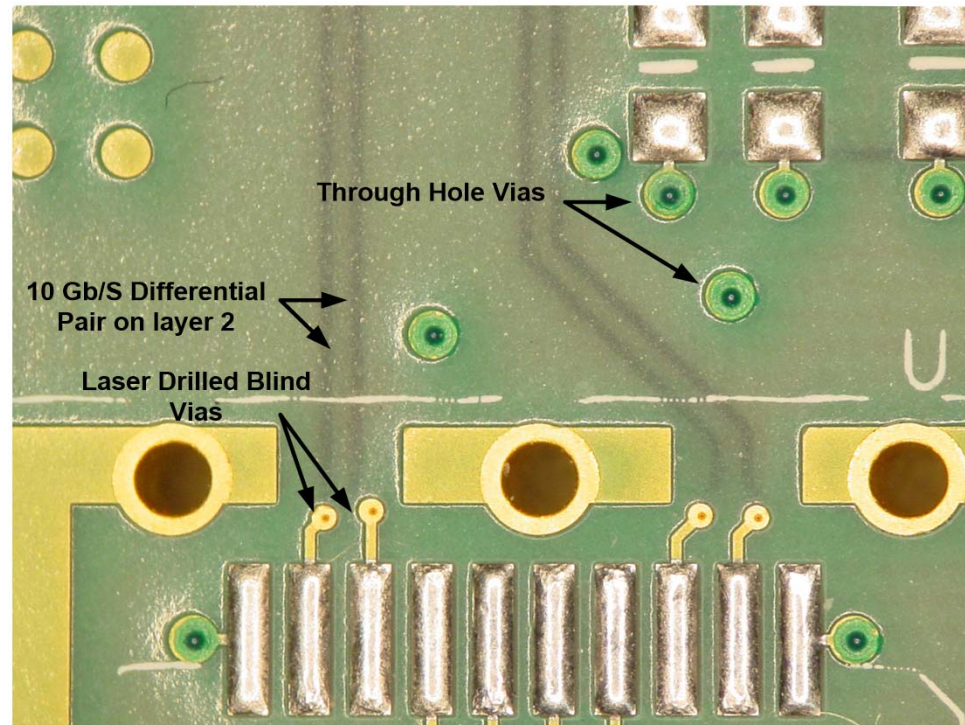
By accessing layer 2 with a blind via, the effect of the via is held to a minimum. By routing signals on L2, the effects of plating and etching associated with routing on L1 are eliminated. Notice that the through hole vias have been plugged and the pads are covered with solder mask.

HIGH SPEED SIGNALING SUMMARY

- **High speed differential signaling has become an integral part of all electronics.**

- **It is possible to achieve very high data rates with common materials as long as sources of signal degradation are understood and accounted for. Signals paths as high as 28 Gb/S are currently possible with copper traces and standard laminates. (56 Gb/S over a 24" (61 cm) path in copper is operating successfully in a laboratory.)**

- **Successful high speed design demands the use of good analytical tools as well as rigorous control of materials used to fabricate PCBs.**

- **10 Gb/S is commonly being done in materials called "FR-4".**

- **Up to about 5 Gb/S, vias can safely be represented as small parasitic capacitances. They are visible, but are not significant sources of signal degradation. Above 5 Gb/S, vias may degrade signal quality if not used carefully.**

LOCATING AC COUPLING CAPACITORS

- **AC coupling capacitors are capacitors placed in series with both sided of a differential pair. Their purpose is to provide DC isolation between the two ends of a differential signaling path.**

- **The reason for this is to deal with DC offsets between the two ends that are outside the range of the receiver.**

- **With the caution that the parasitic capacitance of the vias used to connect to the two ends of the capacitors can cause the problems as discussed in the previous section, their location along the path does not matter.**

ON CLEARING GROUND UNDER AC COUPLING CAPACITOR MOUNTING PADS

- There is a rule of thumb in circulation that states that the ground under the mounting pads of AC coupling capacitors in a differential pair should be removed.

- This is another rule that does not seem to be supported with any proof.

- This is also an extra step in the design process that takes designer time.

- Is it a valuable thing to do or will it do harm?

- At a minimum it should do no harm. If it is a good rule, it should have a benefit that justifies the extra effort.

- This can only be established with tests.

TEST RESULTS FOR AC COUPLING CAPACITORS IN DIFFERENTIAL PAIRS
(Signal traces on L20 of 22 layer PCB.)
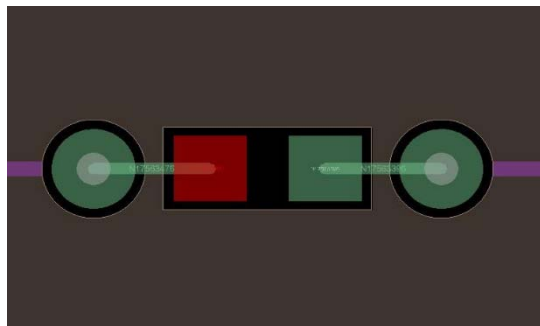
AC CAPACITOR MOUNTING ARTWORK

The ground under the capacitor mounting pads has been cleared away on layer 2. The test traces are located on Layer 20 of a 22 layer PCB. Notice that removing the ground plane results in more loss at high frequencies than if plane is intact.

Loss vs Freq for Series Coupling Cap

L20-Ref   L20A-With Antipad   L20B-Solid GND Plane
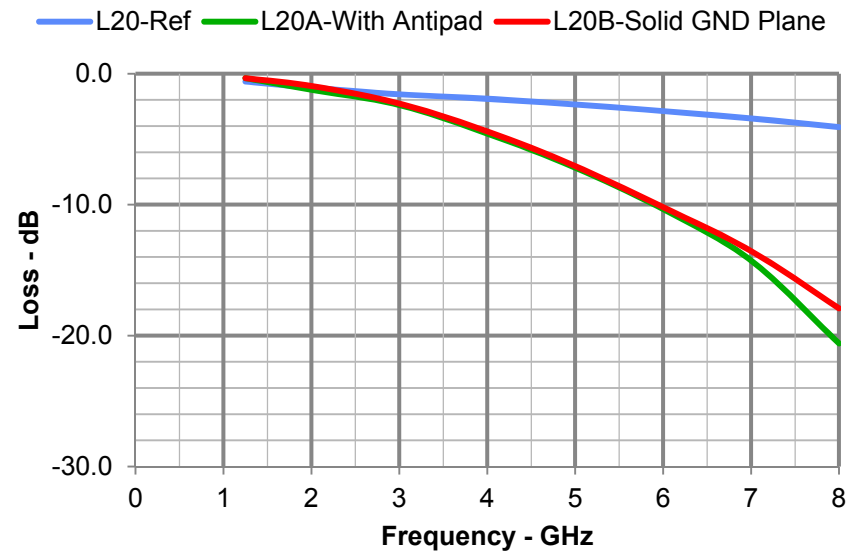
Test data courtesy of John Zasio.

CONNECTORS

- All connectors that are rated for 50 ohms per signal path will work as connectors for differential signaling.

- The primary caution with high pin count connectors are two fold: These are:

- Make sure the plated through holes used to connect to the pins have been managed as described in the section on plated through hole effects.

- Make sure that the receive ends of long data paths with large amounts of loss are not placed next to driver ends of paths where the amplitude is large to avoid cross talk.

- Newer connectors intended for this market have isolation plates between rows of pins to help isolate inputs from outputs.

FLEXIBLE CIRCUITS

- Flexible circuits are often used to connect to assemblies where a rigid connection is not possible.

- Most flexible circuits are one or two layers. When used to transmit high data rate signals the primary concern is crosstalk and via effects discussed earlier.

- If a differential pair is routed on a one layer flexible circuit it will be vulnerable to cross talk from other circuits on the same flex circuit as well as outside sources. It is rare that single layer flex circuits work well with high data rate signals.

- The best way to deal with high speed signals on a flex circuit is with one that has two layers. One layer is a solid plane connected to logic ground and the other is the signal layer.

TWISTED PAIRS

- Twisted pairs are a common method for connecting differential pairs between two boxes. Most of the wired Internet is connected using 100 ohm differential pairs.

- The two big advantages of twisted pairs are that the connection method is the lowest cost possible and by virtue of the twisting, the pair is relatively immune to noise coupled from outside sources.

- All that is needed to connect a twisted pair differential pair to a PCB is to make sure that the two on board connections are each 50 ohms and that the vias are managed as discussed earlier.

- 10 Gb/S differential signaling is routinely done across 100 feet (30 meters) of shielded, twisted pairs.

DESIGN RULES

- Successful high speed differential signaling requires great care with the routing of signals as well as in the choice of materials.

- Route all signals as 50 ohm traces taking care to protect from cross talk and in the formation of connecting vias and holes attached to those signals.

- Make sure the laminate materials chosen will meet the skew and loss targets of the data rate being handled.

- Be sure the documentation (fabrication drawing, stackup drawing and fabrication notes) contain adequate information to produce the desired PCB.

- Do not allow the fabricator to substitute materials that may be less expensive but might render the PCB unusable.

RECORDING DESIGN RULES

- There are a number of documents that are required to insure a high data rate design meets its goals. Among these are:

- A design document with all of the routing rules, stackup drawing, via usage rules, materials callout and other information needed by the layout team.

- A fabrication drawing with a full set of fabrication and drill information as well as a stackup drawing showing precisely what is needed in the finished PCB.

- Do not put an impedance requirement on the fabrication drawing. The overall stackup dimensions must be met to achieve successful results and a fabricator must not alter the stackup for any reason. (Yes, this puts the responsibility for designing the stackup correctly on the design team not the fabricator.)

FABRICATION NOTES FOR "10 Gb/S FASTER" PCBS.

Prepared by: Lee W. Ritchey, Speeding Edge, Revised August 31, 2015

Purpose: This document contains the fabrication notes to be applied to all of the daughter PCBs in the YYYY products. A separate set of notes will be generated for the backplane.

NOTES: (UNLESS OTHERWISE SPECIFIED)

1. Reference General Specification for Printed Circuit Boards #XXXXXXX
2. **Any deviation from these instructions must be approved in writing by principal or agent.**
3. Material: Use only materials specified in stackup drawing accompanying design.
   Board Lamination: Overall thickness: 0.xxxx" ± the lesser of 0.010" or 10%.
1. Copper weight: see layer stackup drawing.
2. Drilling: All holes to be located by X & Y coordinates from NC drill data supplied. See separate Drill Table for drilled hole sizes and quantity. Pad stacks are designed for the drilled hole sizes shown. Drill Table will contain special callouts for Press-Fit holes. **Do not change drill sizes.**
3. Minimum annular ring of 2 mils, unless otherwise specified. Also see note 20.
4. Copper plating: Hole wall copper plating to be 0.001" minimum (drill size - 0.002").
5. All exposed copper to be plated with electroplated gold over electroplated nickel. 5-15 micro-inches gold over 150 micro-inches nickel minimum. (Palladium allowed between nickel and gold)
6. Soldermask: Liquid photo-imageable solder mask to be applied over bare copper or gold/nickel plating unless otherwise specified. Color- green.
7. Legend/Silkscreen: Use nonconductive white ink.
8. Mark with supplier ID and date code on bottom or far side.
9. All inside corners and slots shall have 0.062 radius ±0.005" or less radius.
10. No modification of film without prior authorization.
    For exceptions see notes 16 & 20.
1. Stripes of copper may be plotted on each layer on one side of the PCB edge as shown on fabrication drawing. These "stacking stripes" are intended to be exposed when the PCB is removed from the panel. **Do not remove/modify stacking stripes.**
2. Compare CAD net list to net list generated from Gerber data prior to fabricating board. Resolve differences prior to building board.
3. Non-functional pads are to be removed from all inner layers.
4. Conductors: Width and Spacing: Build to Gerber data, however compare widths to Fabrication Drawing Data Set Table and resolve differences prior to fabricating board. GERBER TRACE WIDTHS ARE FINISHED TRACE WIDTHS. Finish width accuracy on inner layers ±0.0005". Finished width accuracy on outer layers ±0.001". Fabricator may add manufacturing allowances to trace widths in working film only to accomplish the specified finished trace width.
5. This is a controlled cross section PCB. All fabrication instructions must be complied with in order to assure valid results on completed assemblies. Etch all trace to widths specified in Gerber files. All dielectric thicknesses specified on layer stack-up cross-section on Fabrication drawing. **Do not change glass weave styles specified on stackup drawing.**
6. First delivery to include Diazo set of production films and a copy of the stackup sheet used to select laminates.
7. Teardrop only on 23 mil and smaller through-hole pads at trace exit location. For 23 mil pads, flash another 23 mil pad off set from pad center by 3 mils.
8. Thieving allowed on outer layers to insure uniform plating. Thieving shall be no closer than 0.100" from any other copper feature on the outer layers and shall not be within 0.100" of traces on the first buried signal layer beneath the outer layers. Thieving pattern shall be at the supplier's discretion and not be solid copper.
9. Dimensions of dielectric layers and copper thicknesses and width of 5 mil traces protruding from PCB to be measured on one PCB of each lot using stacking stripes at 500X magnification. Report to be included with first delivery along with copy of traveler used to fabricate PCB showing laminates used in fabrication.
10. Drilled hole true position difference from CAD data is not to exceed 0.005" TIR.
11. Via capping is required on 12 mil vias from BGA side with epoxy followed by LPI Soldermask. Opposite side Soldermask encroachment onto via pads to be 0.008" over drill diameter.
12. All signal and power layer copper finish to be VLP or HVLP copper foil.
13. Fabricator applied finishes to internal signal and plane layers to be Atotech Bondfilm or equivalent that does not degrade the VLP or HVLP copper surface finish.

A FULL SET OF FABRICATION NOTES

FOR A HIGH PERFORMANCE PCB

HOLE AND DRILL CHART					
ALL UNITS ARE IN MILS					
CODE	FINISHED HOLE SIZE	TOLERANCE	DRILL BIT SIZE	PLATING	QTY
+	See Notes 5 & 7		12.0	PLATED	186
⊕	24.0	+/-2.0	28.0	PLATED	55
✦	See Notes 5 & 7		40.0	PLATED	8
⊛	See Notes 5 & 7		43.0	PLATED	8
⊕	39.0	+/-2.0	43.0	PLATED	152
▣	96.0		96.0	NON-PLATED	6
②	157.0		157.0	NON-PLATED	4

Notice that drill chart lists drilled hole size, not finished hole size as the default. The reason is the need to insure drill size is not too large for capture pads or too small to insure proper plating.

Plated hole size is only specified for holes that have press fit connectors.

Trace width is specified rather than impedance.

STACKUP DRAWING SHOWING NEEDED INFORMATION

ISOLA I-TERA TEST PCB, 16 LAYERS, 81/1/11 Rev 2.0

Layer #	Material Name	Material Type	Material Construction	Copper Type S = RTF, X = HVLP	Material Pressed Er (at ~2 GHz)	Material Unpressed Thickness (mils)	Material Pressed Thickness (mils)	Picture	Copper Thickness (mils)	Copper Thickness (oz)	Single Ended Trace Width (mils)
							0.7	Solder Mask			
1	Top								2.2	1.5	
	I-TERA	Prepreg	2 x 3313 RC = 60%			9.4	9.2	Prepreg			
2	Ground			X					0.6	0.5	
	I-TERA	Core	1 x 1086 RC = 68%	core			4	Core			
3	Sig 1			X					0.6	0.5	4
	I-TERA	Prepreg	1 x 3313 RC = 60%			4.7	4.3	Prepreg			
4	GND			X					0.6	0.5	
	I-TERA	Core	1 x 1086 RC = 68%	core			4	Core			
5	Sig 2			X					0.6	0.5	4
	I-TERA	Prepreg	1 x 3313 RC = 60%			4.7	4.3	Prepreg			
6	GND			X					0.6	0.5	
	I-TERA	Core	1 x 1086 RC = 68%	core			4	Core			
7	Sig 3			X					0.6	0.5	4
	I-TERA	Prepreg	1 x 3313 RC = 60%			4.7	4.3	Prepreg			
8	GND			S					0.6	0.5	
	I-TERA	Core	2 x 2116/2 x 1080 RC = 62%	core			18	Core			
9	GND			S					0.6	0.5	
	I-TERA	Prepreg	1 x 3313 RC = 60%			4.7	4.3	Prepreg			
10	Sig 4			S					0.6	0.5	4
	I-TERA	Core	1 x 1086 RC = 68%	core			4	Core			
11	GND			S					0.6	0.5	
	I-TERA	Prepreg	1 x 3313 RC = 60%			4.7	4.3	Prepreg			
12	Sig 5			S					0.6	0.5	4
	I-TERA	Core	1 x 1086 RC = 68%	core			4	Core			
13	GND			S					0.6	0.5	
	I-TERA	Prepreg	1 x 3313 RC = 60%			4.7	4.3	Prepreg			
14	Sig 6			S					0.6	0.5	4
	I-TERA	Core	1 x 1086 RC = 68%	core			4	Core			
15	Ground			S					0.6	0.5	
	I-TERA	Prepreg	2 x 3313 RC = 60%			9.4	9.2	Prepreg			
16	BOTTOM						c`		2.2	1.5	
							0.7	Solder Mask			
							--------		--------		
						87.6	100.4		12.8		
						Material Thickness	Total Thickness		Copper Thickness		

Impedance is shown on this drawing as it is the engineering drawing. Place only that part of the stackup drawing to the left of the first impedance column on the fabrication drawing to avoid second guessing by fabricators.

CONCLUSIONS

- Successful design of very high speed differential data links requires substantially more attention to detail than has been necessary with previous technologies.

- The tools and information needed to succeed is readily available on today's market.

- The changes needed are so radical that very few fabricators are aware of what is needed and will often attempt to redesign a stack up to suit the materials that they have on hand. The usual reason given it reduced cost.

- It is imperative that what is needed of a fabricator is clearly stated and is not deviated from for any reason.

- If this is done properly, it is possible to achieve signaling rates that were deemed impossible only a few years ago.

REFERENCE MATERIAL

1. **RIGHT THE FIRST TIME, A PRACTICAL HANDBOOK ON HIGH SPEED PCB AND SYSTEM DESIGN, Volume 1, Lee W. Ritchey, Speeding Edge, Fall 2003. Volume 2 was published in April 2007.**

2. **SIGNAL INTEGRITY- SIMPLIFIED, Eric Bogatin, Prentice Hall, 2004.**

3. **7-TA3, Short May Not Be Better, Steinberger, Mike, etal, DesignCon 2010**

4. **Ritchey. Lee W, etal, 5-TP5 High Speed Signal Path Losses as Related to PCB Laminate Type and Copper Roughness, DesignCon 2013**

5. **Ritchey, Lee W, "Designing a PCB Stackup," Current Source, Volume 3, Issue 3, September 2009.**

6. **Loyer, Jeff, etal, "Fiber Weave Effect: Practical Impact Analysis and Mitigating Strategies", DesignCon 2007**

USEFUL WEB SITES

- **SPEEDING EDGE**
- **http://www.speedingedge.com**

- **UNIVERSITY OF MISSOURI, ROLLA, EMC LAB**
  http://www.emclab.umr.edu/

- **IPC (Institute of Printed Circuits)**
  http://www.ipc.org/index.html

- **ANSI/IBIS MODELS**
  http://www.eigroup.org/ibis/

- **IEEE (Institute of Electrical and Electronic Engineers**
  http://www.ieee.org

- **ISOLA LAMINATES-Best laminate information**
- **http://www.isola-group.com**

- **NELCO LAMINATES- Good laminate information**
- **http://www.parknelco.com**

USEFUL HIGH SPEED INFO

- *SI Reflector- SI-LIST-REQUEST@FREELISTS.ORG*
  This is a SI discussion group that is very useful. To join the group send an email to the above address and type in the subject line SUBSCRIBE.

- *DesignCon- www.designcon.com*
  This is the best conference world wide that deals with advances in high speed signaling. It is held in January each year in Santa Clara, CA.