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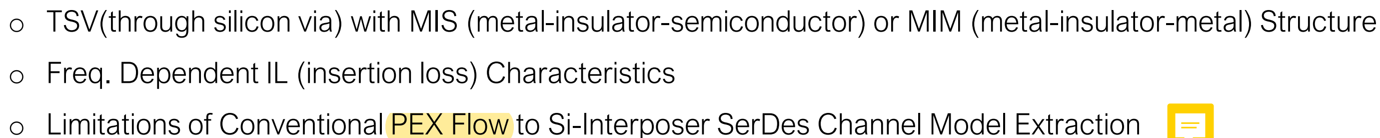
Hybrid PEX Flow for 2.5D Si-Interposer SerDes Signal Channel Model Extraction by Considering High Loss Silicon Substrate Effects

Jun So Pak, Samsung Electronics Co., Ltd.
junso.pak@samsung.com

Bo Pu, Gibak Han, Wonyoung Kong, Ingun(Lars) Jung, Sungwook Moon, Samsung Electronics Co., Ltd.
{bob.pu, gibak.han, wy0217.kong, ingun.jung, sw2013.moon}@samsung.com

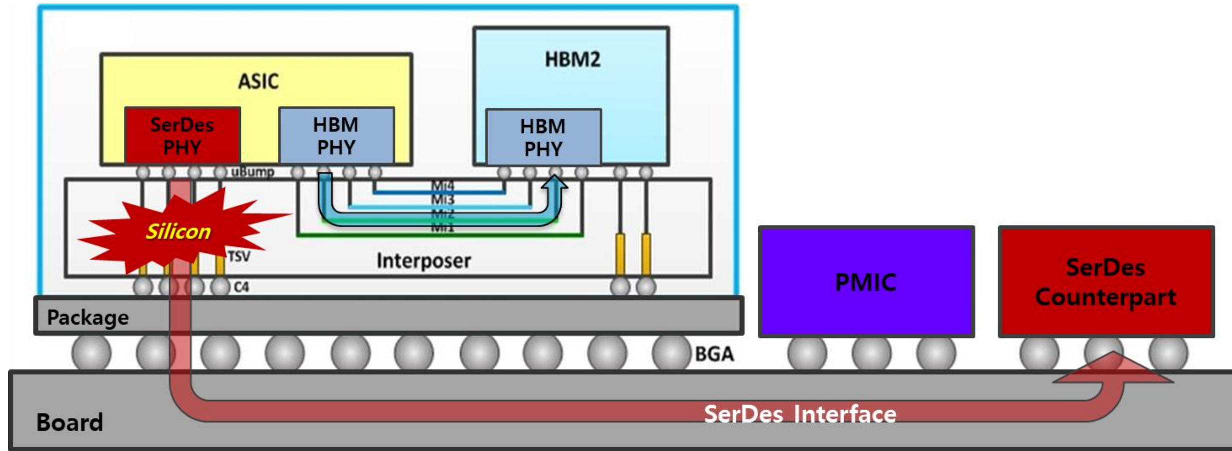
Contents

- **Background & Motivation**
  - HPC (high performance computing) Chip on Si-Interposer due to HBM (high bandwidth memory)
  - What is the Critical Component in SerDes Si-Interposer Channel?
- **TSV**
  - TSV(through silicon via) with MIS (metal-insulator-semiconductor) or MIM (metal-insulator-metal) Structure
  - Freq. Dependent IL (insertion loss) Characteristics
  - Limitations of Conventional PEX Flow to Si-Interposer SerDes Channel Model Extraction



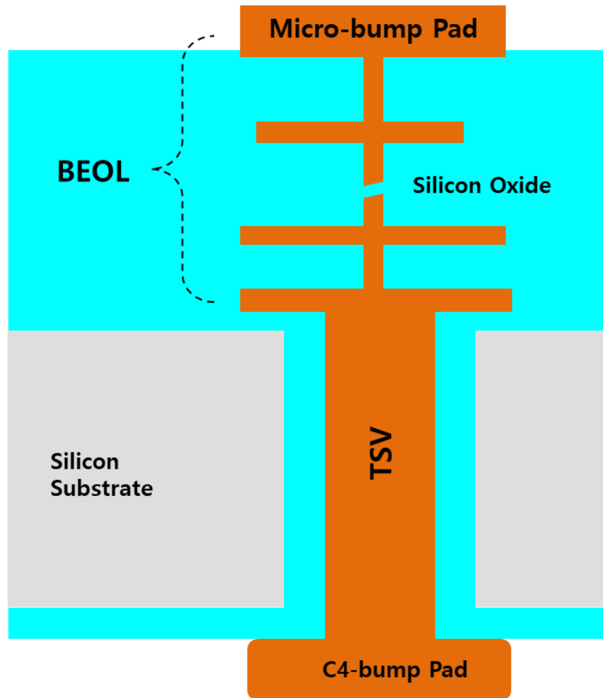
- **Proposed Hybrid PEX Flow for Si-Interposer SerDes Channel**
  - Key Difference referring to Silicon Substrate between Conventional & Proposed Hybrid PEX Flow
  - What makes Proposed Hybrid PEX Flow Important for Si-Interposer SerDes Channel?
  - Proposed Hybrid PEX Flow
- **Summary**

HPC Chip on Si-Interposer



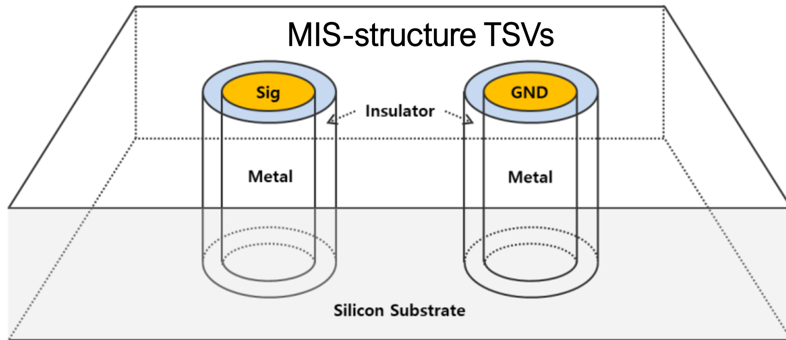
- SerDes Si-Interposer Channel Configuration for External Connection
  - **[Micro-bump ~ BEOL (back-end of line) ~ TSV ~ C4-bump]** ~ PKG ~ BGA ~ Board
  - **Well-known** Critical **TSV** to SI Performance of High-speed Si-Interposer Channel (PCIe Gen4/5, SerDes 56G/112G)
  - How about **BEOL & C4-bump** Impact on the HSI Channel?
  - How to Extract **High-Freq. Resistances & Capacitances of BEOL & C4-bump ?**

How to Extract High-Freq. Model Parameters of BEOL & c4-bump ?



- Model Parameters
  - Micro-bump Pad
    - Resistance / Capacitance / Inductance?
    - Conventional PEX Flow can cover? or 3D Full-wave Tool?
  - BEOL & Silicon-Substrate
    - Resistance / Capacitance / Inductance?
    - Conventional PEX Flow can cover? or 3D Full-wave Tool?
  - TSV & Silicon-Substrate
    - Resistance / Capacitance / Inductance by Well-known 3D Full-wave Tool
    - Conventional PEX Flow can cover?
  - C4-bump Pad & Silicon-Substrate
    - Resistance / Capacitance / Inductance by Well-known 3D Full-wave Tool
  - **How about *Silicon-Substrate Effect on BEOL?***
    - **Same BEOL Environment as TSVs**
    - 3D Full-wave Tool can cover?
    - ***Reasonable Flow considering Design Complexity?***

Remind TSV Model Parameters



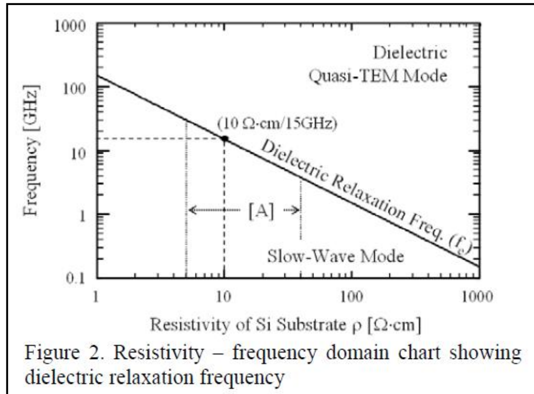
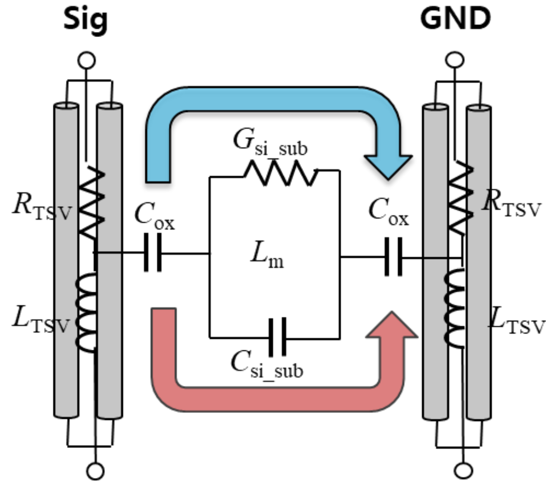


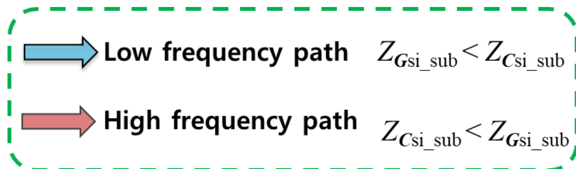
Figure 2. Resistivity – frequency domain chart showing dielectric relaxation frequency

[1] J. S. Pak, et al.," Slow wave and dielectric quasi-TEM modes of Metal-Insulator-Semiconductor (MIS) structure Through Silicon Via (TSV) in signal propagation and power delivery in 3D chip package," in 2010 ECTC, Las Vegas, NV, USA, 2010.

- TSV (Through Silicon Via)
  - **MIS-structure**
    - **Metal-Insulator-Semiconductor**
    - Metal (TSV barrel) surrounded by Insulator (Silicon Oxide) in Semiconductor (Silicon Substrate)
    - TSV Electrical Characteristics following **Slow-Wave Mode**
    - **Large Capacitance & Low Inductance due to** Silicon Substrate
  - Model Parameters
    - **Resistance**: TSV itself, **Silicon Substrate** (Small Conductivity)
    - **Capacitance**: MIS Capacitance between TSV & Silicon Substrate, **Silicon Substrate Capacitance between Two TSVs**
    - **Inductance**: Two Signal & GND TSVs' Loop Inductance
  - **Slow-Wave Mode @ TSVs**
    - **Coming from *Shunt LARGE Resistance* & *SMALL Capacitance of Silicon Substrate between Two TSVs***
    - Due to Small Conductivity Silicon Substrate
    - Resulting in Freq. Dependent Electrical Characteristics

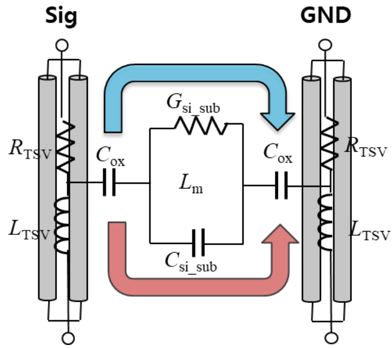
Freq. Dependent Electrical Characteristics of TSV Model





- TSV Model
  - Key TSV Model Parameters for Signal Insertion Loss
    - Parameters of Signal Path from Signal TSV to GND TSV
    - Signal TSV MIS Cap; C_{ox} → Silicon Substrate Conductance; G_{si_sub} & Capacitance; C_{si_sub} → GND TSV MIS Cap; C_{ox}
  - Low Impedance Path between Signal & Ground TSVs
    - @ Low Freq. (➡)
      - $Z_{Gsi_sub} < Z_{Csi_sub}$
      - $Z_{Sig_GND_low_freq} \sim 1/(j\pi \mathbf{C_{ox}})$
      - **High Insertion Loss Increment** ($C_{ox} > 10xC_{si_sub}$)
    - @ High Freq. (➡)
      - $Z_{Gsi_sub} > Z_{Csi_sub}$
      - $Z_{Sig_GND_high_freq} \sim 1/(j\pi \mathbf{C_{si_sub}})$
      - **Low Insertion Loss Increment**

Freq. Dependent Electrical Characteristics of TSV Model



Low frequency path $Z_{G_{si_sub}} < Z_{C_{si_sub}}$

High frequency path $Z_{C_{si_sub}} < Z_{G_{si_sub}}$

Diff. Insertion Loss of GSSG TSV Ch.

Sdd21

Low Insertion Loss Increment

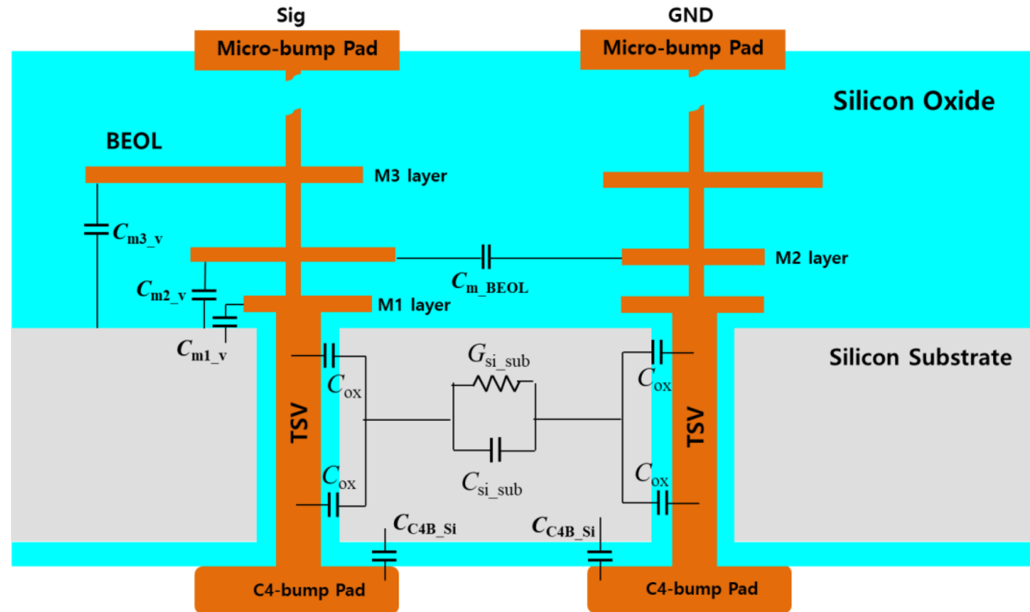
High Insertion Loss Increment

0.00, -0.20, -0.40, -0.60, -0.80, -1.00, -1.20

0.00, 10.00, 20.00, 30.00, 40.00, 50.00

Freq [GHz]

How about BEOL & C4-bump Pad?



- BEOL & C4-bump Pad
  - Electrically **Coupled to Silicon Substrate through Silicon Oxide** = Same as TSV
  - **C4-bump Pad**: Large Dimension & Model Extraction with TSV by **3D Full-wave Tool**
  - **BEOL**: Thin Metal Layer & Narrow Strap-type Power/GND Design & High Density/Complex Design → **What Tool?**

BEOL coupled to TSV & BEOL through Silicon Substrate

Sig
GND
Silicon Oxide
M2 layer
BEOL
M1 layer
TSV
C_{m1_v}
G_{si_sub}
C_{m1_v}
TSV
C_{ox}
C_{si_sub}
C_{ox}
Silicon Substrate

Thin/Narrow/Dense Design above Silicon Substrate

Electrically Coupled to TSV & BEOL through Silicon Substrate

- How to Express Silicon Substrate Effects on BEOL?
  - Conventional PEX Flow
    - Can extract C_{mN_v} (BEOL MIS Cap) values
    - **BUT, those extracted C_{mN_v} are combined into Single Node → NOT Connected to each related Silicon Substrate Gsi_sub & Csi_sub!!!**
    - **Impossible to express High Freq. Characteristics**
  - 3D Full-wave Tool
    - **Can express partial design → NOT extract All C_{mN_v} (BEOL MIS Cap) values**
    - **Impossible to apply real Si-Interposer Design with Reasonable Reiew TAT (turn-around time)**

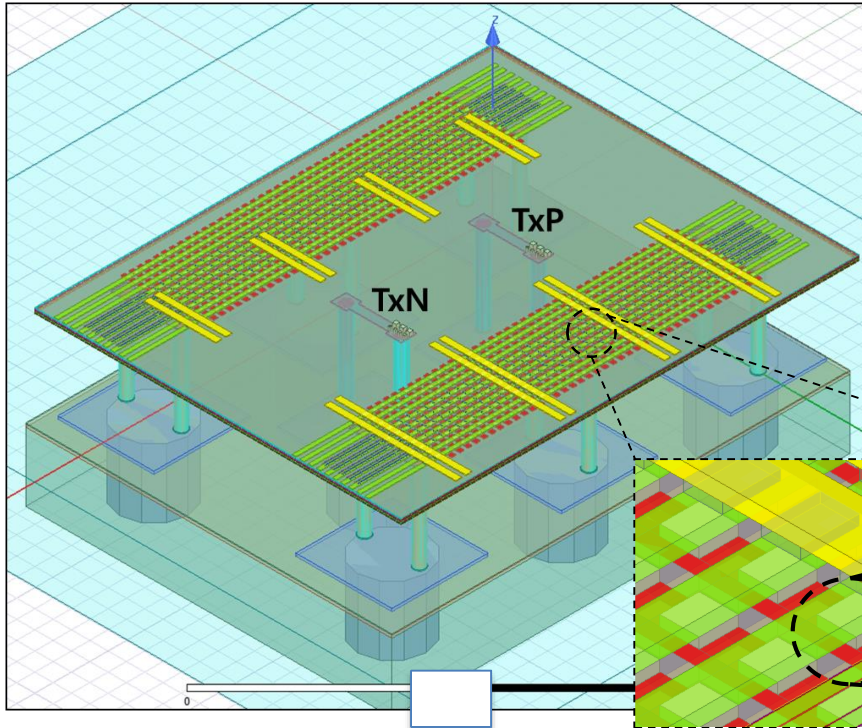
Need BEOL Modeling Flow during TSV Modeling

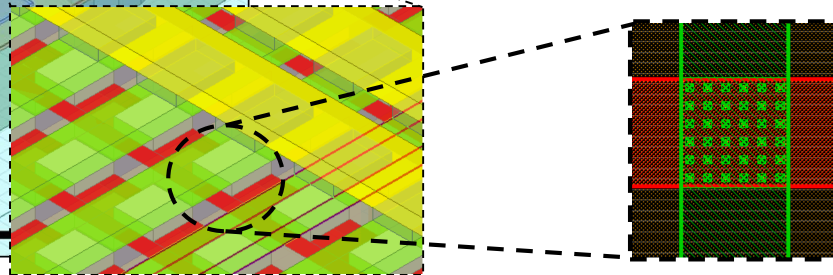
→ Hybrid PEX Flow

- **Proposed Hybrid PEX Flow** instead of **Electrically Isolating** Conventional PEX Flow for BEOL & TSV
  - Adopting Conventional PEX Flow
    - **Apply R-Only PEX** Option to Si-Interposer Design
    - **Extract** Signal/Power/GND Partial **Resistances of Micro-bump Pad, BEOL (Strap/Via), & C4-bump Pad**
    - **Assign short connection path to TSV** between M1 Layer to C4-bump Pad
    - **Convert** Partial Resistances **to S-parameter** by assigning Ports to **Signal-GND & Power-GND** at Micro-bump & C4-bump Sides separately
  - Enabling **3D Full-wave Tool to deal Interactions among BEOL, Silicon Substrate, & TSVs**
    - **Convert M1 Layer Strap Design to Solid Design for letting 3D Full-wave Tool solve BEOL**
      - Consider **Multi-layer Strap Design (M1, M2,,,,MN) MIS Cap almost SAME as M1 Layer Solid Design MIS Cap**
      - Consider **Simple Vertical Structure of Si-Interposer SerDes Channel** for minimizing Loading Capacitance

        While Complex Power/GND Design
    - **Apply Micro-bump & C4-bump Structures for including their Parameters & minimizing Port Parasitic Cap**

Proposed Hybrid PEX Flow Verification





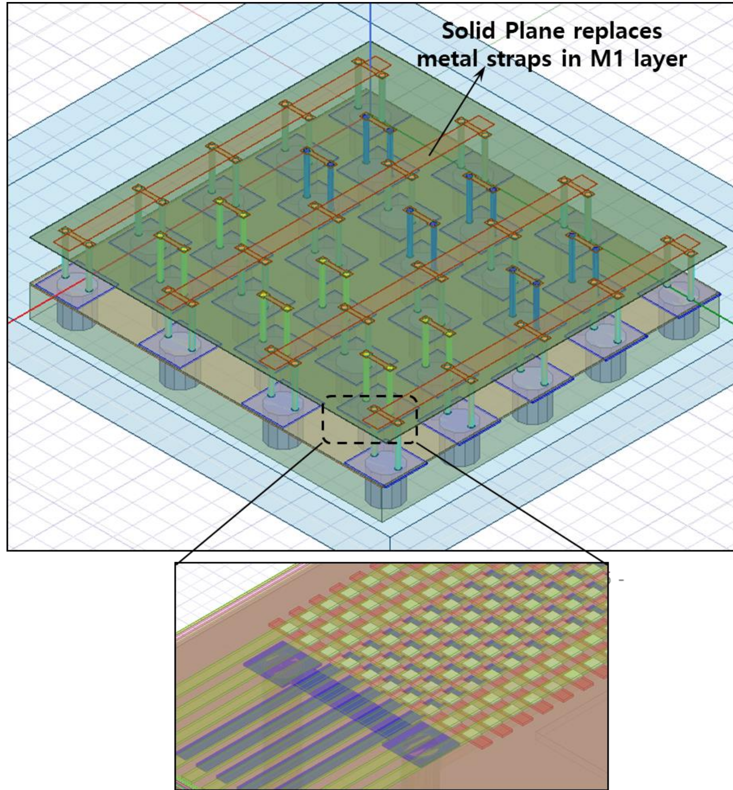
- Verification based on 3D Full-wave Tool
  - Manually Setup 3D Model
    - Adopt **Multi-layer Strap-type BEOL & Dual-TSV Design**
    - Apply **Merged Multiple Micro-via** between Layer by modifying Via Material Conductivity
      - Micro-via # > **150,000EA**
    - Apply **Cylinder-shape Micro-bump & C4-bump**

M1 Layer Solid MIS Cap vs Multi-layer Strap MIS Cap

	Cm_v (Verical Cap)	Cm_s (Sidewall Cap)	Total Cap
Strap Design (BEOL All Layers)	82%	18%	100%
Proposed Solid Design (M1)	**102%**	**2%**	**104%** (Conservative)
Difference	+20%	-16%	**+4%** (Reasonable)

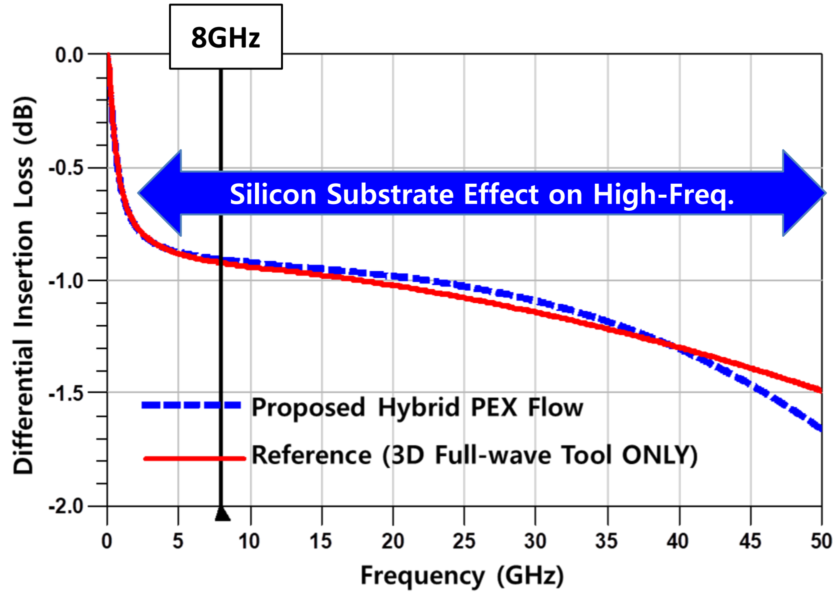
- Comparison MIS Cap of Proposed Solid M1 Design & Original Strap Multi-layer Design
  - Proposed M1 Layer Solid Converting Method well cover Original Design MIS Cap Value
    - Show 4% Conservative & Reasonable Result
    - Use Simple Capacitance Calculation Equation such as Cap = εx [Overlap Area] / [Oxide Thickness]
    - NOT consider Signal-GND capacitance because of Long Distance & Thin BEOL Area
  - 3D Full-wave Tool
    - **Can express partial design → NOT extract All C_{mN_v} (BEOL MIS Cap) values**
    - **Impossible to apply real Si-Interposer Design with Reasonable Review TAT (turn-around time)**

Proposed M1 Layer Solid Design



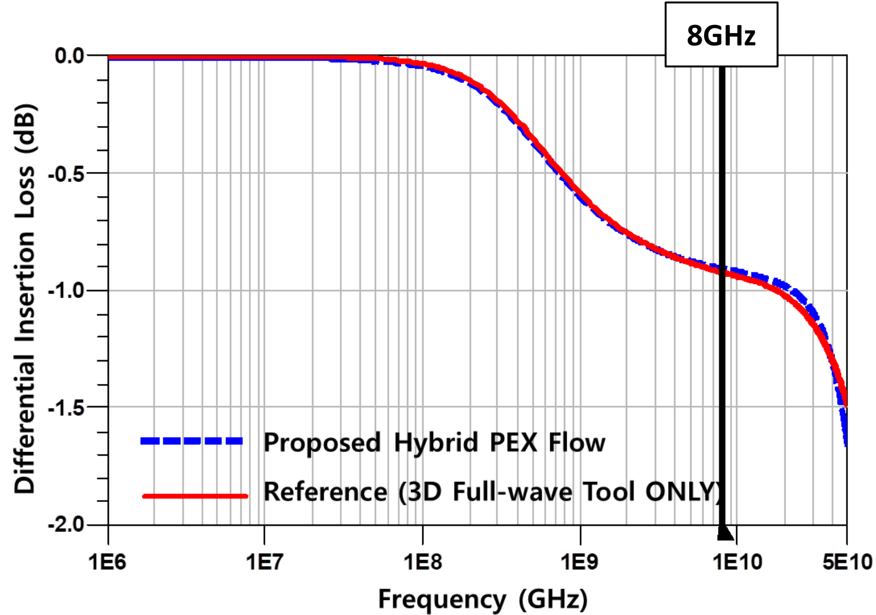
- Proposed M1 Layer Solid Design
  - Let Larger Design Area Analysis Possible
    - C4-bump #: 8 → 32
    - Power Net Included
    - Small Design Review TAT → Good to Design Optimization
  - **Weak Point**
    - Many Manual Jobs → High Human Error Risk
    - Long Initial Design Setting
    - Still, Partial Design Analysis
    - NOT YET, Measurement Correlation

Comparison Sdd21 of Hybrid PEX Flow vs 3D Full-wave Tool Only



- Hybrid PEX Flow
  - Well Agreement with 3D Full-wave Tool Result
    - **Hybrid PEX Flow shows the Discrepancy owing to Over-estimated Inductance Value from Conventional On-chip PEX Tool**
    - NOT Apply Inductance option → MUST Consider Mutual Inductance

Comparison Sdd21 in Log-scaled X-axis



- Hybrid PEX Flow
  - Well Agreement in DC Level

Comparison Z11

Impedance Z11 (Magnitude)

Proposed Hybrid PEX Flow

Reference (3D Full-wave Tool ONLY)

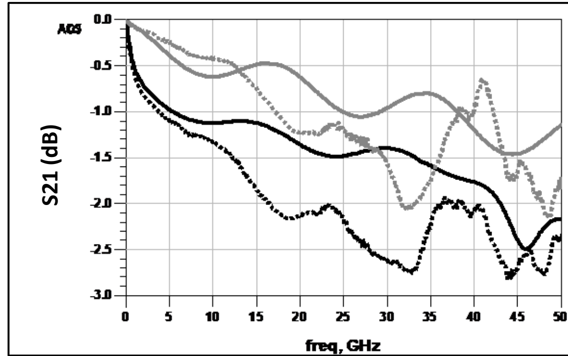
Lowering Resonance Freq.

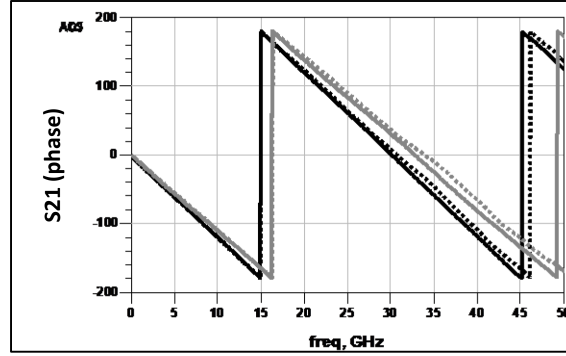
1E6 1E7 1E8 1E9 1E10 5E10

Frequency (GHz)

- Hybrid PEX Flow
  - Well Agreement in Capacitance & Resistance
  - But, Over-estimated Inductance lowers Resonance Freq.

Measurement vs Proposed Hybrid PEX (TSV+PKG)



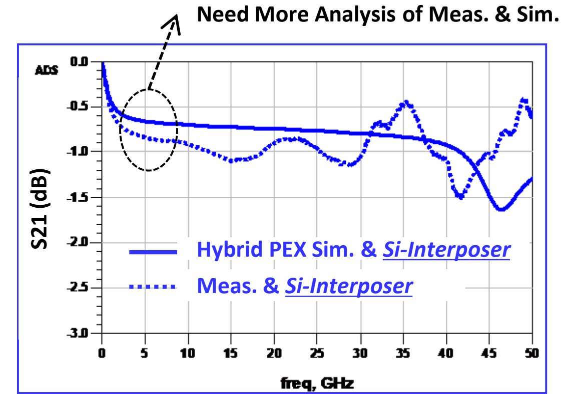


Hybrid PEX Sim. & Si-Interposer + PKG

Meas. & Si-Interposer + PKG

3D Full-wave Sim. & PKG

Meas. & PKG



- Hybrid PEX Flow
  - Interposer: BEOL + TSV + C4-bump → Differences from the previous Results come from Different BEOL Design. (Smaller Cap)
  - Overall Differences between Measurements & Hybrid PEX Simulation mostly come from PKG modeling
  - Need more Analysis for Simulation: Probing Pad Effects, Insulator Thickness, & Silicon Substrate Conductivity

Summary

- **@ Background & Motivation**
  - HPC Chips on Si-Interposer need SerDes Channel including BEOL, TSV, & C4-bump Pad
  - Their Larger Capacitances can be up to 1 pF & Critical Component to SerDes Si-Interposer Channel
- **@ Remind TSV Model Parameters**
  - BEOL, TSV, & C4-bump Pad have MIS (metal-insulator-semiconductor) Structure
  - Their IL shows Freq. Dependent Characteristics due to Silicon Substrate and Consequent MIS Cap
  - Important to SerDes Cannel because SerDes Nyquist Freq. over 10GHz
  - Conventional On-chip PEX Flow gives Wrong way to Si-Interposer SerDes Channel Design
- **@ Proposed Hybrid PEX Flow for Si-Interposer SerDes Channel**
  - For SerDes Si-Interposer Channel, High Freq. Electrical Performance must be well estimated
  - Adopt Conventional On-chip PEX Flow for modeling Resistance only of BEOL & C4bump Pad
  - Adopt 3D Full-wave Tool for modeling Silicon Substrate on BEOL, TSV, & C4-Bump Pad by converting Strap-type M1 Layer Design to Solid-type M1 Layer Design
- **Proposed Hybrid PEX Flow shows Reasonable Results**

Thank you!

QUESTIONS?