Signal Integrity Issues for High-Speed Serial Differential Interconnects

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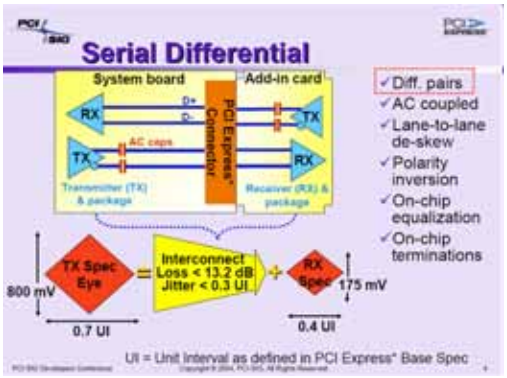
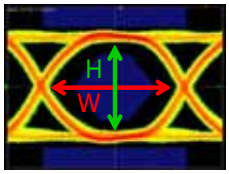
Outline

1. Introduction
2. Properties of Differential Signaling
3. Differential Bend
4. Differential Delay Lines
5. Differential traces crossing slot
6. Optimized Decoupling Capacitor
7. Conclusions

1. Introduction (1/3)





Eye Diagram

PCI Express, USB2.0, Searial ATA, 1394, etc.

LVDS (Low Voltage Differential Signaling)

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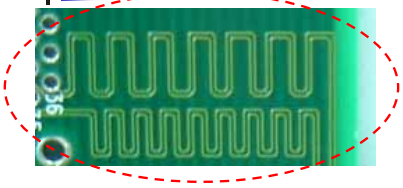
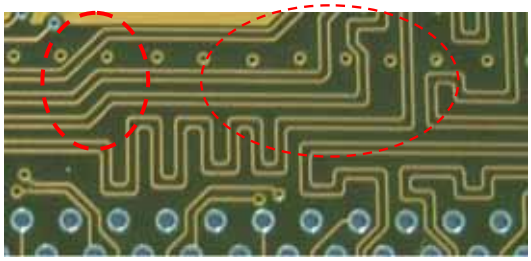
1. Introduction (2/3)



Differential Delay Line

Differential Bend

Dual Differential Bend



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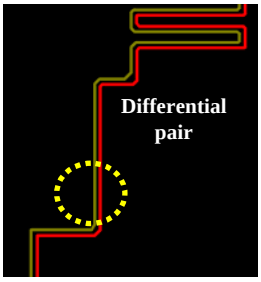
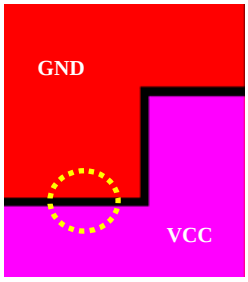
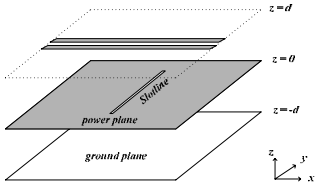
1. Introduction (3/3)

Differential Pair crossing Slot







Signal layer *Power plane*

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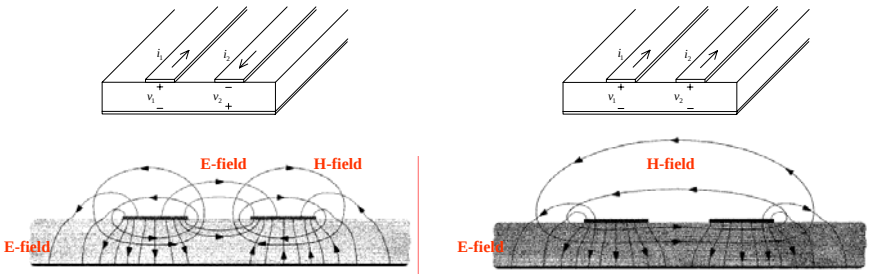
Differential Signaling

Differential signaling (*odd-mode propagation*) implies that two traces in a microstrip or strip geometry are coupled and sourced with signals of equal-magnitude and 180°-phase-shift between them.

odd-mode propagation ***even-mode propagation***



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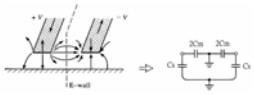
Properties and Benefits of Differential Signaling

Properties :

- **Switching** in differential signaling relies on the crossing of the signals in the two traces.
- The **virtual ground** provides an alternative reference.



- The **return current has two paths** back to the source, on the adjacent trace and on the reference plane.

Benefits :

- ***Large immunity*** to reflection noise and signal attenuation.
- ***EMI reduction*** due to the cancellation of the magnetic field resulting from the opposing current flows.
- ***Less susceptible*** to external common mode noise.

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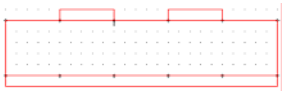
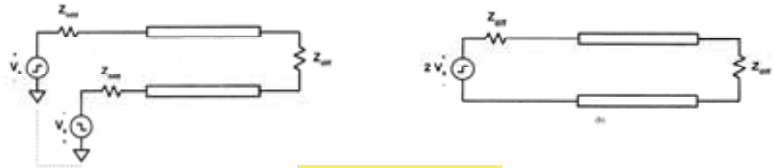
Differential Impedance Calculation



	object3	object4
object3	66.991	13.369
object4	13.369	67.073

$$Z_0 = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{12} & Z_{22} \end{bmatrix} \longrightarrow \begin{aligned} Z_{differential} &= 2\times(Z_{11} - Z_{12}) \\ Z_{common} &= 1/2\times(Z_{11} + Z_{12}) \end{aligned}$$

Simulation by Ansoft SI2D



$$Z_{differential} = 2\times Z_{odd}$$

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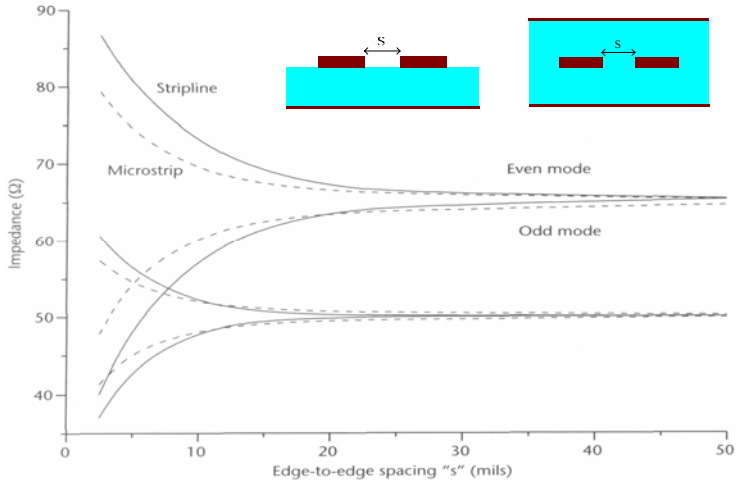
Ref : Per E. Fornberg, Mark Kanda, P. M. Melinda, and H. H. Stephen, "The impact of nonideal return path on differential signal integrity," *IEEE Trans. Electromagn. Compat.*, Vol. 44, pp.671-676, Feb. 2002.

Impedance vs. Trace Spacing



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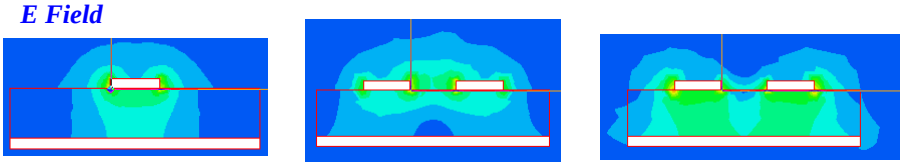
Ref :Thierauf, High-speed circuit board signal integrity.

Simulation by Ansoft SI2D

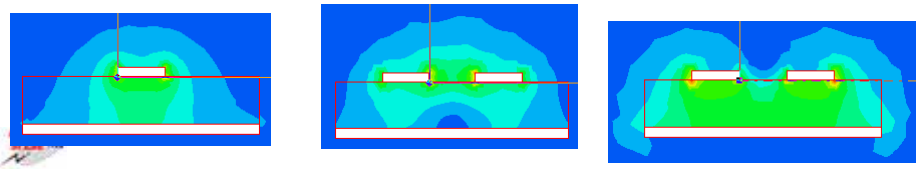
Field Distribution of Differential Microstrip Line

Single line | Differential mode | Common mode

E Field



H Field



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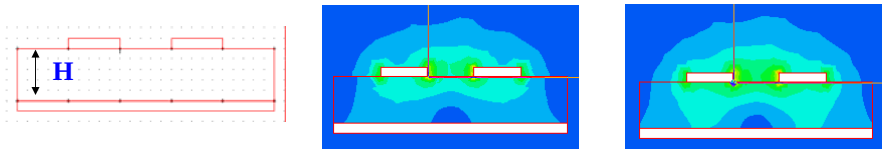
Simulation by Ansoft SI2D

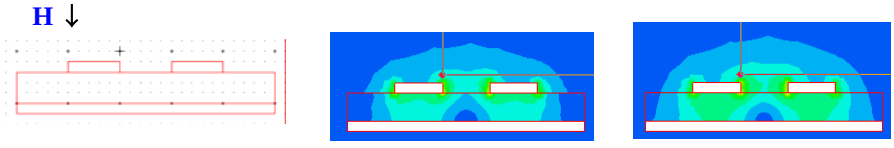
Field Distribution of Differential Microstrip Line

Differential mode

E Field | *H Field*



H ↓



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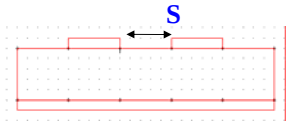
Simulation by Ansoft SI2D

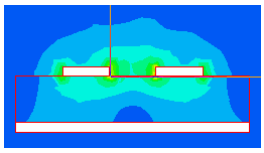
Field Distribution of Differential Microstrip Line

Differential mode

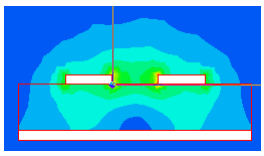
S



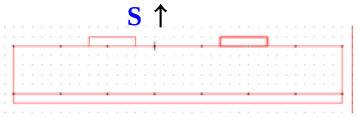
E Field



H Field



S ↑



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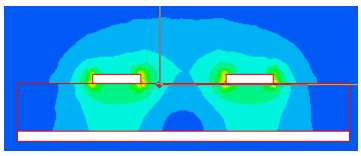
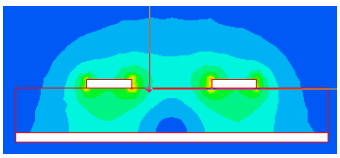


H Field



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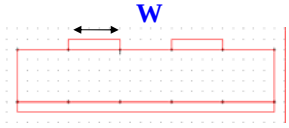
Simulation by Ansoft SI2D

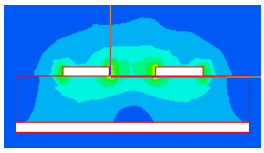
Field Distribution of Differential Microstrip Line

Differential mode

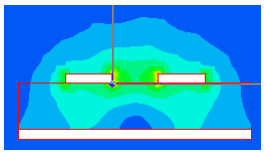
W



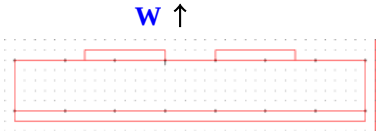
E Field



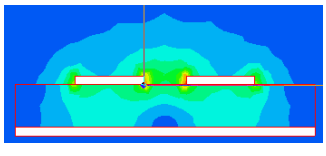
H Field



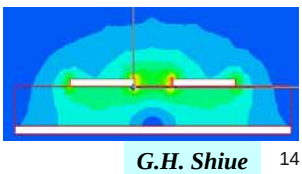
W ↑



E Field



H Field



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Outline

1. *Introduction*
2. *Properties of Differential Signaling*
3. *Differential Bend*
4. *Differential Delay Lines*
5. *Differential traces crossing slot*
6. *Optimized Decoupling Capacitor*
7. *Conclusions*

Ref. : G.H. Shiue, W.D. Guo, and R.B. Wu, "Circuit modeling and noise reduction for bent differential transmission lines," *IEEE 13th Topical Meeting on Electrical Performance of Electronic Packaging*, pp. 143-146, Oct. 2004.

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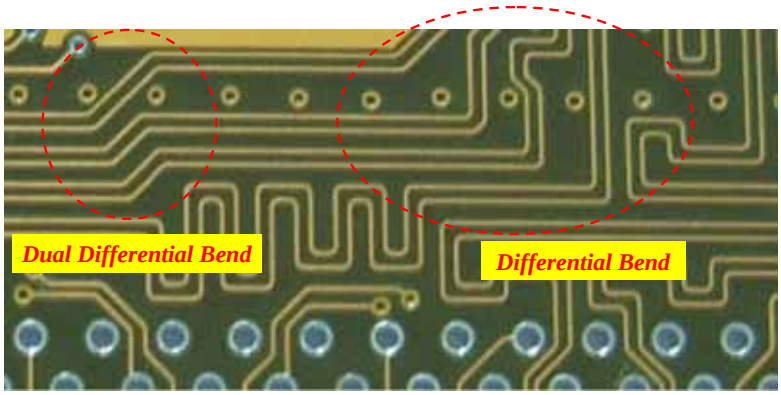
Practical Differential Bend Structures



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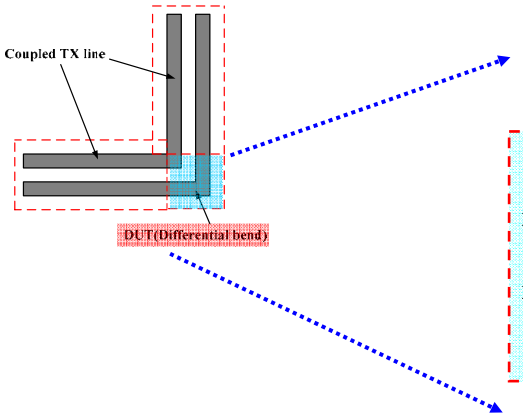
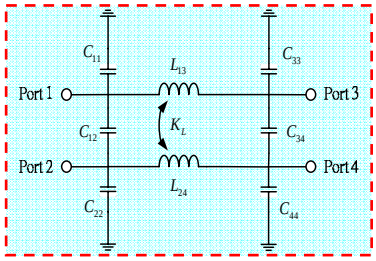
Bent Coupled Transmission Line



Equivalent circuit model



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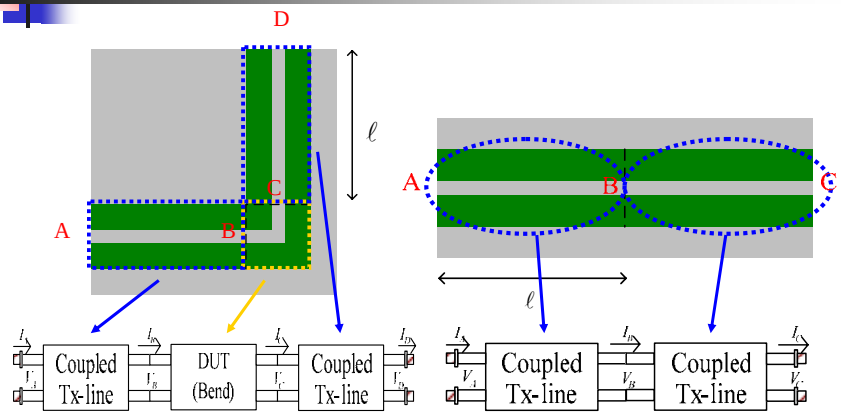
De-embedding Technique for Strongly Coupled Structures



$$\begin{bmatrix} \vec{V}_A \\ \vec{I}_B \end{bmatrix} = \begin{bmatrix} \vec{A}_l & \vec{B}_l \\ \vec{C}_l & \vec{D}_l \end{bmatrix} \begin{bmatrix} \vec{A}_D & \vec{B}_D \\ \vec{C}_D & \vec{D}_D \end{bmatrix} \begin{bmatrix} \vec{A}_l & -\vec{B}_l \\ -\vec{C}_l & \vec{D}_l \end{bmatrix}^{-1} \begin{bmatrix} \vec{V}_D \\ \vec{I}_D \end{bmatrix} \qquad \begin{bmatrix} \vec{V}_A \\ \vec{I}_B \end{bmatrix} = \begin{bmatrix} \vec{A}_l & \vec{B}_l \\ \vec{C}_l & \vec{D}_l \end{bmatrix} \begin{bmatrix} \vec{A}_l & -\vec{B}_l \\ -\vec{C}_l & \vec{D}_l \end{bmatrix}^{-1} \begin{bmatrix} \vec{V}_C \\ \vec{I}_C \end{bmatrix}$$

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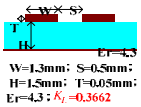
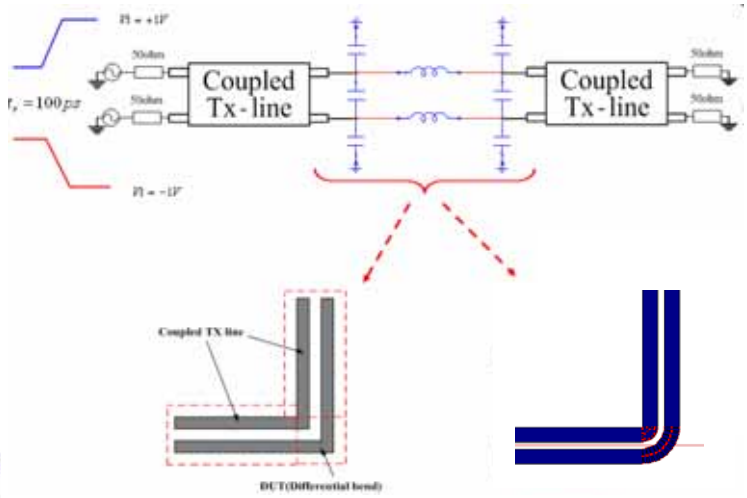
Simulation Setup



W=1.3mm; S=0.5mm;
H=1.5mm; T=0.05mm;
Er=4.3 ; K_f =0.3662



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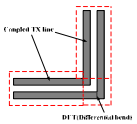
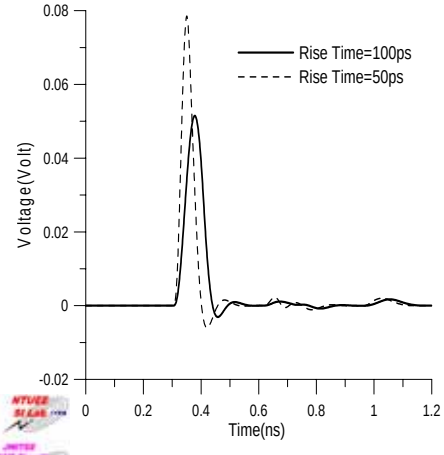
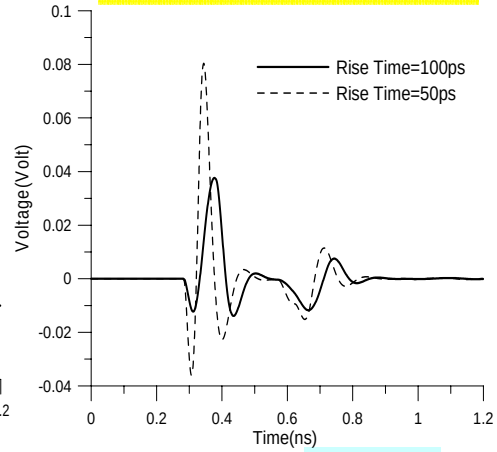
Time Domain Simulation Results —Rise Time Effect



common mode noise at receiver



reflected differential mode noise at sending end



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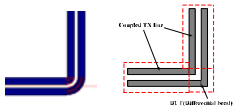
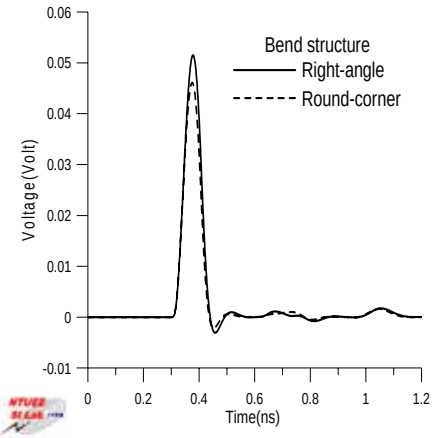
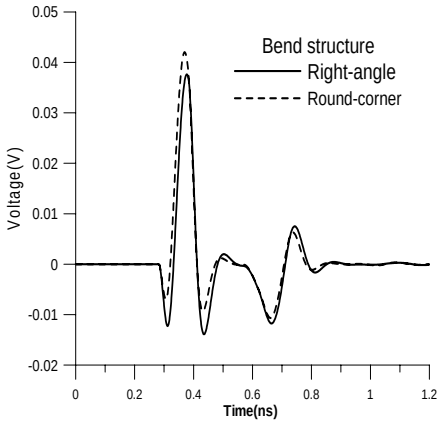
Time Domain Simulation Results —Different Bend Effect



common mode noise at receiver



reflected differential mode noise at sending end



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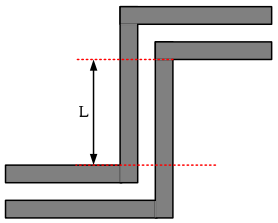
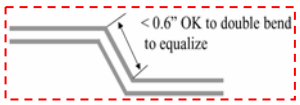
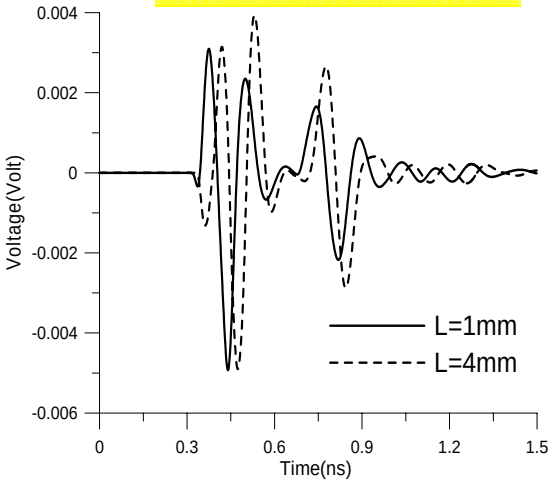
Time Domain Simulation Results —Dual Bend Effect

common mode noise at receiver





Ref : Intel layout guideline



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1. *Introduction*
2. *Properties of Differential Signaling*
3. *Mixed-mode S-Parameter*
4. *Differential Bends*
5. *Differential Delay Lines*
6. *Differential traces crossing slot*
7. *Conclusions*

Ref. : W.D. Guo, G.H. Shiue, and R.B. Wu, "Comparison between flat spiral and serpentine differential delay lines on TDR and TDT," *IEEE 13th Topical Meeting on Electrical Performance of Electronic Packaging*, pp. 147-150, Oct. 2004.

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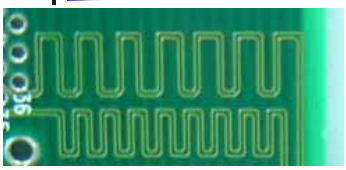
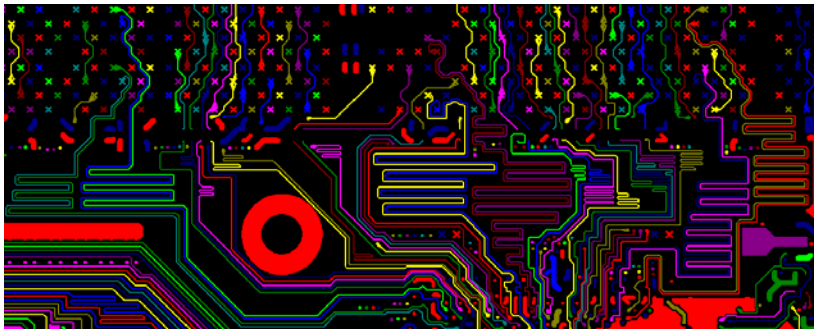
Practical Differential Bend Structures



Differential Delay Line



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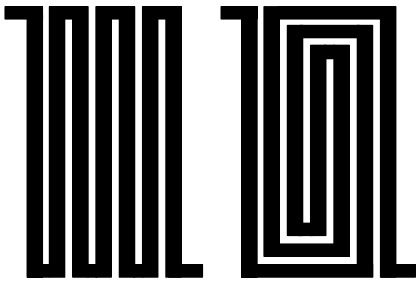
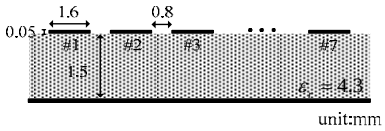
Single Delay Lines

serpentine flat spiral





unit:mm

Quantitatively, the magnitude of near-end and far-end crosstalk can be formulated as

$$V_{(\text{near end})} = \frac{V_{(\text{input})}}{4}\left(\frac{L_m}{L_s} + \frac{C_m}{C_s}\right)$$

$$V_{(\text{far end})} = -\frac{V_{(\text{input})} \times T_D}{2T_r}\left(\frac{L_m}{L_s} - \frac{C_m}{C_s}\right)$$

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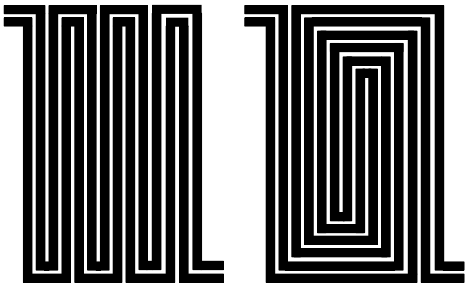
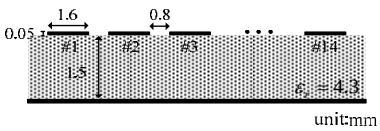
Differential Delay Lines

serpentine flat spiral





unit:mm

$V_2 = -V_1 \quad Q_2 = -Q_1$

$$C_{s,\ differ.} = (C_{11} + C_{22} - C_{12} - C_{21})/2$$

$$C_{m,\ differ.\ to\#3} = C_{31} - C_{32}$$

$$C_{m,\ differ.\ to\#4} = C_{41} - C_{42}$$

$$L_{s,\ differ.} = (L_{11} + L_{22} - L_{12} - L_{21})/2$$

$$L_{m,\ differ.\ to\#3} = L_{31} - L_{32}$$

$$L_{m,\ differ.\ to\#4} = L_{41} - L_{42}$$

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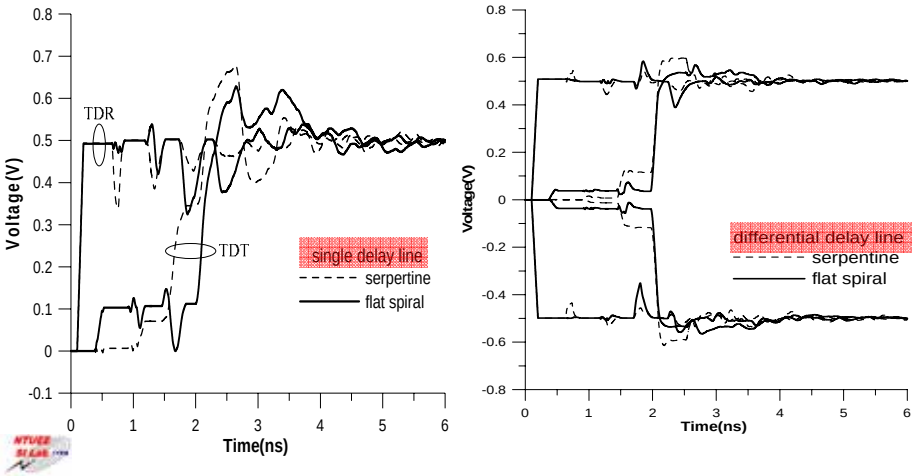
Time Domain Simulation Results



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Outline

1. Introduction
2. Properties of Differential Signaling
3. Differential Bend
4. Differential Delay Lines
5. Differential traces crossing slot
6. Optimized Decoupling Capacitor
7. Conclusions

Ref. : G.H. Shiue, S.M. Lin, and R.B. Wu, "Reduction in reflections and ground bounce for signal line through a split power plane by using differential coupled microstrip lines," *IEEE 12th Topical Meeting on Electrical Performance of Electronic Packaging* , pp. 107-110, Oct. 2003.

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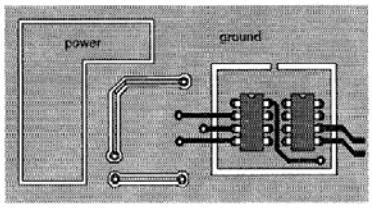
Motivation(1/2)

- **Slots are common in PCB or MLC**
  - Split image planes for multiple power distribution
  - Isolated islands in power/ground plane to isolate a noisy or sensitive circuit from other circuits
- **Signal lines crossing slots to communicate with other chips cause SI concerns:**
  - *Reflection* due to the discontinuity in signal return path
  - *Ground bounce* between power and ground planes



Ref. : H. J. Liaw and H. Merkelo, "Signal integrity issues at split ground and power planes, " *Proceedings of 46th IEEE Electronic Components and Technology Conference*, 1996, pp. 752 –755.

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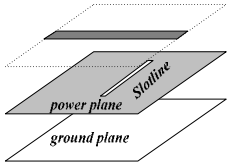
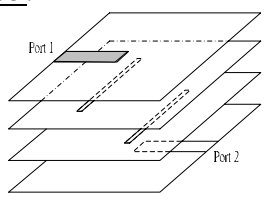
Motivation(2/2)

- Although ground bounce caused by a single slot coupling is only about 5% of input signal, the effects can not be ignored as multi-trace signal flows through the slot simultaneously.
- The slot induced bounce may result in significant coupled noise on distant quiet signal line with peak-to-peak noise voltage exceeding 15% of the input signal level.





Ref. : C. T. Wu, G. H. Shiue, S. M. Lin, and R. B. Wu, "Composite effects of reflections and ground bounce for signal line through a split power plane," *IEEE Trans. Adv. Packaging*, Vol. 25, pp. 297-301, May 2002.

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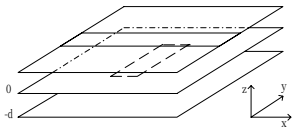
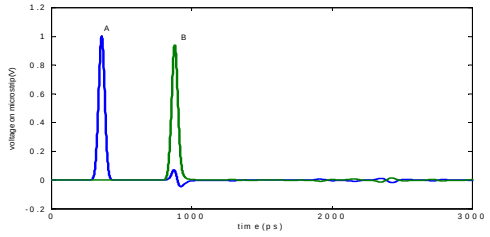
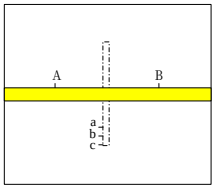
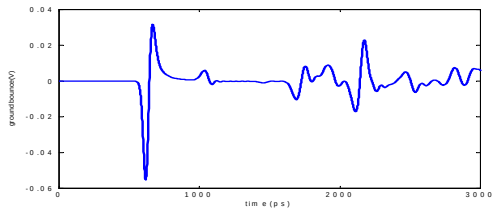
Single Trace crossing Slot









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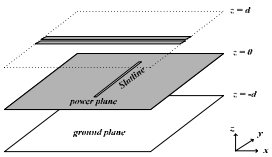
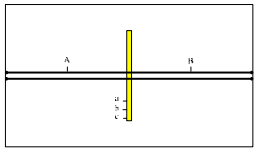
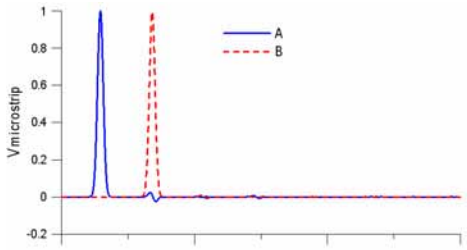
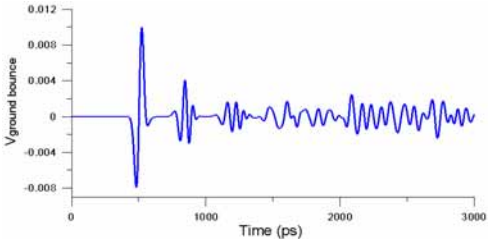
Differential Pair crossing Slot



Coupling factor = 0.35







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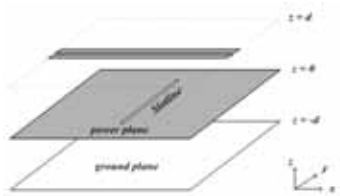

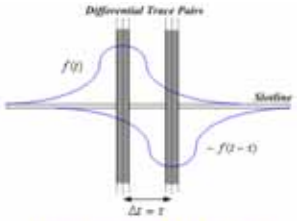

The resultant slot voltage

w(mm)	s(mm)	coupling factor	V_{sb}/V_{in} (%)
0.25	0.25	0.305	0.89%
0.38	0.50	0.180	1.71%
0.50	1.00	0.082	2.48%

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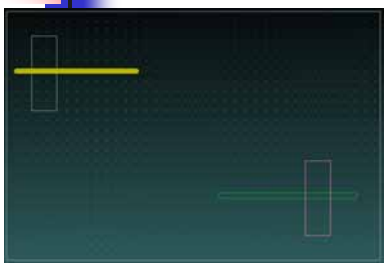
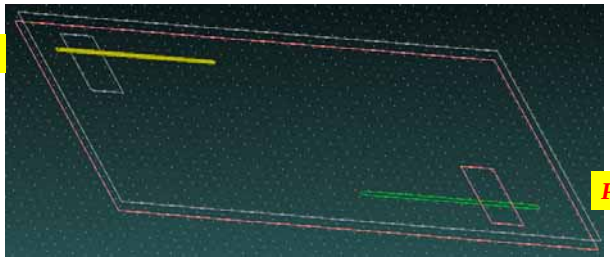
Simulation by Ansoft SIwave 3.0

Noise Coupling by Slot (1/5)



Port 1



Port 2

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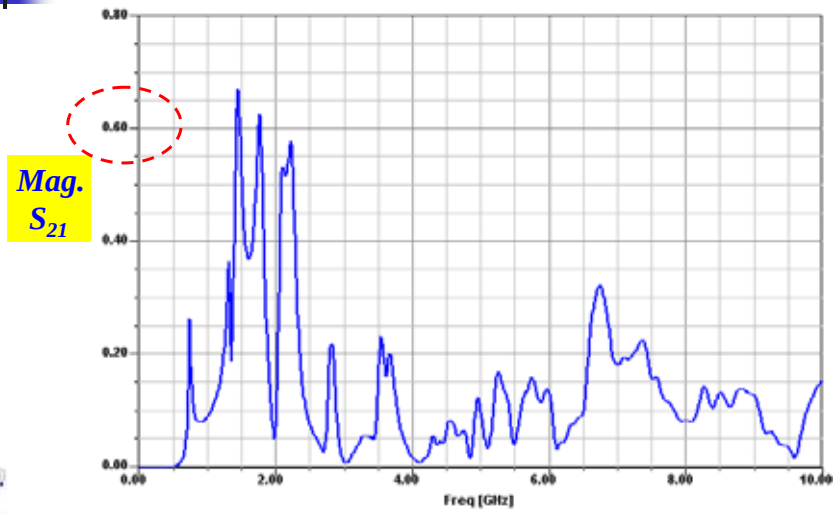
Simulation by Ansoft SIwave 3.0

Noise Coupling by Slot (2/5)



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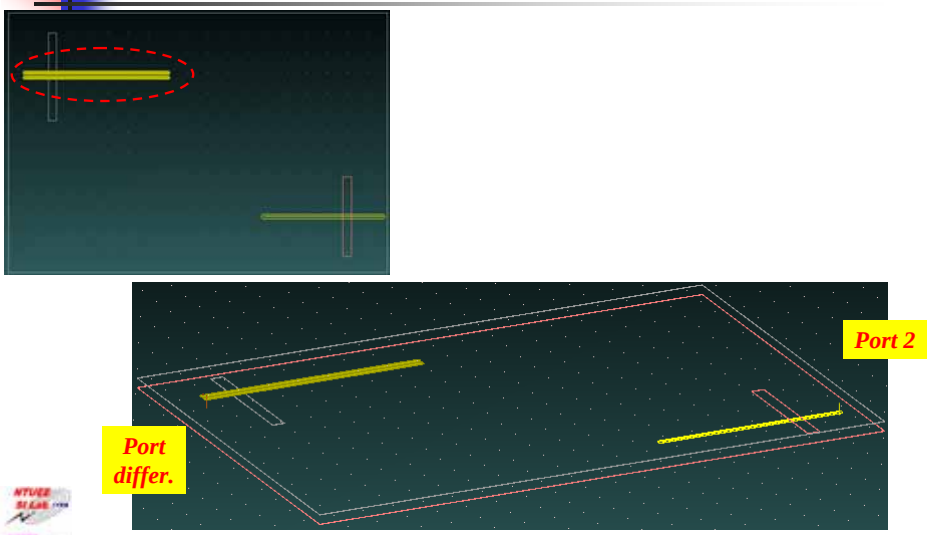
Simulation by Ansoft SIwave 3.0

Noise Coupling by Slot (3/5)



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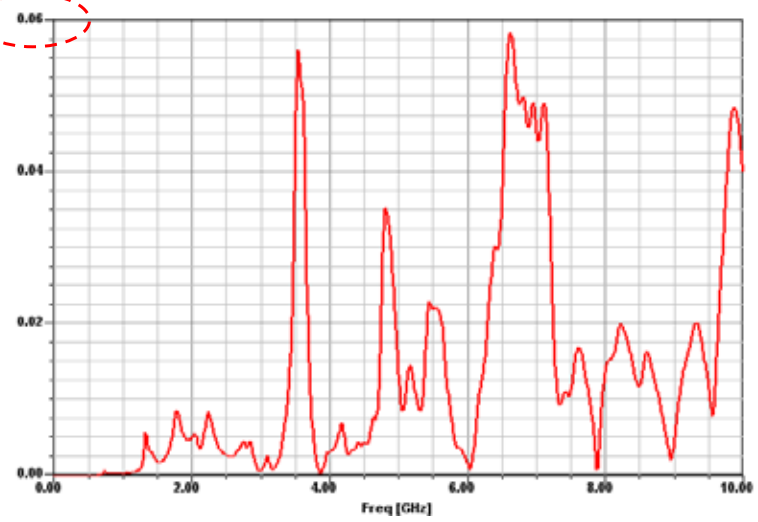
Simulation by Ansoft SIwave 3.0

Noise Coupling by Slot (4/5)



Mag. $S_{differ.2}$

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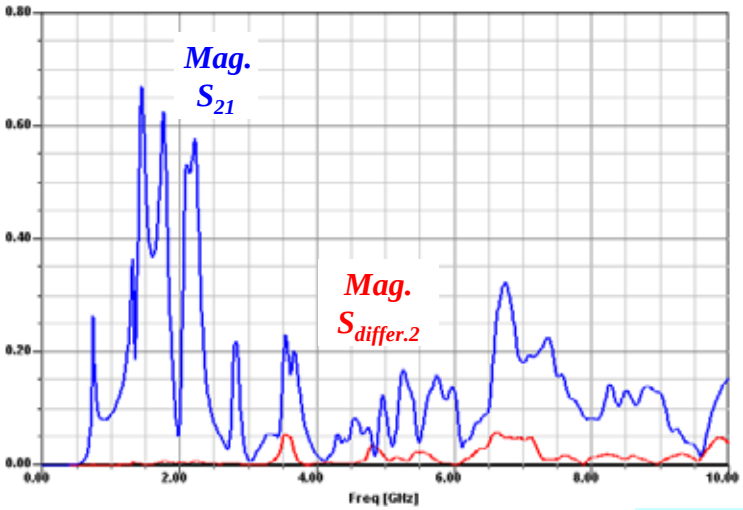
Simulation by Ansoft SIwave 3.0

Noise Coupling by Slot (5/5)



Mag. S_{21}

Mag. $S_{differ.2}$

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Outline

1. *Introduction*
2. *Properties of Differential Signaling*
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6. *Optimized Decoupling Capacitor*
7. *Conclusions*

Ref. : K.B. Wu, A.S. Liu, G.H. Shiue, C.M. Lin, and Ruey-Beei Wu ,"Optimization for the locations of decoupling capacitors in suppressing the ground bounce by genetic algorithm," *Progress in Electromagnetics Research Symposium*, Hangzhou, Zhejiang, China, Aug. 2005.

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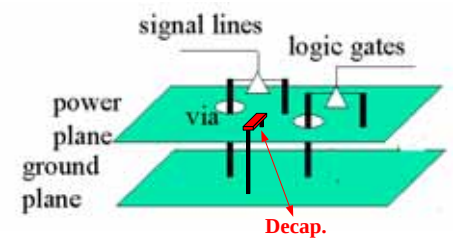
Motivation

- In high-speed digital printed circuit board (PCB), noise may happen on the power bus due to a sudden change during the high-to-low or low-to-high transition.
- Simultaneous switching noise (SSN) may result in signal integrity and electromagnetic interference problems in high-speed system.



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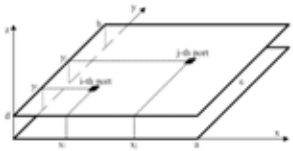
Cavity Model for Bare Board



$$Z_{ij} = j\omega\mu h \sum_{m=0}^{\infty}\sum_{n=0}^{\infty} \frac{\chi_{mn}^2}{ab(k_{xm}^2 + k_{ym}^2 - k^2)} \cos(k_{ym}y_i)\cos(k_{xm}x_i)\,\mathrm{sinc}\left(\frac{k_{ym}dy_i}{2}\right)$$
$$\times \mathrm{sinc}\left(\frac{k_{xm}dx_i}{2}\right)\cos(k_{ym}y_j)\cos(k_{xm}x_j)\,\mathrm{sinc}\left(\frac{k_{ym}dy_j}{2}\right)\mathrm{sinc}\left(\frac{k_{xm}dx_j}{2}\right)$$

where $k_{xm} = m\pi/a$, $k_{ym} = n\pi/b$, $k = \omega\sqrt{\varepsilon_0\varepsilon\mu}$ and

$$\begin{cases} \chi_{mn}^2 = 1 \text{ for m=n=0} \\ \chi_{mn}^2 = 2 \text{ for m=0 or n=0} \\ \chi_{mn}^2 = 4 \text{ for m} \neq 0,\ \text{n} \neq 0 \end{cases}$$

Ref. : M. Xu and T. H. Hubing, "Estimating the power bus Impedance of printed circuit boards with embedded capacitance," *IEEE Trans. Adv. Packa.*, Vol. 25, pp. 424-432, Aug. 2002.

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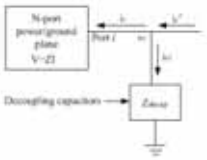
Decoupling Capacitors Connected to Bare Board



$$V = \begin{bmatrix} V_1 \\ V_2 \\ \bullet \\ \bullet \\ V_n \end{bmatrix} = \begin{bmatrix} Z_{decap,1} \cdot I_{c1} \\ Z_{decap,2} \cdot I_{c2} \\ \bullet \\ \bullet \\ Z_{decap,n} \cdot I_{cn} \end{bmatrix} = \begin{bmatrix} Z_{decap,1} & 0 & 0 & 0 & 0 \\ 0 & Z_{decap,2} & 0 & 0 & 0 \\ 0 & 0 & \bullet & 0 & 0 \\ 0 & 0 & 0 & \bullet & 0 \\ 0 & 0 & & & Z_{decap,n} \end{bmatrix}_{n\times n} \begin{bmatrix} I_{c1} \\ I_{c2} \\ \bullet \\ \bullet \\ I_{cn} \end{bmatrix} = Z_{decap} \cdot I_c$$

$$I' = I_c + I \Rightarrow I' = \frac{Z \cdot Z_{decap}}{(Z + Z_{decap})} \cdot I = \left(Z^{-1} + Z_{decap}^{-1}\right)^{-1} \cdot I = Z_{in} \cdot I$$

where $Z_{decap} = \begin{bmatrix} Z_{decap,1} & 0 & 0 & 0 & 0 \\ 0 & Z_{decap,2} & 0 & 0 & 0 \\ 0 & 0 & \bullet & 0 & 0 \\ 0 & 0 & 0 & \bullet & 0 \\ 0 & 0 & & & Z_{decap,n} \end{bmatrix}_{n\times n}$ is a diagonal matrix with *i*-th diagonal element $z_{decap,i} = (1/j\omega C_i) + j\omega L_{ESL,i} + R_{ESR,i}$

Ref. : J. Choi, S. Chun, and M. Swaminathan, "Modeling and transient simulation of planes in electronic packages," *IEEE Trans. Adv. Packa.*, Vol. 23, pp. 340-352, Aug. 2000.

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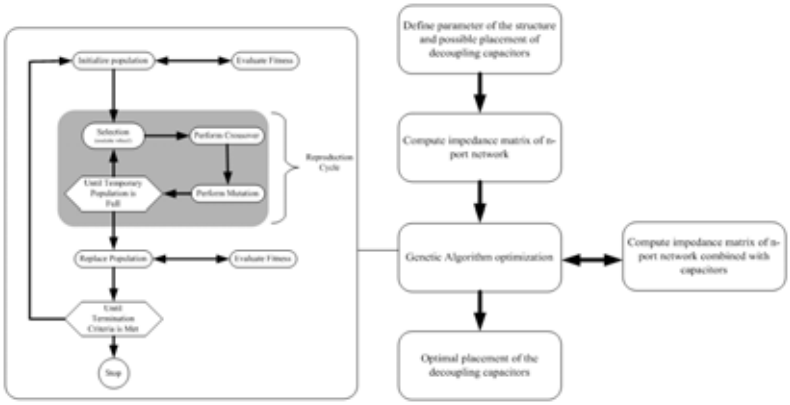
G.H. Shiue

Block Diagram of Proposed Method Combined with Genetic Algorithm Optimizer



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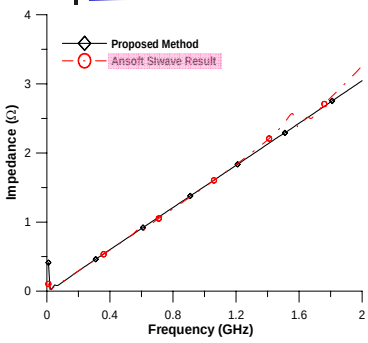
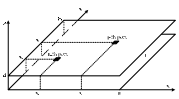
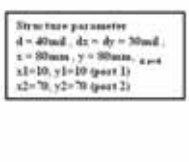
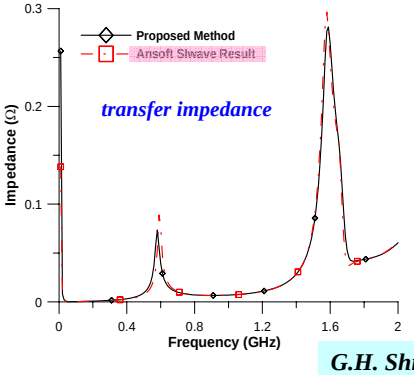
Optimal Result – with Parasitic Effect



input impedance







transfer impedance

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Conclusions

- Differential signaling has become a popular choice for multi-gigabit digital applications, due to its low noise generation and high common-mode noise immunity.
- The dual coupled bend can be helpful for reducing the common mode noise, however the compensation becomes less effective if the length of coupled lines between the two coupled bends increases. .
- In case of differential serpentine and flat spiral delay lines where the crosstalk induced noise is greatly reduced.
- Using differential coupled microstrip lines flowing above a split power or ground plane can significantly reduce the effects of slot induced ground bounce and the reduction factor depends on the coupling factor.
- GA optimizer is proposed to deal with the problem of the optimal placement, value, and amount of decoupling capacitors.

Thank you for your attendance !

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