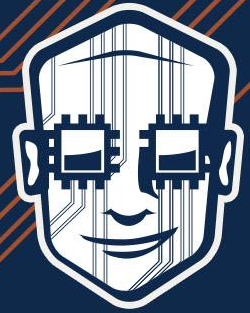


DESIGNCON[®] 2015



**EFFECTIVE ROUGHNESS
DIELECTRIC TO REPRESENT
COPPER FOIL ROUGHNESS IN
PRINTED CIRCUIT BOARDS**

14-TH4

**Marina Koledintseva (Oracle), Oleg Kashurkin (Missouri
S&T), Tracey Vincent (CST of America), and
Scott Hinaga (Cisco Systems)**

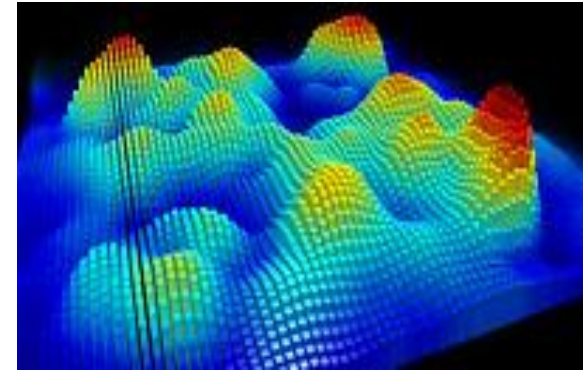


Abstract

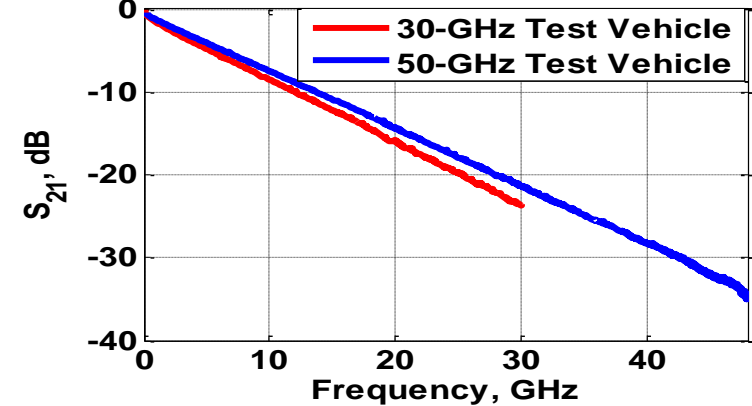
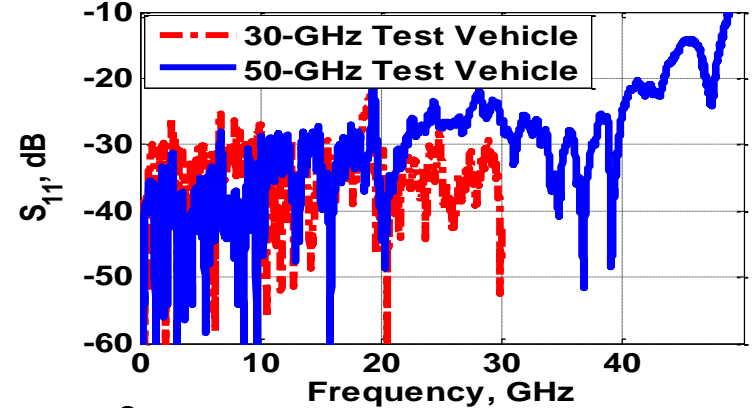
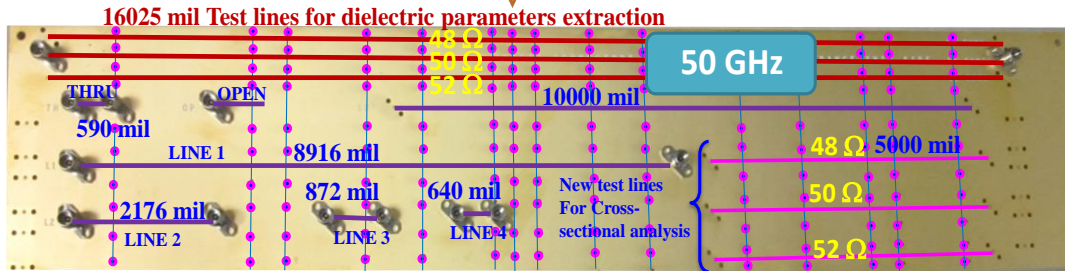
- Conductor roughness must be included in simulations of PCB designs at frequencies above a few gigahertz - to accurately predict the insertion loss and delay time on the transmission lines.
- An effective roughness dielectric (ERD) model can be used to substitute an inhomogeneous interface between copper foil and laminate dielectric in a PCB.
- It is tempting to have an analytical model to predict ERD parameters. We provide a basis for such a model.
- However, an empirical approach based on the matching between the measured and numerically modeled results has proven to be simpler and more efficient. Based on the extracted ERD parameters “design curves” have been built.
- The verification using 3D full-wave numerical simulations of a set of stripline test vehicles has been done.
- The parameters of an ambient laminate dielectric free of conductor roughness effects in the striplines are determined using differential extrapolation roughness measurement (DERM) technique.
- The agreement of the 3D full-wave modeling results and measurements on multiple test structures validates the proposed approach.

Outline

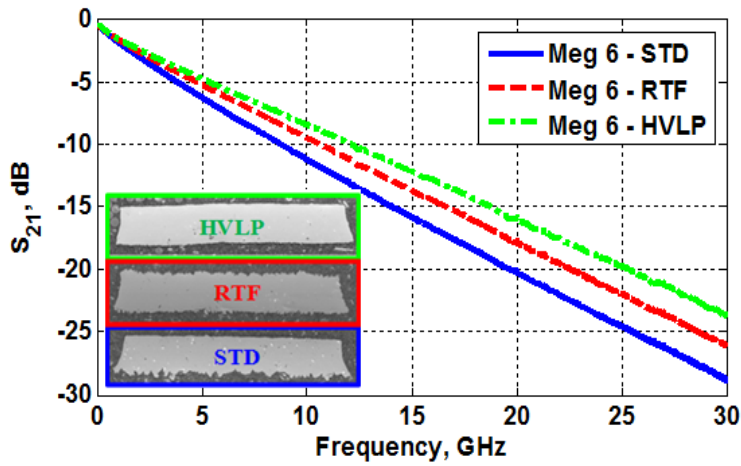
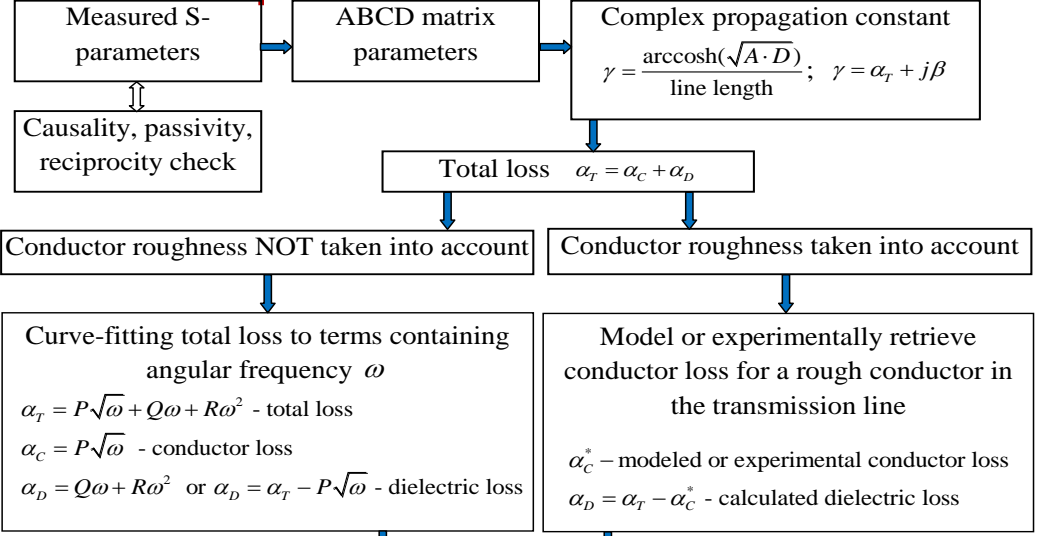
- I. Introduction
- II. Description of S3 Technique to Extract DK and DF of PCB Substrate Dielectrics
- III. Copper Foil Roughness Quantification
- IV. PCB Dielectric Material Parameters Extraction
- V. Extraction of Effective Roughness Dielectric (ERD) Parameters
- VI. Validation of ERD Extracted Data by Numerical Simulations
- VII. Design Curves for Conductor Roughness Modeling in PCB Designs
- VIII. Conclusions



S3 Technique: from Measured S-parameters to DK & DF of a PCB Dielectric Substrate

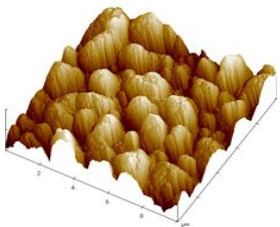


S3 Technique to Extract DK & DF of a PCB Dielectric Substrate



Roughness characterization:

- Analytical Models
- Numerical Models
- Experimental



A. Koul, M. Koledintseva et al, "Differential extrapolation method for separating dielectric and rough conductor losses in printed circuit boards", *IEEE Trans. Electromag. Compat.*, vol. 54, no. 2, Apr. 2012, pp. 421-433.

Solving the system of equations for complex permittivity $\epsilon_r = \epsilon'_r - j\epsilon''_r$

$$\begin{cases} \beta = \frac{\omega}{c} \sqrt{(\epsilon'_r)^2 + (\epsilon''_r)^2} \times \cos(\delta/2) \\ \alpha_d = \frac{\omega}{c} \sqrt{(\epsilon'_r)^2 + (\epsilon''_r)^2} \times \sin(\delta/2) \end{cases}$$

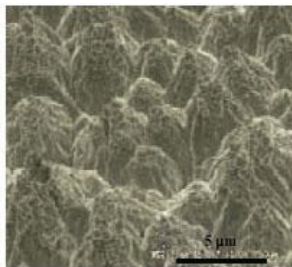
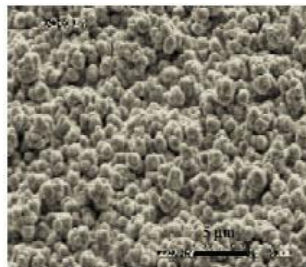
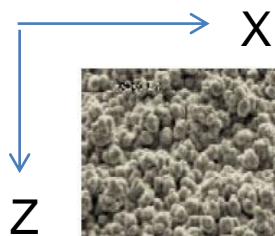
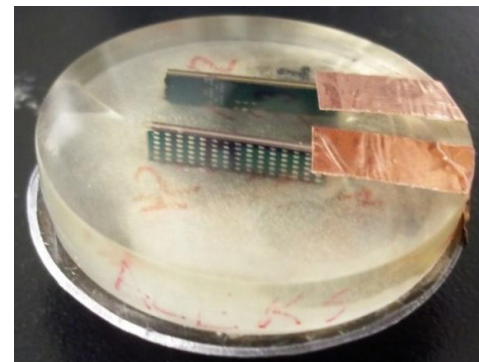
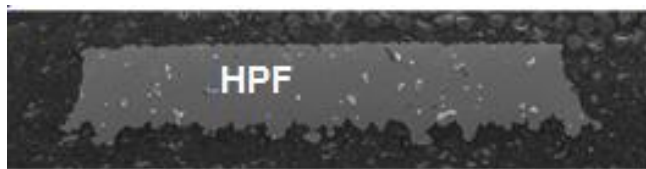
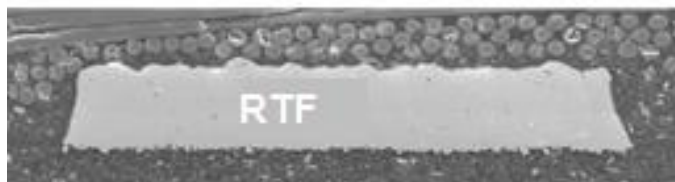
c – speed of light in vacuum

$$\epsilon'_r = x \sqrt{\frac{x}{x+y}} \quad \text{and} \quad \epsilon''_r = x \sqrt{\frac{y}{x+y}}$$

$$x = \left(\frac{\beta c}{\omega}\right)^2 \quad \text{and} \quad y = \left(\frac{2c\alpha_d}{\omega}\right)^2$$

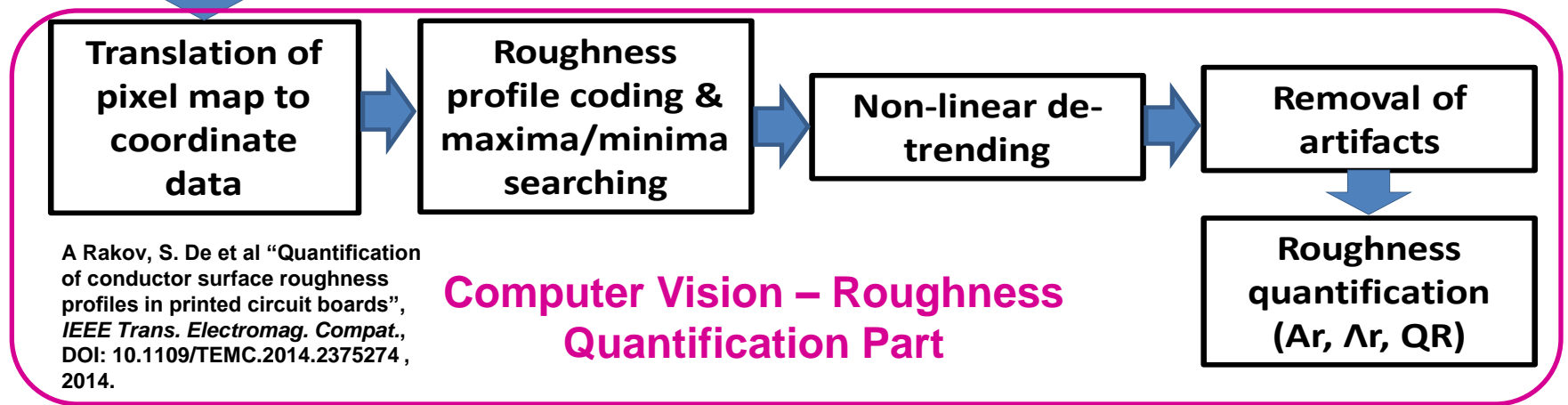
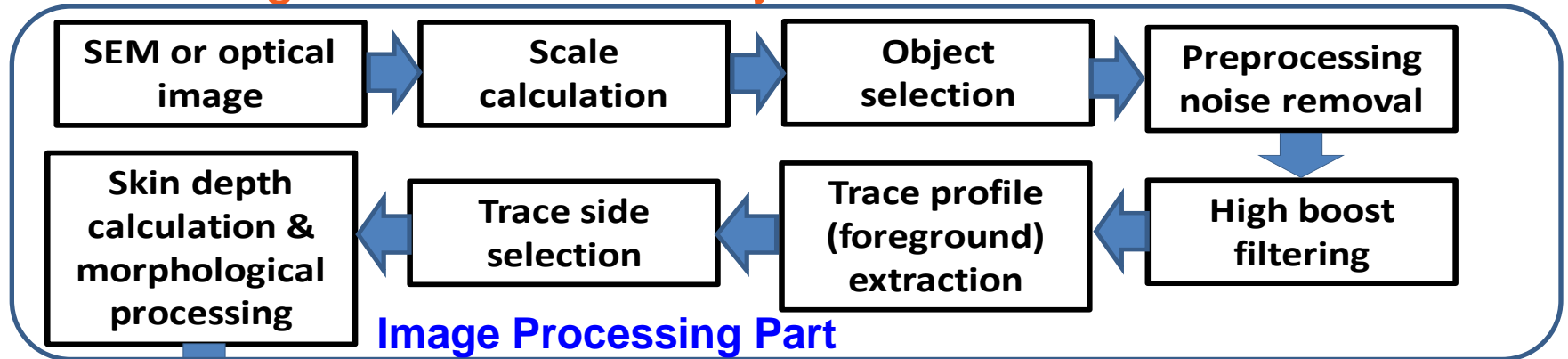
Extracted Dk and Df: $Dk = \epsilon'_r$
 $Df = \tan \delta = \epsilon''_r / \epsilon'_r$

Copper Foil Types



Foils are mostly isotropic in X and Z

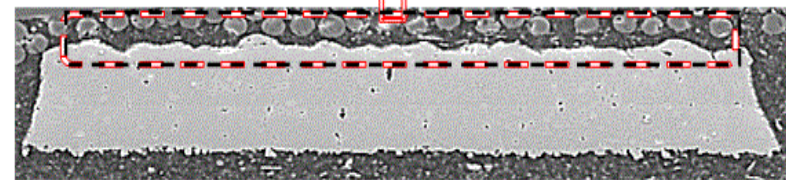
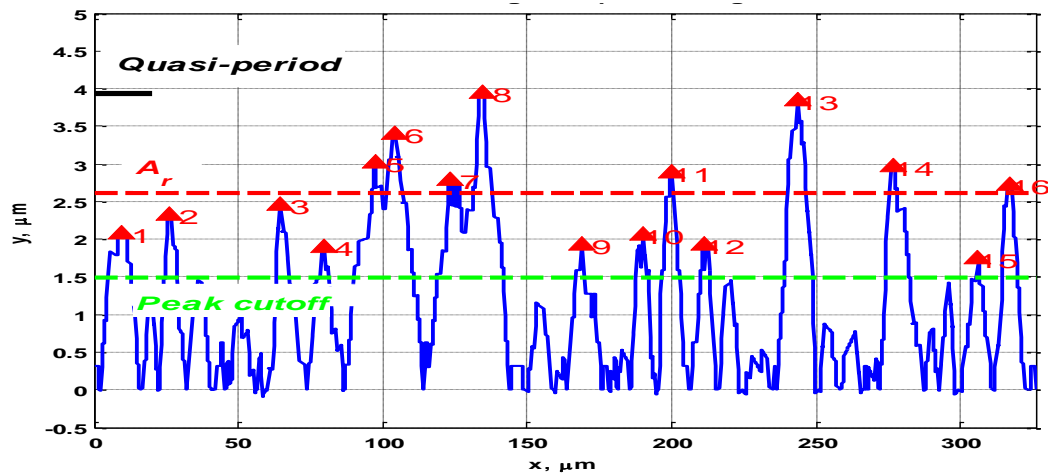
Roughness Profile Analysis & Quantification



A Rakov, S. De et al “Quantification of conductor surface roughness profiles in printed circuit boards”, *IEEE Trans. Electromag. Compat.*, DOI: 10.1109/TEM.C.2014.2375274, 2014.

Computer Vision – Roughness Quantification Part

Roughness Profile Analysis & Quantification



Average peak-to-valley amplitude:
$$A_r = \frac{\sum_{i=1}^{N_{peak}} |y_{i, peak}|}{N_{peak}} + \frac{\sum_{i=1}^{N_{valley}} |y_{i, valley}|}{N_{valley}}$$

Roughness quasi-period:
$$\Lambda = \frac{L \times N_{valley} + L \times N_{peak}}{2 \times N_{valley} \times N_{peak}}$$

Roughness factor:
$$QR = \left(\frac{A_r}{\Lambda} \right)_{oxide} + \left(\frac{A_r}{\Lambda} \right)_{foil}$$

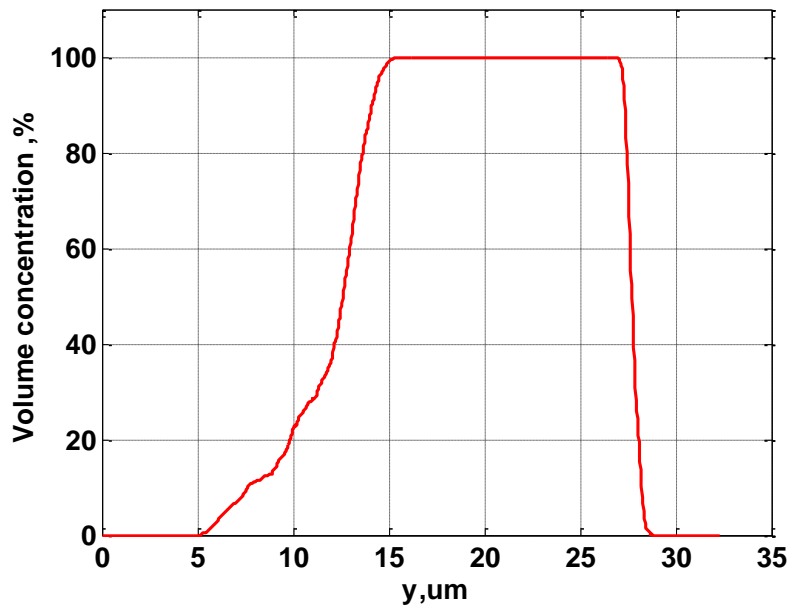
$$QR_1 = \frac{A_{r1}}{\Lambda_{r1}} \Big|_{oxide} \quad \text{and} \quad QR_2 = \frac{A_{r2}}{\Lambda_{r2}} \Big|_{foil}$$

S. De, A.Y. Gafarov, M.Y. Koledintseva, R.J. Stanley, J.L. Drewniak, and S. Hinaga, "Semi-automatic copper foil surface roughness detection from PCB microsection images", *Proc. Int. IEEE Symp. Electromag. Compat.*, Pittsburgh, PA, Aug. 5-10, 2012, pp. 132-137.

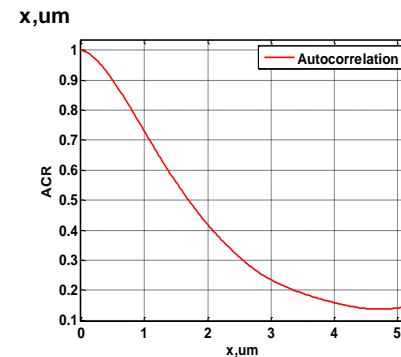
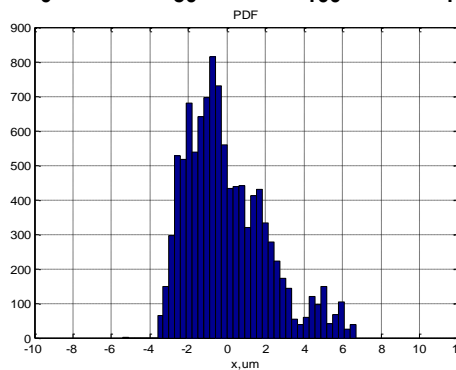
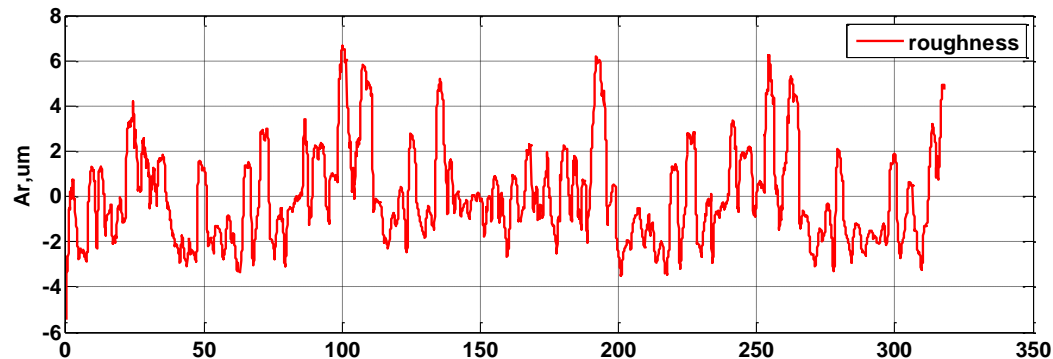
Metallic Inclusions Concentration Variation with Height



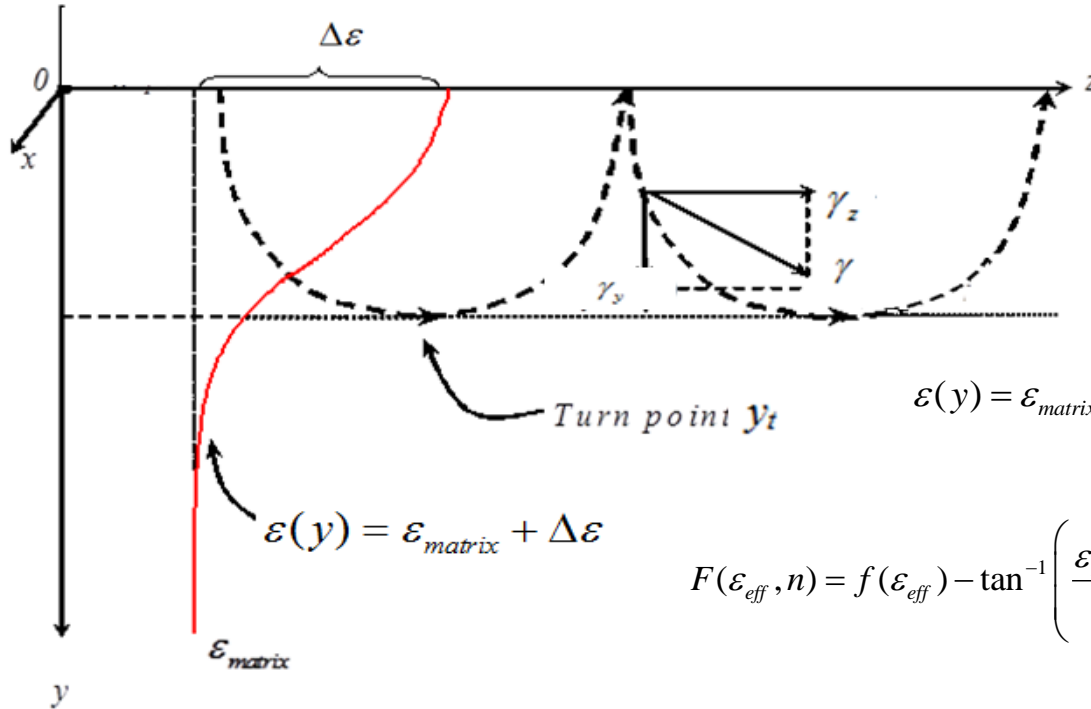
STD Foil, "foil" side



$$v_f(y) = \exp(-\eta y)$$



Basis for Analytical Model Development



$$f(\epsilon_{eff}) = k_0 \int_0^{y_t} \sqrt{\epsilon(y) - \epsilon_{eff}} dy$$

$$\epsilon(y) = \epsilon_{matrix} \left[1 + v_f(y) \frac{\epsilon_{incl} - \epsilon_{matrix}}{\epsilon_{matrix} + (1 - v_f(y)) N_y (\epsilon_{incl} - \epsilon_{matrix})} \right]$$

$$F(\epsilon_{eff}, n) = f(\epsilon_{eff}) - \tan^{-1} \left(\frac{\epsilon_{matrix} + \Delta\epsilon}{\epsilon_{metal}} \cdot \frac{\sqrt{\epsilon_{eff} - \epsilon_{metal}}}{\sqrt{(\epsilon_{matrix} + \Delta\epsilon) - \epsilon_{eff}}} \right) - \pi(n-1) - \frac{\pi}{4} = 0$$

D. Marcuse, *Theory of Dielectric Optical Waveguides* (Optics and Photonics Series), Academic Press, 1991, Chapter 2.

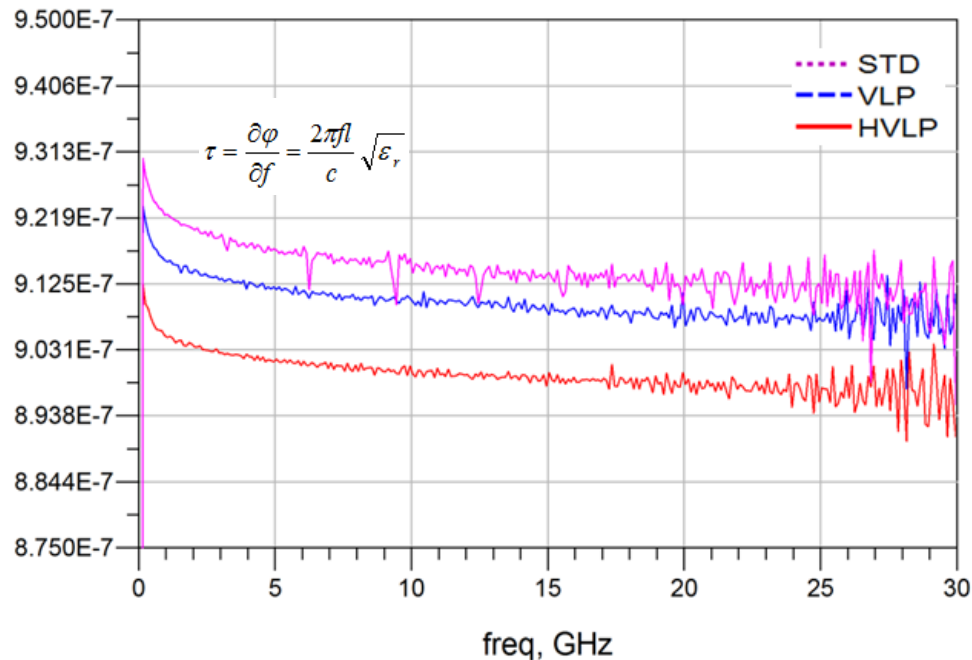
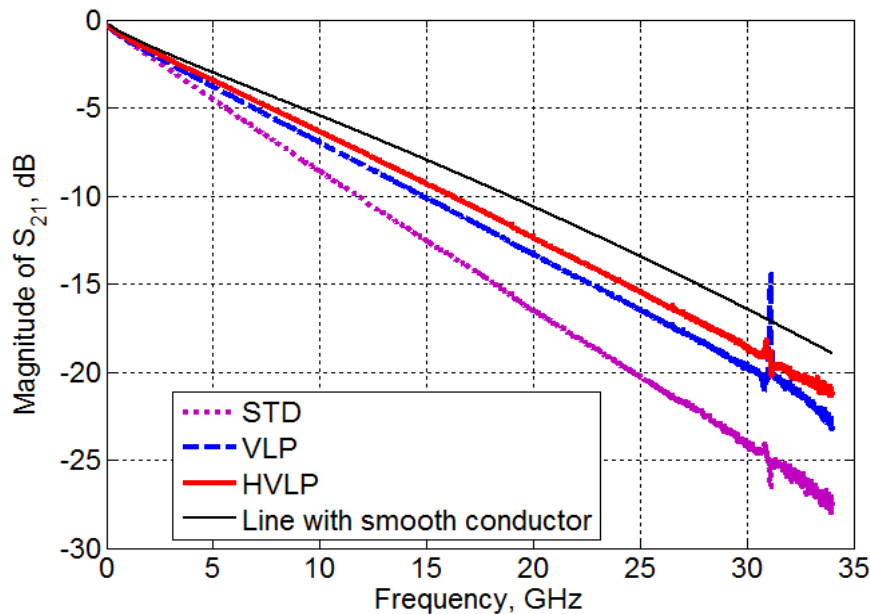
$$\epsilon_{incl} \approx -j \frac{\sigma_{incl}}{\omega \epsilon_0}$$

$$N_y = \frac{1}{a^2} \ln(a)$$

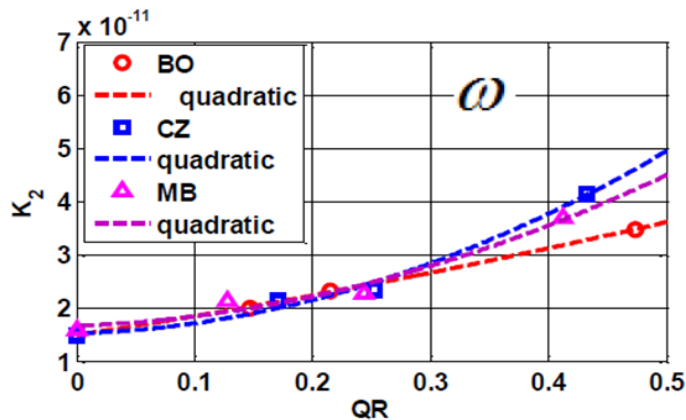
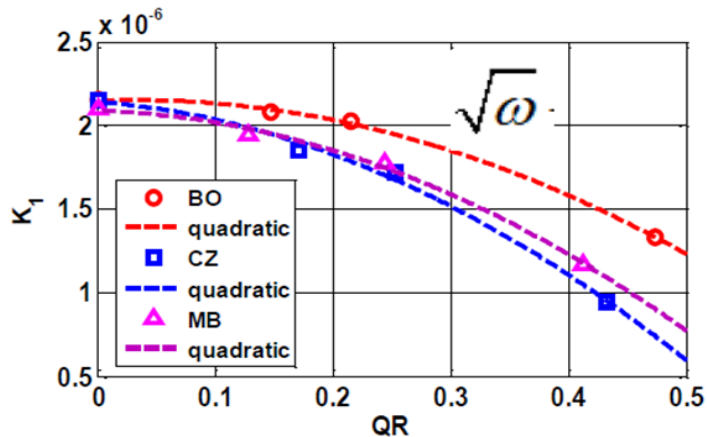
Geometrical Data of Test Vehicles

		w_1 μm	w_2 μm	t μm	P μm	h_1 μm	h_2 μm	A_{r1} μm	A_{r2} μm	Λ_1 μm	Λ_2 μm	QR_1	QR_2	ΣQR
Group "BO"	STD	337.9	343.2	16.44	712.8	308.0	286.0	0.85	6.20	25.0	14.2	0.034	0.44	0.474
	VLP	364.3	368.5	16.8	769	308.0	286.4	0.87	2.38	24.7	13	0.035	0.18	0.215
	HVLP	329.3	331.3	15.3	691.7	303.0	292.0	1.25	1.13	14.3	19.2	0.087	0.06	0.147
Group "CZ"	STD	326.2	338.2	15.9	885.7	289.8	282.5	1.47	6.19	20.6	17.3	0.073	0.359	0.432
	VLP	328.0	333.4	15.0	735.9	312.4	284.1	1.33	2.83	20.4	15.2	0.056	0.187	0.252
	HVLP	323.7	322.2	14.9	690.7	311.5	296.3	1.81	1.26	14.7	26.7	0.124	0.047	0.171
Group "MB"	STD	328.1	334.2	15.7	864.6	308.0	286.0	1.32	6.13	25.3	17.2	0.052	0.359	0.412
	VLP	329.5	331.2	15.4	735.8	313.7	282.5	1.04	3.01	19.9	15.8	0.053	0.191	0.244
	HVLP	340.0	342.4	15.0	706.6	311.0	297.3	1.30	1.04	16.9	20.7	0.077	0.050	0.128

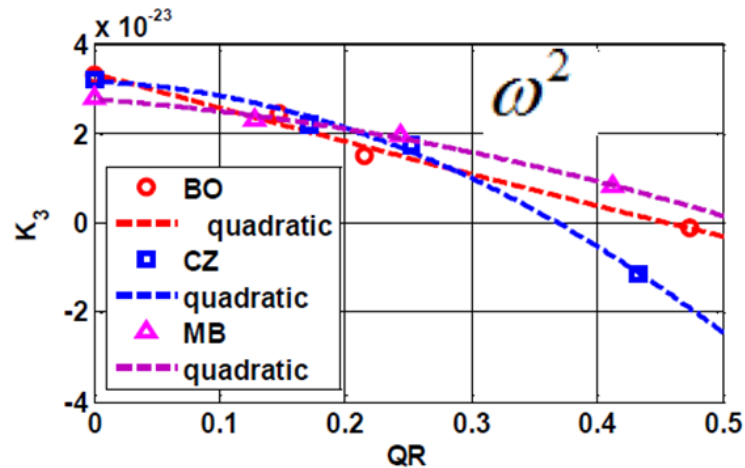
Raw Measured Insertion Loss and Group Delay (“BO” Group)



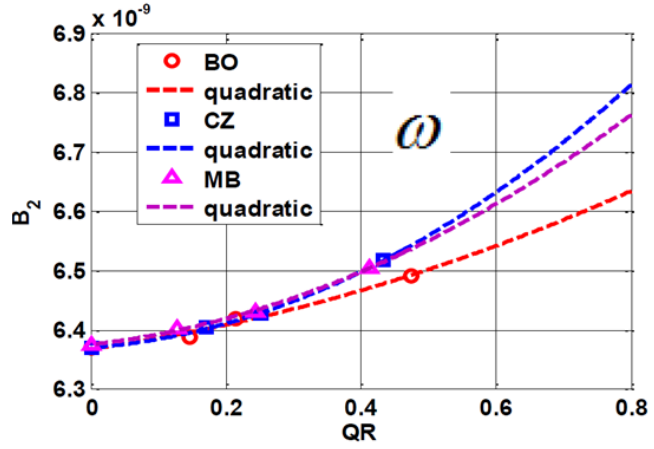
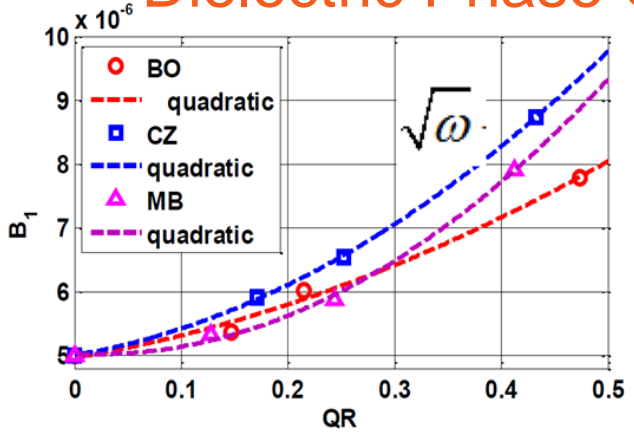
Dielectric Loss Extraction Using DERM



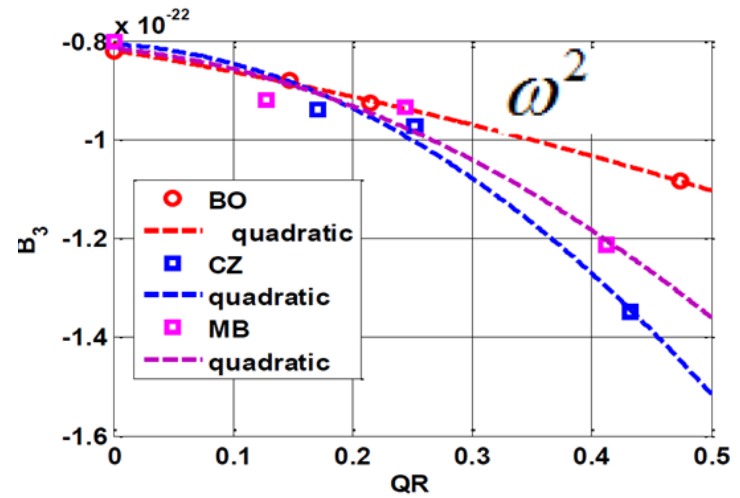
$$\alpha_T = K_1\sqrt{\omega} + K_2\omega + K_3\omega^2$$



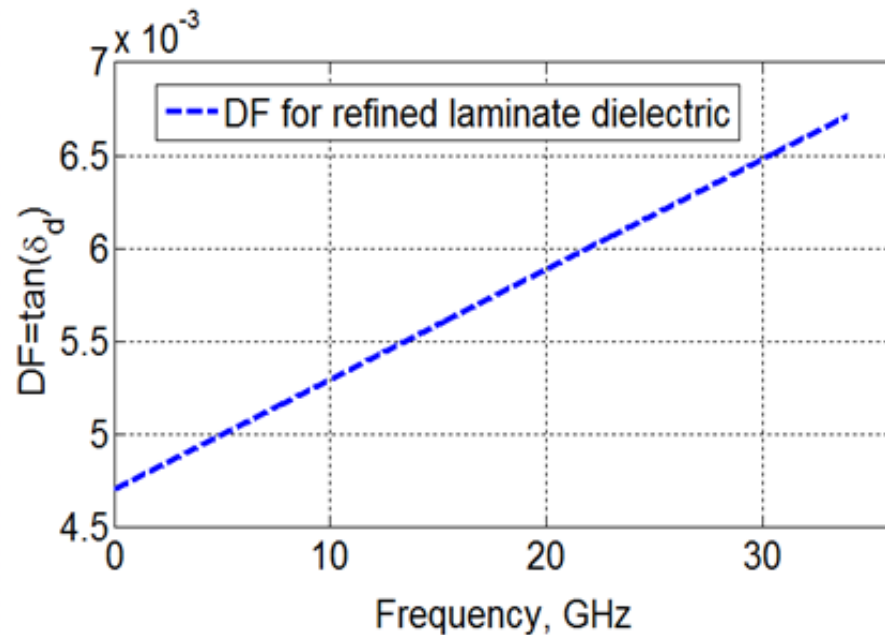
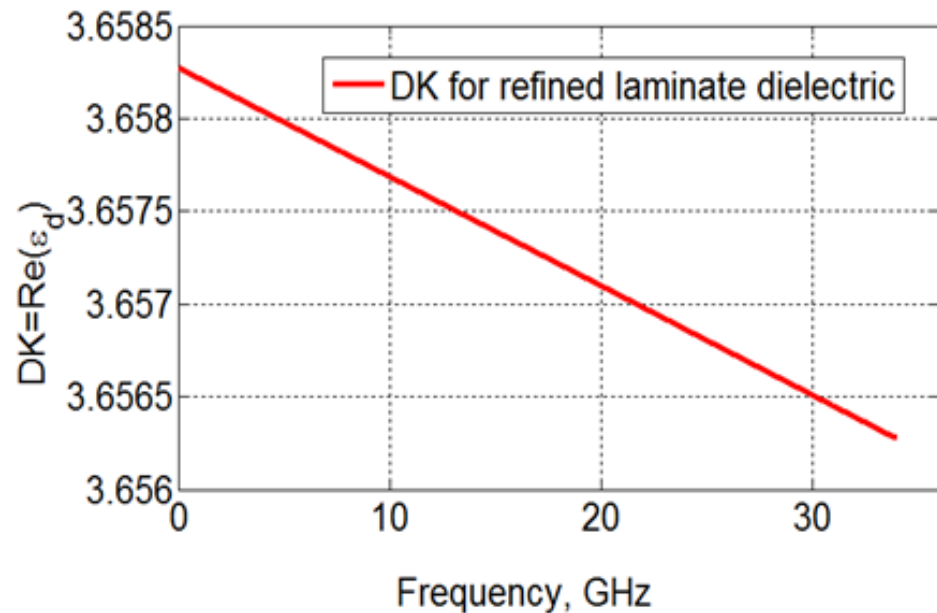
Dielectric Phase Constant Extraction Using DERM



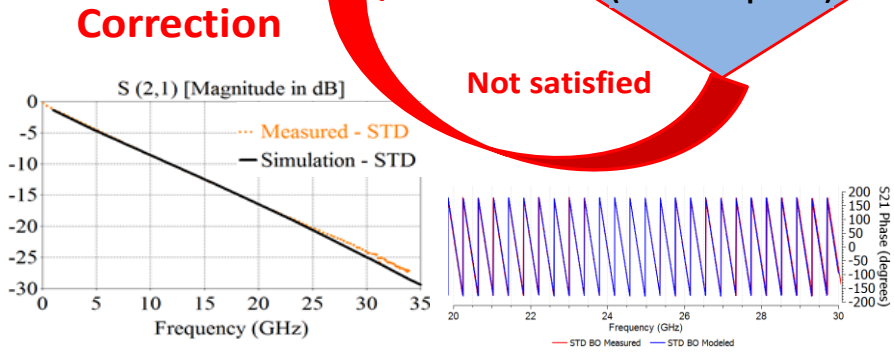
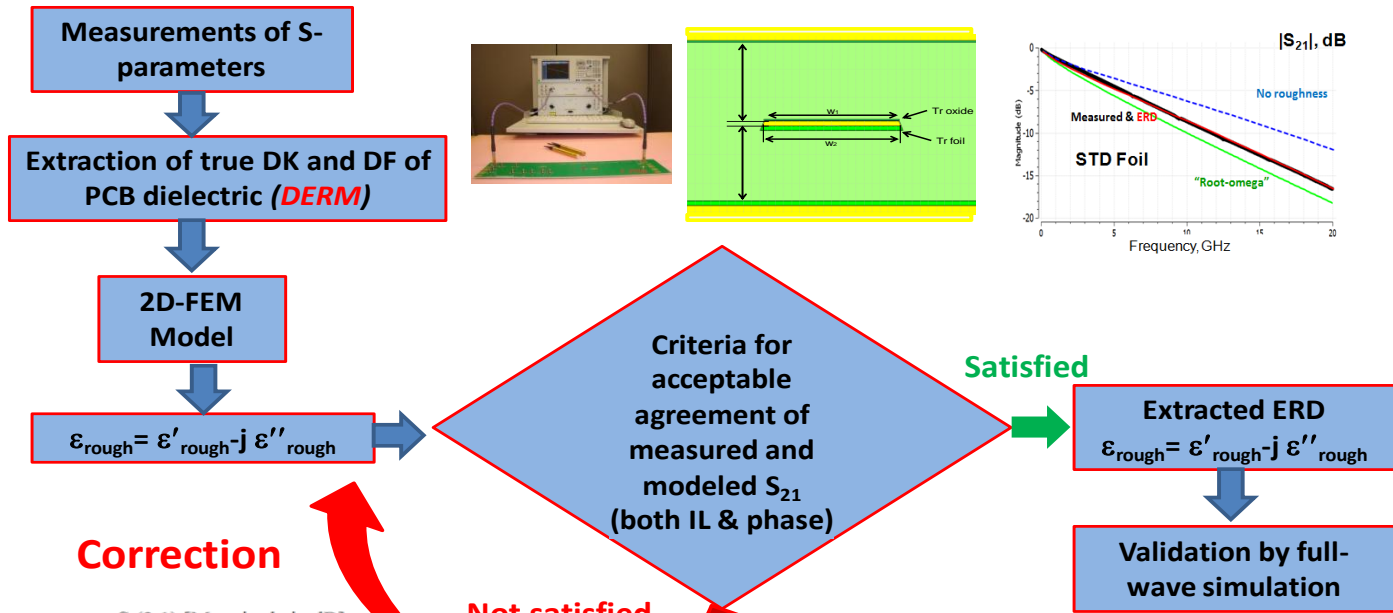
$$\beta_T = B_1 \sqrt{\omega} + B_2 \omega + B_3 \omega^2$$



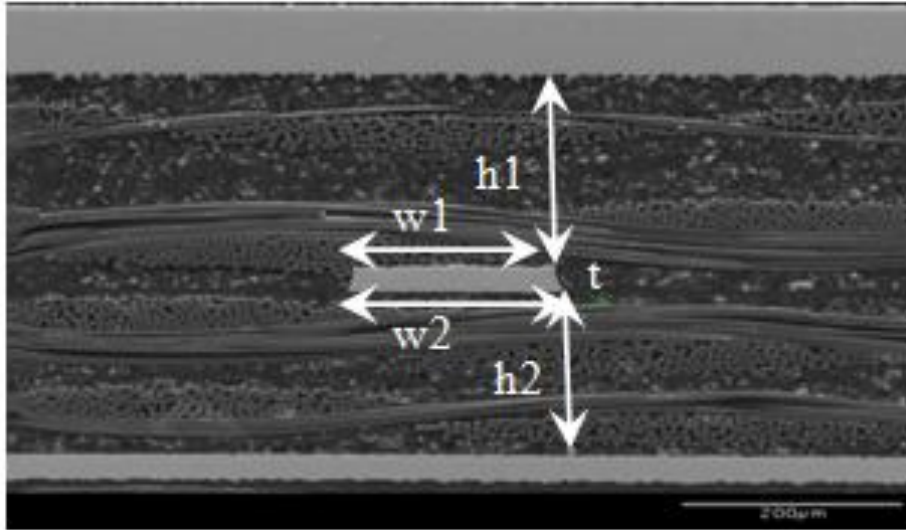
Refined from Conductor Roughness DK & DF of PCB Laminate Dielectric (Megtron 6)



ERD Dielectric Extraction Procedure



2D-FEM Model to Extract ERD Parameters



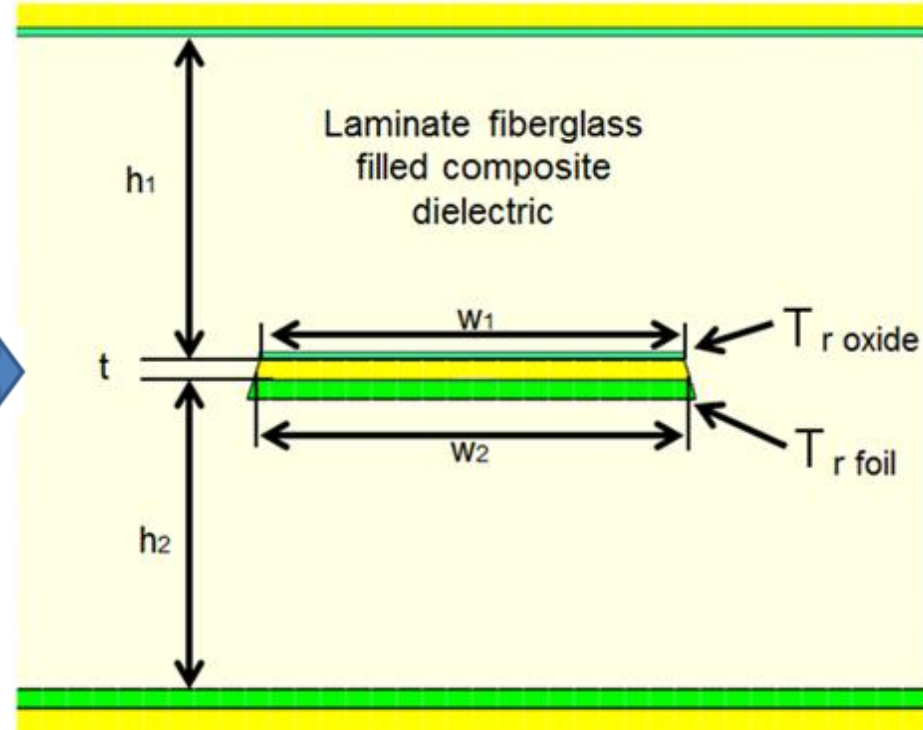
Copper foil conductors



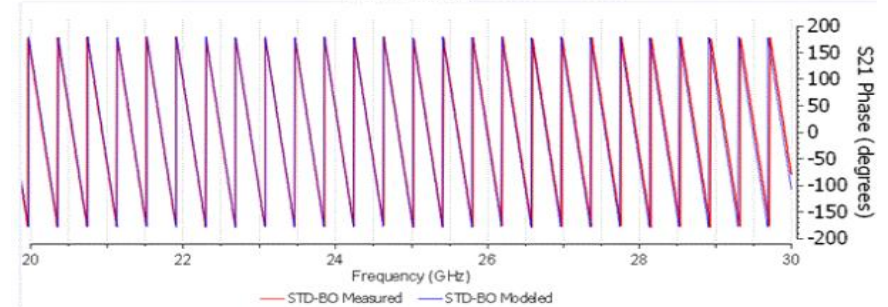
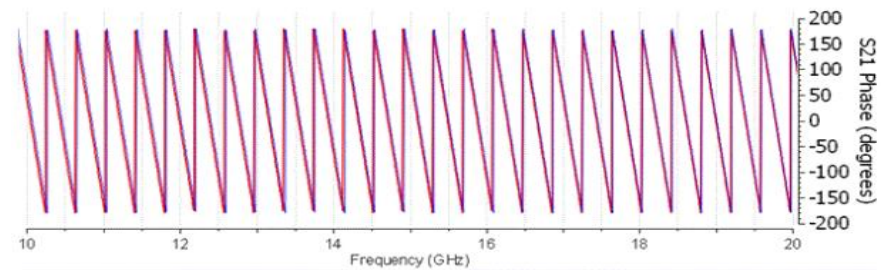
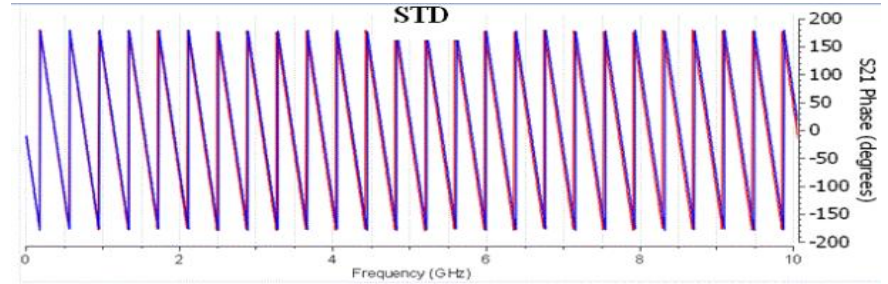
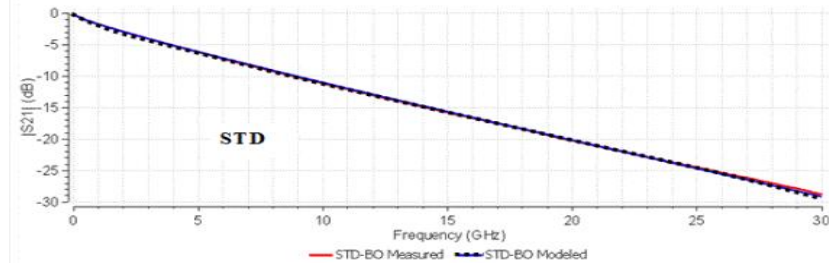
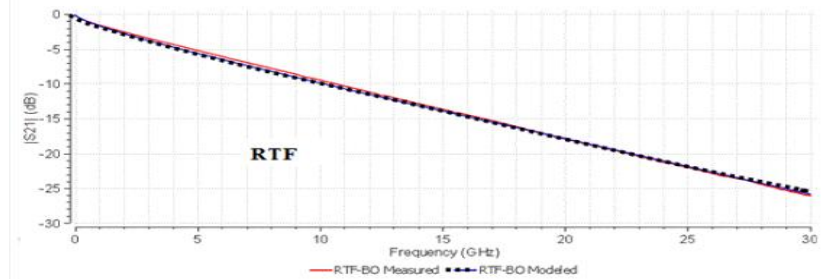
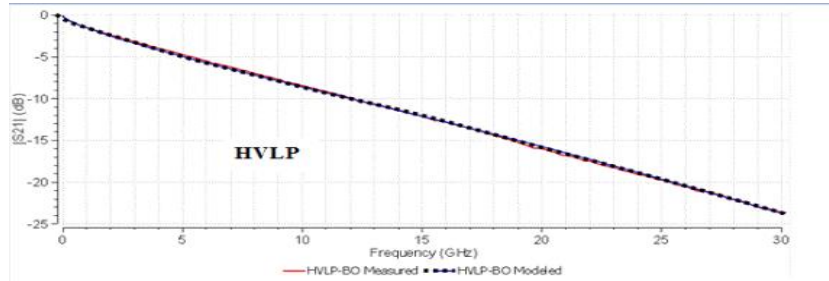
Effective 'roughness dielectric'



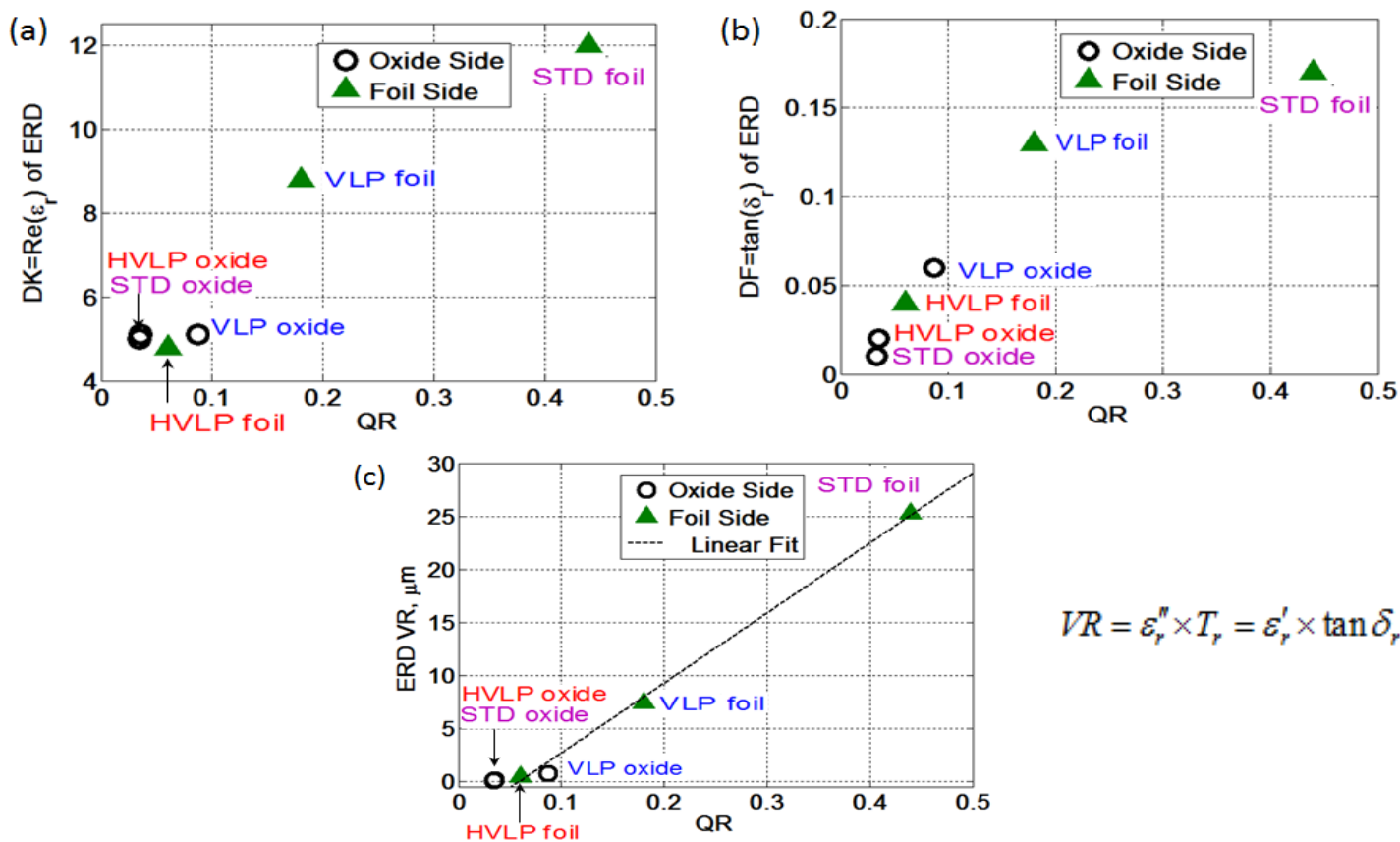
Laminate dielectric



Modeled & Measured S-parameters for ERD Extraction



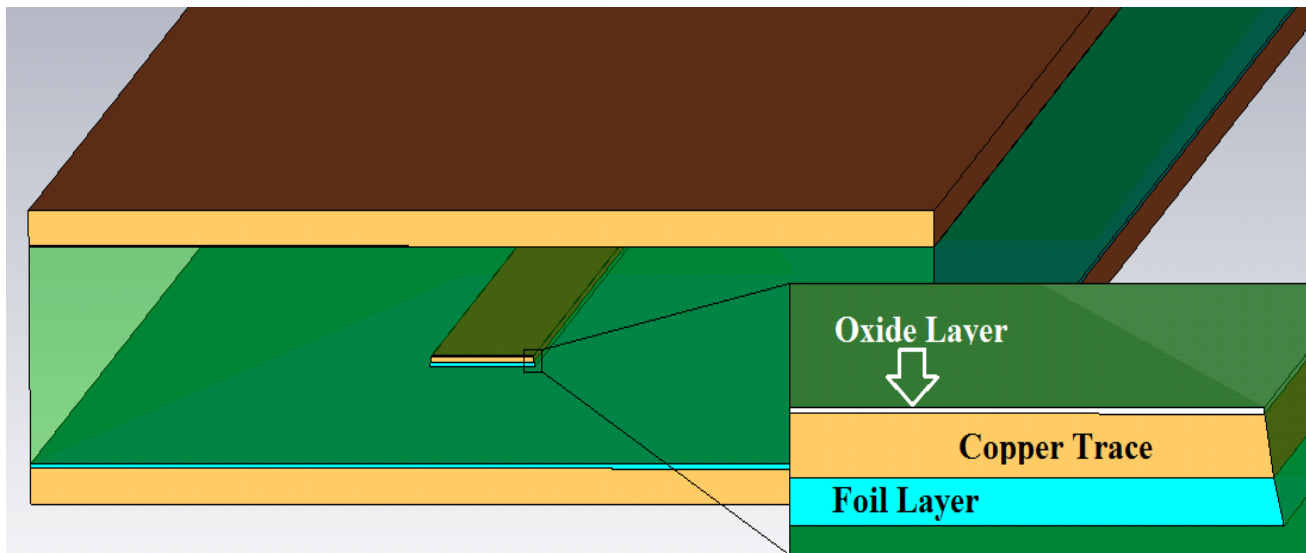
Scatter Plots for DK, DF, and VR of Roughness Layers



$$VR = \epsilon_r'' \times T_r = \epsilon_r' \times \tan \delta_r \times T_r$$

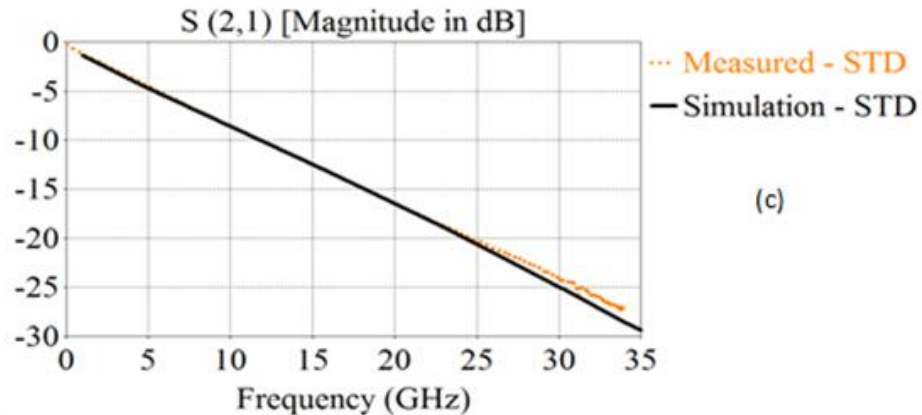
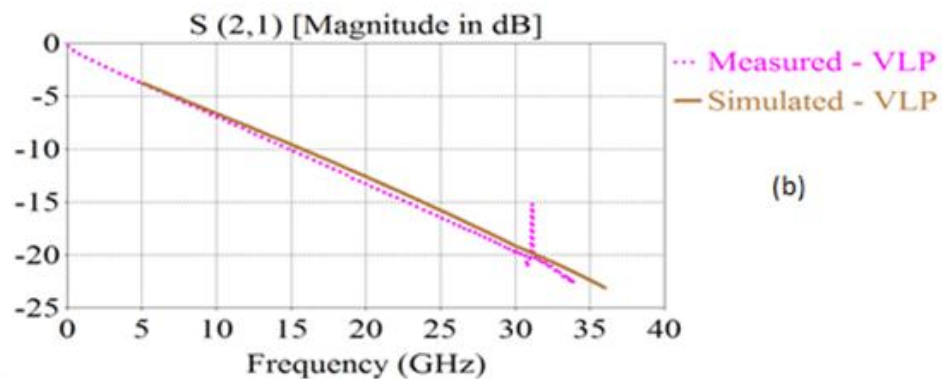
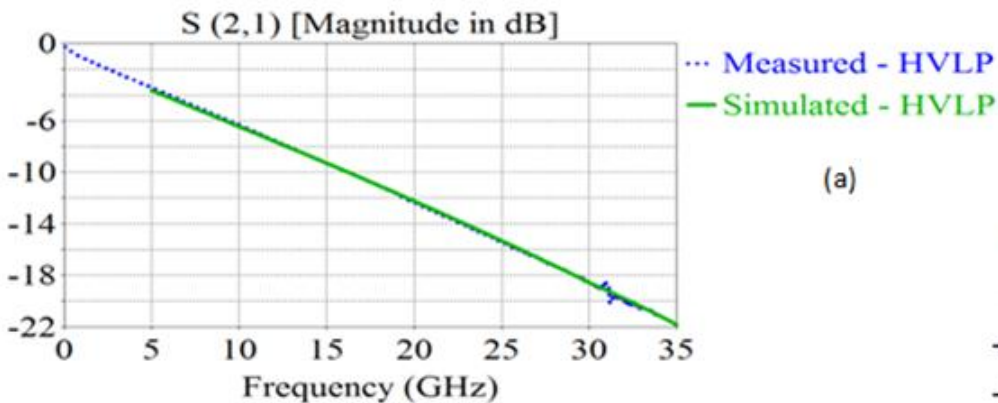
Validation by Full-wave 3D Numerical Modeling

CST Studio Suite 3D (Full-wave FD MoM) model is used for validation of the extracted ERD data

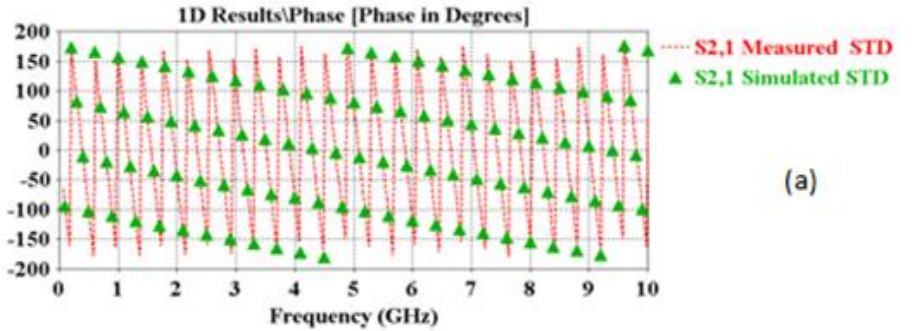


T. Vincent, M. Koledintseva, A. Ciccomancini, and S. Hinaga, "Effective roughness dielectric in a PCB: measurement and full-wave simulation verification", *IEEE Symp. Electromag. Compat.*, Raleigh, NC, 3-8 Aug. 2014, pp. 798-802.

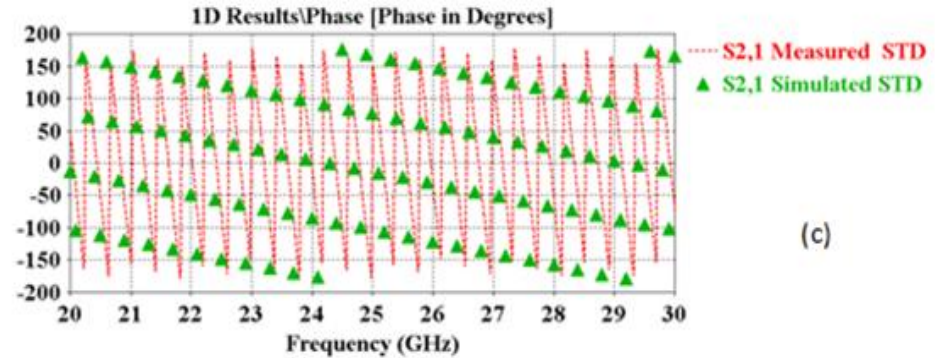
Insertion Loss Agreement Validation



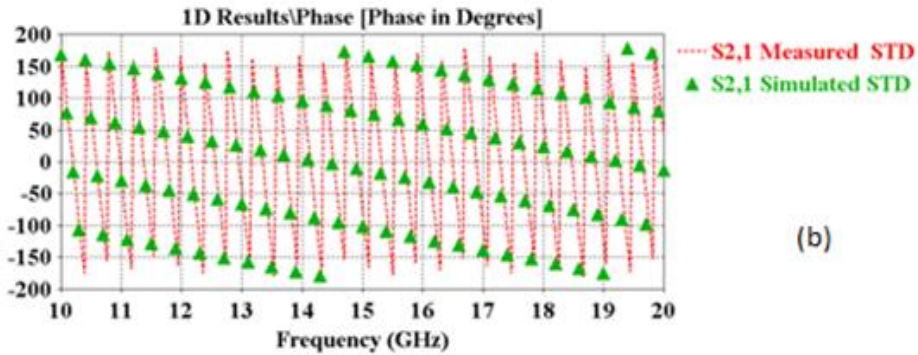
Phase Agreement Validation



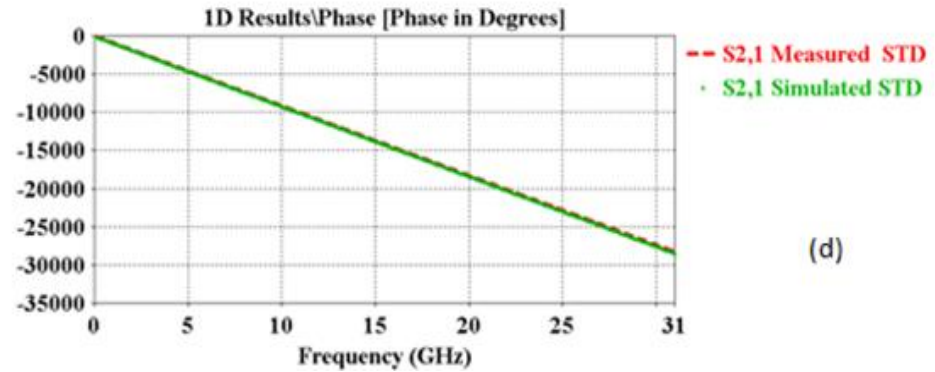
(a)



(c)

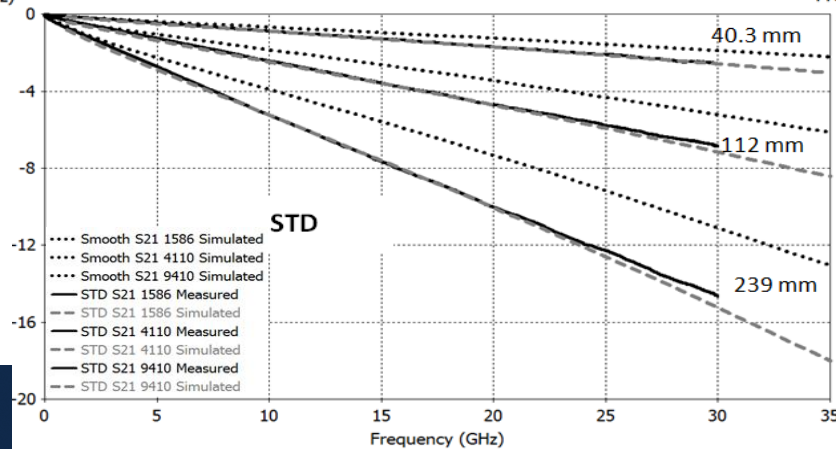
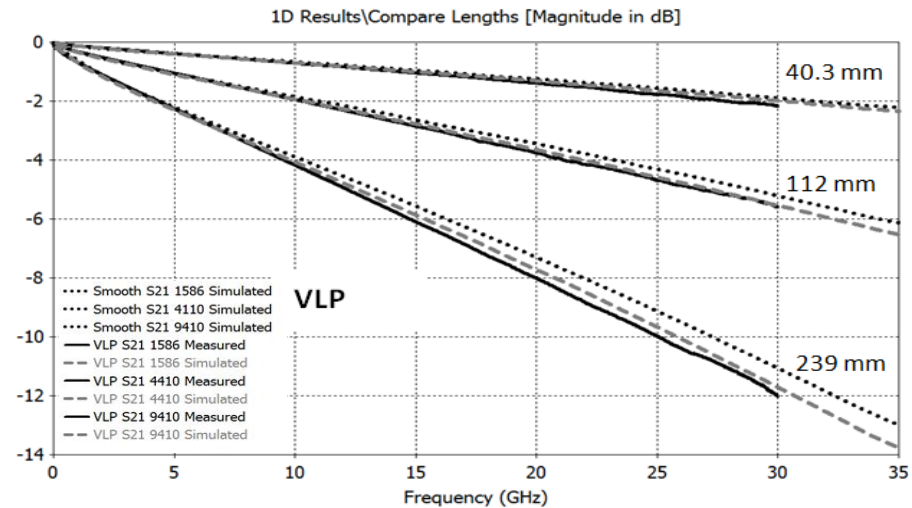
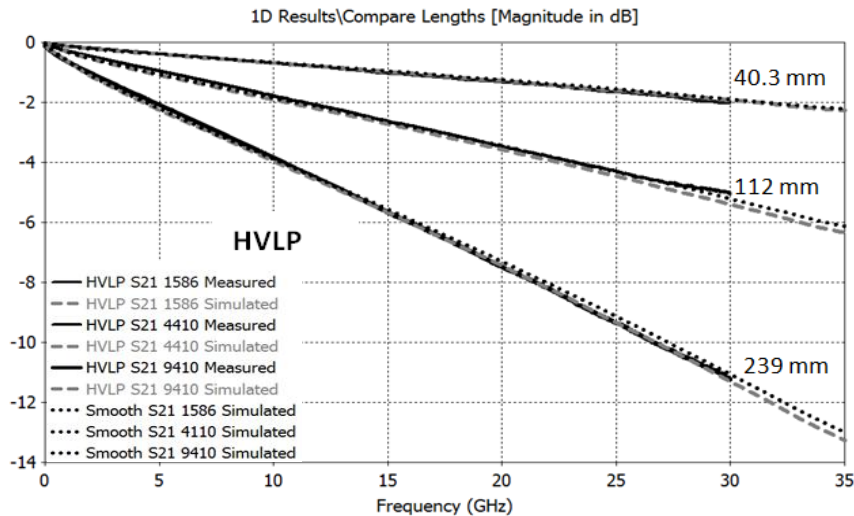


(b)

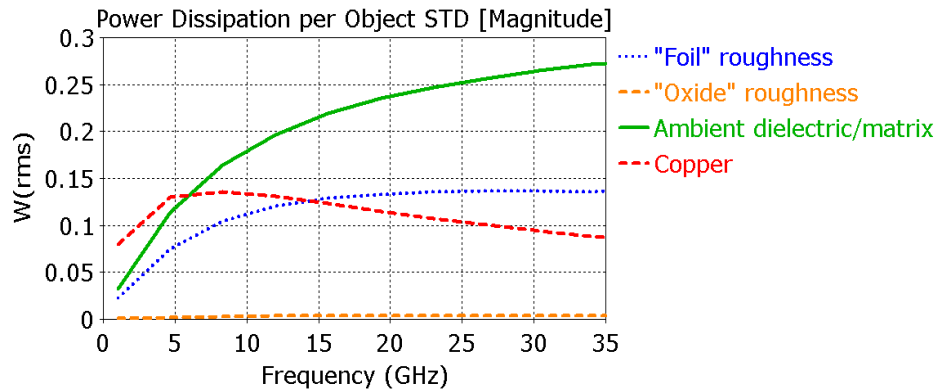
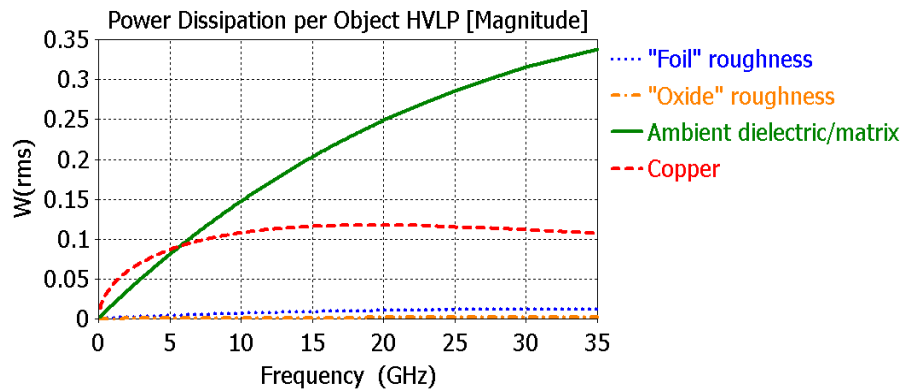
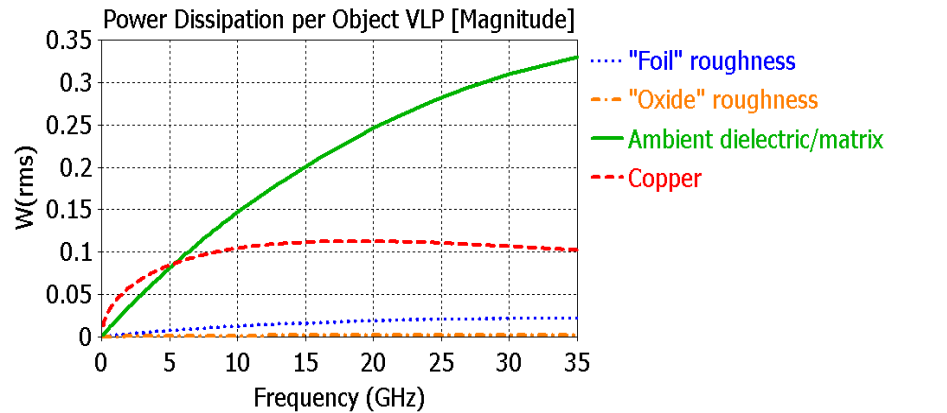


(d)

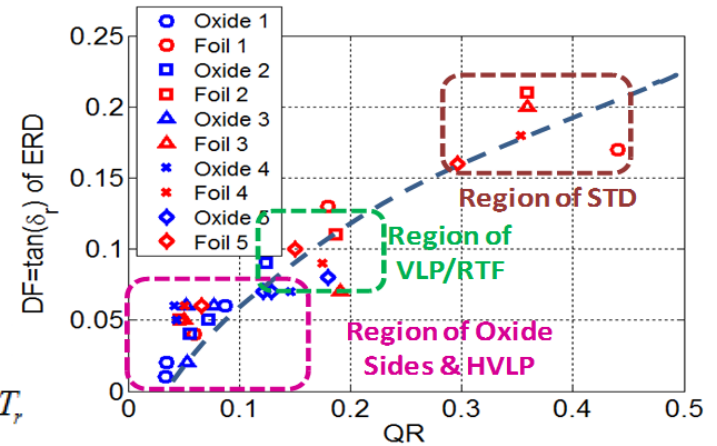
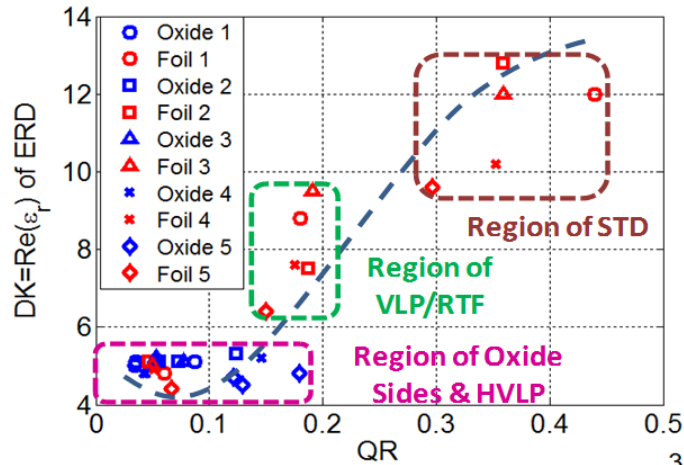
Validation for Different Line Lengths



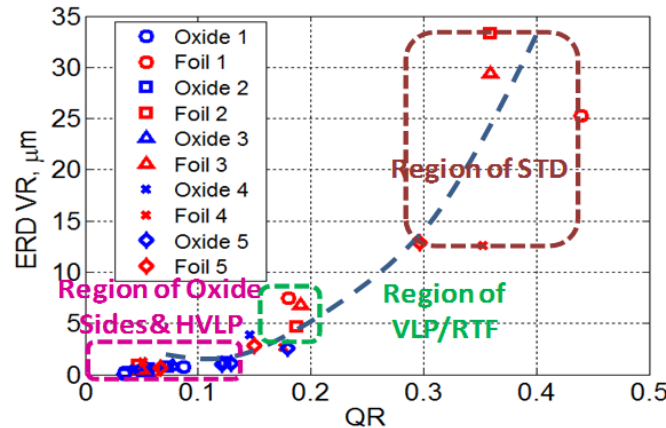
Power Dissipation Analysis



Design Curves for Effective Roughness Dielectric Parameters



$$VR = \epsilon_r'' \times T_r = \epsilon_r' \times \tan \delta_r \times T_r$$



Sets 1,2,3 – 13mil traces
Sets 4, 5 – 7 mil traces

Conclusions

- To model PCB designs, it is important to know the geometry of a transmission line, the correct roughness-independent DK and DF data of the laminate dielectric substrate used in this line, and a type of a foil.
- The parameters of a laminate dielectric substrate used in the modeling are determined using differential extrapolation roughness measurement technique (DERM).
- The effective roughness dielectric (ERD) approach to represent foil surface roughness in a PCB is validated using 3D full-wave simulations.
- “Design curves” (nomograms) to model roughness layers have been developed based on the collected data points from testing multiple test vehicles with different foils.
- If an electronics designer does not have possibilities of foil roughness inspection, *e.g.*, using an SEM or optical microscopy cross-sectional analysis, the recommended “design curves”, or pre-computed values of complex permittivity and thickness of “roughness dielectrics” for the known types of foils may still be used in the numerical modeling.

Thank you!

