

# Accuracy-Improved Coupling Capacitance Model for Through-Silicon Via (TSV) Arrays Using Dimensional Analysis

Tarek Ramadan <sup>1,3</sup>, Student Member, IEEE, Eslam Yahya <sup>2,4</sup>, Member, IEEE, Mohamed Dessouky <sup>1,3</sup>, Member, IEEE and Yehea Ismail <sup>2</sup>, Fellow, IEEE

<sup>1</sup> Mentor Graphics Corporation

<sup>2</sup>Center of Nanoelectronics and Devices (CND), American University in Cairo, Zewail University for Science and Technology (ZC)

<sup>3</sup> Faculty of Engineering, Ain Shams University, Cairo, Egypt

<sup>4</sup> Faculty of Engineering, Benha University, Benha, Egypt

**Abstract**—In this paper, we show that using the relation between the inductance matrix and the capacitance matrix in a homogeneous medium to extract the coupling capacitance in a through silicon via (TSV) array is inaccurate. This is because this relation assumes a lossless, homogeneous surrounding medium. We show that this model can cause an error up to 70% in coupling capacitance compared to Q3D extractor simulations. Instead of using high accuracy, time consuming numerical electromagnetic techniques, we suggest a correction methodology for the inverse inductance model so that it can account for the non-homogeneous nature of the TSVs surrounding medium and the lossy nature of the silicon substrate. Dimensional analysis is used to understand the correction function dependencies on TSV dimensions and to reduce the number of independent variables needed for regression analysis. Once the independent variables are reduced, multiple regression techniques are used to estimate the correction function for TSV arrays. Q3D extractor simulations are used to show that the corrected model reduces the coupling capacitance error significantly. Then, the correction function behavior vs. frequency is discussed.

**Index Terms**—TSV, 3D-IC, 2.5D-IC, SiP.

## I. INTRODUCTION

Three dimensional integrated circuits (3D-ICs) is an emerging technology that can enable the "More than Moore" concept. IC designers can go beyond the transistor scaling limit in System on Chip (SoC) by stacking multiple dies in the vertical direction (3D-IC). Beside improving the form factor, 3D-IC technology allows the integration of dies that were manufactured using different fabrication process nodes and/or different foundries. A stepping stone to 3D-IC is 2.5D-IC where multiple dies are placed side by side on an interposer (already in production by FPGA manufacturers). Memory manufactures are already leveraging 3D-IC to create hybrid memory cubes (HMCs).

Through-Silicon Vias (TSVs) are needed as the vertical interconnect between the stacked dies. A TSV in the simplest form is a copper/tungsten cylinder coated with a thin layer of silicon dioxide (also known as oxide liner) to enable electrical isolation from/to the surrounding medium. TSVs are usually

fabricated in the form of arrays to connect high density I/Os between chips.

In order to be able to estimate the 3D-IC circuits performance, an accurate and fast estimation of TSV parasitic elements (resistance, inductance and capacitance) in a TSV array is needed. [1], [2] and [3] use the relation between the inductance matrix and the capacitance matrix in a homogeneous medium for capacitance extraction:

$$[L][C] = \mu\epsilon_{si} \quad (1)$$

Where [L] is the inductance matrix per unit length, [C] is the capacitance matrix per unit length,  $\mu$  is the permeability of free space and  $\epsilon_{si}$  is the permittivity of silicon ( $11.9\epsilon_0$ ). Mutual and self inductance of TSVs can be estimated using the well-known models in [4]. Then, the capacitance matrix will be the only unknown in (1). However, this approach is inaccurate for coupling capacitance modeling as the model assumes a lossless, homogeneous surrounding medium. While in case of TSV arrays, the surrounding medium is lossy and non-homogeneous. In this paper, an improved model that can show better accuracy for the coupling capacitance extraction is presented.

## II. CURRENT COUPLING CAPACITANCE MODEL

Fig. 1 shows the current coupling capacitance model between two TSVs. TSV parameters are  $r$  (TSV radius),  $h$  (TSV height),  $p$  (TSVs pitch) and  $t_{ox}$  (oxide liner thickness). [1], [2] and [3] suggest the following model to extract the coupling capacitance of two TSVs as shown in Fig. 1:

$$C_{ox} = \frac{\pi\epsilon_o\epsilon_{ox}h}{\ln\left(\frac{r+t_{ox}}{r}\right)} \quad (2)$$

$$[C_{si}] = \mu\epsilon_o\epsilon_{si} [L]^{-1} h^2 \quad (3)$$

Then the total coupling capacitance between the two TSVs is:

$$C_{tot} = \frac{0.5C_{ox}C_{si}}{0.5C_{ox} + C_{si}} \quad (4)$$

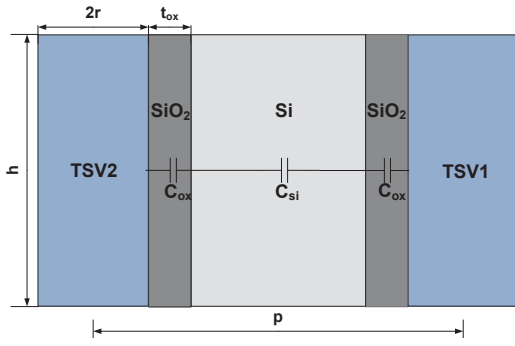


Fig. 1. Current Equivalent Model of coupling capacitance between TSVs

Where  $C_{ox}$  is the capacitance due to the oxide liner and  $C_{si}$  is the capacitance due to the silicon substrate coupling. According to [5], (3) assumes lossless, homogeneous surrounding medium. This is not the case for TSV arrays as the silicon substrate has a non-zero conductivity ( $\sigma_{si}$ ) and the interface between silicon and silicon dioxide causes the surrounding medium to be non-homogeneous. For the previous reasons, it is expected that the coupling capacitance extraction using (3) will be inaccurate. The previous theoretical assumption is discussed and validated using Q3D extractor simulations in [6]. The inverse inductance model extraction results are compared to Q3D extraction results as the reference. The percentage error is calculated using:

$$Error = \frac{C_{model} - C_{Q3D}}{C_{Q3D}} \times 100 \quad (5)$$

In [6], we show that the percentage error calculated using (5) can reach -70%, which means that the current model in (3) underestimates the coupling capacitance value.

In order to provide correction for (3), the increase in coupling capacitance can be modeled as a capacitor in parallel:

$$[C_{si}] = \mu\epsilon_o\epsilon_{si}[L]^{-1}h^2 + [C_{correction}] \quad (6)$$

In the next section, we will show how to estimate  $C_{correction}$  dependency on TSV dimensions using the dimensional analysis technique.

### III. DIMENSIONAL ANALYSIS

Dimensional analysis is a powerful technique that can be used to reduce the number of independent variables required for regression analysis. Authors in [7] used dimensional analysis to derive closed form expressions for resistance, inductance and capacitance of a single TSV. The same approach can be used to find  $C_{correction}$  in case of TSV arrays. The steps will be as follows:

- 1) List the different independent variables and their units:  
At a single operating frequency = 1GHz and silicon substrate conductivity ( $\sigma_{si}$ ) = 10m/S,  $C_{correction}$  is a

TABLE I  
INITIAL DIMENSIONAL MATRIX

	$C$	$\epsilon$	$h$	$r$	$t_{ox}$	$p$
$\Omega$	-1	-1	0	0	0	0
$m$	0	-1	1	1	1	1
$s$	1	1	0	0	0	0

TABLE II  
REARRANGED DIMENSIONAL MATRIX

	$C$	$r$	$h$	$t_{ox}$	$\epsilon$	$p$
$\Omega$	-1	0	0	0	-1	0
$m$	0	1	1	1	-1	1

TABLE III  
FINAL DIMENSIONAL MATRIX

	$C$	$r$	$h$	$t_{ox}$	$\epsilon$	$p$
$\Omega$	-1	0	0	0	-1	0
$m$	0	1	1	1	-1	1
$\pi_1$	1	0	0	0	-1	-1
$\pi_2$	0	1	0	0	0	-1
$\pi_3$	0	0	1	0	0	-1
$\pi_4$	0	0	0	1	0	-1

function of TSVs dimensions and surrounding medium permittivity.

$$C_{correction}[\Omega^{-1}s] = f(\epsilon[\Omega^{-1}m^{-1}s], h[m], r[m], t_{ox}[m], p[m]) \quad (7)$$

- 2) Construct the dimensional matrix:

The initial matrix is as shown in Table I. Sub-matrix [A] is highlighted in green.

- 3) Simplify [A]:

Some rearrangement and row operations are needed until [A] is non singular. The rearranged matrix is shown in Table II. Sub-matrix [B] is highlighted in yellow.

- 4) Find [C] and [D] then append them to Table II:

$$C = -[A^{-1}.B]^T \quad (8)$$

$$D = I \quad (9)$$

Final matrix is shown in Table III.

- 5) Find  $\pi$  factors using Table III:

$$\pi_1 = \frac{C}{\epsilon p} \quad (10)$$

$$\pi_2 = \frac{r}{p} \quad (11)$$

$$\pi_3 = \frac{h}{p} \quad (12)$$

$$\pi_4 = \frac{t_{ox}}{p} \quad (13)$$

$$\pi_1 = f(\pi_2, \pi_3, \pi_4) \quad (14)$$

Then, substitute by (10), (11), (12) and (13) in (14). This results in:

$$\frac{C}{\epsilon p} = f\left(\frac{h}{p}, \frac{r}{p}, \frac{t_{ox}}{p}\right) \quad (15)$$

It is noticed from (15) that the dimensional analysis reduced the number of independent variables needed for regression analysis from 5 variables ( $\epsilon$ ,  $h$ ,  $r$ ,  $t_{ox}$  and  $p$ ) to 3 variables ( $h/p$ ,  $r/p$  and  $t_{ox}/p$ ).

#### IV. REGRESSION ANALYSIS

Regression analysis is the study of the relationship between one or several predictors (independent variables) and the response (dependent variable). To perform regression analysis on a data set, a regression model is first developed, then the best fit parameters are estimated using the least-square method. In order to find  $C_{correction}$ , we need to perform multiple regression as there are more than one independent variable involved. Q3D extractor is used to generate the data points for TSV arrays when ( $h/p$ ), ( $r/p$ ) and ( $t_{ox}/p$ ) are the independent variables and ( $C/\epsilon p$ ) is the dependent variable. The data points are generated at a single frequency =  $1GHz$  and silicon conductivity ( $\sigma_{si}$ ) =  $10S/m$ . Then, the data points are passed to Matlab for multiple, non linear regression. The resulting  $C_{correction}$  function is:

$$C_{correction} = \epsilon_{si} p [10.3426e^{r/p} - 10.3606e^{t_{ox}/p} - 0.0009e^{h/p}] \quad (16)$$

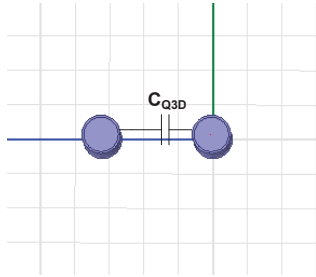


Fig. 2. 2 TSVs Structure in Q3D

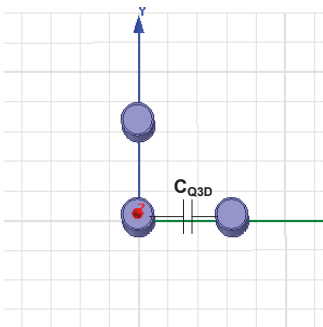


Fig. 3. 3 TSVs Structure in Q3D

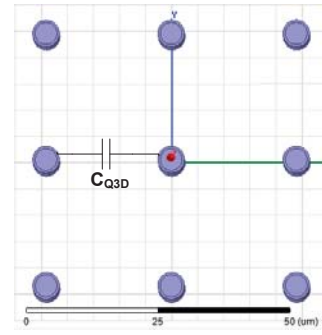


Fig. 4. 3x3 TSV Array in Q3D

(16) is valid for TSV aspect ratio ( $h/2r$ )  $\simeq 10$ . This is a typical industrial value that allows reliable fabrication of TSVs. The exponential dependence of  $C_{correction}$  on  $h/p$ ,  $t_{ox}/p$  and  $r/p$  in (16) is expected from theoretical analysis. This is because  $C_{correction}$  fits the model of the capacitance between two cylindrical, parallel wires as in [8].

To validate the correction approach, different TSVs configurations are used. The correction function was used for 2 TSVs structure as shown in Fig. 2, 3 TSVs structure as shown in Fig. 3 and a 3x3 regular TSV array structure as shown in Fig. 4. It can be noticed from the figures that we consider the coupling capacitance between the neighboring TSVs only as they have the most significant coupling capacitance values.

TABLE IV  
COUPLING CAPACITANCE ERROR REDUCTION IN CASE OF 2 TSVs  
STRUCTURE IN FIG. 2

$r$ ( $\mu m$ )	$t_{ox}$ ( $\mu m$ )	$h$ ( $\mu m$ )	$p$ ( $\mu m$ )	Error before correction (%)	Error after correction (%)
4	0.83	80	17	-31	-7
2.1	0.46	40	24	-43.2	-1.6
1.6	0.37	32	16	-38.6	-0.4
3.6	0.84	72	24	-33.1	3.5

TABLE V  
COUPLING CAPACITANCE ERROR REDUCTION IN CASE OF 3 TSVs  
STRUCTURE IN FIG. 3

$r$ ( $\mu m$ )	$t_{ox}$ ( $\mu m$ )	$h$ ( $\mu m$ )	$p$ ( $\mu m$ )	Error before correction (%)	Error after correction (%)
4	0.83	80	17	-35.9	-8.1
2.1	0.46	40	24	-45.8	-1.2
1.6	0.37	32	16	-41.9	-0.6
3.6	0.84	72	24	-38.7	-2

Tables IV, V and VI show the coupling capacitance error across different TSV dimensions in case of 2 TSVs structure, 3 TSVs structure and 3x3 TSV array structure respectively. The coupling capacitance before correction is estimated using the uncorrected model in (3). The coupling capacitance after correction is estimated using the corrected model in (6) and

TABLE VI  
COUPLING CAPACITANCE ERROR REDUCTION IN CASE OF 3X3 TSV  
ARRAY STRUCTURE IN FIG.4

$r$ ( $\mu\text{m}$ )	$t_{\text{ox}}$ ( $\mu\text{m}$ )	$h$ ( $\mu\text{m}$ )	$p$ ( $\mu\text{m}$ )	Error before correction (%)	Error after correction (%)
4	0.83	80	17	-34.4	0.9
2.1	0.46	40	24	-43.3	3
1.6	0.37	32	16	-56.4	-4
3.6	0.84	72	24	-41.6	3.5

(16). In all cases, the percentage error in coupling capacitance is calculated using (5) with having Q3D extractor results as the reference coupling capacitance values. It can be noticed from the tables that the percentage error in coupling capacitance is reduced after correction.

#### V. $C_{\text{CORRECTION}}$ VS. FREQUENCY

Silicon substrate behavior vs. frequency has been studied in [9]. Silicon substrate is usually modeled as a conductance ( $G$ ) representing the conductive nature of the substrate and a capacitance ( $C$ ) representing the dielectric nature of the substrate. Based on the operating frequency, one nature may dominate:

- 1) At low frequency ( $\omega C < G$ ): the conductive nature dominates the substrate behavior and the silicon substrate is a lossy medium. This means that the uncorrected model in (3) will produce large coupling capacitance error. Consequently, a significant value of  $C_{\text{correction}}$  is needed in (6).
- 2) At high frequency ( $\omega C > G$ ): the dielectric nature dominates the substrate behavior. The losses effect is diminished and the silicon substrate can be considered as a lossless medium. This means that the uncorrected model in (3) will produce a small coupling capacitance error. Consequently, a small value of  $C_{\text{correction}}$  is needed in (6).

From [9], The frequency value that separates the conductive nature from the dielectric nature is:

$$f_{\text{sat}} = \frac{\sigma_{\text{si}}}{2\pi\epsilon_{\text{si}}} \quad (17)$$

When a TSV array is operating at a frequency equals or higher than  $f_{\text{sat}}$ , the uncorrected model in (3) provides sufficient accuracy for coupling capacitance extraction and no  $C_{\text{correction}}$  is needed. The previous physical expectation is validated using Q3D extractor. A 3x3 TSV array is built with the following TSV parameters:  $h = 40\mu\text{m}$ ,  $r = 2.1\mu\text{m}$ ,  $p = 24\mu\text{m}$ ,  $t_{\text{ox}} = 0.45\mu\text{m}$  and  $\sigma_{\text{si}} = 10\text{S/m}$ . According to (17),  $f_{\text{sat}} \approx 15\text{GHz}$ . The coupling capacitance of the TSV array was extracted at different frequency points. The results are shown in Fig. 5. As shown in Fig. 5,  $C_{\text{correction}} \approx 0$  when  $f \geq f_{\text{sat}}$ .

#### VI. CONCLUSION

This paper shows that using the relation between the inductance matrix and the capacitance matrix in a homogeneous

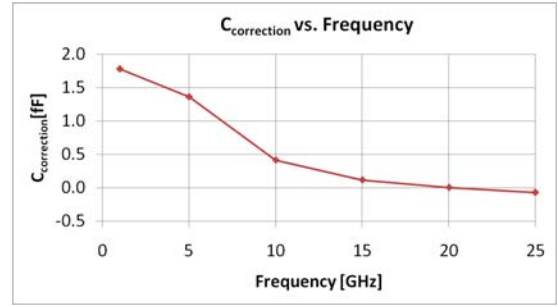


Fig. 5.  $C_{\text{correction}}$  vs. Frequency for 3x3 TSV Array

medium for TSVs coupling capacitance modeling is inaccurate. This is because the model assumes lossless, homogeneous medium surrounding the TSVs. In this work, we provide a good compromise of accuracy vs. run time by introducing a correction mechanism for the current model. The correction mechanism is implemented as a function of TSVs dimensions using dimensional analysis. The corrected model shows accuracy improvement over the uncorrected model when having Q3D extractor simulations results as the reference results. Then, we introduce the expected behavior of the correction function vs. frequency and validate it using Q3D extractor simulations.

#### VII. ACKNOWLEDGMENT

This research was partially funded by Zewail City of Science and Technology, AUC, the STDF, Intel, Mentor Graphics, ITIDA, SRC, ASRT and MCIT.

#### REFERENCES

- [1] C.-D. Wang, Y.-J. Chang, Y.-C. Lu, P.-S. Chen, W.-C. Lo, Y.-P. Chiou, and T.-L. Wu, "Abf-based tsv arrays with improved signal integrity on 3-d ic/interposers: Equivalent models and experiments," *Components, Packaging and Manufacturing Technology, IEEE Transactions on*, vol. 3, no. 10, pp. 1744–1753, Oct 2013.
- [2] T. Song, C. Liu, Y. Peng, and S. K. Lim, "Full-chip multiple tsv-to-tdv coupling extraction and optimization in 3d ics," in *Design Automation Conference (DAC), 2013 50th ACM / EDAC / IEEE*, May 2013, pp. 1–7.
- [3] Y.-J. Chang, H.-H. Chuang, Y.-C. Lu, Y.-P. Chiou, T.-L. Wu, P.-S. Chen, S.-H. Wu, T.-Y. Kuo, C.-J. Zhan, and W.-C. Lo, "Novel crosstalk modeling for multiple through-silicon-vias (tsv) on 3-d ic: Experimental validation and application to faraday cage design," in *Electrical Performance of Electronic Packaging and Systems (EPEPS), 2012 IEEE 21st Conference on*, Oct 2012, pp. 232–235.
- [4] E. B. Rosa, *The Self And Mutual Inductances of Linear Conductors*, 1st ed. U.S. Dept. of Commerce and Labor, Bureau of Standards, 1908.
- [5] C. R. Paul, *Analysis of Multiconductor Transmission Lines*, 2nd ed. Wiley-IEEE Press, 2007.
- [6] T. Ramadan, E. Yahya, Y. Ismail, and M. Dessouky, "Coupling capacitance extraction in through silicon via (tsv) arrays," *International Conference on Electronics, Circuits and Systems (ICECS)*, 2015.
- [7] K. Salah and Y. Ismail, "A novel dimensional analysis method for tsv modeling and analysis in three dimensional integrated circuits," in *Circuits and Systems (ISCAS), 2014 IEEE International Symposium on*, June 2014, pp. 2764–2767.
- [8] M. A. Laughton and M. G. Say, *Electrical Engineer's Reference Book (Fourteenth Edition)*, fourteenth edition ed. Butterworth-Heinemann, 1985.
- [9] A. Engin and S. Narasimhan, "Modeling of crosstalk in through silicon vias," *Electromagnetic Compatibility, IEEE Transactions on*, vol. 55, no. 1, pp. 149–158, Feb 2013.