Fast Hierarchical Optimization Method for High Speed Channel Design Using Channel Operating Margin (COM)

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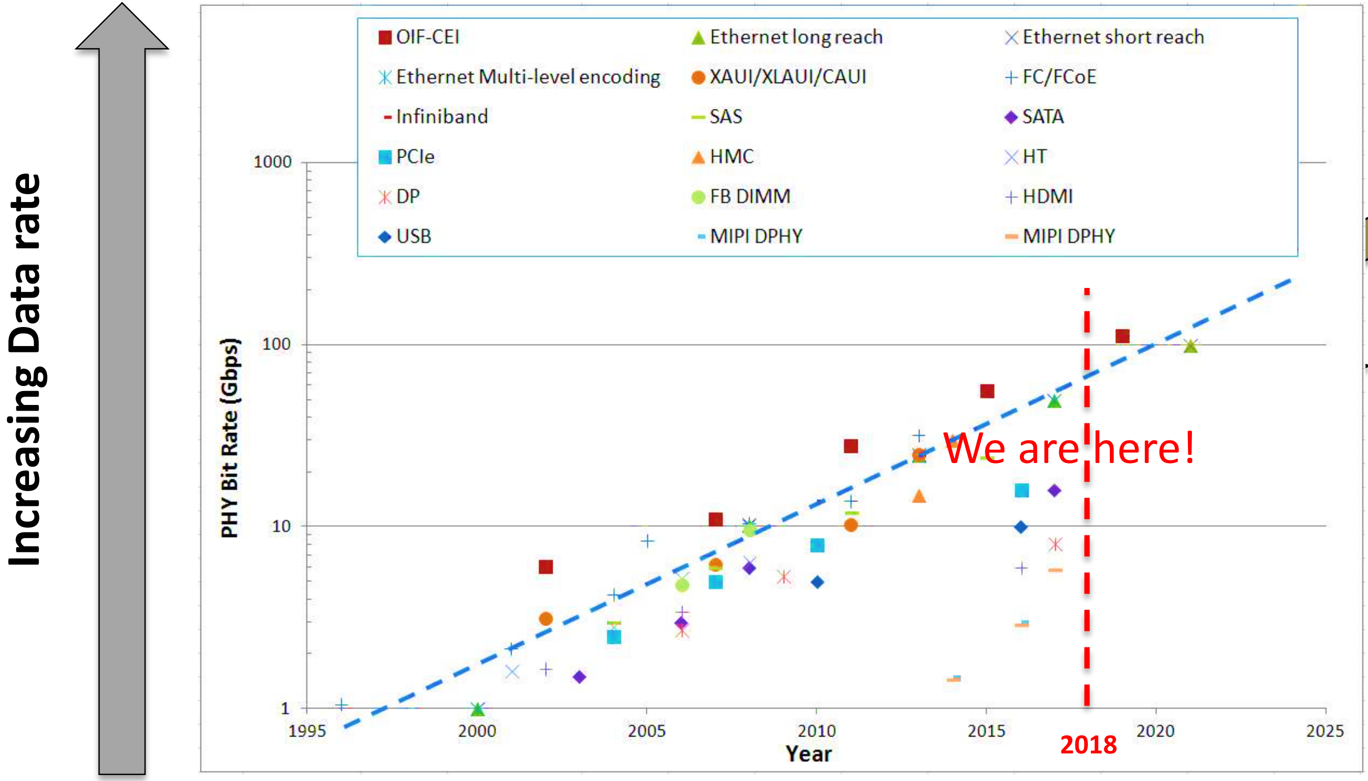
Outline

- **Motivation and Introduction;**
- **An Overview of Channel Operating Margin (COM);**
- **Conventional Optimization Method by COM;**
- **Proposed Design Flow based on our Hierarchical Optimization Method;**
- **Design Strategy of Via in High Speed Channel;**
- **Channel Operating Margin Analysis for Designed Channel;**
- **Conclusion and Future Plan.**

Motivation



[Reference] High-Speed I/O Speed Roadmap, International Technology Roadmap for Semiconductors (ITRS)

❖ **Trend !**

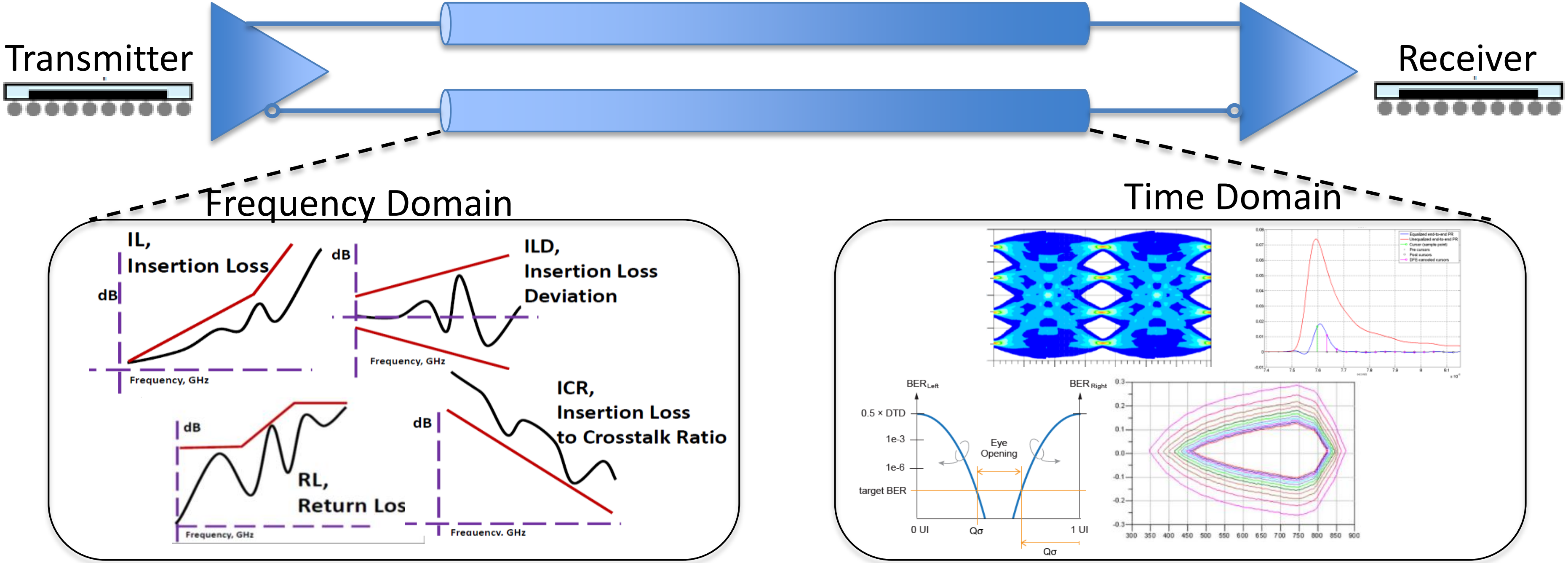
- Higher Complexity
- More Cost

Challenging Area

- Loss
- Impedance
- Crosstalk
- Jitter
- …

Motivation

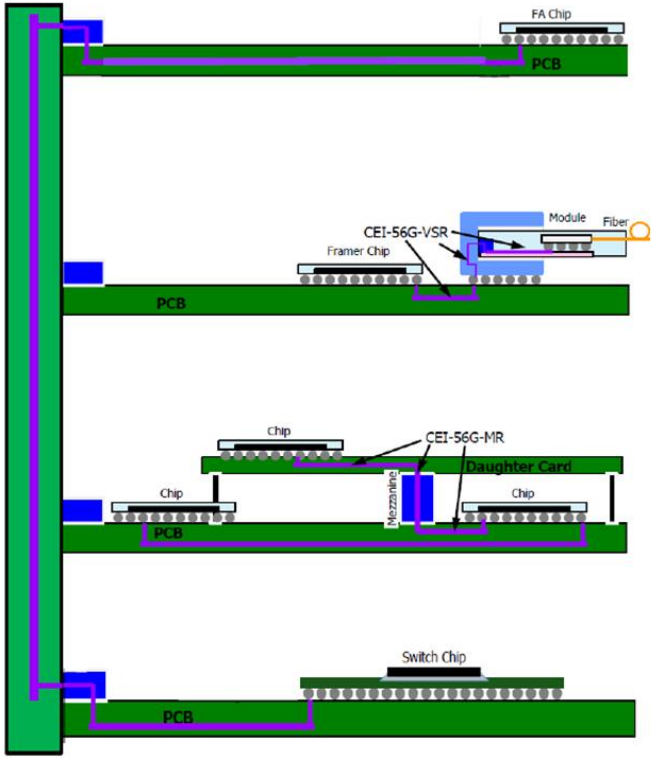
- **Diverse and complicate criteria in both time and frequency domains are used to estimate the performance of channel for high speed signal propagation.**



Definition of 56G Channel

- **Definition of the high speed channel applications by OIF CEI-56G.**

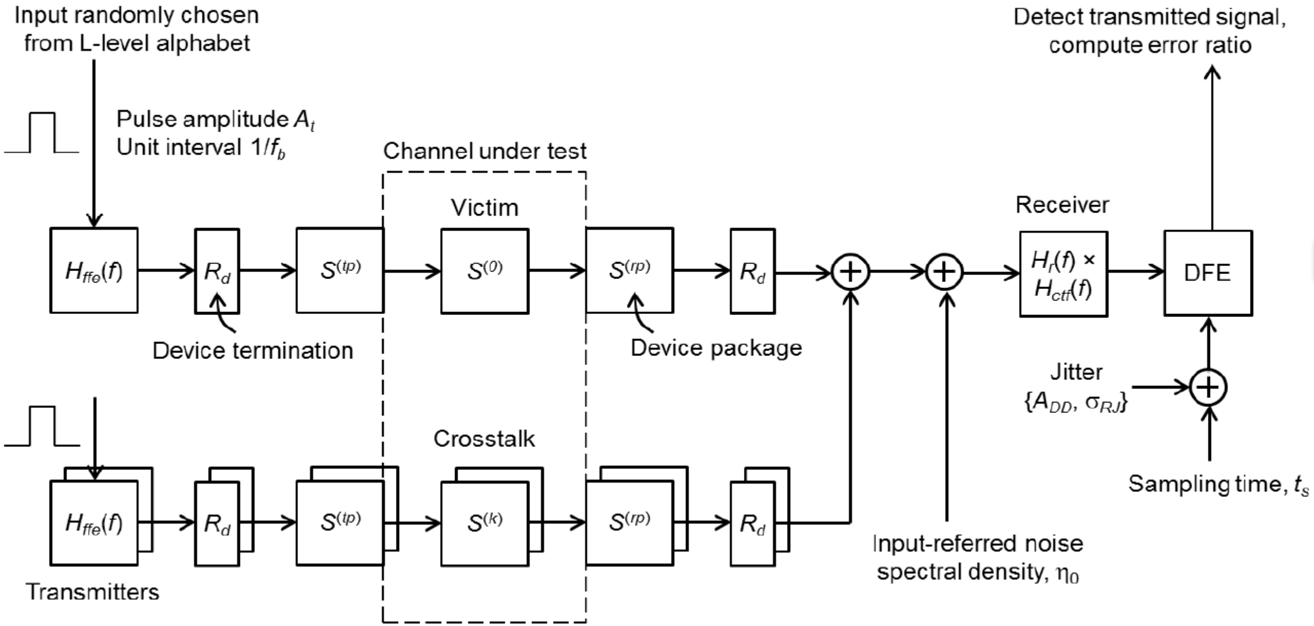
Scenarios	Interface	Distance	Maximum Loss	Modulation
Chip to OE	CEI-56G-USR	<1 cm	2 dB@ 28GHz	NRZ
Chip to nearby OE	CEI-56G-XSR	<5 cm	6 dB@ 28GHz	NRZ or PAM4
Chip to Module	CEI-56G-VSR	<10 cm	10 dB@ 14GHz 23 dB@ 28GHz	NRZ or PAM4
Chip to Chip	CEI-56G-MR	<50 cm	20 dB@ 14GHz 47 dB@ 28GHz	PAM4
Backplane	CEI-56G-LR	<100 cm	35 dB@ 14GHz 64.5-94 dB@ 28GHz	PAM4



- [Ref] OIF CEI-56G Common Electrical, OIF document number: OIF2014.380.02, 2015.
- [Ref] Geoff Zhang, Hongtao Zhang, Santiago Asuncion, and Brandon Jiao, “A Tutorial on PAM4 Signaling for 56G Serial Link Applications”, *DesignCon 2017*, Santa Clara, CA, 2017.

Introduction

- **An Overview of Channel Operating Margin Schematic.**
- COM has been proposed as a figure of merit to evaluate the quality of channel.



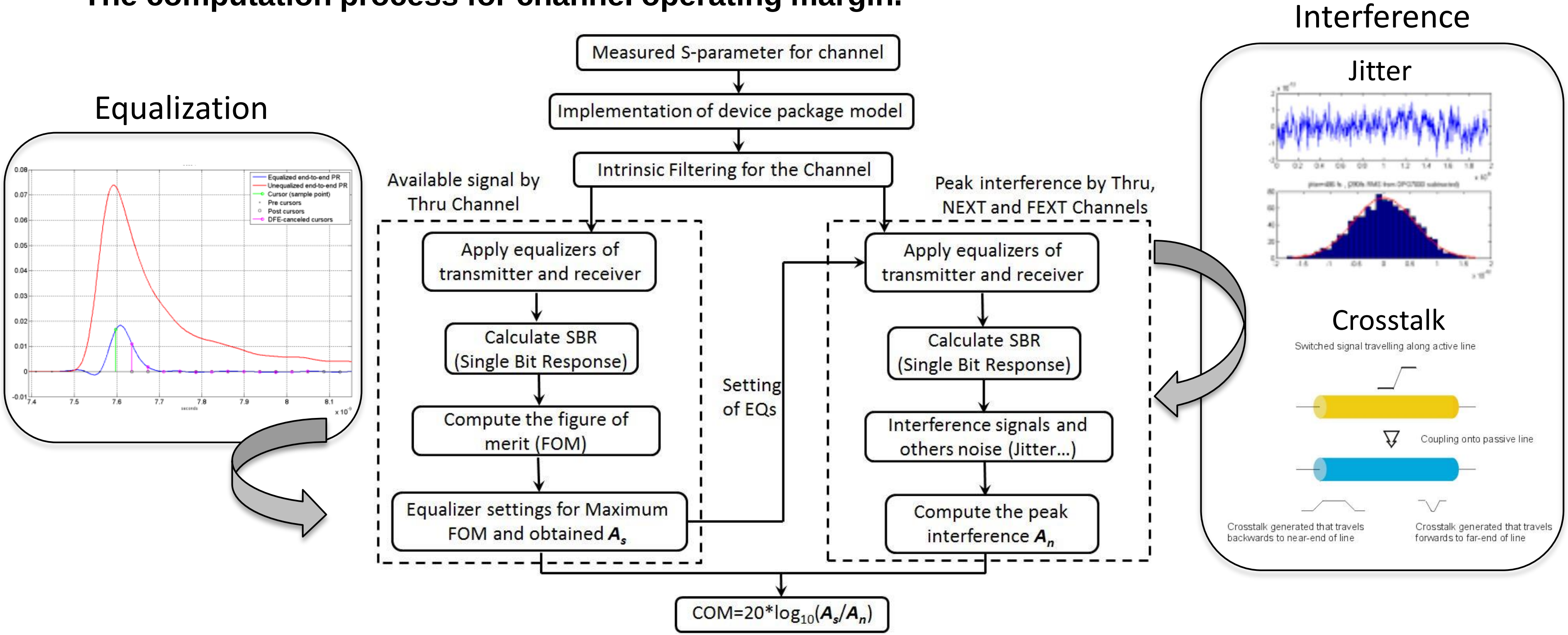
Signal to Noise Ratio

$$COM = 20 * log_{10}(\frac{A_s}{A_n})$$

[Ref] IEEE Std 802.3bj-2014 IEEE Standard for Ethernet Amendment 2: Physical Layer Specifications and Management Parameters for 100 Gb/s Operation Over Backplanes and Copper Cables.

Introduction

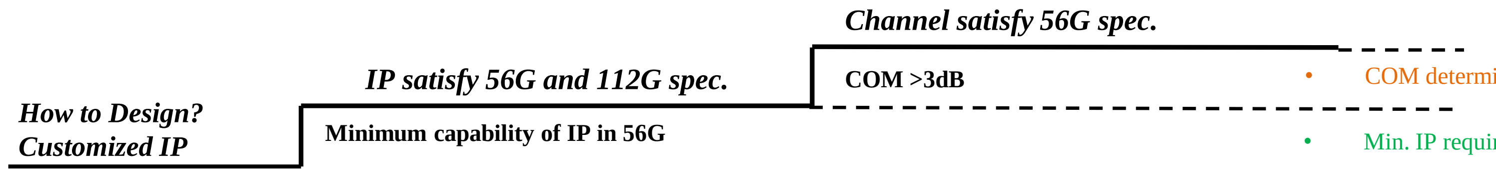
- **The computation process for channel operating margin.**



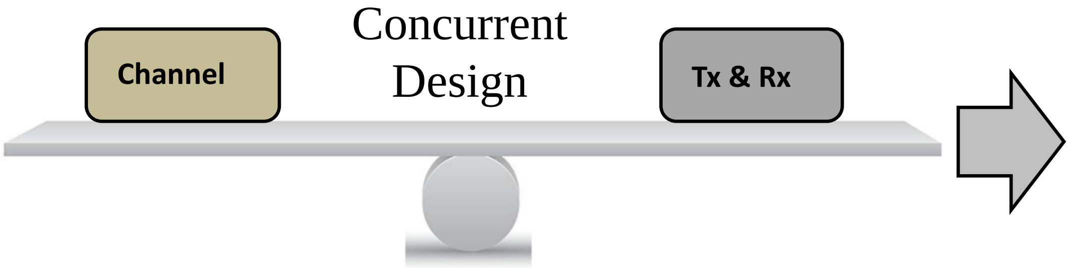
Introduction

- **Can COM be used as a deign guide in the design stage, not the evaluation period?**

	Loss	Modulation	Equalizer Design	Criterion-Design Stage	Design of IP and Channel
<25Gbps	Low	NRZ	Normal	Multi-mask	Separate
>25Gbps	High	NRZ/PAM4	Very High to enlarge eye and reduce BER, Hard to determine	COM	Concurrent Budgeting



- COM determine the channel in 56G
- Min. IP requirement of 56G by IEEE Spec.

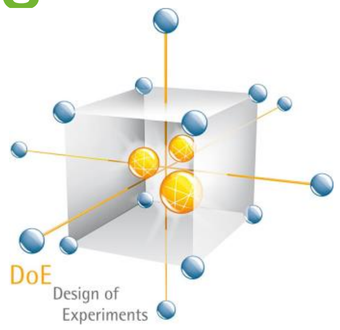


- ❖ A good enough design
- ❖ Avoid Over and Less Design

- Time saving in the design stage
- Cost saving in the fabrication.

Conventional Channel Design Methods

- **One factor at a time (OFAT) experiment**
  - Cons: It cannot consider the mutual effects between factors.
- **Design of Experiments + Response Surface Method**
  - Pros: Can ***include the interaction*** between factors;
  - Cons: Huge time cost for the interaction with large factors;
- **Design of Experiments + Artificial Neural Networks**
  - Pros: Can ***handle the insufficient accuracy*** of RSM for non-linear and higher order responses (An appropriate approach for channel design based on previous data)
  - Cons: Requires large enough data to train the ANN to ensure accuracy (Not possible in the early design stage)



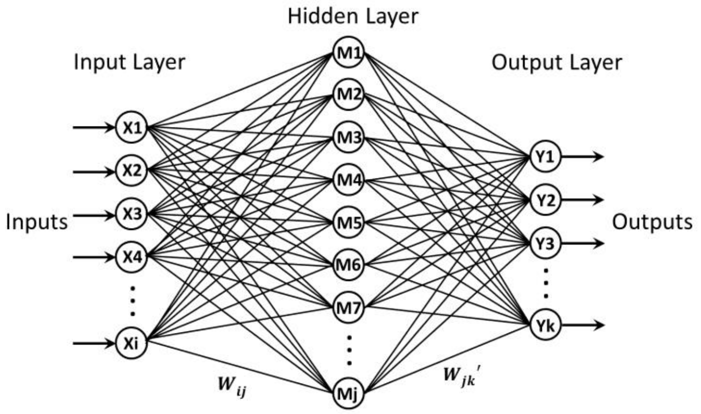


Fig. A typical structure for ANN.

Proposed Design Flow

- **Design Flow based on proposed Fast hierarchical optimization COM method.**

✓ TAT Reduction

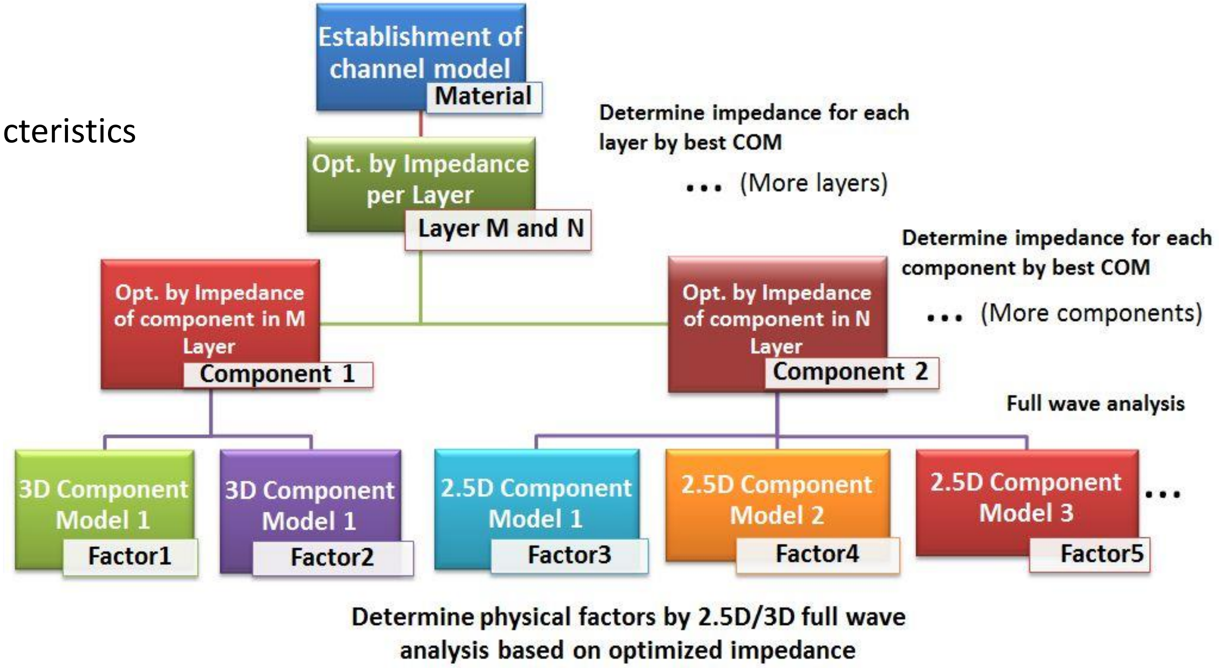
- Hierarchical structure
- Electrical to Physical Characteristics

✓ Realistic Scenario

- Interaction among factors

✓ High Accuracy

- Channel Sim. + 2.5D/3D



Proposed Design Flow

❖ **Components in a typical 56G LR Channel**

▪ ***Silicon Range***

- Transmitter and receiver

▪ ***Material & Stack up***

- Conductive and dielectric

▪ ***PCB, Package and Connector***

- Transmission line - Microstrip and Stripline
- Via and ball - discontinuity
- Cable connector
- Discrete device - AC capacitor, etc.

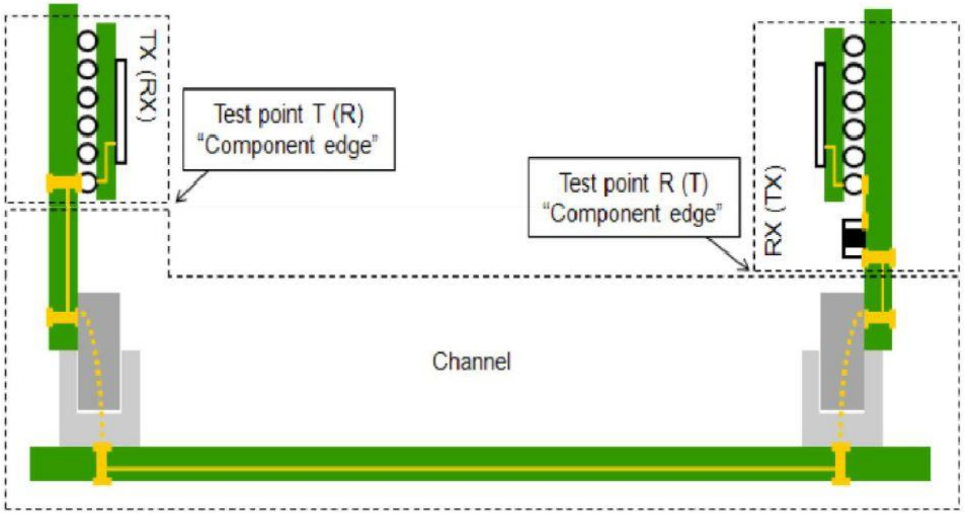
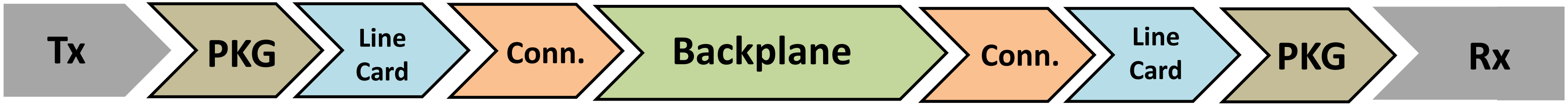


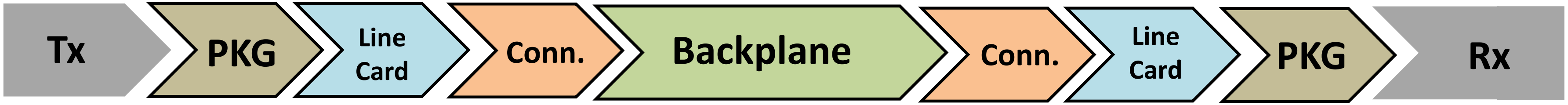
Fig. Configuration of long reach channel defined by OIE-CEI.



Conventional DoE for Channel Design

❖ **The most common DoE for channel design is a horizontal algorithm by physical geometry:**

- **Consider all physical parameters at the same level.**
- **To extract the best case by burden iterations.**



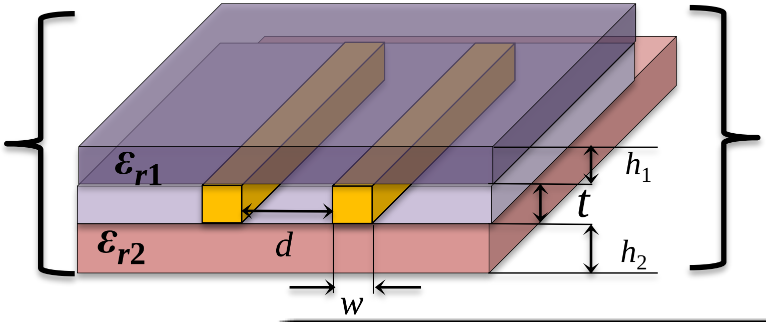
Simulation Times Required by Conventional DOE

	Via_layerA	Trace_layer A	Via_layerB	Trace_layerB	Connector_ layerC	Via_layerC	Trace_layerC
Variables (Physical Parameters)	2 (Pad & Antipad)	2 (Trace Width & gap of diff. lines)	2 (Pad & Antipad)	2 (Trace Width & gap of diff. lines)	1 (Impedance)	2 (Pad & Antipad)	2 (Trace Width & gap of diff. lines)
Sweep variables in a ±10% range (At least 5 set-5% as step to ensure accuracy)	10	10	10	10	10	10	10
Total Simulation Times:	$2^6 * 10^7$						

Proposed Design Flow

- **Step1: The optimization starts on the top level with <u>three layers</u> of the channel.**
  (line card layer A, backplane layer C and line card layer B)

Various <u>Physical</u> Parameters

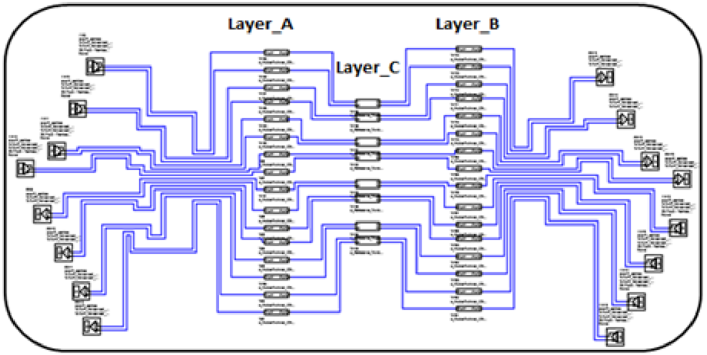


Physical → Electrical

Simplification

Single <u>Electrical</u> Characteristic
(Representative Value containing diverse physical factors)

Z *Impedance*



- Establishment of channel model by layer
- <u>Determined the optimized total impedance for layer_A, layer_B and layer_C.</u>

- Layer_A&B: Line card
- Layer_C: Backplane
- Terminations: Tx and Rx

After Performing COM

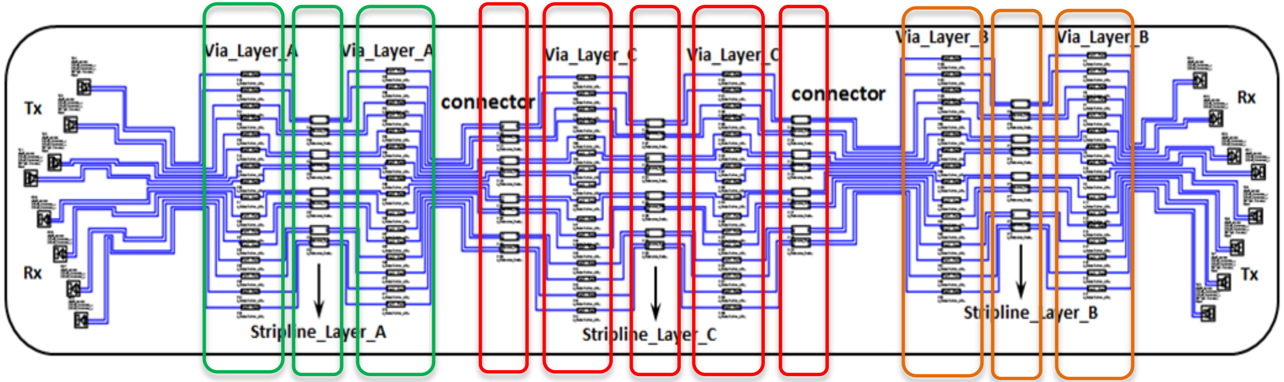
Proposed Design Flow

- **Step2: Expanded each layer to corresponding components and determine the optimized impedance for each device by COM computation.**

Single Electrical Characteristic → **Expanded Electrical Characteristics**

Z *Impedance* — *Impedance Matrix* ***[Z*** $_{\text{(Via, Line, Connector, etc.)}}$ ***]***

- Determined the optimized impedance for each component in every layer_A&B&C
- ±10% Variance sweeping for via and trace impedance separately to get best COM.



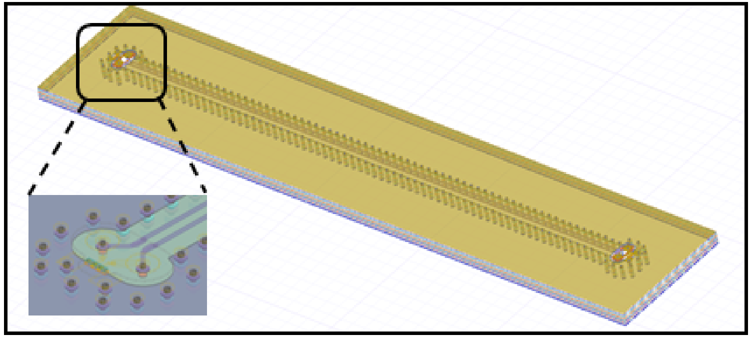
Proposed Design Flow

❖ **Step 3: 2.5D or 3D simulator used to extract the precise geometry for complex structure**

- Handling Inhomogeneous configurations in Z-axis: Via, Connector
- Accuracy guaranteed: 2.5D or 3D full-wave simulator

❖ **Step 4: Perform COM with the obtained alternative parameters and determine the best one.**

- Consider the bias of physical factors due to process in fabrication for alternative parameters



- **Determined the physical parameters based on optimized impedance using 2.5D and 3D simulator**
- **Channel Completion and analysis to get best COM.**

Proposed Design Flow

- **Iterations cost in our proposed design flow with a hierarchical optimization method.**

Proposed Fast Hierarchical Optimization Method

	Layer_A	Layer_B	Layer_C
Variables	1	1	1
Sweep variables in a ±10% range	10	10	10
Total Simulation Times:	$1^2 * 10^3 = 1000$		

Variables	2	2	3
Sweep variables in a ±10% range	10	10	10
Total Simulation Times:	$12 * 10^3 = 12000$		

Variables	2	2	2
Physical Parameters	2	2	2
Extraction of parameters by 2.5D/3D	1	1	1
Total Simulation Times:	$2^2 * 2^2 * 2^2 = 2^6$		

- **Determined the optimized total impedance for layer_A, layer_B and layer_C.**
- **Determined the optimized impedance for each component in every layer_A&B&C.**
- **Determined the physical parameters based on optimized impedance using 2.5D and 3D simulator**

Comparison for Conventional and Proposed Methods

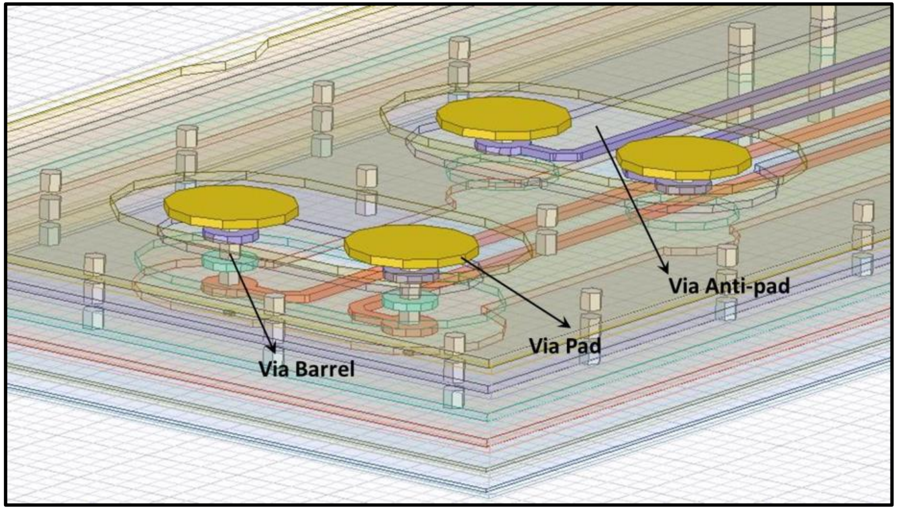
- **Time: A amazing time reduction is realized by the proposed methods.**
- **Accuracy: Higher accuracy gets ensured.**

Comparison of Iterations and Accuracy of Different Methods

Opt. method	**Conventional (Physical Parameters based)**	**Proposed (Hierarchy)**
Loop Sweeping	$2^6 * 10^7$	13064
Estimated Time Cost (Avg. 5 min. for each COM calculation of 56G)	74074 Months	1.512 Months
TAT reduction	(1-1.512/74074) *100% = **99.9979%**	
Accuracy	**Normal (2D Channel Designer)**	**High (Enhanced by 2.5D/3D simulator)**

Design Strategy of Via

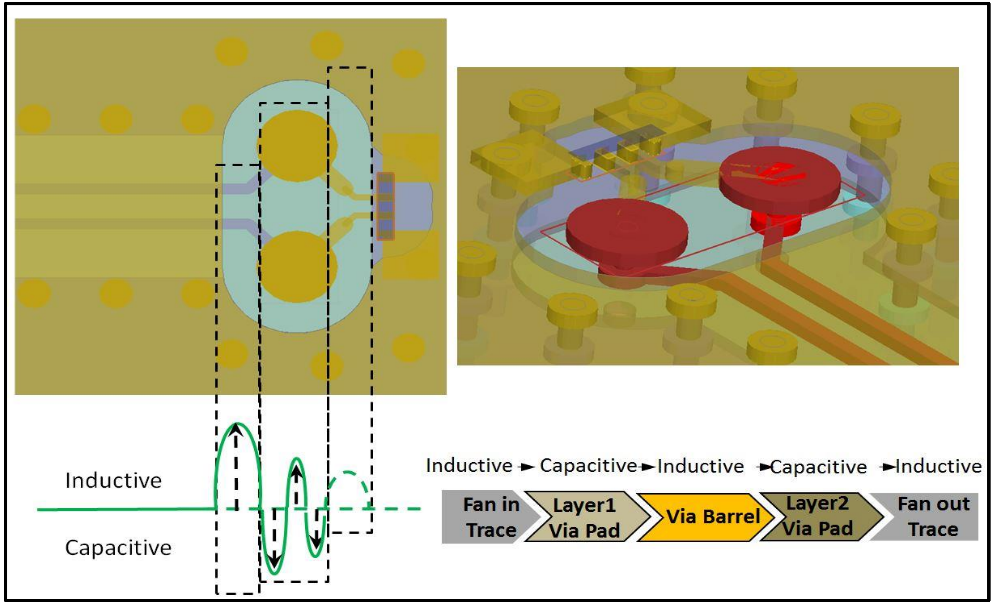
- **Via is the most common discontinuity in a passive channel, and a stable impedance transition is demanded at Via area.**
- Amateur design of the discontinuity - Via may cause disaster for high speed channel with multiple Gbp data rate.
- The basic factors of a typical via are via barrel, via pad and anti-pad.



Design Strategy of Via

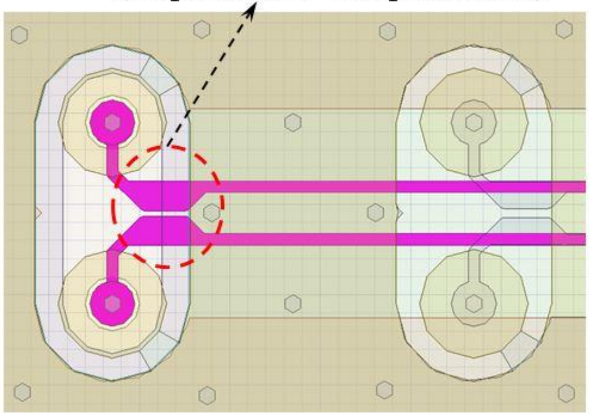
- **Parasitic of Via to affect the stabilization of impedance.**

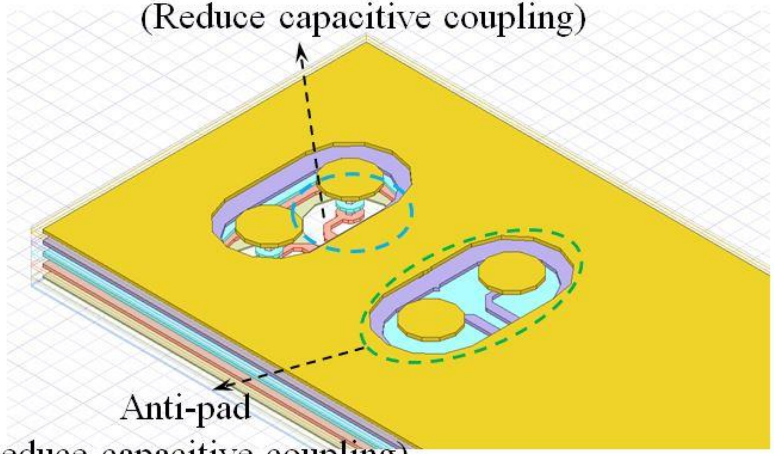
- Inductive effect generating positive fluctuation: loop by via barrel and a return path.
- Capacitive effect generating negative fluctuation: coupling between pad and nearby ground.



Design Strategy of Via

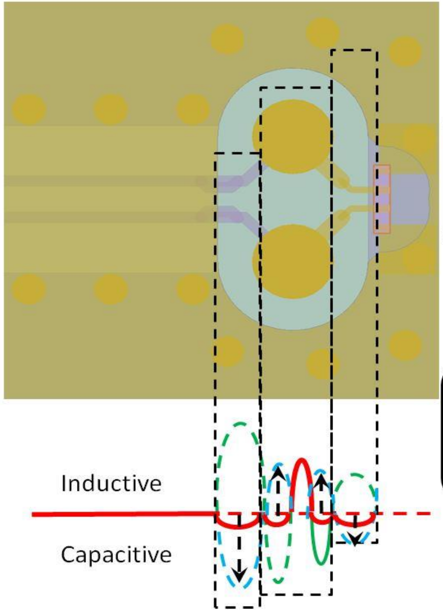
- **Proposed strategy to mitigate the variance on impedance**
- Transition coupled area: working as capacitance compensation
- Defected ground structure: to handle the redundant vertical capacitance.

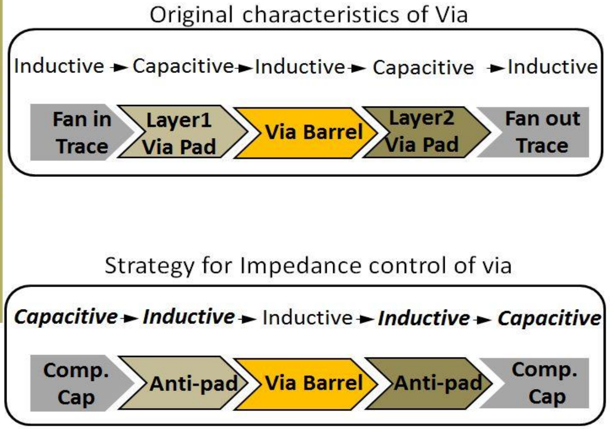




Design Strategy of Via

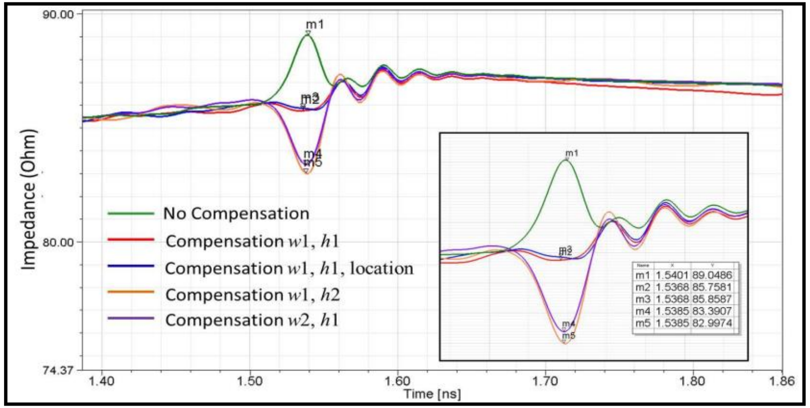
- **Expected stable impedance by implementing the design guide of via.**





Fluctuation Reduction for a study case

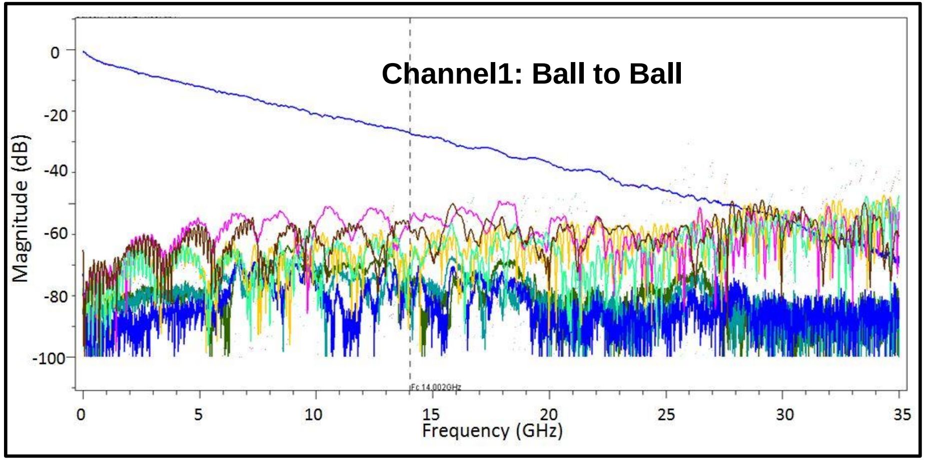
9.0486 ohm → 0.8587 ohm: 90.51% Reduced

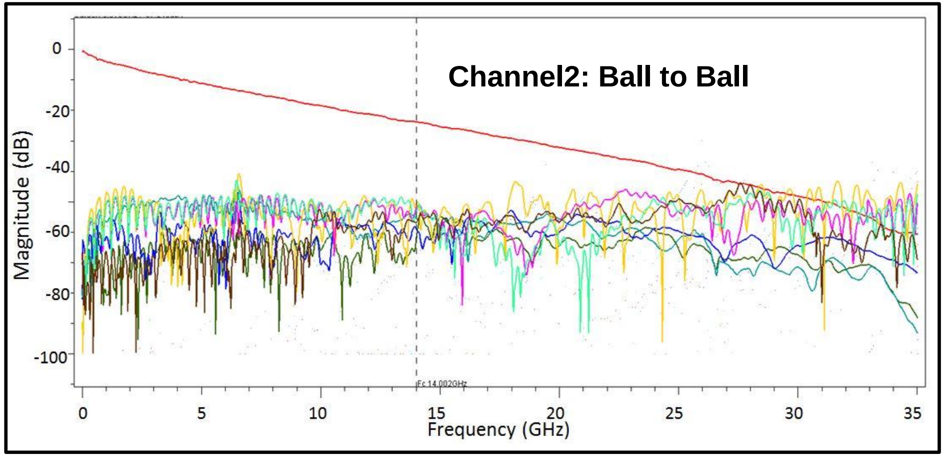


COM Analysis for Designed Channel

- **Two channels (*Ball to Ball, without Package*) with different insertion loss and crosstalk levels are design to demonstrate the effect of loss and crosstalk on the channel operating margin.**

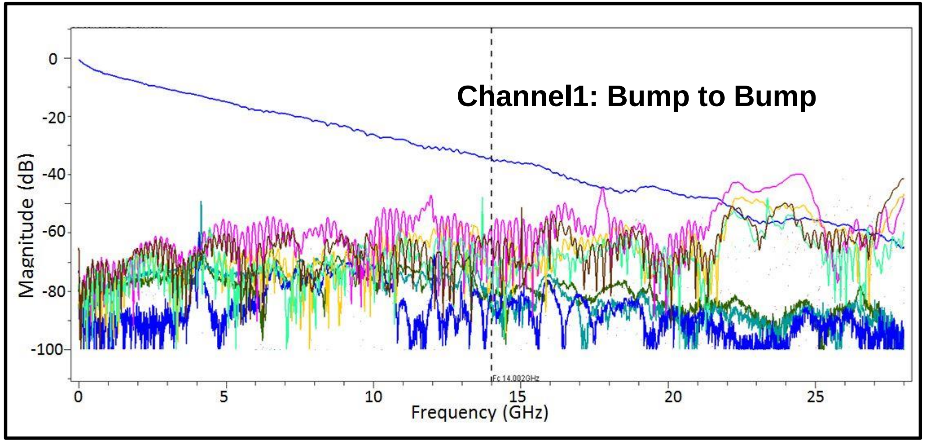
- Channel 1 has more insertion loss at Nyquist frequency of 14GHz but less power sum RMS value for crosstalk
- channel 2 is designed with a less insertion loss to channel1 but with a worse condition of crosstalk.

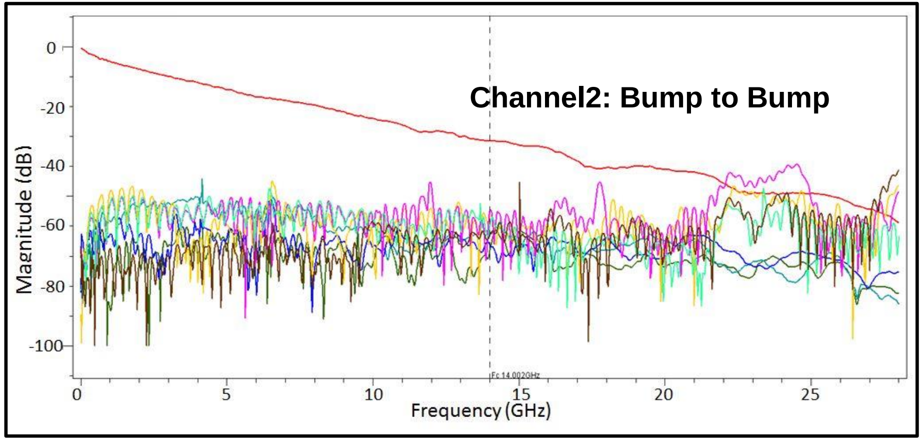




COM Analysis for Designed Channel

- **Effect on COM by the addition of package**
- **Does the package model defined in IEEE 802.3 COM need to be updated?**
- Conditions of two above mentioned channels (*Bump to Bump, with real designed package*)
- IEEE pre-defined package (IEEE 802.3bj)
- Real designed package (Figure below)





COM Analysis for Designed Channel

- **Crosstalk of package also generates a influence on the COM.**
- A difference is observed between the IEEE pre-defined package (w/o Xtalk) and real package (w/ Xtalk), although there is the similar level for loss.

Table 1: Definition of parameters for the package model used in COM extraction.

Parameter	Definition	Setting	Units
C_d	Single-ended device capacitance	[1.8e-4 1.8e-4]	nF
z_p select	Test cases of package model	[1 2]	Test case
z_p (TX)	Victim transmitter package trace lengths	[12 30]	mm
z_p (NEXT)	NEXT aggressor transmitter package trace lengths	[12 12]	mm
z_p (FEXT)	FEXT aggressor transmitter package trace lengths	[12 30]	mm
z_p (RX)	Victim receiver package trace lengths	[12 30]	mm
C_p	Single-ended package-to-board capacitance	[1.1e-4 1.1e-4]	nF
R_0	Reference single-ended impedance	50	Ohm
R_d	Single-ended termination resistance	[55 55]	Ohm

Table 2: Comparison of COM for channels with diverse package conditions.

Cases	Package Condition	COM (dB)
Channel 1	Without package	5.7470
	With IEEE pre-defined package	3.9445
	With real package	3.5176
Channel 2	Without package	4.5540
	With IEEE pre-defined package	3.5175
	With real package	3.4785

Conclusion and Future Plan

- In this paper, we first propose a design flow for channel design by a fast hierarchical optimization method based on COM.
- Advantages on accuracy and speed for our proposed hierarchical design flow was demonstrated.
- Novel design strategy to mitigate the fluctuation of impedance at via was addressed
- Characteristic such as loss and crosstalk of the designed channel is demonstrated。
- The effect of package on the COM was discussed by a comparison of diverse package conditions.
- In future works, we will concentrated on the enhancement of the design flow and contribute to the accurate COM criterion for high speed links.

Reference

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- [2] Mike Peng Li, "Design and Verification for High-Speed I/Os at Multiple to 60 Gbps With Jitter, Signal Integrity, and Power Optimization", *DesignCon 2015*, Santa Clara, CA, 2015.
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- [4] C. Filip, D. Araujo, P. V. Gurswamy, M. Rowlands. A. Gafarov, and P. Anmula, "Optimization Methods for High-Speed SerDes Channels using COM Metric" , *DesignCon 2017*, Santa Clara, CA, 2017.
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- [7] IEEE Std 802.3bj-2014 IEEE Standard for Ethernet Amendment 2: Physical Layer Specifications and Management Parameters for 100 Gb/s Operation Over Backplanes and Copper Cables.

Thank you!

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QUESTIONS?