Enhancement of Differential Signal Integrity by Employing a Novel Face Via Structure

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***Abstract*—This paper proposes a novel differential via structure, which is dubbed as face via, to improve the impedance discontinuities at the via transition. The performance of the proposed face via is verified by simulated and measured impedances in time domain reflection responses and by equivalent circuit modeling. In this paper, the conventional cylinder via and the proposed face via were designed and fabricated to demonstrate the effectiveness of the face via in differential signal channels. The analysis indicates that the proposed differential via structure provides a very effective way to minimize the impedance discontinuities at vias by controlling the size of face in the via. The analysis of the eye diagram identified the improvement of signal integrity in channel characteristics. Furthermore, in order to consider the complexity in digital system at high speed, the performance of face vias in multiple via transitions and the effect of return current vias are also investigated. Finally, the effectiveness of the proposed face via has been successfully validated by the simulation and experiment results.**

***Index Terms*—Differential signal channel, differential via, face via, impedance discontinuities, signal integrity, via transition.**

I. Introduction

In THE latest modern digital system, the operating frequency has drastically increased, and it requires multilayer printed circuit board (PCB) structure due to its increasing geometrical complexity, which produces many geometrical discontinuities and electromagnetic (EM) coupling. To obtain safe signal integrity in this complicated system, differential signaling has been widely used in significant signal delivery because of its superior noise immunity and broad transmission bandwidth [1]. The differential signal traveling in the PCB has been known to effectively reduce coupling noises, but it still needs to be improved in terms of signal integrity, as a digital system requires higher performance in high-end electronic products.

One of the most influential causes of signal integrity degradation in differential signaling is the impedance discontinuities along the transmission line where the differential signals travel. Along the line, these impedance discontinuities need to go through a via, which is composed of a pad, an antipad, and a central cylindrical barrel, and so on. These geometrical discontinuities can degrade signal integrity, of course, in terms of via impedance, which is affected by the pad capacitance and the barrel inductance [2].

So far, numerous researches in characterizing the behavior of the via structure have been presented [3]–[8]. The impedance mismatch of a single-ended signal at the via transition has been minimized by adjusting the via parameters, such as via diameter, height, stub length, pad size, antipad size, and ground via locations [3]–[5]. The impedance mismatch in differential signals at the via transition has also been reduced by changing the pitch of the signal vias, the distance between the signal via and the ground via, and so on [5], [6]. The shape of the antipad has been changed to alleviate the impedance mismatch problems [7], [8]. Despite all these efforts, however, signal integrity in the differential lines has not improved quite much, especially in terms of impedance discontinuities.

In this paper, we propose a new differential signal via structure, which is called face via, to match the impedance of the differential trace with that of the via in differential signaling. So far, the typical through hole via has been treated as a cylindrical structure [9], [10], and the equivalent circuit for a pair of through silicon via has been also developed on the basis of the cylindrical structure [11]–[13]. Therefore, a simple twin-rod model could be used to estimate the performance of a differential via [14]. The suggested via, however, uses a face barrel instead of the cylinder barrel to provide an intuitive method to control the characteristic impedance in a differential via. By choosing appropriate geometrical parameters, the proposed via structure maintains the impedance fluctuations efficiently and enhances the differential signal integrity dramatically, especially in multiple via transitions. Furthermore, the fabrication process of the proposed via does not require a complicated process; it only needs one additional drilling, which could be quite optimistic in the application of the mass product.

This paper is organized as follows. Section II introduces and describes the proposed face via structure and its manufacturing process in the PCB. In Section III, frequency domain and time domain simulations are investigated to demonstrate the effectiveness of the proposed via structure using an EM simulator. Then, the performance of the proposed via structure for a single via transition is verified through an experimental measurement in Section IV. Finally, experiments for multiple via transitions and simulations for return current vias are investigated in Section V, and a conclusion is addressed in Section VI.

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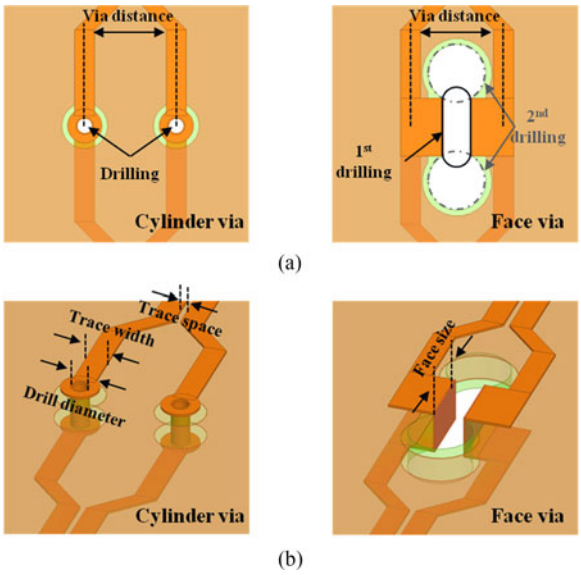

Fig. 1. Conceptual illustration of a conventional cylinder and the proposed face via at (a) top view and at (b) side view: via distance = 1.6 mm for both vias, drill diameter in the cylinder via = 0.3 mm, first drill diameter in the face via = 0.5 mm, and second drill diameter in the face via = 1.0 mm.

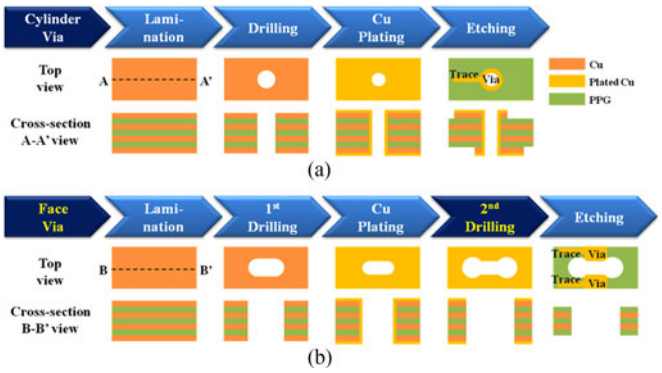

Fig. 2. Comparison of the two fabrication processes (a) in a conventional cylinder via and (b) in the proposed face via in PCB.

II. Face Via

Conventional through hole via connects the two pads in different layers, physically and electrically, through the copper-plated through hole. As the common drilling process is employed for this process, the vias are cylindrical shape in the PCB. Accordingly previous papers have been about the cylindrical via structure so far. It seems that the control of impedance in a cylindrical via, however, has not been easy in a wide range, especially in the control of capacitance. In this paper, we propose a flat via structure as shown in Fig. 1: this is to control the impedance of the differential via in a wide range with more ease, having flat walls facing each other instead of cylindrical walls. As the impedance change of the face via can vary in a wide range depending on the area and distance of the two flat walls, we can easily control the differential impedance by widening or thinning the face size.

Fig. 2 shows the comparison of the two fabrication processes for cylinder via and face via. As illustrated in Fig. 2(a), in conventional multilayer PCBs, the PCB layers are laminated, drilled, and then metalized the through hole with copper. After copper plating, the unused copper surface is etched out to achieve the desired circuit patterns [15]. The basic PCB fabrication processes of the proposed face via are similar to those of the conventional via except for one more additional drilling process. The oblong hole is obtained by performing the first drilling process, as shown in Fig. 2(b), and then copper plating is performed to connect the conductors between the layers. After copper plating, the second drilling process is carried out on both ends of the oblong hole to separate the plated oblong hole into two different face vias. This step is considered the only large difference in the conventional process for the cylinder via. Consequently, the middle walls of the oblong hole remain, and each face wall serves as a barrel that connects the layers. In summary, only one additional drilling process is required to fabricate the face via.

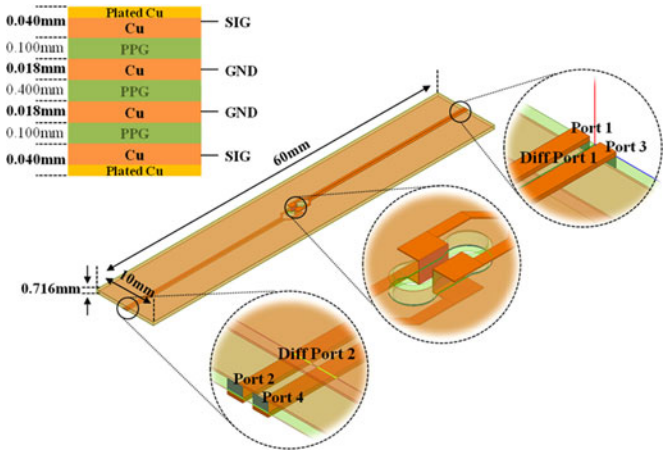

Fig. 3. Geometry of face via for the EM simulation with a PCB stack-up and each port description.

III. EM Simulation

In this section, we describe the simulated results of the scattering parameters (*S*-parameter) in the frequency domain and the characteristic impedance in time domain for the proposed face via. The frequency domain simulation was conducted up to 10 GHz using a three-dimensional (3-D) EM full-wave solver ANSYS high frequency structural simulator (HFSS), and the Agilent advanced design system (ADS) software was used for the time domain simulation. ANSYS Q3D was adopted for the parasitic parameter extraction in the differential via. The effects of surface roughness, etch factor, woven fiberglass substrate, and photo-imageable solder resist ink were not considered in the simulation.

A. Frequency Domain Simulation

Fig. 3 shows a four-layer PCB with a top signal layer, two inner ground layers, and a bottom signal layer, which was used for the EM simulation. The port numbers of the differential lines are described in Fig. 3, and the PCB stack-up and cross sectional dimension of PCB are also presented. The PCB is 60 mm ×

TABLE I
DETAILED GEOMETRICAL DIMENSIONS IN THE PCB FOR SIMULATION

Case ID	Via Type	Trace Width (mm)	Trace Space (mm)	Face Size (mm)	First Drill Size (mm)
A2	Face	0.25	0.1	1.00	0.5
B2	Face	0.25	0.1	1.25	0.5
C2	Face	0.25	0.1	1.50	0.5
D2	Face	0.25	0.1	1.75	0.5
E2	Face	0.25	0.1	2.00	0.5
R2	Cylinder	0.25	0.1	-	0.3

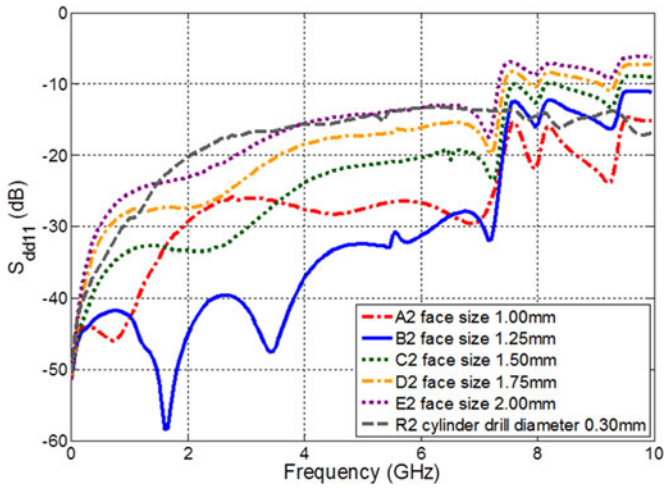

Fig. 4. Comparison of *S*dd11 for the conventional cylinder via and the proposed face via with various face sizes.

10 mm in size and 0.716mm thick. All substrates are of FR-4 with a relative dielectric constant of 3.7 and a loss tangent of 0.02. We assume the copper conductivity of 5.8×10^7 S/ m. The length of the microstrip line in each top and bottom layer is 30 mm, and the layer is transited at the middle of design under test (DUT). The via distance in the two differential lines, as described in Fig. 1(a), is mainly determined by the second drilling size. Since the second drilling size of 1.0 mm in consideration of PCB manufacturing process capability, via distance is 1.6 mm. For later comparison, other geometries related to the traces are identical in the left and right portions of Fig. 1(a), except for the geometry of the two vias. The detailed vias and the PCB dimensions of DUTs for simulation are summarized in Fig. 1 and Table I, respectively. Note that the differential transmission line systems usually target 85–100 Ω. In this paper, however, the differential impedance targets 70 Ω because of the PCB manufacturing limitation. If the face size below 1 mm is available, the differential characteristic impedance of the face via will be 85 Ω.

The simulated S_{dd11}s, which are the reflection in the differential mode, and S_{dd21}s, which are the insertion loss in the differential mode, are depicted with different sizes of the face via, as shown in Figs. 4 and 5. The size of the face varies from 1 to 2 mm with a 0.25 mm step interval, whereas a drill bit with a diameter of 0.3 mm is used in the cylinder via. The *S*-parameter plots in Figs. 4 and 5 are normalized to 70 Ω of the

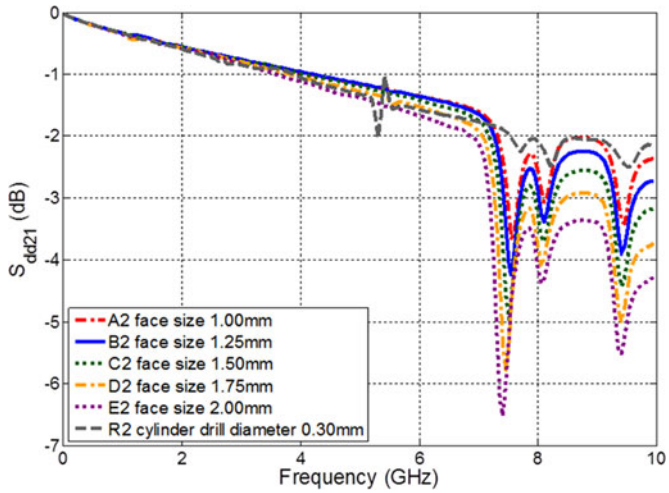

Fig. 5. Comparison of *S*dd21 for the conventional cylinder via and the proposed face via with various face sizes.

differential impedance in the microstrip line to observe the face via performance without reflection noise effects in each port.

It is clear that S_{dd21}s increase and S_{dd21}s decrease as the frequency goes up, and the performance of the face via could be superior to that of cylinder via from 0 to 7 GHz. Furthermore, when the face size is 1.25 mm, in the "B2" case, the reflection of the signal is the least and the transmission of the signal is the greatest. Beyond 7 GHz, the superiority of the face via seems to end possibly due to the resonances caused by second drilling. It has been confirmed that these resonances can be eliminated by using smaller drill bit size in the EM simulation. In summary, the S_{dd11} and S_{dd21} of the face via vary according to face size and an optimal face via size could be determined, which maintains the better signal transfer characteristics than the cylinder via.

B. Time Domain Simulation

The *S*-parameters extracted from the EM simulation in the previous section are imported into the ADS simulator to examine the behaviors in the time domain. Fig. 6 shows the time domain transmission (TDT) responses of the DUT with an incident step input signal of 35 ps rise time and 1V magnitude. The propagation time from port 1 to port 2 is about 333 ps. Fig. 7 illustrates the time domain reflection (TDR) responses in the cylinder via and in various face vias with different face sizes.

The impedance of the differential microstrip line with 0.25mm width and 0.1mm distance between the lines is calculated to be 69 Ω, and Fig. 7 shows the expected impedance except at 380 ps, where the impedance fluctuates. Since it takes 323 ps to arrive at the fluctuating impedance, this occurrence can be due to the impedance mismatches in the vias because they coincide with the propagation time (333 ps) in the TDT responses in Fig. 6.

In Fig. 7, the cylinder via acts as an inductive load, whereas the face via gradually acts as a capacitive load when the face size increases. Moreover, it is clearly shown that there exists an optimal face size. The capacitance and inductance of the face via are strongly influenced by face size, thus indicating

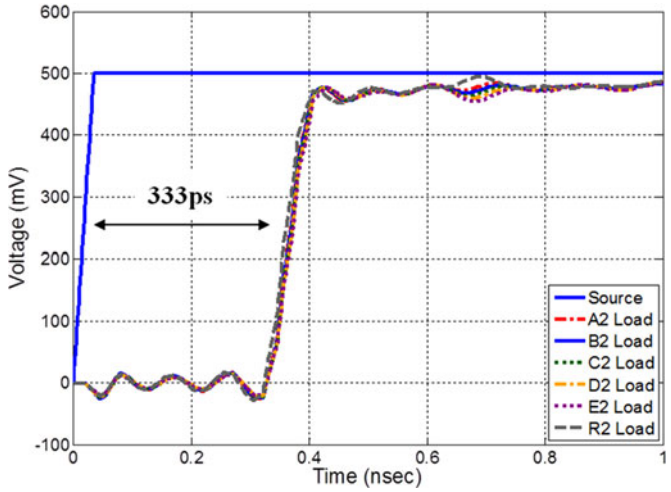

Fig. 6. TDT responses of the DUT in the circuit model. The *S*-parameters used in the analysis are from the EM simulation.

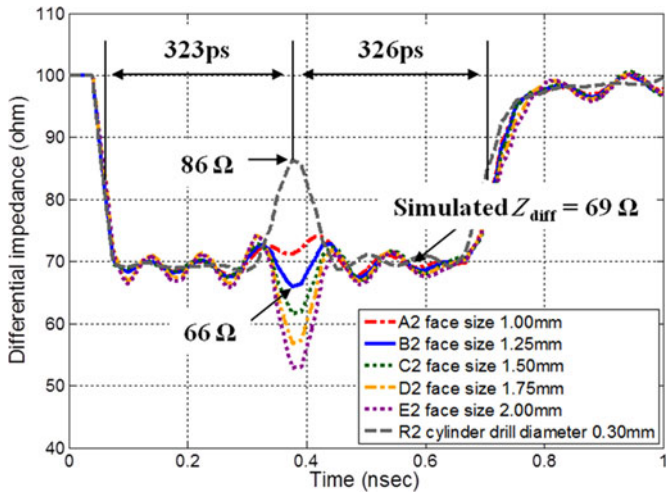

Fig. 7. Comparison of the circuit-simulated TDR responses between the cylinder via and the face via with face size variations.

that we can control the differential impedance of the face via by adjusting the face size. As compared with the cylinder via, the differential impedance discrepancy between traces and vias is reduced from 17 Ω (86 − 69 Ω) to 3 Ω (66 − 69 Ω) when the face size is 1.25 mm. The following section describes the analysis of the equivalent circuit model that can validate the results of the ADS analysis.

C. Differential Via Modeling

To characterize the differential via, we compute the capacitance and inductance separately and neglect the possible coupling between the magnetic field and electric field, i.e., with quasi-static approximation. This approximation is valid when via hole is much smaller than the wavelength, as stated in [16]. The equivalent circuit model for the differential via is described in Fig. 8. C_{ii} represents the self-capacitance of a single via and C_{ij} represents a mutual-capacitance between the vias. Likewise, L_{ii} represents the self-inductance of a single via and L_{ij} represents a mutual-inductance between the vias [17]–[20].

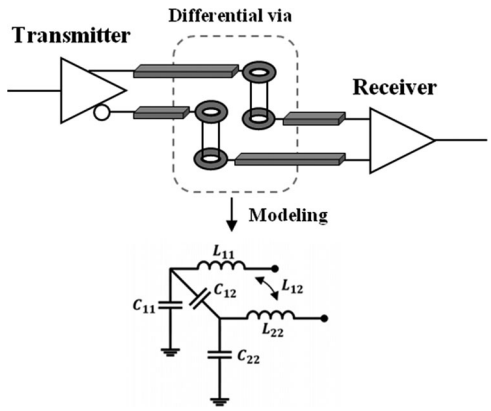

Fig. 8. Equivalent circuit model for the differential via [17]–[20].

TABLE II
COMPARISON OF THE PARASITIC PARAMETERS IN THE DIFFERENTIAL VIA FROM Q3D AND ADS ANALYSES

Case ID	Via type	Q3D					ADS
		C_{11} (pF)	C_{12} (pF)	L_{11} (nH)	L_{12} (nH)	Z_{diff} (Ω)	Z_{diff} (Ω)
R2	Cylinder	0.193	0.0006	0.473	0.075	90.5	86.0
B2	Face	0.430	0.0251	0.670	0.193	63.0	66.0

The differential impedance (Z_{diff}) is twice the odd-mode impedance (Z_{odd}) when the odd-mode impedance is defined by the ratio of odd-mode inductance (L_{odd}) to odd-mode capacitance (C_{odd}),

$$Z_{\text{diff}} = 2 \times Z_{\text{odd}} \tag{1}$$

$$Z_{\text{odd}} = \sqrt{\frac{L_{\text{odd}}}{C_{\text{odd}}}} \tag{2}$$

where

$$L_{\text{odd}} = L_{11} - L_{12} \tag{3}$$

$$C_{\text{odd}} = C_{11} + 2C_{12}. \tag{4}$$

Consequently, the Z_{diff} of the differential via can be calculated as

$$Z_{\text{diff}} = 2 \times \sqrt{\frac{L_{11} - L_{12}}{C_{11} + 2C_{12}}}. \tag{5}$$

Table II describes the parasitic parameters extracted by Q3D, and the calculated differential impedance Z_{diff} by using (5) and Z_{diff} from the ADS analysis. These data show a good agreement in both methods, and minor deviations within 5%. With an accurate drilling process in PCB fabrication, we can control the face size more precisely for better impedance matching.

IV. EXPERIMENTAL VERIFICATION

A. Structure of the Designed Test Vehicle

Fig. 9 shows the designed and fabricated test vehicles. All characteristics, such as the dimension and material parameters in the PCB, are identical to those used in the EM simulation

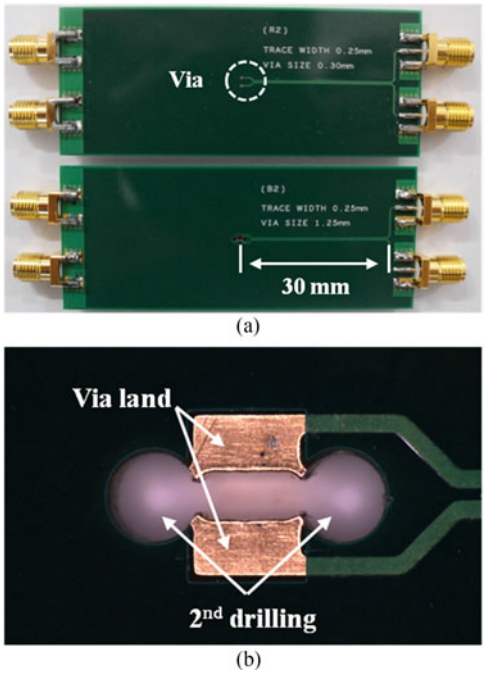

Fig. 9. Test vehicles for measurement. (a) Top: cylinder via(R2) and bottom: face via(B2) with a face size of 1.25 mm. (b) Enlarged view of the fabricated face via.

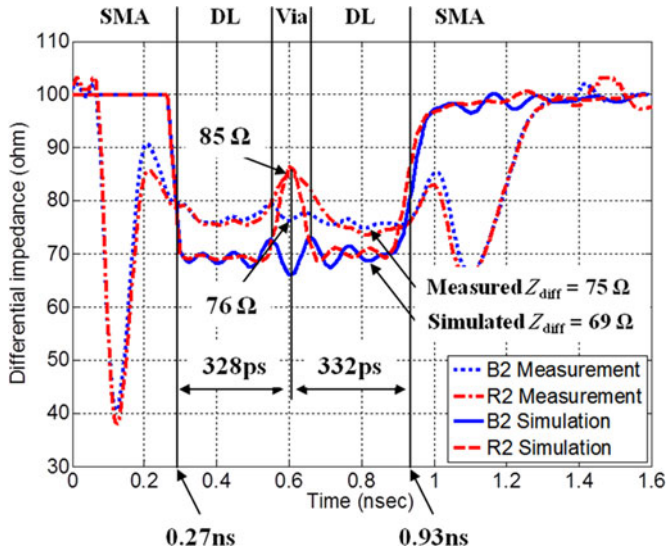

Fig. 10. Comparison of the simulated and measured TDR responses from the conventional cylinder via and the proposed face via. The measured peak Z_{diff} in the cylinder via is 85 Ω and the measured Z_{diff} in the face via in the same instance is 76 Ω.

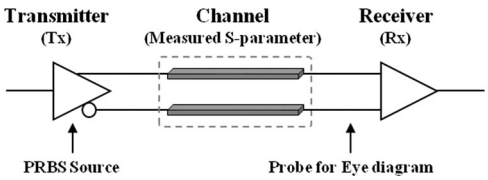

Fig. 11. Block diagram of the channel model for the transient simulation.

as described in Figs. 1 and 3. On the basis of the EM simulation results, we fabricated the "B2" case, which shows good impedance matching with a trace width of 0.25 mm, and the "R2" case for the cylinder via for comparison. For the TDR measurement, the SubMiniature version A (SMA) connectors were added at the ends of the microstrip lines. The E5071C ENA series network analyzer was used to measure the TDR responses and *S*-parameters.

B. Differential Impedance in TDR Measurement

The test vehicles were connected to the four port TDR meter with a 35 ps rise time and a 20 GHz bandwidth for each case. Fig. 10 shows the simulated and measured TDR responses between the cylinder and face vias. The large fluctuations in the TDR responses up to 270 ps are due to the SMA connector, and another fluctuation at around 600 ps in R2 is due to the discontinuity in the cylinder via. Therefore, the waveform can be divided into five areas: 1) SMA area at differential port 1 from 0 to 270 ps, 2) differential line area from 270 to 550 ps, 3) via dominant area from 550 to 650 ps, 4) differential line area again from 650 to 930 ps, and finally 5) SMA area over 930 ps. A via transition occurs at around 600 ps. These timing sequences related to the signal propagation are well matched with the measured and simulated values in TDR and TDT, except for a small difference in the magnitude of Z_{diff}.

The impedance mismatch of 6 Ω (75 − 69 Ω) turned out to be due to the over etching in the microstrip line, and it makes the width as smaller as 210 μm, which corresponds to the characteristic impedance of 75 Ω. Even with this deviation, however, we can observe that the cylinder via acts as an inductive load. By employing the proposed face via, the self- and mutual-capacitances at the via transition can be increased, thus making the impedance of the differential via smaller. Note that the difference between the peak impedance and the line impedance is about 10 Ω in the cylinder via, whereas the difference is about 1 Ω in the face via in the same instance. So it is clear that by employing the proposed via structure, we can make the impedance fluctuation minimally at the via transition area.

C. Channel Simulation Using the Measured S-Parameters

An eye diagram has been used as a common way for characterizing the channel performance [21]. Channel topology consists of a differential transmitter model (Tx), measured four port *S*-parameters, and a differential receiver model (Rx), as described in Fig. 11. The probe point for the eye diagram is in front of the Rx and Tx includes the functionality of a pseudo-random binary sequence (PRBS) source. Each eye diagram is obtained by using the PRBS source with voltage amplitude of 1.2 V, a rise-fall time of 35 ps, and data rates of 3.2 and 6.4 Gbps.

Fig. 12 shows the eye diagrams through the cylinder via and the proposed face via at a rate of (a) 3.2 Gbps and (b) 6.4 Gbps, respectively. It is apparent that the eye opening of the face via is improved quite a lot and the overshoot and undershoot have been decreased in the proposed via. With the face via, the eye heights are improved by 14% and 132% at a data rate of 3.2 and 6.4 Gbps, and the timing jitters are improved by 5% and 20%, respectively. The eye heights and timing jitters are summarized

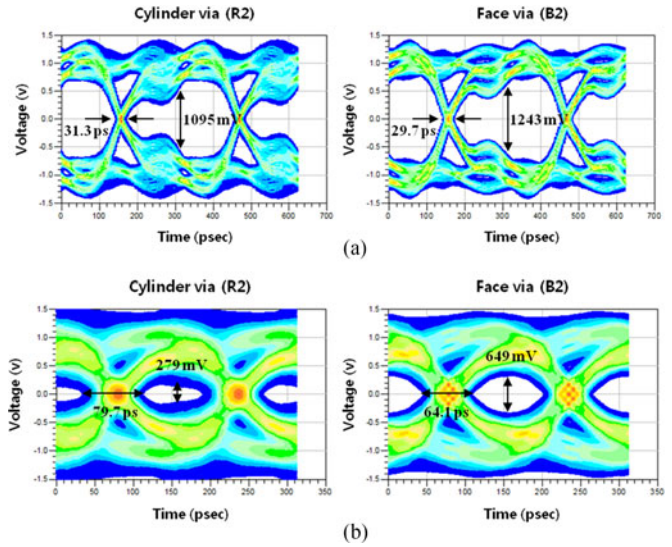

Fig. 12. Comparison of the eye diagram in the cylinder and face vias using the measured *S*-parameter at a data rate of (a) 3.2 Gbps and (b) 6.4 Gbps.

TABLE III
EYE DIAGRAM PARAMETERS OF THE CYLINDER AND FACE VIAS

Date Rate	Case ID	Via Type	Eye Height (mV)	Timing Jitter (ps)
3.2 Gbps	**R2**	Cylinder	1095	31.3
	B2	Face	1243	29.7
6.4Gbps	**R2**	Cylinder	279	79.7
	B2	Face	649	64.1

in Table III. The improvement in the eye diagram by employing the face via is clearly verified as the data rate increases. Based on the impedance measurement in TDR and the eye diagram analysis, it seems that the validity of the performance of the face via is successfully demonstrated.

V. APPLICATIONS OF THE FACE VIA

So far, the performance of the standalone face via has been discussed in the previous sections. In this section, the extended applications of the face via are described. The channel characteristics with multiple vias are investigated in the face and cylinder vias. The effects of the return ground vias are then analyzed to suggest a design guide for the PCB designers.

A. Analysis of a Large Number of Via Transitions

As the more components are integrated together into a small form factor system with increased signal complexities, signal traces are frequently routed through multiple vias [22]. For example, the address signal of a DDR4 un-buffered memory module which adopts fly-by topology penetrates several vias to interconnect dynamic random access memories [23]. Therefore, the effect of multiple via transitions in signal integrity needs to be analyzed.

Fig. 13 shows the designed and fabricated test vehicles with nine differential vias. The distance between differential vias is separated by 15 mm to be free from the influence of the

Fig. 13. Test vehicles for measurement for multiple (nine) via transitions. Top: cylinder via(R2) and bottom: face via(B2) with a face size of 1.25 mm.

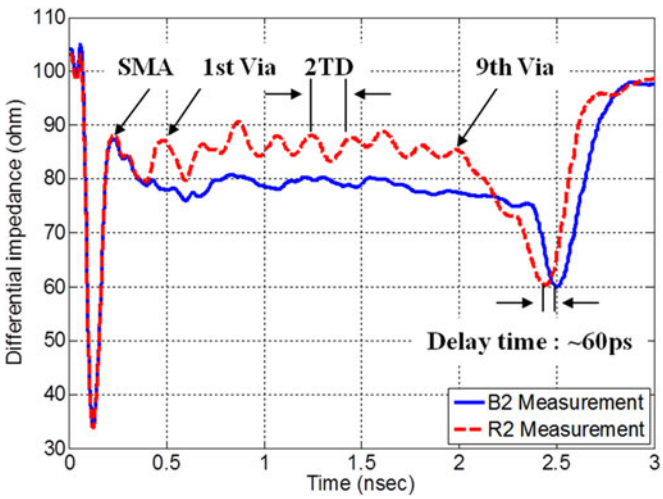

Fig. 14. Comparison of the measured TDR responses for multiple via transitions between the cylinder via and the face via.

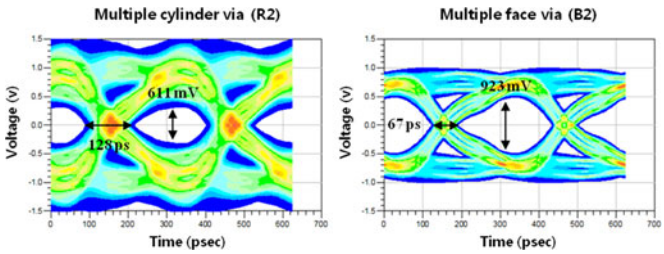

Fig. 15. Comparison of the eye diagram for multiple via transitions between the cylinder via and the face via using the measured *S*-parameter at 3.2 Gbps.

previous differential via and the traces are routed on the outer layers which mean that only full via transition is considered. The other design parameters, such as trace width, space, drill sizes, via distance, and stack-up, are identical to the parameters in the previous sections.

The measurement results of the TDR responses are described in Fig. 14. The TDR waveform of the conventional channel is composed of nine ridge-and-valleys coming from the nine vias for every two TD, where TD is the time delay of the distance between the two adjacent differential vias (15 mm). Note that the TDR waveform of the face via is almost flat because of the proposed face via. A 60ps time delay is observed in B2 in comparison with the signal in R2. This time delay is due to the increase in the capacitance and inductance in B2 in comparison with the data in R2, as shown in Table II.

TABLE IV
EYE DIAGRAM PARAMETERS OF THE CYLINDER AND FACE VIAS WITH MULTIPLE VIA TRANSITIONS (NINE VIAS)

Date Rate	Case ID	Via Type	Eye Height (mV)	Timing Jitter (ps)
3.2 Gbps	**R2**	Cylinder	611	128
	B2	Face	923	67

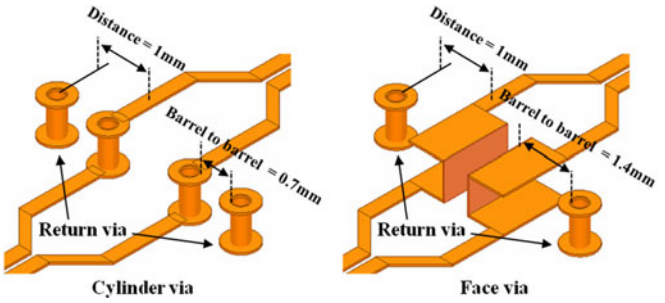

Fig. 16. Illustration of a conventional cylinder via and the proposed face via with return current vias: return via distance = 1.0 mm for both vias.

Fig. 15 presents the eye diagram for multiple via transitions using the measured *S*-parameter. With the PRBS input signal of 3.2 Gbps at the Tx of the conventional channel, an eye height of 611 mV and a timing jitter of 128 ps are observed at Rx, respectively. On the other hand, the eye height of 923 mV and a timing jitter of 67 ps are transmitted to Rx in the proposed face via channel. The eye diagram performances are summarized in Table IV. In summary, the reflected noises associated with the impedance mismatch are increased as the signal propagates through more vias. Therefore, it is concluded that the proposed via is more effective in the long channel with multiple via transitions.

B. Analysis of the Effect of Return Current Vias

With the advances in high-speed and high-density systems, a return current via is required for each signal via to achieve the high performance circuit. In order to investigate the influence of the return current vias, which usually improve the signal integrity, we added two ground vias around the signal vias in the EM simulation, as shown in Fig. 16. These ground vias provide low inductance paths for the returning currents [24].

Fig. 16 describes the geometrical via structures with return current vias in the EM simulation. All return current vias are located at the same distance from the center of the signal lines and the other design parameters are identical to the parameters in the previous sections. Fig. 17 shows the eye diagrams through the cylinder via and the face via at a rate of 6.4 Gbps (a) without and (b) with return current vias, respectively. The improvement of the eye height by adding the return current vias is 49 mV in the cylinder via and 34 mV in the face via. That is, the improvement caused by installing the return current vias around the conventional cylinder vias is larger than that around the face vias, in this specific example. The distance from the (center of the) signal line to the (center of the) return via is 1 mm in both cases, but note that the effective distance in the face

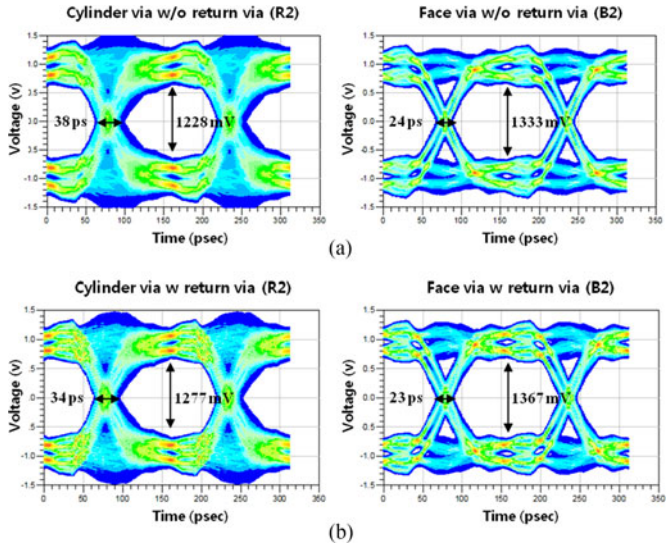

Fig. 17. Comparison of the eye diagram in the cylinder and face via using the simulated *S*-parameter at 6.4 Gbps (a) without and (b) with return current vias.

TABLE V
EYE DIAGRAM PARAMETERS OF THE CYLINDER AND FACE VIAS WITH AND WITHOUT RETURN CURRENT VIAS

Return Current Via	Case ID	Via Type	Eye Height (mV)	Timing Jitter (ps)
Not applied	**R2**	Cylinder	1228	38
	B2	Face	1333	24
Applied	**R2**	Cylinder	1277	34
	B2	Face	1367	23

via is farther than that in the cylinder via, which could make the return current via less effective. The eye diagram parameters are summarized in Table V. In summary, the return current vias are more effective in the cylinder via, but because of the intrinsic improvement of the face vias in the signal integrity, the eye opening in the face vias (1367 mV) became larger than the eye opening in the cylinder vias (1277 mV).

VI. CONCLUSION

In a high-speed digital system with a multilayer PCB, smooth transitions between the differential trace and the via are desirable to minimize the impedance mismatch because the impedance discontinuities cause signal reflections and deteriorate the signal integrity in differential signal channels. In this paper, we present a novel differential via structure, which is dubbed as face via, to control the via impedance. First, the EM simulation was performed to extract the *S*-parameters for both the conventional cylinder via and the proposed face via. And then the TDR responses were calculated using a circuit simulator, and found that a reflection-less face via can be designed by controlling the face size.

Based on the simulation results, test vehicles with an optimum face size were designed and fabricated. By measuring the TDR responses, the reflection-less performance of the face via for differential signaling was experimentally validated. To demonstrate the effectiveness of the face via considering the practical

application, channel simulations for multiple via transitions, and single via transition were performed using the measured *S*-parameters. The results show that the face via is more and more effective than the cylinder via as the data rate and layer transitions of the signal are increased.

Since only one additional process of drilling is required in the proposed face via and the enhancement in signal integrity is large as described in Section V, the proposed face via structure is expected to be extensively used for next-generation's high-performance digital systems, especially with the enhancement of the precise PCB fabrication technology.

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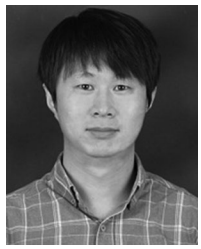

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