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COMPARATIVE MODELING OF SINGLE-ENDED THROUGH-SILICON VIAS IN GS AND GSG CONFIGURATIONS UP TO V-BAND FREQUENCIES

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Abstract—This work presents a novel comparative modeling scheme for single-ended (SE) through-silicon vias (TSVs) in GSG and GS configurations. Physical scalable models based on the equations developed herein indicate that the use of two symmetric ground TSVs in GSG configuration relatively increases the parasitic capacitance and conductance in the silicon substrate. However, this increase in the parasitic capacitance requires that the parasitic inductance of SE TSV is reduced to maintain the same phase velocity in silicon. According to the modeling results, the GSG configuration has a larger insertion loss than that of the GS configuration because the former has a higher substrate conductance. Nevertheless, when measured using RF coaxial probes, the GSG configuration exhibits a larger measurement bandwidth than the GS configuration. Finally, with the assistance of a double-sided probing system, wideband S-parameter measurement can validate the established equivalent-circuit model of SE TSV in GSG configuration up to V-band frequencies.

1. INTRODUCTION

The systematic development of electronic products in terms of their constituent components has increased the miniaturization, efficiency and integration of integrated circuit (IC) technologies, subsequently reducing their power consumption and simplifying assembly processes. The concept of a system has been elevated to that of "system-on-chip" (SoC). However, faced with challenges such as heterogeneous integration and driven by the pressure of time-to-market delivery

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for electronic products, component technologies have undergone a rapid transformation, i.e., from the use of SoC to the use of system-in-package (SiP), to achieve hardware integration. In particular, mobile communications applications, whose functions are increasingly complex yet whose sizes must not be increased, several emerging 3D SiPs (e.g., package on package (PoP), wire-bonded stacked chips and silicon interposer) have been extensively adopted in recent years [1, 2]. Among various 3D SiPs, silicon interposer is the most popular technology, which is expected to lead to an electronic system with a smaller size, higher operating frequency, and lower power consumption than those of conventional 2D SiPs. Undoubtedly, through silicon vias (TSVs) play a vital role in a silicon interposer to serve as a vertical interconnection between chips in a stacked structure [3]. TSVs reduce wire resistance and delay, thereby increasing transmission bandwidth. However, unlike planar interconnects, vertical interconnects such as TSVs often have a 3D metallization structure or pattern; in addition, their physical scalable models are more difficult to establish. Generally, modeling TSVs is still in its early stage of development for 3D SiPs. Most works have focused on the physical modeling of a single-ended (SE) TSV in the ground-signal (GS) configuration based on a two-wire transmission line theory [5–7]. However, results of the above studies are inapplicable for extending to the ground-signal-ground (GSG) configuration. Hence, in [8], the GSG configuration models that were directly extended from that of the GS configuration based on an expedient circuit arrangement rather than a rigorous electromagnetic (EM) theory. Moreover, owing to the limitations adopting a coplanar probing system, previous measurements on SE TSVs for model validation purpose have relied on a dual-TSV chain (TSV-line-TSV) test vehicle [6, 9–14]. Since the SE TSV has a considerably weaker parasitic effect than that of the planar lines that connect two SE TSVs, characterizing a SE TSV that requires de-embedding parasitic effects from the lines and the other SE TSV is rather difficult. Therefore, in most related works, the measured S-parameters or extracted equivalent-circuit parameters are associated with the entire test vehicle [6, 9–12]. Only a few works have involved a de-embedding operation to characterize the distributed parameters of a SE TSV in a GSG configuration up to 20 GHz [13, 14]. By using the double-sided probing system, our recent works have undertaken a direct measurement on a SE TSV in GS or GSG configuration [15, 16]. In those works, a hybrid EM and circuit model has been proposed to account for the measured S-parameters of the SE TSV in GSG configuration. However, scalability of the established model in terms of multiple geometry and material parameters is complex and time

consuming. Moreover, due to inadequate calibration capability, the measured data can validate the modeled results only up to Q-band frequencies where the silicon substrate effect is mainly conductive rather than capacitive. This work makes significant progress in correlating an analytical model with measurement data for SE TSVs in the GSG configuration over an extremely wide frequency range. The proposed modeling approach superimposes the potential differences between TSVs to evaluate the silicon substrate capacitance in terms of the pitch-to-diameter ratio of TSVs and the angle between the two ground TSVs to the signal TSV. Consequently, the silicon substrate capacitance in the GSG configuration increases relative to the GS configuration, causing the inductance of SE TSV in the GSG configuration to decrease relative to the GS configuration in order to maintain the same phase velocity in silicon. Finally, via the double-sided probing system, the two SE TSV configurations GS and GSG are measured with S-parameters to validate their comparative modeling results. Despite the common Short-Open-Load-Thru (SOLT) method of full two-port calibration, no standard thru-kit is available. Alternatively, a direct (probe-tip) contact is performed between the two RF coaxial probes. Along with these efforts, the measured S-parameters agree quite closely with the modeled results over the applicable frequency range of the probes. The maximum frequency range of agreement is from DC to V-band frequencies, which, to our knowledge, is the highest frequency range for the model of an isolated SE TSV with measurement verification.

2. PHYSICAL SCALABLE MODEL OF A SE TSV

Figure 1 shows the cross section and equivalent circuit of a SE TSV in GSG configuration with a pitch p between the signal and ground TSVs. TSVs, which are made of copper, have a conductivity of σ_c, and are cylindrical with a diameter of d and a height of h, and they are formed by etching through the silicon substrate with permittivity ε_{si}, conductivity σ_{si} and loss tangent $\tan\delta_{c,si}$. To prevent high dc resistance due to the direct contact of TSVs with the silicon substrate, a thin oxide film with a thickness of t_{ox} and permittivity of ε_{ox} is grown around the surface of the TSVs for isolation. Table 1 lists the important material and thickness parameters. In a physical equivalent circuit of a SE TSV (Figure 1), L_s and R_s denote the inductance and resistance of SE TSV, respectively; C_{ox} represents the capacitance associated with the thin oxide film between TSV and silicon substrate; and C_{si} and G_{si} refer to the capacitance and conductance of silicon substrate, respectively. Next, an attempt is made to find the silicon

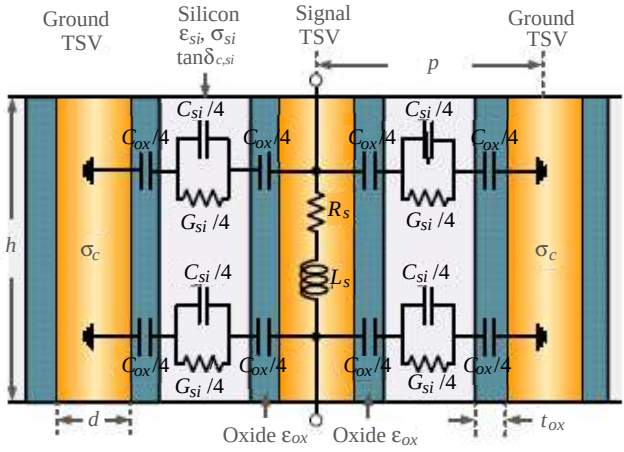


Figure 1. Physical modeling of a SE TSV in GSG configuration.

Table 1. Physical parameters of the studied TSVs.

Parameter	Value	Description
σ_{si}	11.5 S/m	Conductivity of silicon
σ_c	5.96×10^7 S/m	Conductivity of copper
ε_{si}	1.054×10^{-10} F/m	Permittivity of silicon
ε_{ox}	3.453×10^{-11} F/m	Permittivity of oxide
$\tan \delta_{c,si}$	0.05	Loss tangent of silicon
d	50 μm	Diameter of TSV
h	100 μm	Height of TSV
t_{ox}	0.6 μm	Thickness of oxide layer
p	250/500 μm	Pitch between two TSVs

substrate capacitance C_{si} by placing a three-wire transmission line, which consists of three identical cylindrical conductors with diameter d, in a space filled with silicon (Figure 2). The three conductors (i.e., A, B and C), are the first ground conductor, signal conductor and second ground conductor of the three-wire transmission line, respectively. Where p denotes the pitch between the signal and each ground conductor. An angle θ is formed between the two ground conductor centers and the signal conductor center. Under excitation, the sum of charges on the three conductors is zero. If the signal

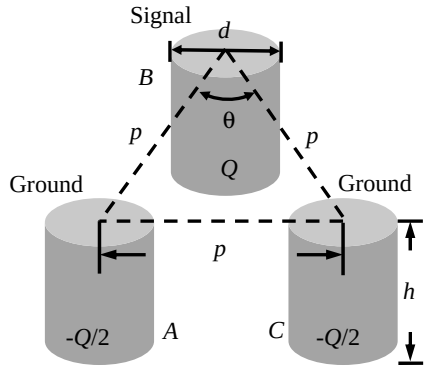


Figure 2. Three-wire transmission line with an angle θ between the two ground conductor centers to the signal conductor center.

conductor B has a charge of Q, then each ground conductor A and C, which are identical, has a charge of $-Q/2$. Assume that the pitch-to-diameter ratio is sufficiently large to disregard the offset distance of the equivalent image line charges from the center cylindrical axis. Superimposed by the potentials of the equivalent image line charges of the three conductors, the potential difference from conductor B to conductor A is derived as

$$V_{BA} \approx \frac{1}{2\pi\varepsilon_{si}h}\left[-\frac{Q}{2}\ln\left(\frac{d}{2p}\right)+Q\ln\left(\frac{2p}{d}\right)-\frac{Q}{2}\ln\left(2\sin\frac{\theta}{2}\right)\right] \quad (1)$$

The capacitance of the three-wire transmission line can be obtained by dividing charge by potential difference, which is written as

$$C_{si,GSG}=\frac{Q}{V_{BA}}\approx\frac{4\pi\varepsilon_{si}h}{3\ln\left(\frac{2p}{d}\right)-\ln\left(2\sin\frac{\theta}{2}\right)} \quad (2)$$

The above equation is compared with the well-known expression of two-wire transmission line as follows:

$$C_{si,GS}=\frac{\pi\varepsilon_{si}h}{\cosh^{-1}\left(\frac{p}{d}\right)} \quad (3)$$

With the assistance of the Ansys-Ansoft Q3D extractor, the value of $C_{si,GSG}$ can also be extracted from a reduced capacitance matrix. Therefore, Figure 3 plots the normalized capacitance C_N, which equals the division of (2) by (3) as a function of the pitch-to-diameter ratio p/d and the intersection angle θ. The theoretical predictions agree

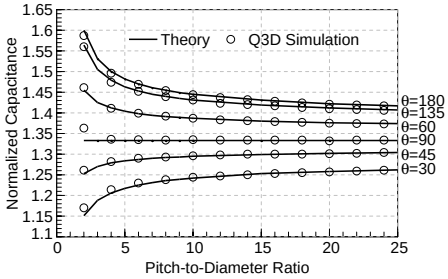


Figure 3. Comparison of the normalized capacitance of three-wire transmission.

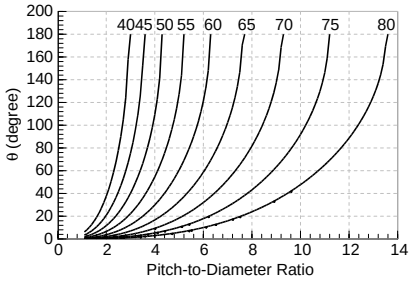


Figure 4. Root loci of constant characteristic impedances for a three-wire transmission line in an ideally lossless and homogeneous silicon medium.

very well with the Q3D simulation results, except for some deviations appearing at the low p/d values where the derived capacitance formula is beyond its applicable range. According to Figure 3, the normalized capacitance increases with θ. Additionally, this capacitance increases or decreases with p/d, depending on whether θ is smaller or greater than 60°. Consider a homogeneous medium in which a TEM mode propagates along a transmission line. Square root of the product of the inductance and capacitance equals the propagation time delay which is given by $\sqrt{\mu_0 \varepsilon_{si}} h$. Thus, the inductance of TSVs can be determined as

$$L_s = \frac{\mu_0 \varepsilon_{si} h^2}{C_{si}} \tag{4}$$

Therefore, the characteristic impedance of a three-wire transmission line in an ideally lossless and homogeneous silicon medium can be written in relation to that of a two-wire transmission line as follows:

$$Z_{0si,GSG} = \frac{Z_{0si,GS}}{C_N} \approx \frac{1}{C_N \pi} \sqrt{\frac{\mu_0}{\varepsilon_{si}}} \cosh^{-1} \frac{p}{d} \tag{5}$$

Figure 4 shows the root loci of the constant $Z_{0si,GSG}$ values, indicating that a smaller ratio of p/d allows for the use of a smaller angle θ to achieve the same constant impedance. For the special case of $\theta = 180°$, the ratio of $p/d = 5$ and 10 results in a $Z_{0si,GSG}$ of 54 Ω and 72 Ω, which are close to the standard impedance of 50 Ω and 75 Ω, respectively. Such an angle θ, in combination with two different p/d ratios, are used in later SE TSV examples to correlate between theory and experiment. The silicon substrate conductance is proportional to the silicon substrate capacitance, subsequently yielding the following

form [17]:

$$G_{si} = \left(\frac{\sigma_{si}}{\varepsilon_{si}} + \omega \tan \delta_{c,si} \right) C_{si} \tag{6}$$

Next, consider the skin effect, in which the conductor resistance can be expressed as

$$R_s = \begin{cases} k \cdot \dfrac{h}{\sigma_c \pi \delta (d - \delta)}, & \text{for } \delta < d/2 \\ k \cdot \dfrac{h}{\sigma_c \pi (d/2)^2}, & \text{for } \delta > d/2 \end{cases} \tag{7}$$

where

$$\delta = \sqrt{\frac{2}{\omega \mu_0 \sigma_c}} \tag{8}$$

is the skin depth of the conductor, and k equals 1.5 and 2 for the GSG and GS configurations, respectively. Finally, the oxide capacitance is found based on a coaxial capacitor [6] and expressed as

$$C_{ox} = \frac{2\pi \varepsilon_{ox} h}{\ln \left(1 + \dfrac{2t_{ox}}{d} \right)} \tag{9}$$

The complex characteristic impedance of SE TSV with consideration of the dissipative loss and the oxide capacitance effect can be expressed

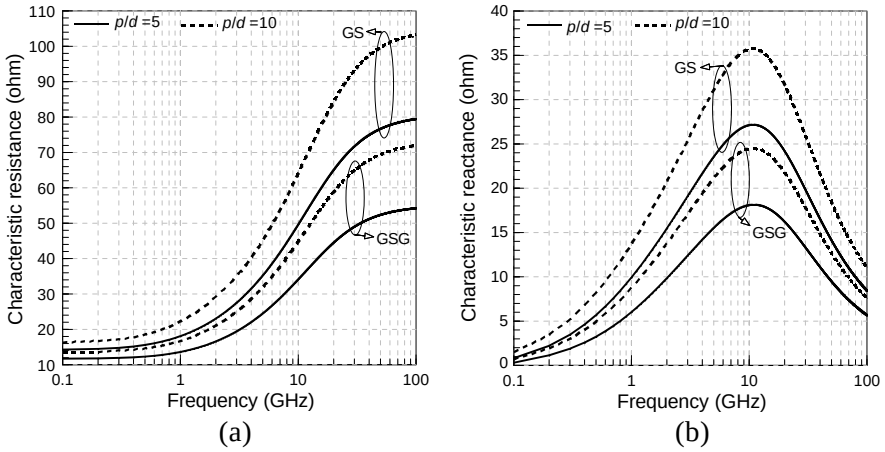


Figure 5. Complex characteristic impedance of SE TSVs in the GS and GSG configurations with $\theta = 180°$. (a) Characteristic resistance R_0. (b) Characteristic reactance X_0.

in terms of the equivalent-circuit parameters as

$$Z_0 = R_0 + jX_0 = \sqrt{\frac{R_s + j\omega L_s}{G_{si} + j\omega C_{si}}} \cdot \sqrt{1 + \frac{2C_{si}}{C_{ox}} + \frac{2G_{si}}{j\omega C_{ox}}} \qquad (10)$$

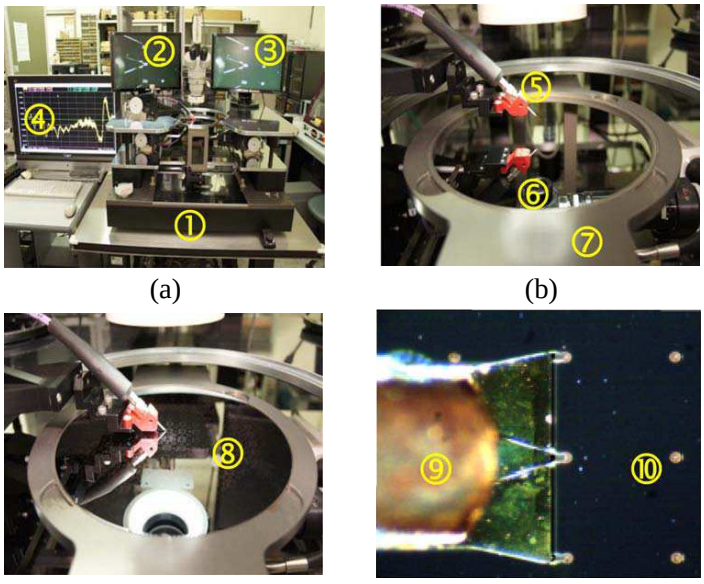
where Figures 5(a) and 5(b) show the real part R_0 and imaginary part X_0, respectively, for the studied SE TSVs in GSG ($\theta = 180^\circ$) and GS configurations. The frequency-dependent property of Z_0 can be explained by dividing the dielectric effect into three categories. The first one is dominated by the effect of oxide capacitance at low frequencies (below several hundreds of MHz); the second one is attributed to the effect of silicon resistance at middle frequencies (from several hundreds of MHz up to tens of GHz); and the last one is mainly due to the effect of silicon capacitance at high frequencies (above tens of GHz). Figures 5(a) and 5(b) reveal that Z_0 approximates a real constant value in the frequency ranges of the first and last categories, whereas it varies greatly with frequency and has a large imaginary component in the frequency range of the second category.

3. MEASUREMENT SETUP AND CALIBRATION

Conventional probing systems have been developed for measuring the signals on the coplanar input/output (I/O) pads of a device under test (DUT) [18]. Therefore, a DUT with I/O terminals on different metal layers generally counts on a back-to-back interconnection to form coplanar test pads for adaptation to the probing system. However, measuring SE TSVs requires tremendous efforts in de-embedding, which is both time consuming and prone to inaccuracy.

To measure 3D interconnects, this work develops a novel double-sided probing system [19], as shown in Figure 6(a), to facilitate the calibration and measurement procedures for a DUT with the test pads on opposite side of a substrate. The probe station of this system uses a sandwich-like holder with a hole in the center of its top and bottom plates, as shown in Figure 6(b), to grip the silicon interposer under testing. This setup allows for access of the top and bottom probes to the opposite terminals of the TSVs that are distributed across the silicon interposer, as shown in Figure 6(c). Figure 6(d) shows a top view of measuring a SE TSV in the GSG configuration with a pair of GSG-type probes.

Owing to the lack of a well-defined thru standard in the proposed double-sided measurement method of SE TSV, our earlier works [15, 19] adopted a short-open-load-reciprocal (SOLR) calibration method to calibrate the vector network analyzer and the probes to ensure the S-parameter measurement accuracy. Theoretically, the

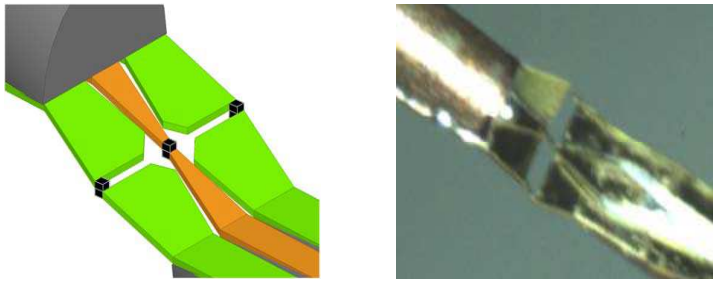


(a) (b)

(c) (d)

Figure 6. Double-sided probing system. (a) Front view of system. (b) Top and bottom probes used in the system. (c) TSV wafer probing. (d) Top view of TSV probing. (① Double-sided probe. station ② Top side display. ③ Bottom side display. ④ VNA display. ⑤ Top probe. ⑥ Bottom probe. ⑦ DUT holder. ⑧ Silicon interposer. ⑨ GSG-type probe. ⑩ TSV.).

SOLR calibration method allows for the use of an undefined reciprocal thru standard to perform the calibration [19, 20]. However, calibration bandwidth is often limited by the crosstalk levels between the top and bottom probes since the SOLR procedure does not include the calibration of forward and reverse isolation, which is required in the SOLT method. To increase the calibration bandwidth, this work reconsiders the short-open-load-thru (SOLT) calibration method and attempts to solve the problem of a thru standard. Open, short and load calibrations are first performed with the assistance of a double-sided (back-to-back) impedance standard substrate (ISS). According to Figure 7, thru calibration is then performed by direct contact between the top and bottom probe tips in the absence of the silicon interposer. In this manner, an equivalent thru standard can be set as a lossless and zero-delay line in its standard definition. Importantly, this thru calibration needs great care because an overpressure contact of the



(a) (b)

Figure 7. Illustration of the direct contact between the upper and lower probes as a thru kit. (a) 3-D geometry. (b) Photograph.

probe tips may cause non-recoverable deformation.

Figures 8(a) and 8(b) compare the magnitude and phase, respectively, of the measured S_{21}-parameter of a SE TSV between the SOLR and SOLT methods. SE TSV is in a GSG configuration with a diameter of 50 µm and a pitch of 250 µm. According to Figure 8(a), the magnitude of S_{21} rises abnormally beyond 20 GHz for the SOLR method. As mentioned earlier, this abnormality is mainly due to the uncalibrated crosstalk results between two (top and bottom) probes. Conversely, the SOLT method is free from this calibration error and, therefore, can greatly enhance the calibration bandwidth to obtain accurate S-parameter measurement results up to the applicable frequency range of the probes.

4. RESULTS AND DISCUSSION

Accuracy and scalability of the proposed SE TSV model are confirmed by taking four measurements on the following SE configurations of 50-µm diameter TSVs: GSG with $p/d = 5$ and $\theta = 180°$, GS with $p/d = 5$, GSG with $p/d = 10$ and $\theta = 180°$, and GS with $p/d = 10$ by using GSG and GS probes with the same pitch as that of the SE TSVs. Furthermore, these measurements are compared to the simulations from the established SE TSV model as well as the full-wave EM simulation software, HFSS. Notably, for a GSG configuration with a p/d of 5 and 10 at $\theta = 180°$, the silicon capacitance (C_{si}) is 1.48 and 1.45 times, respectively, larger than that in GS configuration, as estimated from Figure 3.

In the experiment, the probes used are equipped with 1.85 mm coaxial connectors that have a specification of maximum 67-GHz bandwidth. Moreover, their applicable bandwidth also depends on the type (GSG or GS) and pitch of probes. The GSG probe generally

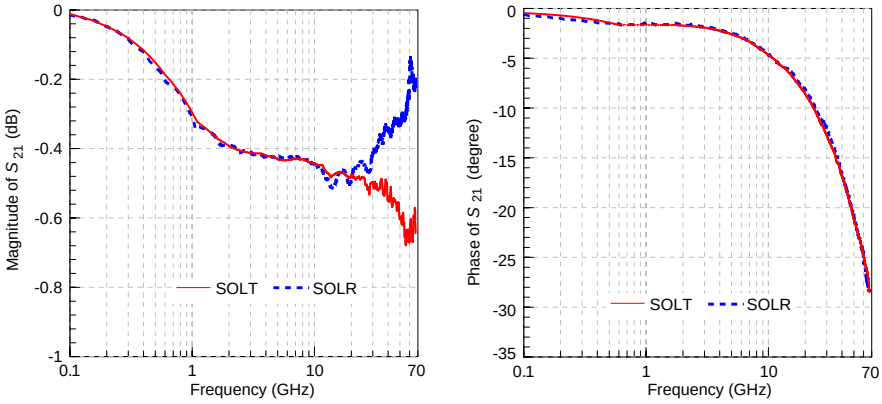


Figure 8. Comparison of the S_{21}-parameter measurement results between SOLT and SOLR calibration methods for the GSG configuration of TSV with $p/d = 5$. (a) Magnitude. (b) Phase.

has a higher bandwidth than the GS one. For both probe types, a smaller pitch implies a higher bandwidth [22]. After SOLT calibration is performed, the double-sided probing system can provide a direct S-parameter measurement of SE TSVs up to the applicable frequency limit of the probes.

Figures 9(a) and 9(b) compare the Magnitude of S_{21} among the proposed model, HFSS simulation and measurement for the SE TSV in GSG and GS configuration, respectively, with p/d equal to 5. For the GSG configuration, the measured data correlate well with the modeled and HFSS simulated results over the applicable frequency range of the 250-µm GSG probe, which reaches 67 GHz. However, due to the applicable frequency limit of the 250-µm GS probe, the measured results for the GS configuration validate the predictions from modeling and EM simulations only up to 20 GHz. In a similar fashion, Figures 9(c) and 9(d) compare the S-parameters resulting from different approaches for the SE TSV in GSG and GS configuration, respectively, with p/d equal to 10. Again, the comparison of measurements with predictions from modeling and EM simulation reveals a satisfactory correlation over the applicable frequency range of the 500-µm GSG probe and 500-µm GS probe, which is up to 45 and 8 GHz, respectively. Notably, for all SE TSV configurations, the modeled and HFSS simulated results closely correspond to each other over the entire studied frequency range.

According to the S-parameter results shown in Figures 9 and 10,

the frequency responses of SE TSVs can be categorized into three regions: MOS dispersion, silicon leakage and silicon propagation. Figures 9 and 10 plot the magnitude and frequency axes in dB/log-log format to illustrate these three frequency regions more clearly. The MOS dispersion region is at low frequencies (e.g., less than several GHz), where the substrate effects are dominated by a MOS capacitor structure that can be represented by an equivalent series circuit of oxide capacitance (C_{ox}) and substrate conductance (G_{si}). In this region, a strong dispersion is observed in the phase of S_{21}-parameters, which is caused mainly by RC time-constant effects. Therefore, the dispersion can be improved by increasing the oxide film thickness to

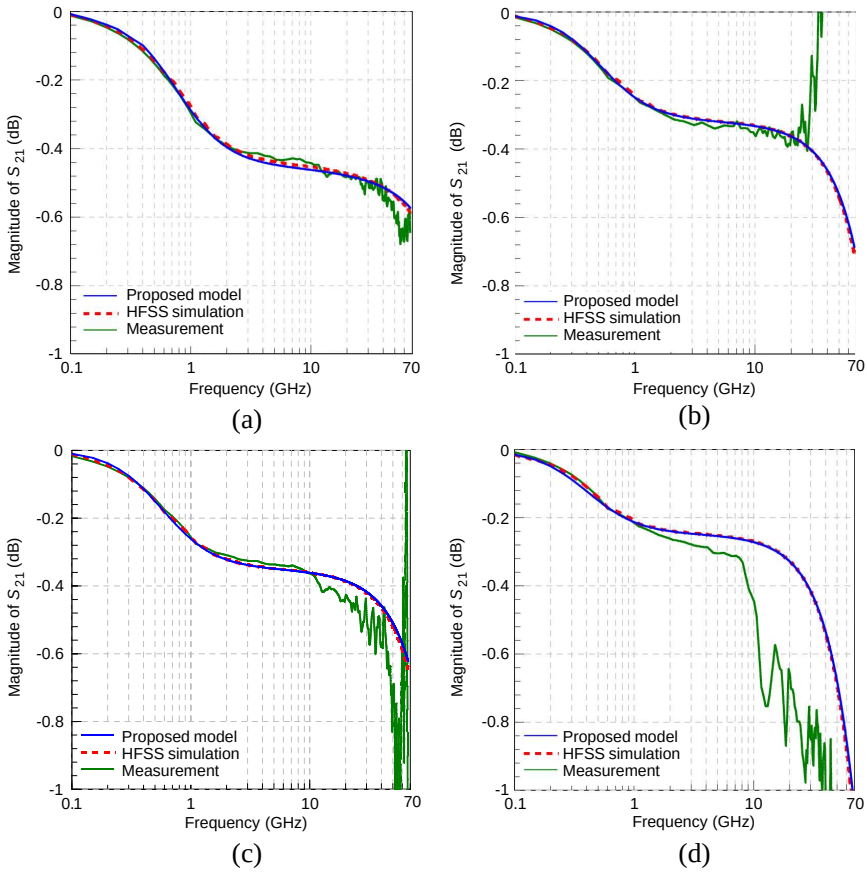


Figure 9. Comparison of the Magnitude of S_{21} among proposed model, HFSS simulation and measurement. (a) $p/d = 5$, GSG. (b) $p/d = 5$, GS. (c) $p/d = 10$, GSG. (d) $p/d = 10$, GS.

reduce the oxide capacitance. Alternatively, the TSV MOS capacitor can be biased to operate at a depletion mode to obtain a smaller effective capacitance. The silicon leakage region is located in the middle frequency range (i.e., from several to ten several GHz), where the substrate effects are mainly dissipative owing to the silicon conductance (G_{si}). In this region, the insertion loss has a low frequency dependence and can be reduced by using a high resistivity silicon substrate, Moreover, making the silicon capacitance (C_{si}) smaller also helps to reduce the insertion loss because C_{si} is in proportion to G_{si} according to (6).

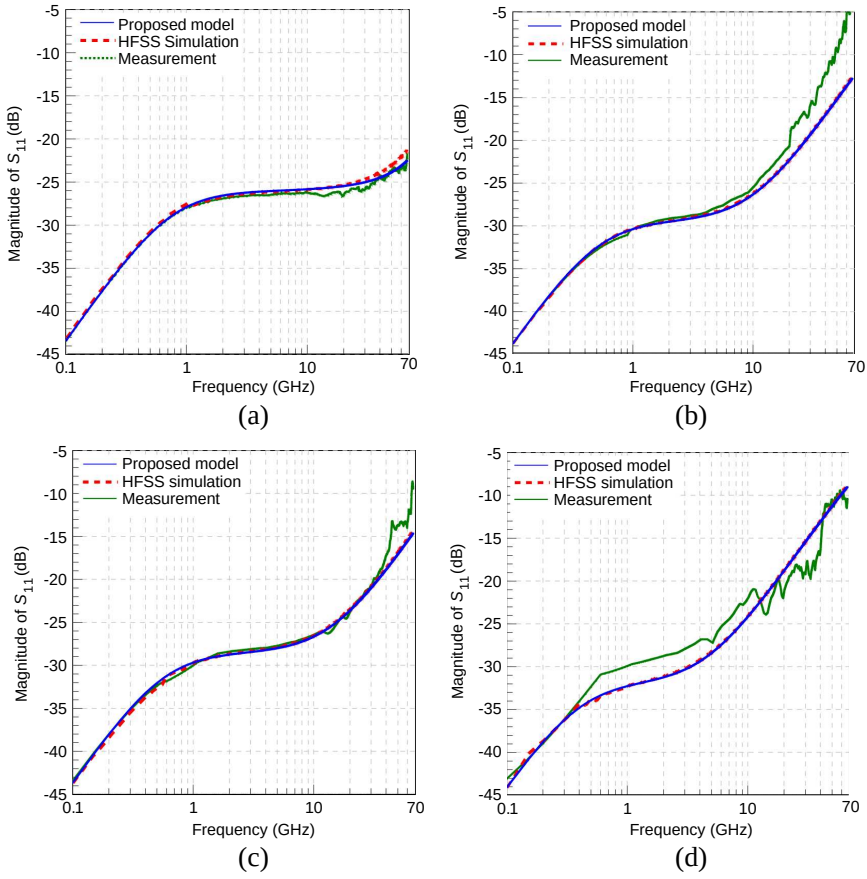


Figure 10. Comparison of the Magnitude of S_{11} among proposed model, HFSS simulation and measurement. (a) $p/d = 5$, GSG (b) $p/d = 5$, GS. (c) $p/d = 10$, GSG. (d) $p/d = 10$, GS.

The silicon propagation region is at high frequencies (i.e., above ten several GHz), where the electromagnetic field of a SE TSV mainly concentrates and propagates in the silicon substrate. The behavior of such substrate effects can be represented by an equivalent parallel circuit of silicon capacitance (C_{si}) and silicon conductance (G_{si}). Owing to the impedance mismatch, a low-pass filter effect on the insertion loss is often observed in this region. Therefore, an effort to improve impedance matching through the control of characteristic impedances, as shown in Figures 5(a) and 5(b), can push the cutoff frequency to higher frequencies.

Comparing the results in Figures 9 and 10 with the same p/d ratios reveals that SE TSV in the GSG configuration exhibits a higher insertion loss in the silicon leakage region than that in GS configuration because the silicon capacitance of the former structure is generally larger than that of the latter structure. However, in the silicon propagation region, the former structure has a smaller impedance mismatch than the latter one, leading to a higher cutoff frequency for the low-pass filter effect on the insertion loss. Obviously, selecting GSG or GS configurations for a SE TSV forms a tradeoff between the loss in middle-frequency region and the loss in the high-frequency region.

5. CONCLUSION

This work presents a fully analytical model for a SE TSV in GSG configuration. The proposed model offers great scalability in terms of TSV physical parameters. Moreover, via the double-sided probing system, the proposed model is validated using measured S-parameters up to the applicable frequency limit of the probes which at maximum reaches V-band frequencies. For the studied SE TSVs with the same pitch-to-diameter ratio, the GSG configuration has a larger silicon capacitance than the GS configuration, causing a higher dielectric leakage loss in the middle-frequency region yet a lower mismatch loss in the high-frequency region.

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