DesignCon® 2015

Package Simulations For Mitigating Noise Coupling Onto Sensitive RF signals

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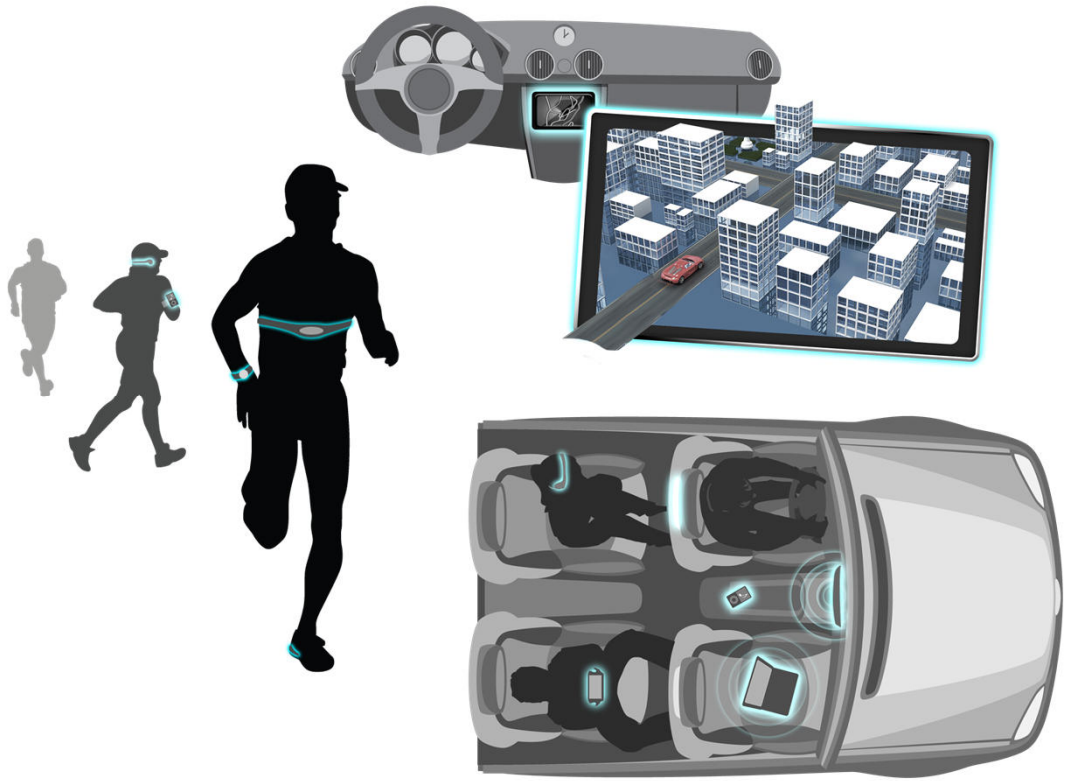
Agenda

- Introduction
- Hazard identification
- Model extraction
  - Pre layout location estimation
  - Coupling mechanisms
  - Layout modifications
  - Production layout extraction
- Model simulation
  - Spice setup
  - Simulation transient length
  - Toggling pattern
  - Tuning drive strength
- Conclusion

Modern SoC trend

- Recent trend is to integrate RF interfaces into a large SoC.
- Internet of Things
  - Bluetooth Low Energy
- Wearable technology
  - Bluetooth
- Connectivity on the move
  - Wi-Fi
- Navigation
  - GNSS

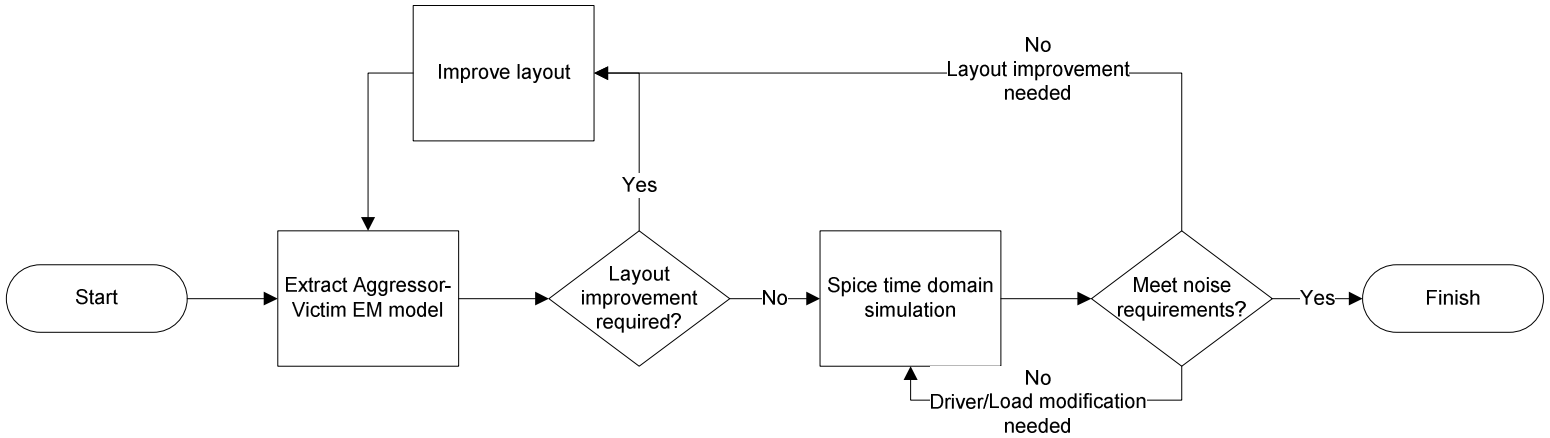


Why this workflow is needed?

- There is a need for robust integration of RF technologies into the SoC.
- Wireless interfaces are influenced to a great extent by digital noise which can couple onto the RF signals.
- Analyzing and understanding the noise coupling mechanism in an IC package.
- Presenting ways to minimize the noise once it is found to be out of spec.
- Successful noise coupling simulations reduce DIE and package manufacturing iterations and minimize lab validation time.

Workflow overview

- Identification of potential aggressors.
- Model extraction and layout improvement.
- Spice simulation and system tuning for optimal performance.

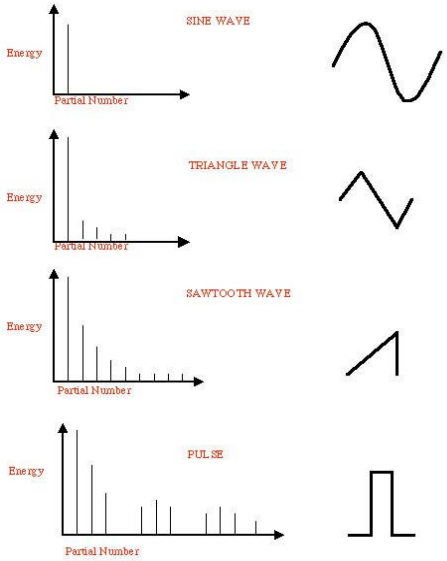


Who can act as an aggressor?

- On early stages of design work there is a need to identify potential hazards to RF interface.
- Interfaces operating at frequencies with harmonics at RF band.
- Interfaces operating at high frequencies with high dI/dt.

$$V_{noise} = M \cdot \frac{dI}{dt}$$

- Interfaces in proximity to the victim RF interface.
- Interfaces with wide busses driving large amounts of charge.



The victim

- In this work, the interface which is subjected to this methodology is Bluetooth.
- All package improvements should be made up to this point of domain intersection, in order to enable us to re-use the designed RF IP in other packages.
- Bluetooth receiver SNR requirements dictate the maximum digital noise level. The Bluetooth band is 2400-2483MHz and a single channel is 1 MHz wide.
- Noise budget calculations show that a maximum of -119dBm/MHz of digital noise is permitted per channel. The permitted maximum out of band digital noise is -27dBm.

$$P_{N\,coupled\,[dBm]} = 10\log\left(P_{N\,[mW]}\right) = 10\log\left(\frac{\left(V_{RFsig[V]} - V_{RFref\,[V]}\right)^2}{Z_{antenna}} \cdot 1000\right)$$

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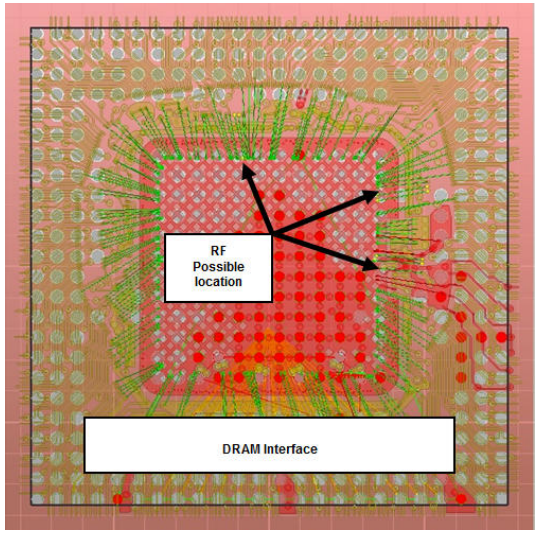
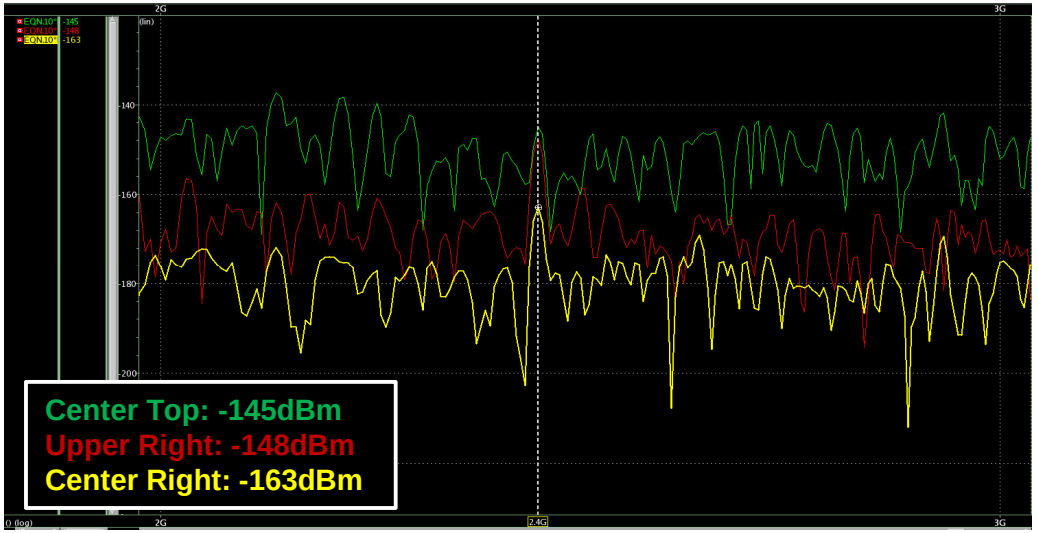
Locating the widest aggressor

- DRAM interface as the widest and the fastest interface will dictate IC's floor-plan.

- DRAM populates entire side of IC. The victim can be located either on the opposite side of the die to the DRAM or on an adjacent side.





2nd aggressor, LCD

- Faraday's law states, that the magnetic flux through the wire loop is proportional to the number of magnetic flux lines that pass through the loop.

$$\Phi_B = \iint_{\Sigma} B(r,t) \cdot dA$$

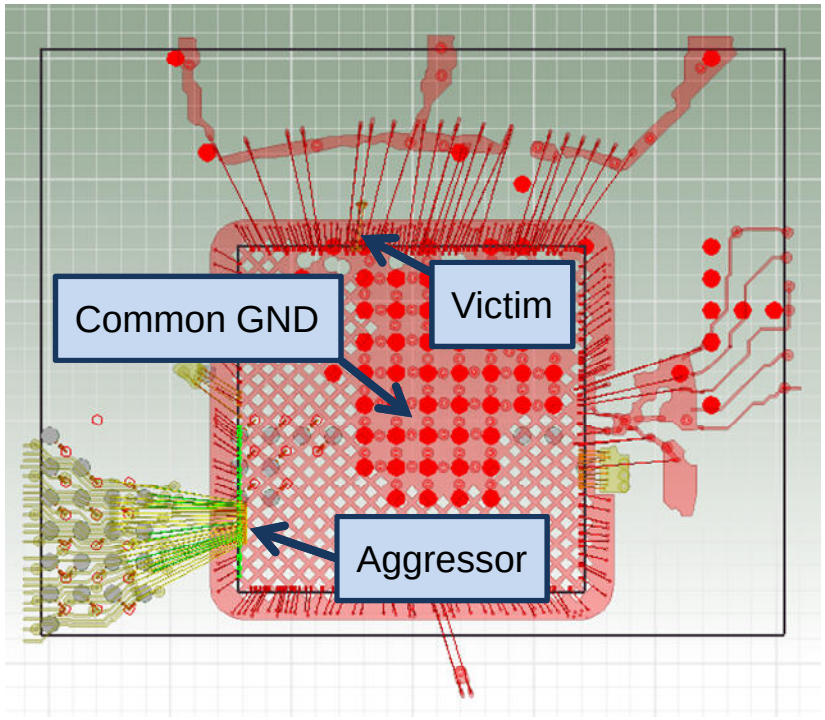
- Locating LCD, the next widest and fastest interface after DRAM should be on adjacent die side to the victim.

- The LCD interface has 30 digital signals, operates at clock frequency of 150MHz and single data rate.

- 2 LCD harmonics may be found in Bluetooth band, at 2400MHz and 2475MHz.

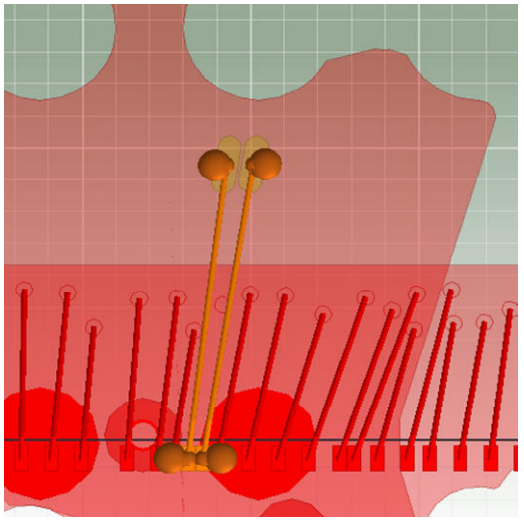
Pre layout location estimation

- Using previous project package with same technology, we estimated location of RF interface (Victim) and LCD interface (Aggressor).



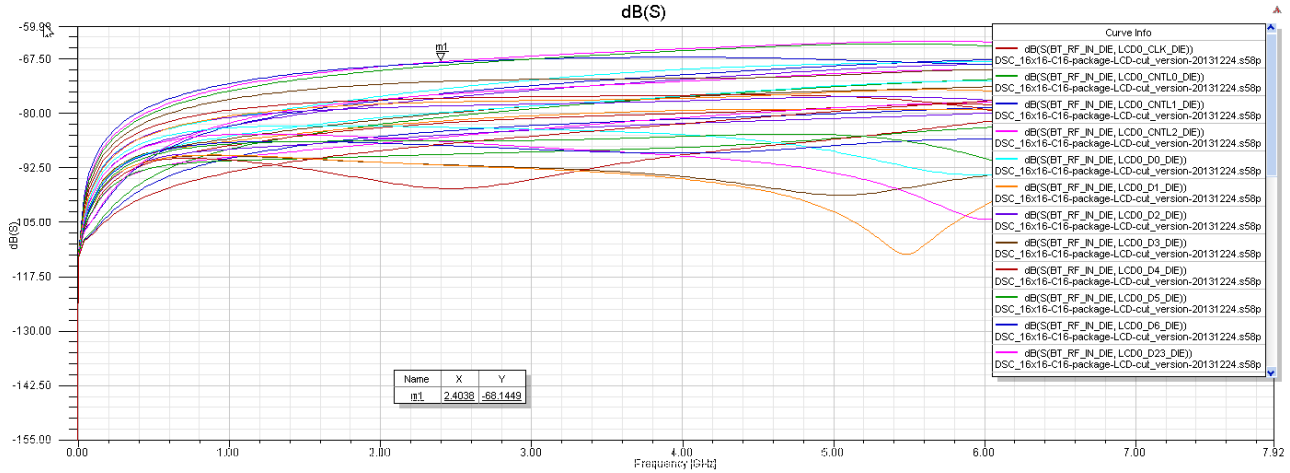
Extraction setup

- Package type is Wire-Bond Ball Grid Array (WB-BGA).
- For the aggressor extraction ports defined at the die pads of each wire-bond and another set of ports at the package balls.
- Victim ports were defined on both sides of the RF signal and RF reference wire-bonds.
- Assuming that victims routing path from wire-bond to the antenna will be a 50 ohm shielded transmission line.
- Perfect Electric Conductor is places under the package to imitate the ground plane on a multi-layer Printed Circuit Board (PCB)



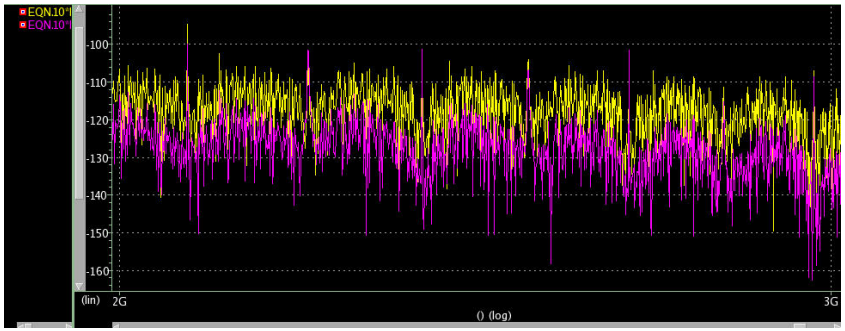
Estimated insertion loss

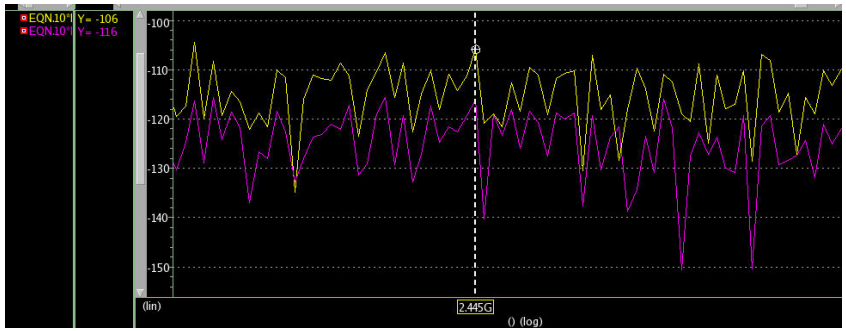
- Observing the generated S-parameters, the minimum isolation received at 2.4GHz is 68dB.
- This is a relative value rather than absolute one and the exact coupled noise cannot be derived from this value.
- To obtain the exact level of coupled noise, a SPICE simulation is required.



Estimated noise level simulation

- An equivalent RLC circuit model is generated and simulated in the SPICE circuit simulator.
- On the left hand side, a 150MHz cyclic pattern of peaks and troughs can be observed as expected for an interface operating at 150MHz. On the right side, a zoomed-in area around the peak noise in the RF band is displayed.
- At a drive strength that will ensure proper interface functionality, peak noise of -106dBm/MHz is observed at 2.445GHz.





Coupling mechanisms

- 2 major mechanisms cause the noise to couple onto the victim.

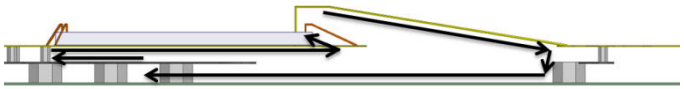
- Inductive coupling:
  - Aggressor wire-bonds act as radiating antennas.
  - Victim wire-bonds act as receiving antennas.
  - Minimizing aggressor current loops and by that decreasing magnetic flux, can reduce noise on victim.

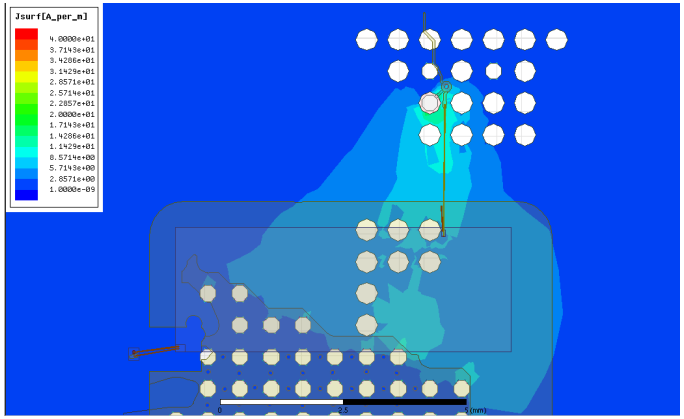
- Capacitive coupling:
  - Although return currents strive to reduce loop inductance, there is still a spread of currents across entire reference plane.
  - These currents cause ground bounce and through parasitic capacitors couple onto the victim.
  - Avoiding laying-out of conductors common to aggressor and victim can reduce noise on victim.

Reducing Fringe fields – Standard design

- WB-BGA design guidelines state that signals should be connected to periphery balls to allow PCB breakout and routing.

- GND wire-bonds should be connected to a common GND plane in the package core region, to short the wire-bonds and reduce GND inductance for PI.

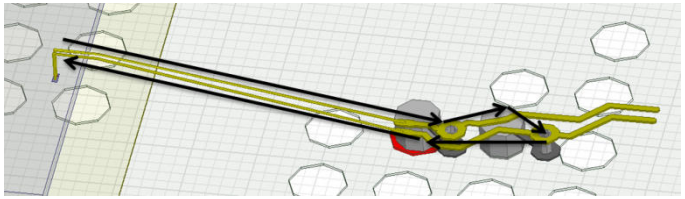


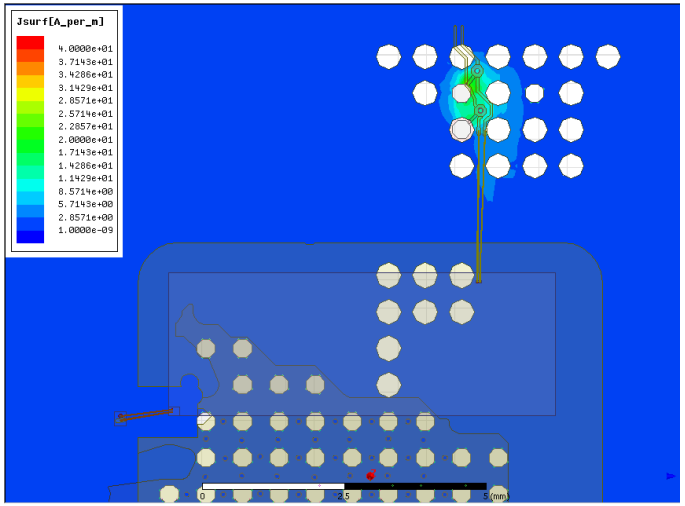


Reducing Fringe fields – Minimal current loop design

- Reducing current loop to its minimum can be achieved by placing the GND wire-bonds and GND balls as close as possible to the signal.

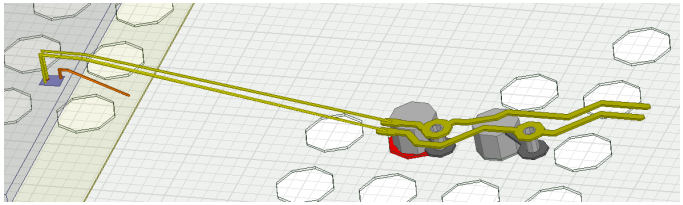
- On the other hand, this arrangement of GND routing is the worst possible in terms of PI.

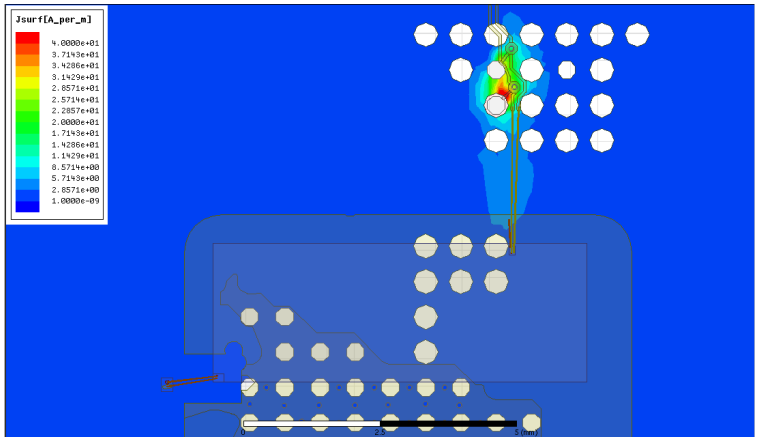




Reducing Fringe fields – Trade Off

- Adding several long profile GND wire-bonds routed to the periphery of the package to minimize current loops.
- Retaining the short profile GND wire-bonds for good PI.
- Extra IO pads and complex package design.

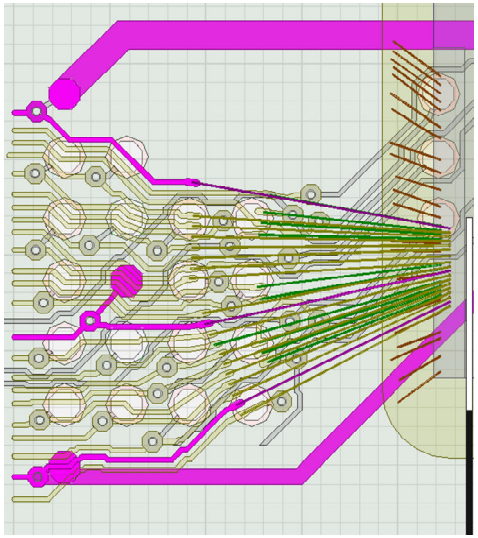


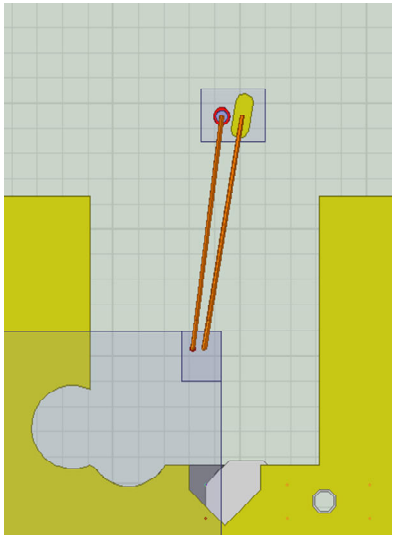


Testing suggested changes

- Perforating common reference plane underneath victim wire-bonds.
  - Reducing capacitive coupling.

- Adding long profile wire-bonds and current sinks at aggressor side.
  - Minimizing current loops.

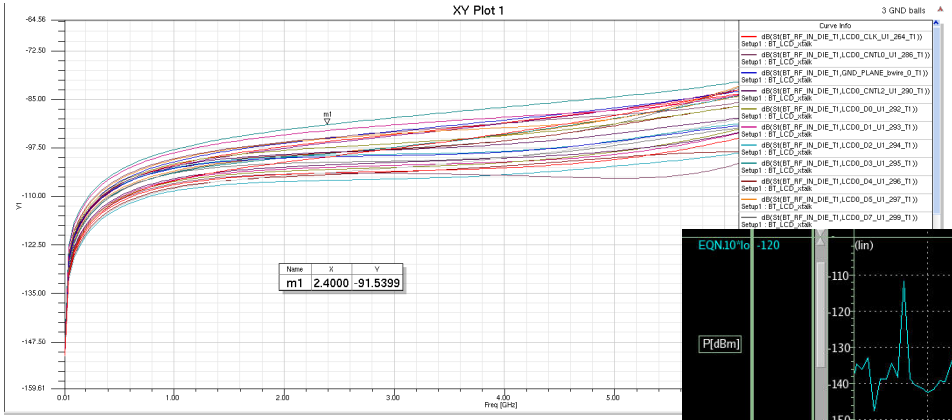


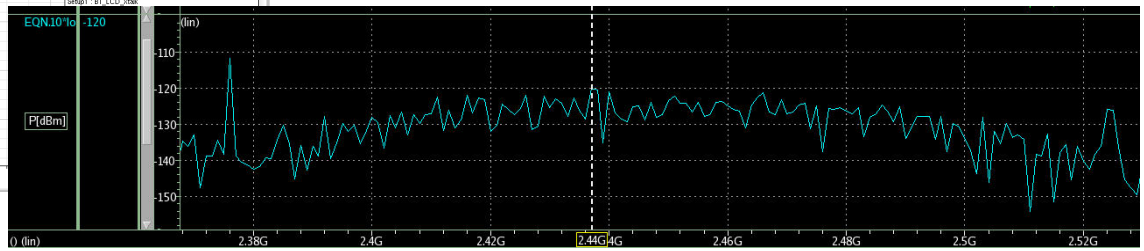


Test design noise level simulation

- Implementing all suggested changes and running extraction and simulation again.

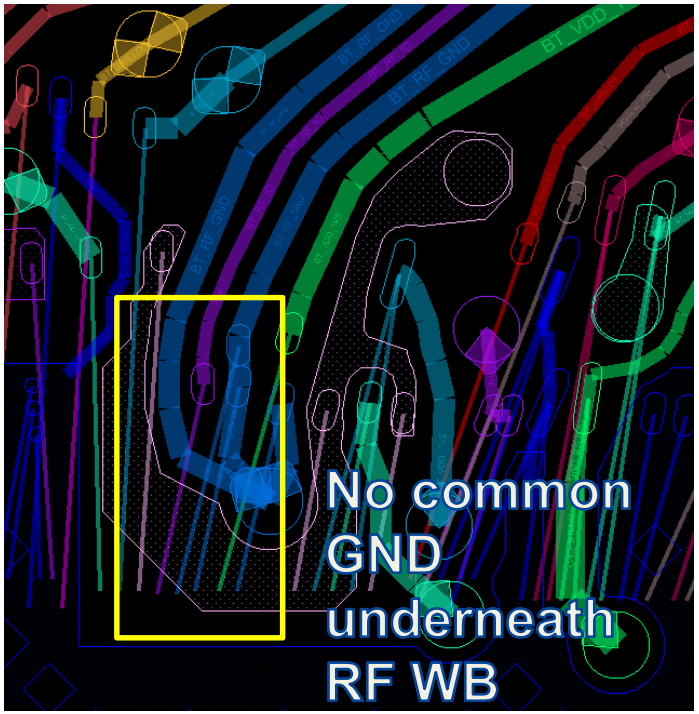
- A dramatic improvement in results can be observed.
  - Insertion loss: -91dB
  - Coupled power: -120dBm (Target: $P_{Coupled}$ <= -120dBm)

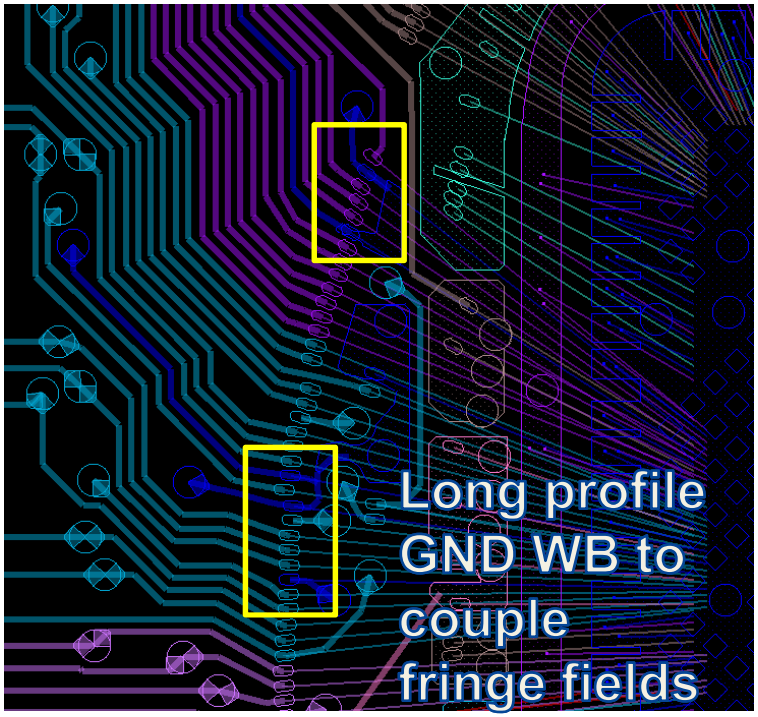




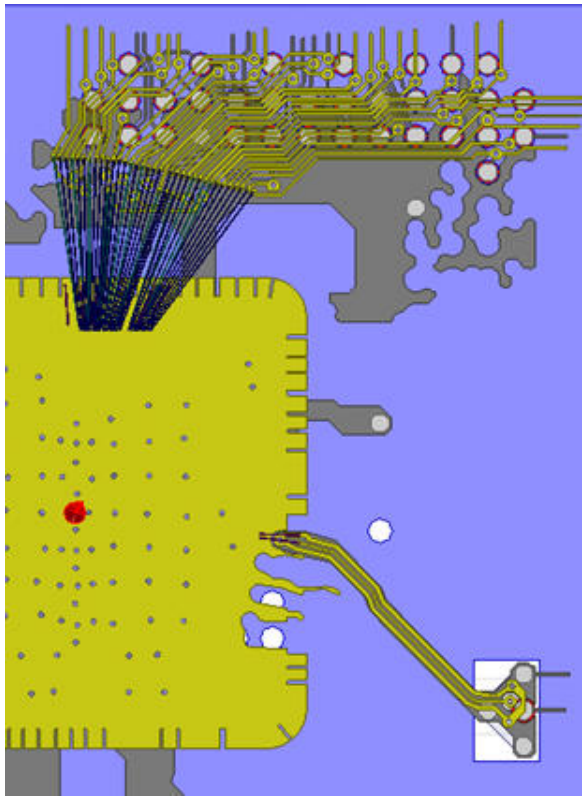
Implementation in official design

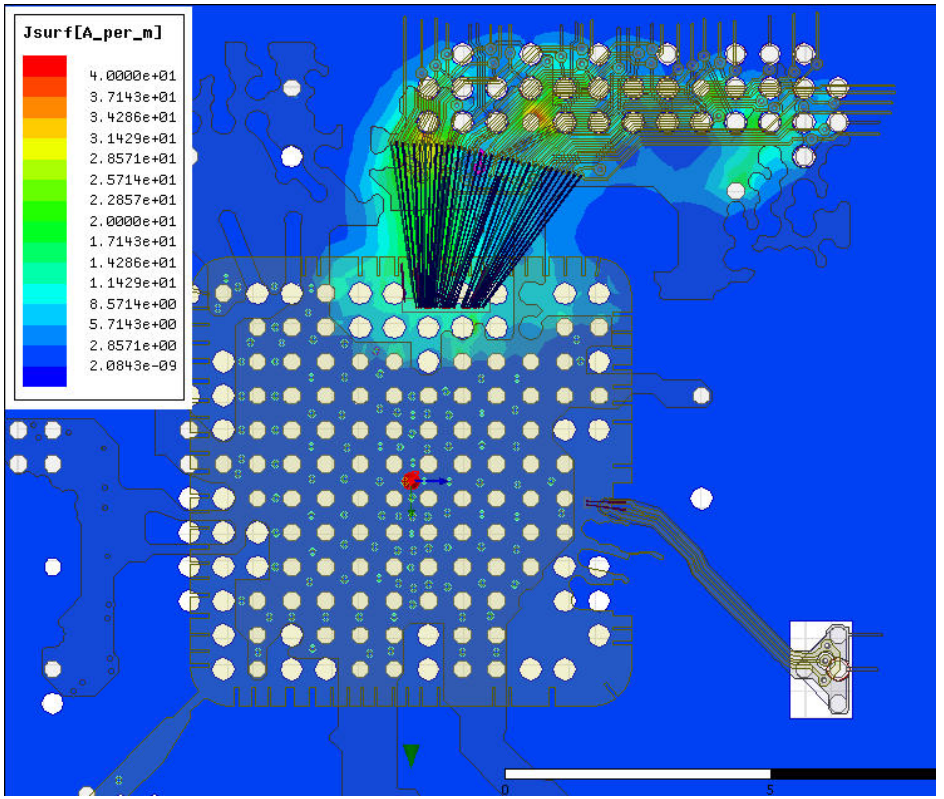
- Suggested improvements are implemented in current project layout.





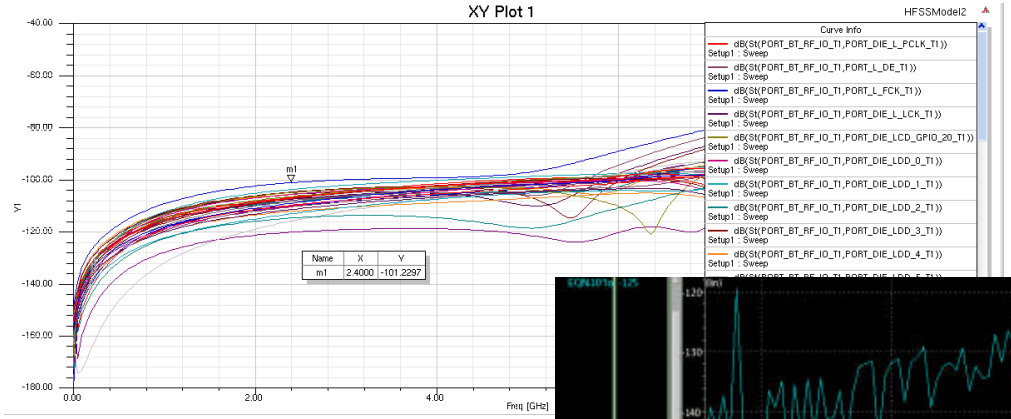
Production layout extraction

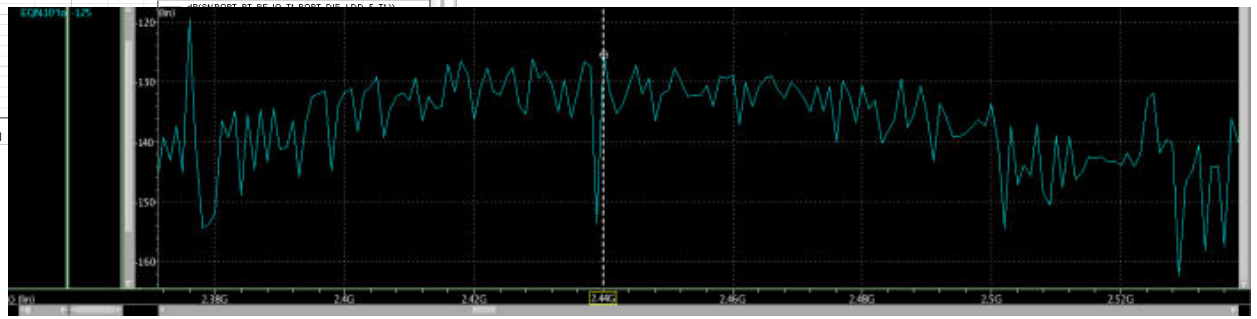




Official layout noise level simulation

- Simulations yield even better results for official layout than study case.
  - Insertion loss: -101dB
  - Coupled power: -125dBm (Target: $P_{Coupled}$ <= -120dBm)





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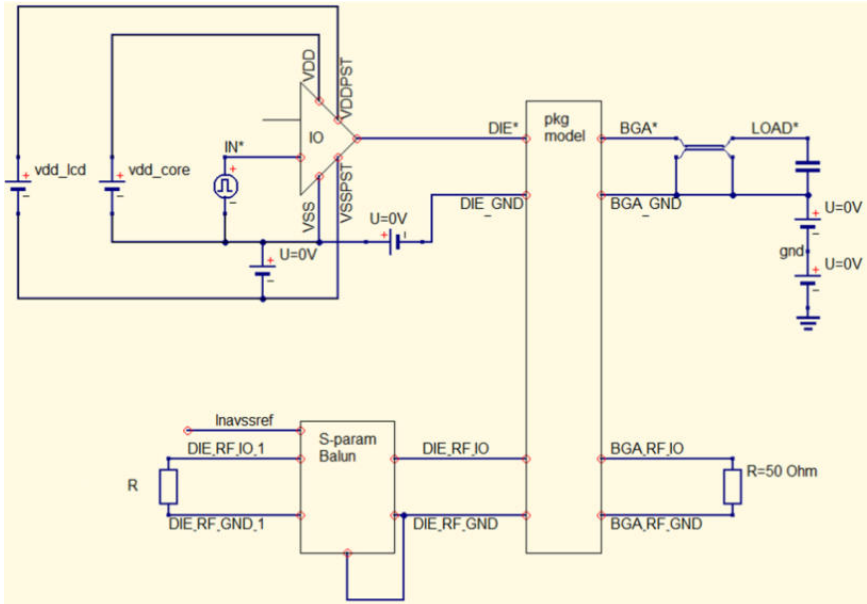
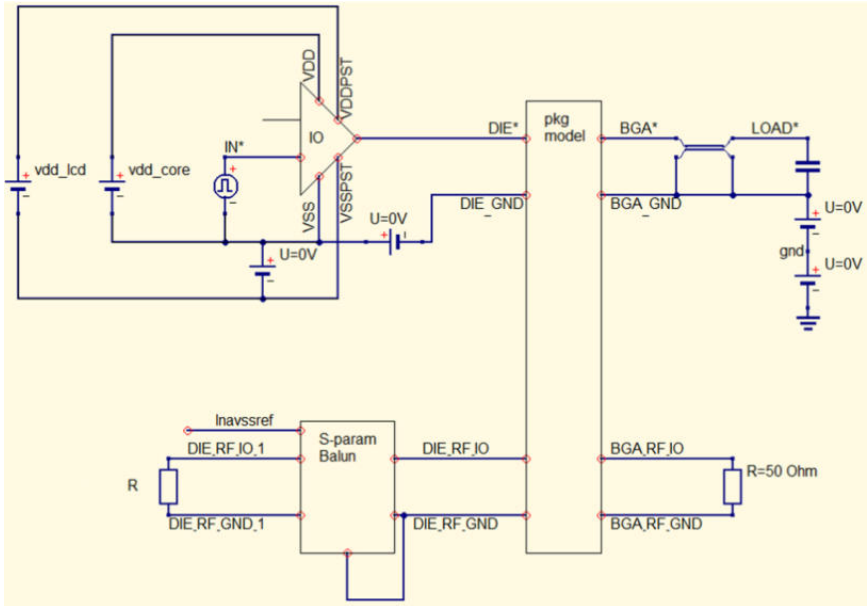
Spice setup – Die side

- To simulate a design as close as possible to a production system, the following spice setup is used.
- Passive and causal package model with extraction ports on die side.
- An aggressor interface IO cells are connected to the aggressor die ports.
- The core and IO supplies are referenced to an extracted return path.
- Balun and its balanced termination model, extracted using a full 3D field solver is connected to victims die port.



Spice setup – PCB side

- To simulate a design as close as possible to a production system, the following spice setup is used.
- Transmission lines of estimated length according to PCB constraints.
- Capacitors imitating the capacitive load of the far end device.
- The RF front-end ports are loaded with a 50ohm resistor to imitate matched impedance on the RF path and antenna.



Simulation transient length

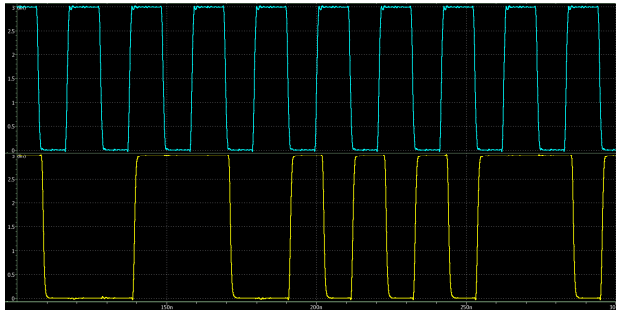
- The victim RF interface has 79 BT channels and each channel spans 1MHz.
- The noise should be integrated over the entire channel width of 1MHz.
- 1MHz wide FFT bin will ensure that the value of the bin is the integration of noise over the 1MHz band.
- Bin width can be described as the sampling frequency of a Fourier transform.
- Bin width dictates the sampling rate and simulation period time.

$$T_s = \frac{1}{f_s} = \frac{1}{(bin\ width)} = \frac{1}{1MHz} = 1\mu\text{sec}$$

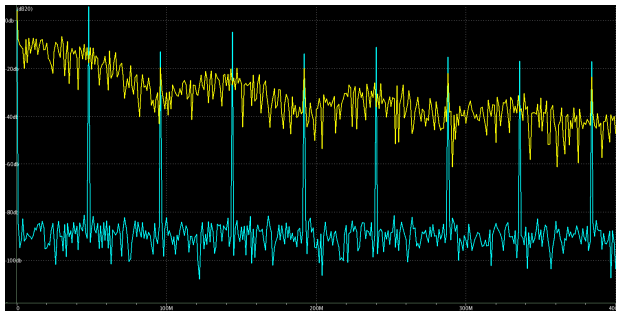
Toggling pattern

- Several patterns widely used to characterize a system: Pulse, Pseudo Random Bit Sequence (PRBS) and walking one/zero. The noisiest patterns are Pulse and PRBS.

- Pulse pattern (Blue):
  - Maximal interface toggling frequency.
  - Most of the energy concentrated at discrete frequencies.
  - Peaks are at every harmonic of the fundamental frequency.

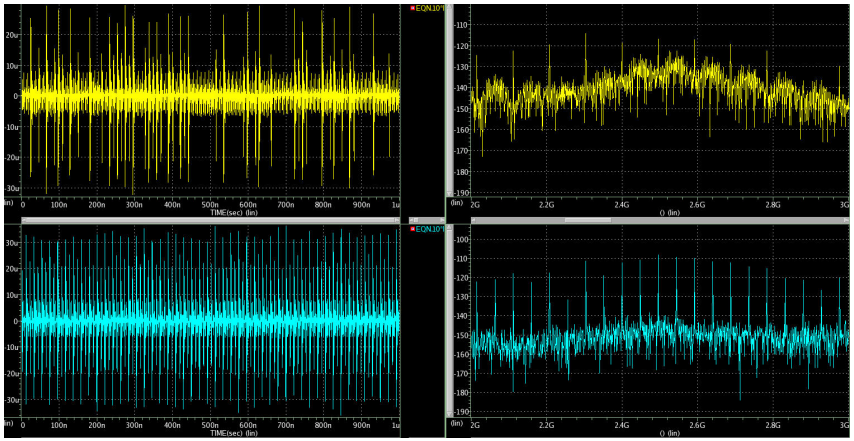


- PRBS pattern (Yellow):
  - Effective toggling frequency is lower than maximal interface frequency.
  - Energy is distributed across the spectrum much more evenly.
  - Interharmonic range energy is a lot higher than in pulse pattern.



Simultaneously Switching Outputs

- In parallel interfaces the outputs can switching simultaneously.
- Same direction switching doubles the amount of magnetic flux and ground bounce.
- Pulse SSO concentrating all of the noise's energy at harmonic frequencies.
- Worst case scenario for memory based interfaces.
- Pulse SSO pattern is a not a suitably realistic pattern for all interfaces.
- For an LCD interface the PRBS SSO pattern is the noisiest, most applicable and true-to-life pattern.



PRBS SSO noise signal and FFT (Top)
and pulse SSO noise and FFT (Bottom).

Tuning drive strength

- There are interfaces that layout modifications can’t be applied on.
- For other interfaces layout modifications cannot improve noise performance due to their proximity to victim.
- Choosing the right drive strength might decrease the noise below threshold level.
- DS reduction is simulated for both aggressor and victim.
- Low DS will reduce noise but at the same time can deteriorate aggressor performance.

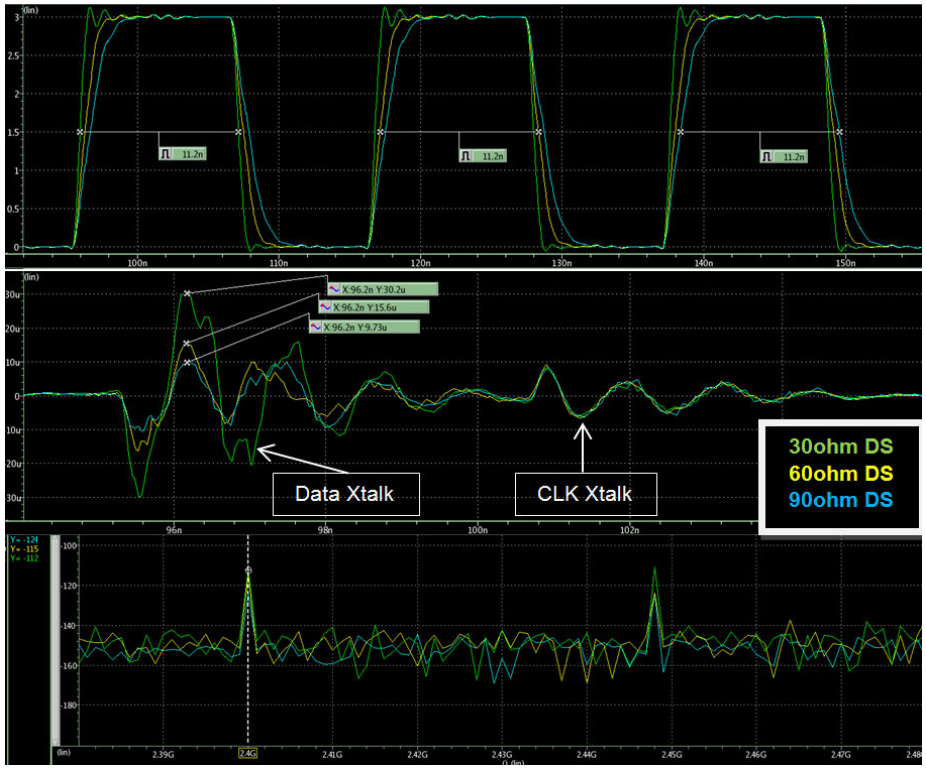
Drive strength simulation results

- The IO under test has 4 DS values:
  - 30ohm (Default) – Strongest drive strength
  - 45ohm – Wasn't simulated
  - 60ohm
  - 90ohm – Weakest drive strength

- No impact on duty cycle or eye diagram of the aggressor.

- Reduction on cross-talk values.

- Coupled noise reduced be 12dB.



Conclusion

- By performing package extraction in the early stages of the development process, design vulnerabilities can be identified.
- Aggressor location relative to victim has major impact on victim's noise level.
- Package layout modifications such as reducing current loops, introducing current sinks and cutting out common conductors around the victim will improve the isolation.
- SPICE simulations of the system, including all drivers, interconnects and loads must be performed because this will model phenomena such as ISI, cross-talk and ringing due to impedance mismatch.
- Choosing the right drive-strength will allow to an aggressor and a victim to co-exist and operate without significantly deteriorating each other's performance.

Thank you