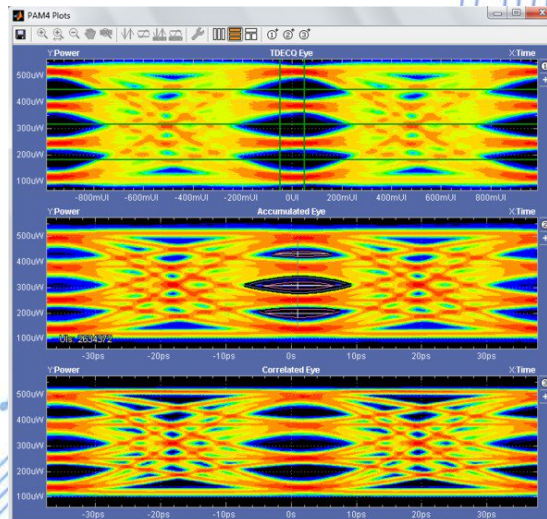


The Case of the Closing Eyes:

**Is PAM the Answer?
Is NRZ dead?**



Agenda

- Introductions
- Overview
- Design Engineering Perspective
- Test & Measurement Perspective
- Summary
- Audience Discussion



Panelists



Cathy Liu

Director, Broadcom Ltd



Mike Li, PhD

Fellow, Intel Corporation



Mark Marlett

Principal Engineer, Inphi Corporation



Ransom Stephens, PhD

Principal, Ransom's Notes



Pavel Zivny

Domain Expert, Tektronix, Inc.



Greg LeCheminant

Sr. Applications Engineer, Keysight Technol

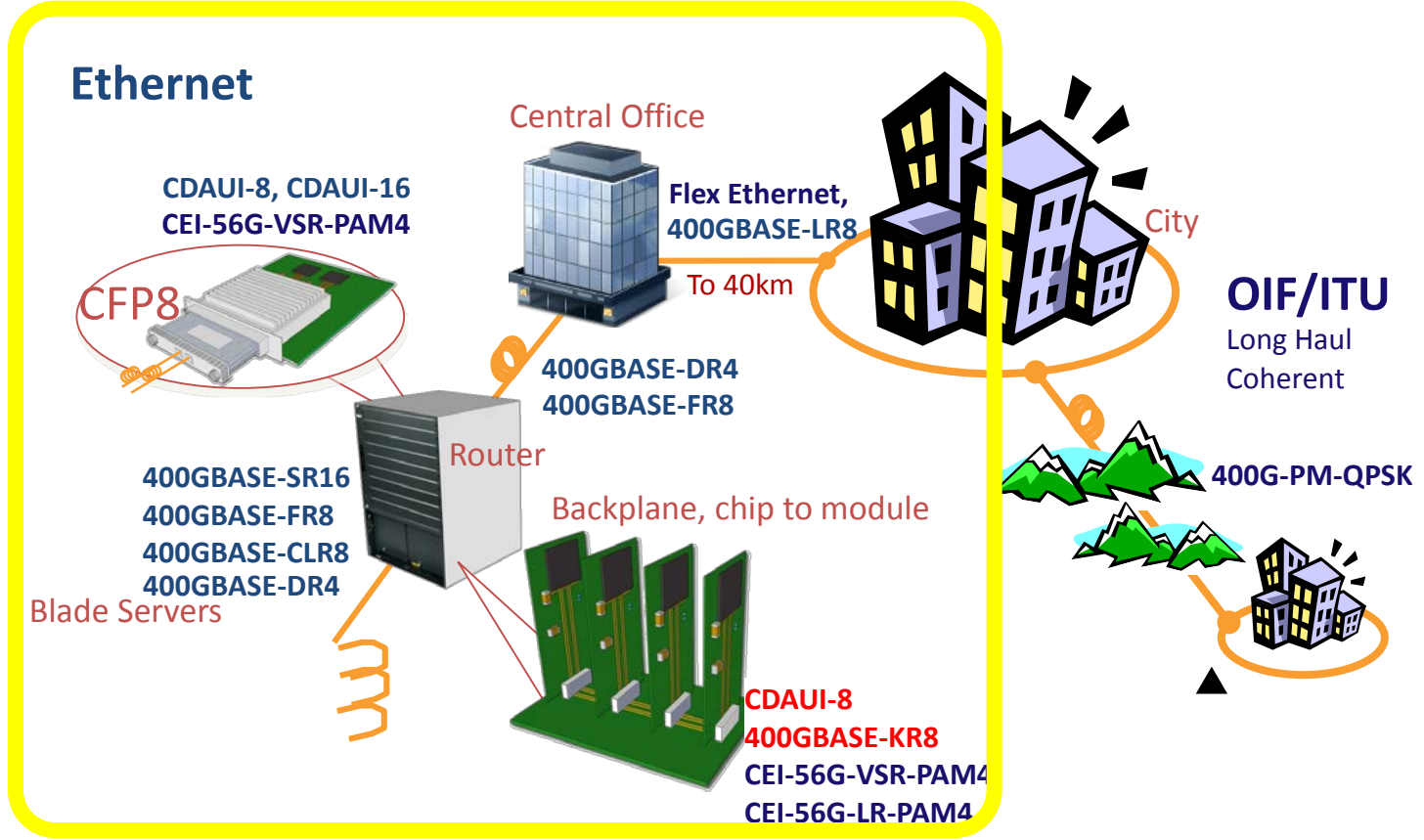


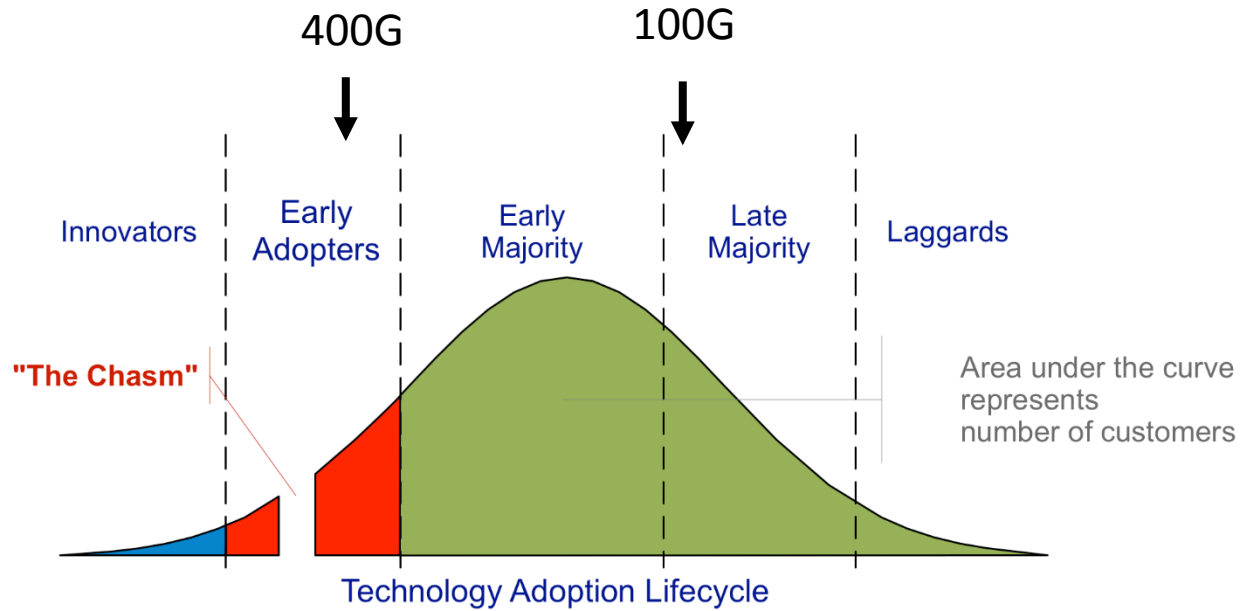
Marty Miller

Chief Scientist, Teledyne-LeCroy Corporat



PAM4 Impact on Communications Network



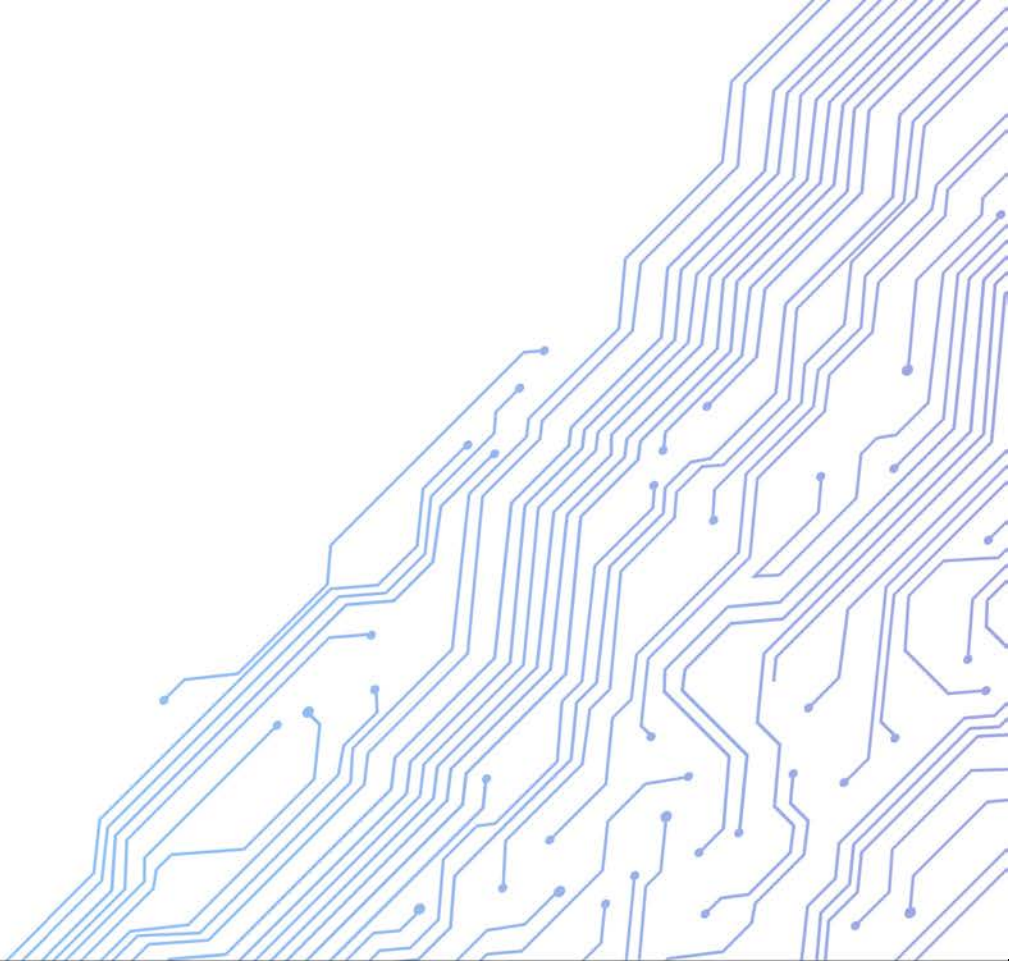


Distance	Standard	Modulation/signaling	e.g.
X,000 km	OIF, OTN, ITU	Complex optical	DP-QPSK
100M (MMF)	Ethernet	PAM2 at 25 GBd	400GBASE-SR16
10 km	Ethernet	PAM4 at 25 GBd	400GBASE-LR8
2 km	Ethernet	PAM4 at 25 GBd	400GBASE-FR8
500 m	Ethernet	PAM4 at 56 GBd	400GBASE-DR4
Backplane < 1m	OIF CEI	PAM4 at 25 GBd	CEI LR
Interconnect module to chip, chip to chip	Ethernet OIF CEI	NRZ PAM4	CDAUI-16, CDAUI-8 CAUI-4 CEI VSR



Is NRZ Dead?

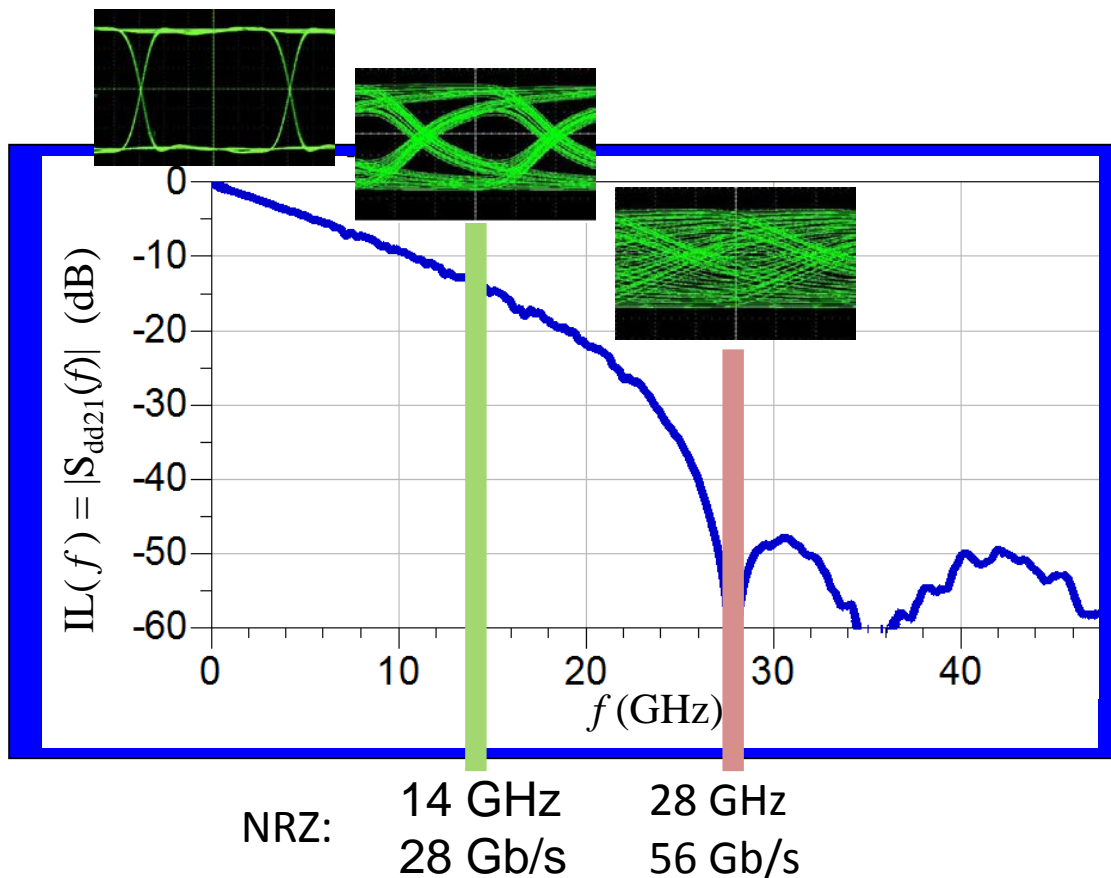
Ransom Stephens, PhD, Ransom's Notes



The problem

- Frequency dependent loss
→ ISI
(inter-symbol interference)
- Equalization is not enough

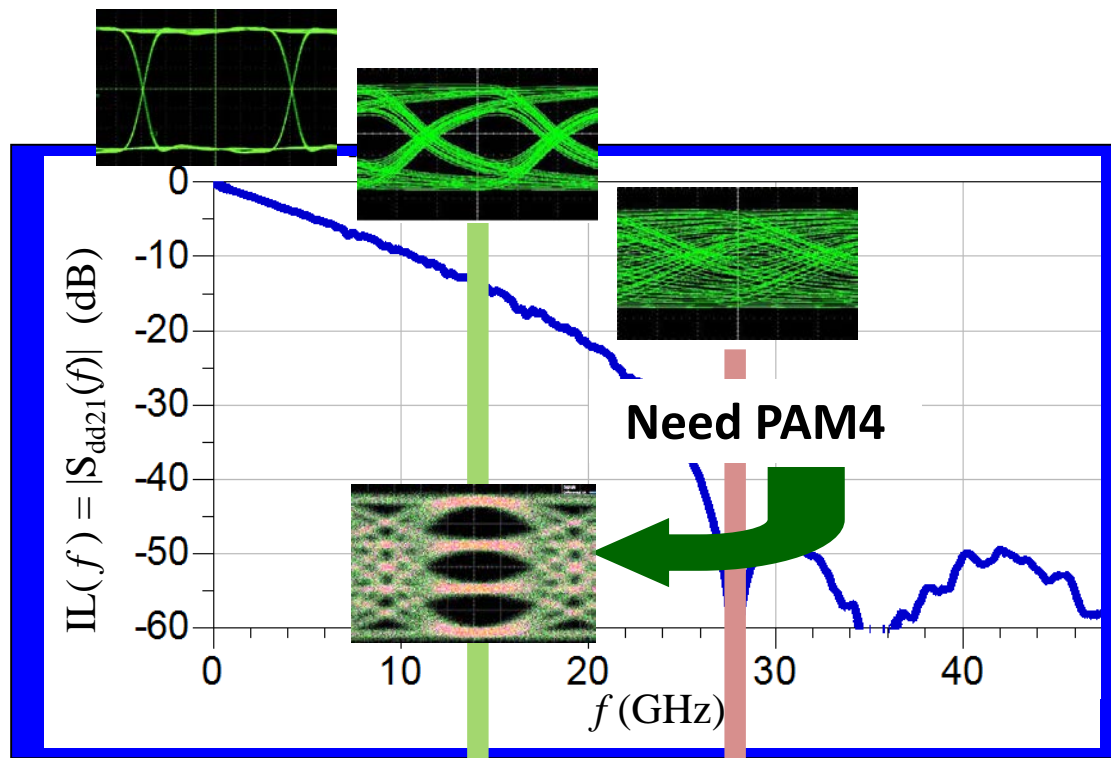
Closed eyes



The problem

- Frequency dependent loss
→ ISI
(inter-symbol interference)
- Equalization is not enough

Closed eyes

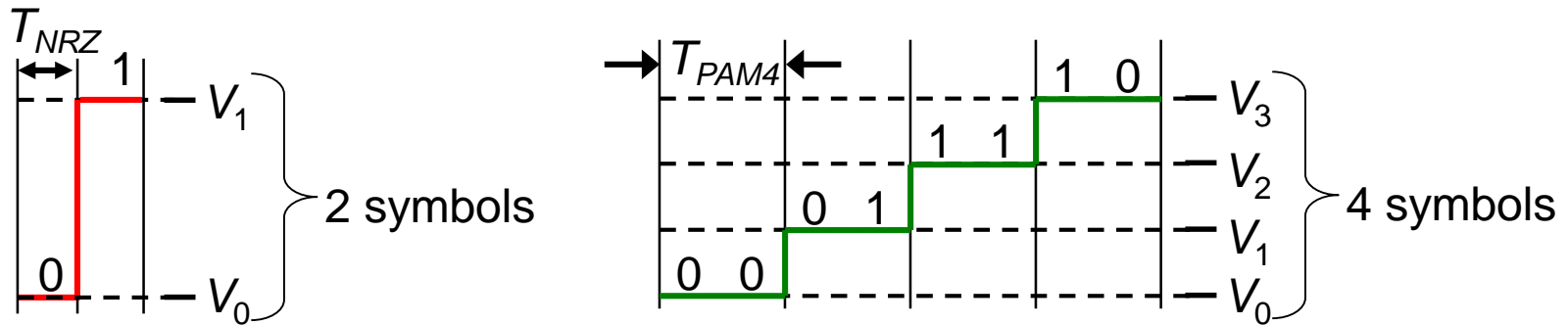


PAM4: 14 GHz
56 Gb/s



PAM4 vs NRZ – bits, symbols, baud

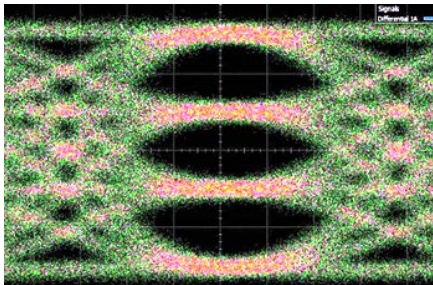
- NRZ bits are *really* PAM2 “symbols”



- NRZ bit rate = symbol rate (Gb/s = Gbaud)
- **PAM4** bit rate = $2 \times$ symbol rate (Gb/s = $2 \times$ Gbaud)
 - PAM4 28 Gbaud = 56 Gb/s



NRZ is dead



PAM4 development

- 3 slicers, 4-level DFE, mushy clock recovery

→ Disruptive Receiver Improvements

DSP-based Receivers

→ PAM8, PAM16, ..., PAM n



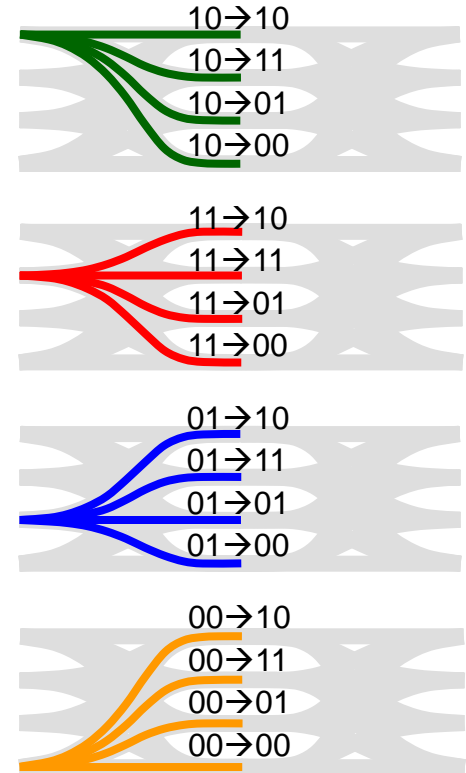
But PAM4 makes everything gets harder

Every signal degradation has greater impact on PAM4 than it had on NRZ

- SNR at least 9.5 dB worse
- 16 symbol transitions
- 6 different rise and fall times, t_{rise} & t_{fall}
- 75% transition density
- Crosstalk, reflections cause more trouble

AND

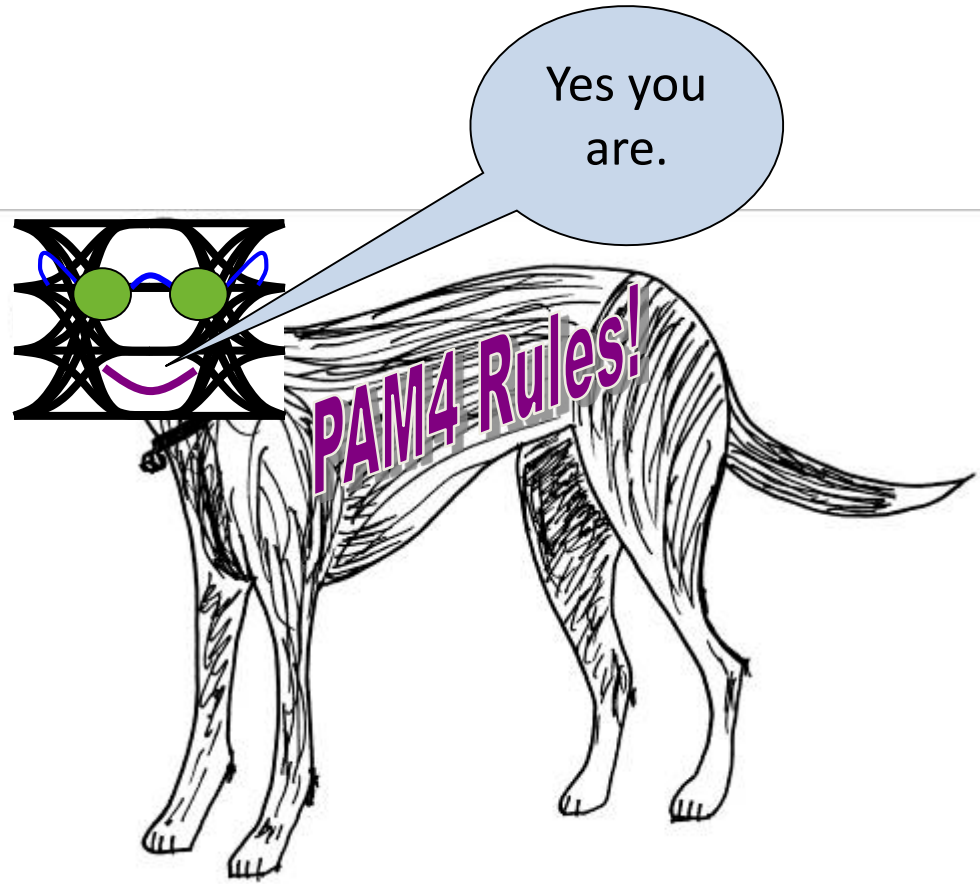
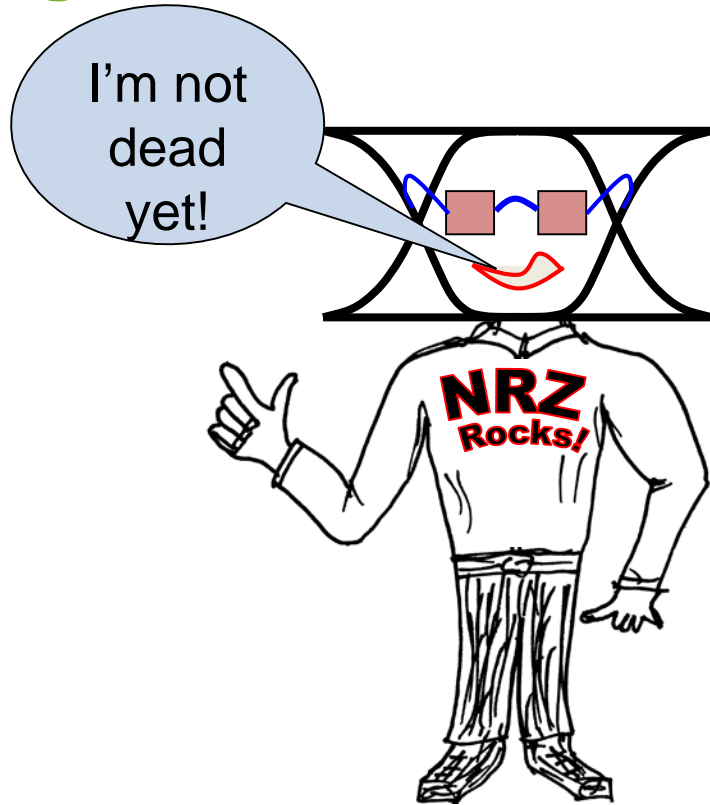
- Forward error correction, FEC → BER < 10^{-5}
 - costs power, latency, space



Long live NRZ!



Long live NRZ!



Path from 56G to 112G

Mike Peng Li, Intel



NRZ vs PAM4 vs Reach at 56G

Parameter	USR	XSR	VSR	MR	LR
Data Rate (Gbps)	18 -58	36 -58	36 -58	36 -58	36 -58
BER	1E-15	1E-15	1E-15	1E-15	1E-15
Distance	10 mm (~0.4")	50 mm (~2")	150 mm (~6")	500 mm (~20")	886 mm (~34.9")
Interconnect	MCM	PCB+ 0 connector	PCB + 1 connector	PCB + 1 connector	PCB + 2 connectors
Insertion Loss (dB) (at f_N)	2	4 (PAM4) 8 (NRZ)	10 (PAM4) 23 (NRZ)	20 (PAM4) 36 (NRZ)	30 (PAM4)
Modulation	NRZ	NRZ or PAM4	PAM or NRZ	PAM4	PAM4
FEC	N	N	Y/N	Y	Y

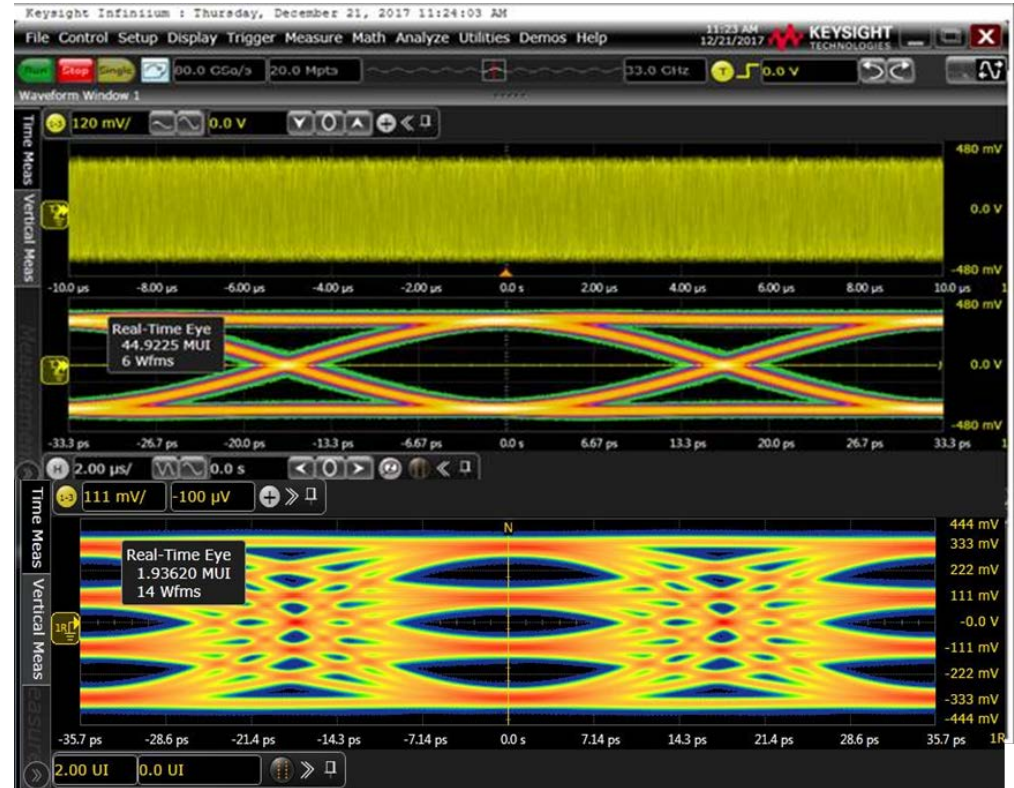


Is NRZ dead? **No !!**



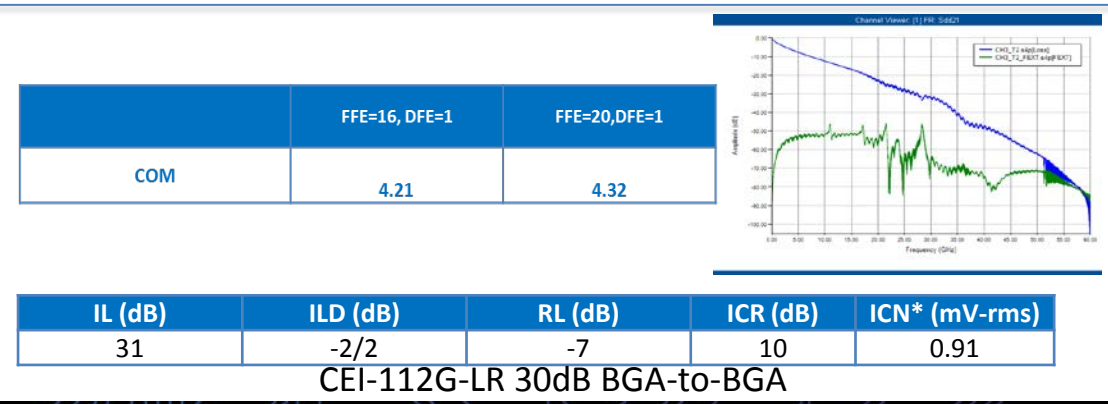
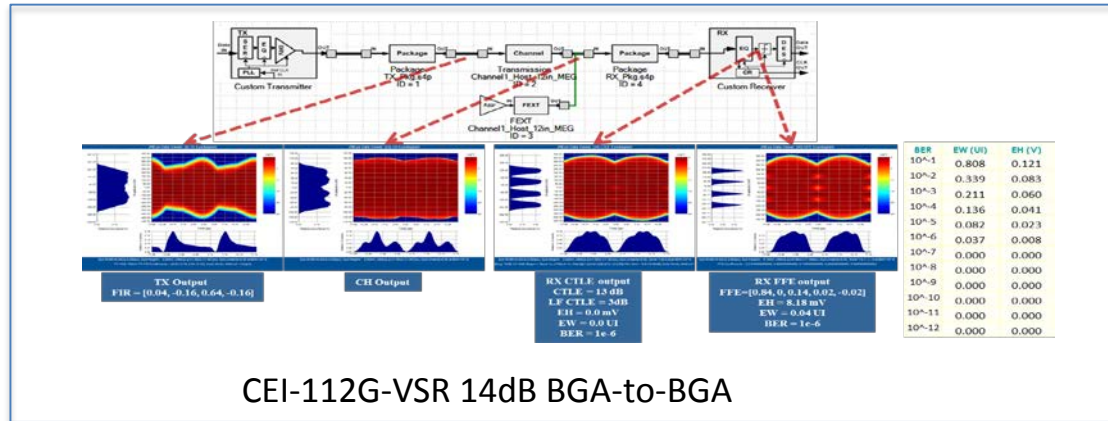
FPGA 58 Gbps PAM4/30 Gbps NRZ Transceiver Measurements

- PAM4: BER of $<1e-9$ observed at 58 Gbps with channel insertion loss (BGA-to-BGA) $< -30\text{dB}$
- NRZ: Error free at 30 Gbps with channel insertion loss (BGA-to-BGA) $< -40\text{dB}$
- TX and RX exceed the Ethernet and CEI 28G NRZ and 56G PAM4 spec



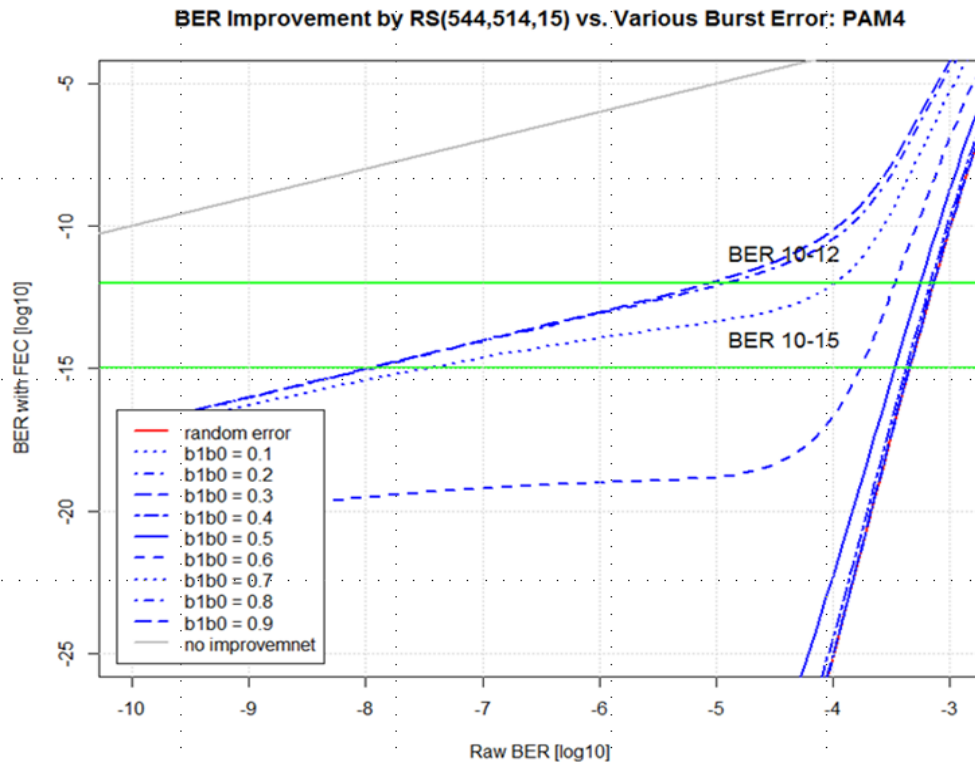
112G Feasibility

- **PAM4: Feasible for 30 dB (at Nyquist) channel, backward compatibility insured, great value proposition**
- **PAM4 and PAM8 comparison analysis has been done for BP/LR channels, and PAM4 out-performs PAM8 in general**
- **Advanced medium (e.g., better PCB materials, cable backplane) needed to be considered to achieve practical reach objectives for BP and DAC**
- **Constraints are in how much power the system can afford, which affects the SERDES implementation choices**



RX Architecture vs RS(544, 514) (i.e., KP FEC) vs Performance

- If the RX does not have DFE, then the main burst error source is eliminated.
- A RX dominated with FFE can compensate reflections without introducing burst errors
- Post FEC BER < 1e-25 achieved with FFE dominate RX, exceeding all system requirements.

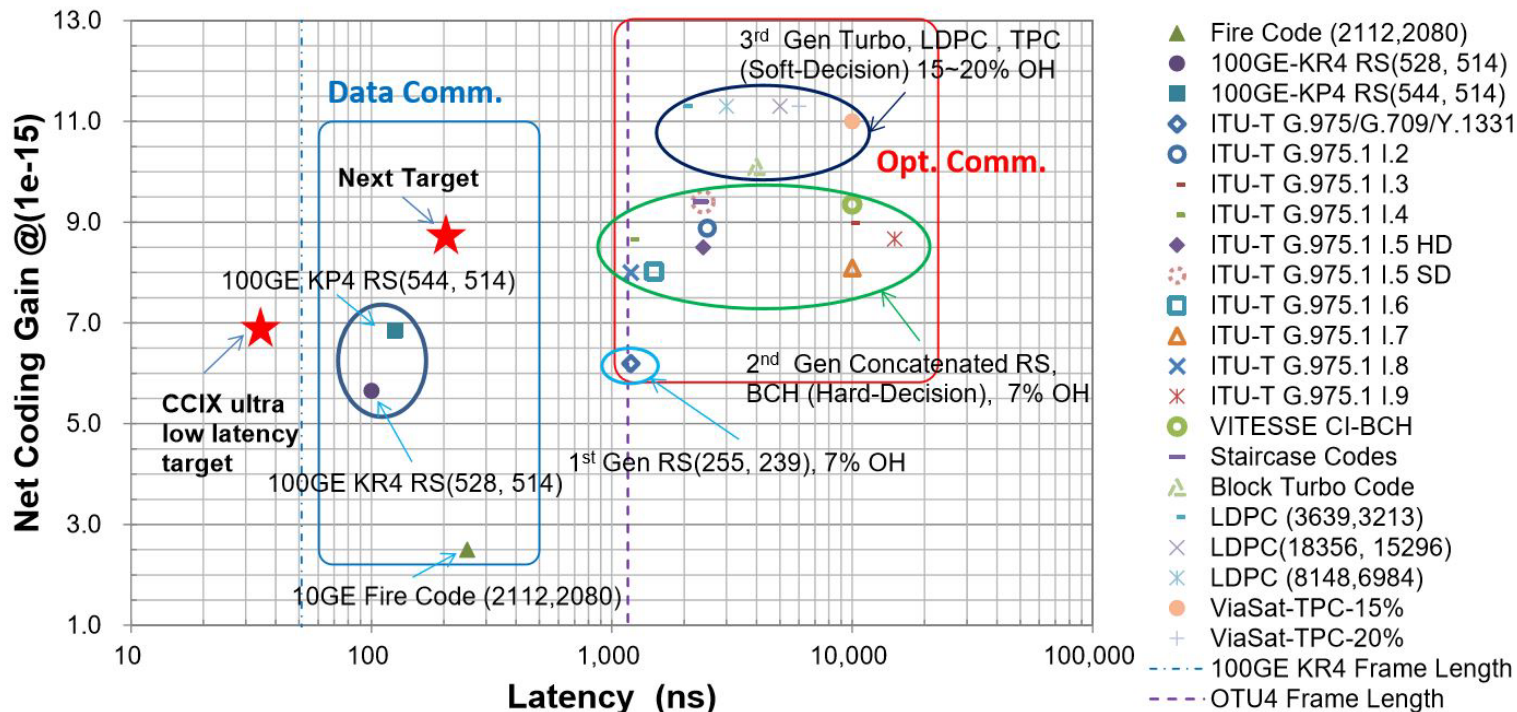


FEC and 112G Outlook

Cathy Liu, Broadcom Limited



Landscape of FEC Technology



Post-FEC Measurements

The screenshot displays the aView Explorer interface for a project named 'AACS Server - JTAG'. The left pane shows a hierarchical tree of components, with 'RSFEC 528' selected under 'SBUS Ring 0'. The main window shows a block diagram of the RSFEC Transmitter and Receiver. The Receiver block includes a 'Receive Statistics' section with the following data:

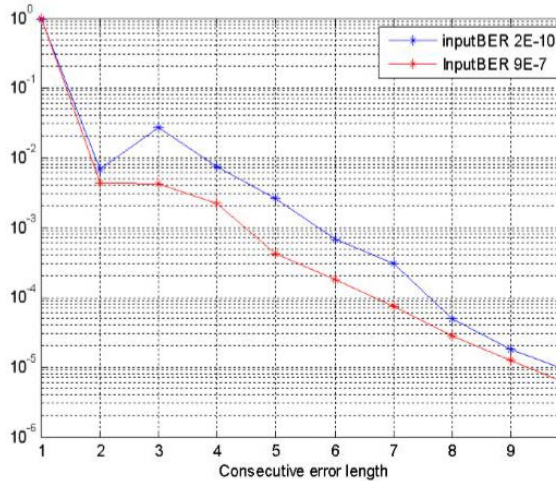
```
Receive Statistics
Halt:false
Halt on max count:false
Clear on Read:OFF
Codewords:68719476735
Corrected:11521685:00, Ratio:0.00E0
Uncorrected:0, CER:0.00E0
cw_0syms:0, Ratio:0.00E0 cw_10syms:0, Ratio:0.00E0
cw_2syms:11525619, Ratio:1.00E-4 cw_10syms:0, Ratio:0.00E0
cw_3syms:6014, Ratio:0.75E-8 cw_10syms:0, Ratio:0.00E0
cw_4syms:52, Ratio:7.57E-10 cw_10syms:0, Ratio:0.00E0
cw_5syms:0, Ratio:0.00E0 cw_10syms:0, Ratio:0.00E0
cw_6syms:0, Ratio:0.00E0 cw_14syms:0, Ratio:0.00E0
cw_7syms:0, Ratio:0.00E0 cw_18syms:0, Ratio:0.00E0
cw_8syms:0, Ratio:0.00E0 cw_18syms:0, Ratio:0.00E0
Lane_Consec_Em: 0:true 1:true 2:true 3:true
```

Annotations on the image include:

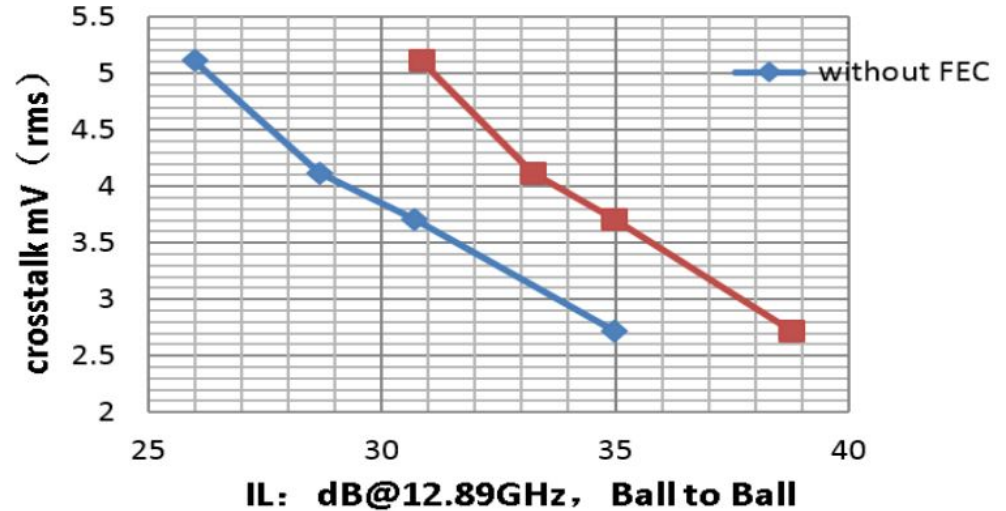
- 'Error free over 68hr' with an arrow pointing to the 'Corrected' and 'Uncorrected' statistics.
- 'Max. symbol in error = 4' with an arrow pointing to the 'cw_4syms' line.



56G PAM4 KP4 FEC Test Results



Error statistic (10 hr)

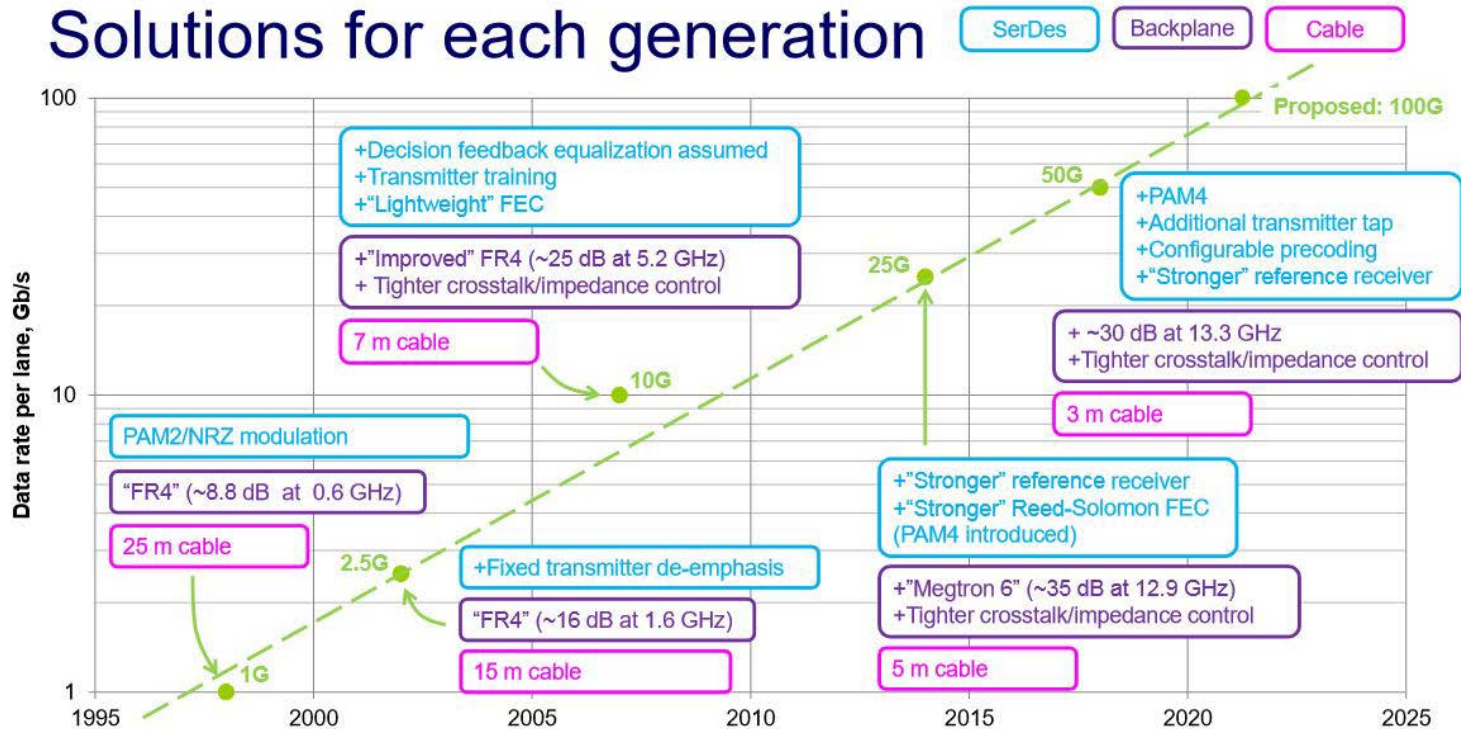


Channel loss and crosstalk tolerance improvement (post-FEC BER < $1e-15$)



112G Outlook

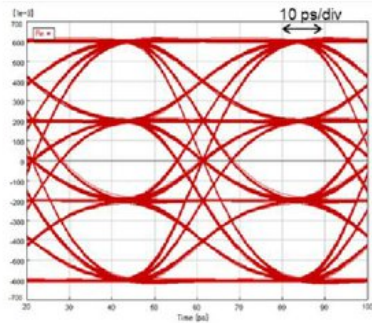
Solutions for each generation



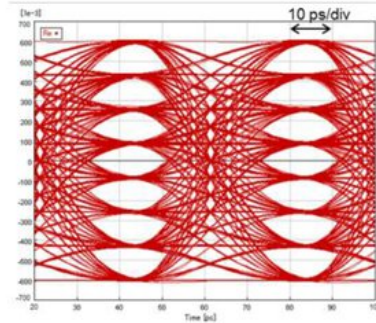
112G Design Challenges



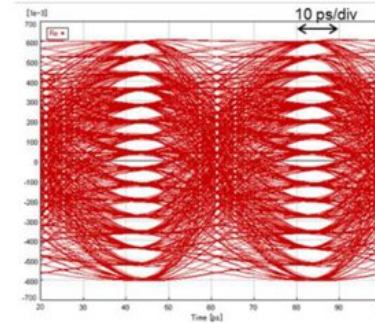
- OIF CEI 112G projects are already underway
- PAM4 is likely signaling format for VSR application
 - NRZ is out
 - Industry has digested PAM4 and FEC challenges through 56G design and production
 - So the biggest challenge of 112G PAM4 design is the doubling bandwidth (component, package, device, T&M...)
- What if PAM4 is not good enough for long reach application?
 - PAM8, PAM16, or QAM?



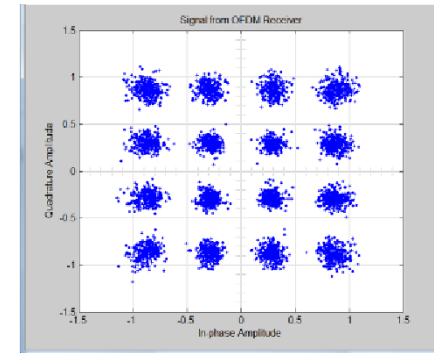
(a) PAM4 (2bits x 25 Gbaud)



(b) PAM8 (3bits x 25 Gbaud)



(c) PAM16 (4bits x 25 Gbaud)

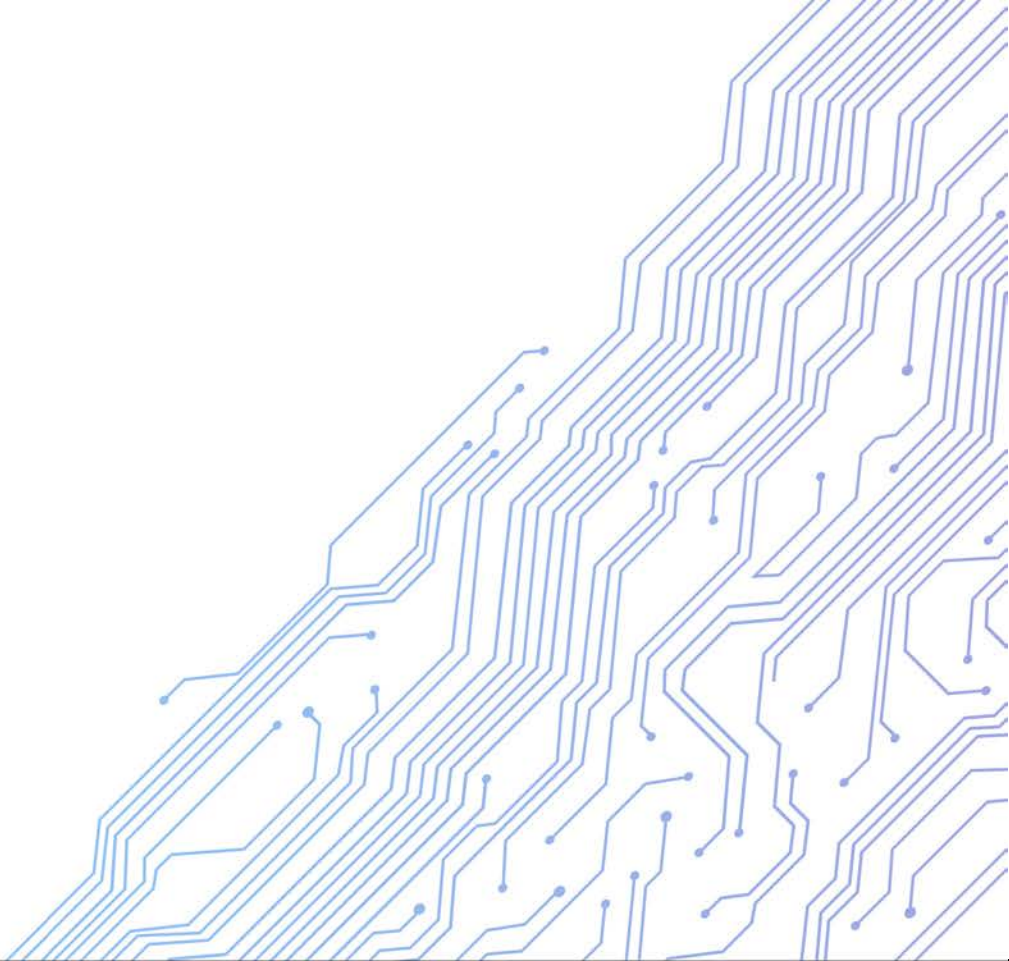


(d) 16QAM



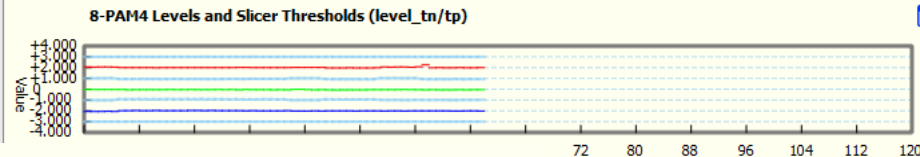
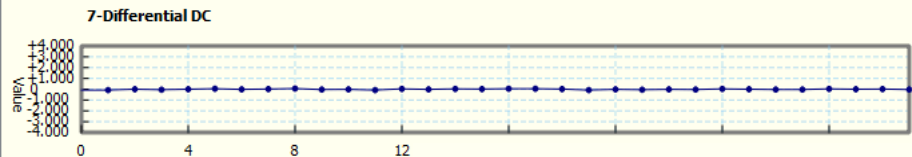
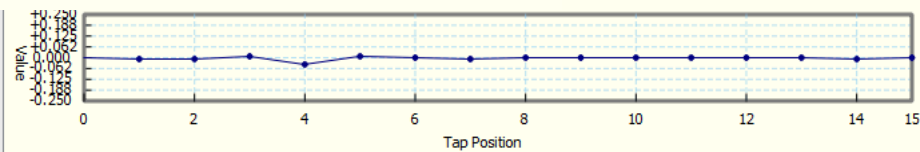
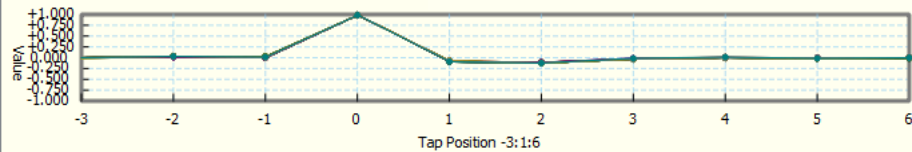
Optics & PAM4

Mark Marlett, Inphi

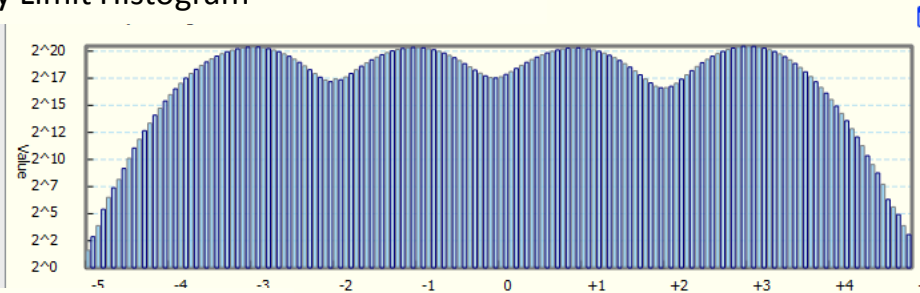
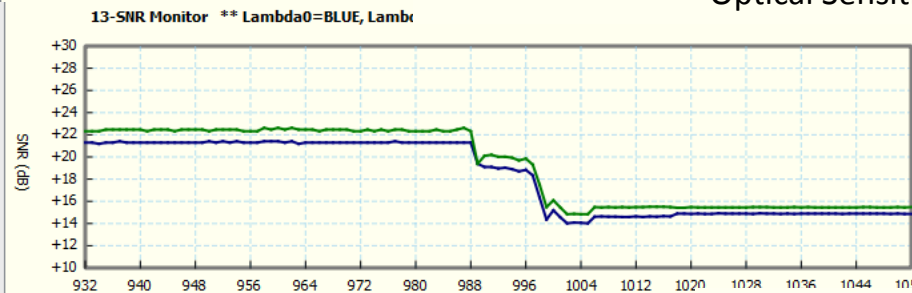


DSP enables PAM4 optical channels

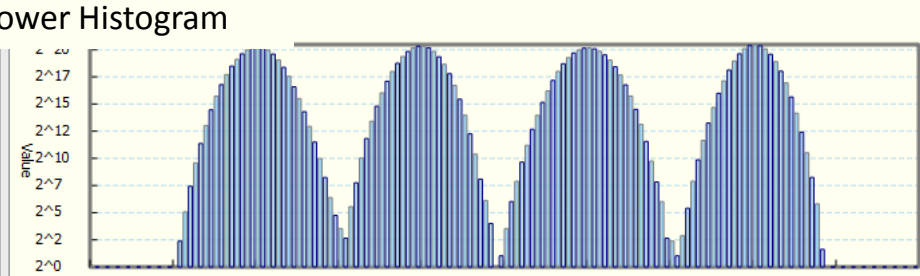
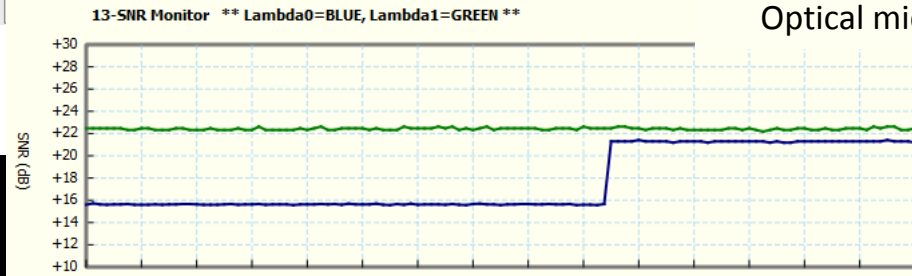
Multi-tap TAP FFE + adaptation of many timing and voltage parameters



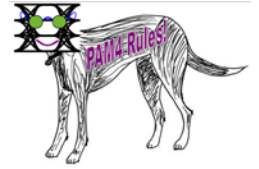
Optical Sensitivity Limit Histogram



Optical mid power Histogram



Optical Communications future



Higher Data rate (400G+) Modules

More DSP

New FEC

Higher baud rates (56Gbaud)

More wavelengths on the same fiber

Fitting more data in these bandwidth limited channels

So where does NRZ (PAM2) fit in?

NRZ is in legacy (<28 Gb/sec)

What is the future of Modulation?

PAM4 -> PAM? -> ??

PAM4+ -> DSP



Receiver test has some big challenges beyond just the PAM4 issues!

Greg LeCheminant, Keysight



Use of FEC allows for a much higher SER for the hardware. (Shouldn't SER/receiver testing be a lot easier now?)

- High coding gain FEC means that a simple SER analysis does not exactly predict the overall link integrity
- Pre-FEC SER could be within the required limit, but if there is a long burst of errors, frames can be lost
- We (T&M) need to do a better job of showing the 'signature' of errors, whether they are random or bursty



Frame loss analysis (counting errors within the FEC frame block) would be helpful

- If the data is 'striped' across multiple lanes, all lanes need to be monitored simultaneously. Is it practical?
- Standards/T&M challenge: Consider new ways to account for long bursts of errors other than frame loss ratio when there are many parallel lanes



Acquisition for PAM4 transmitter characterization

Pavel Zivny, Tektronix



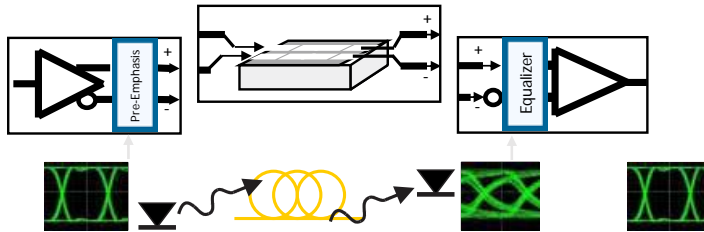
Acquisition for PAM4 transmitter characterization

Pavel Zivny, Tektronix



Traditional link design.

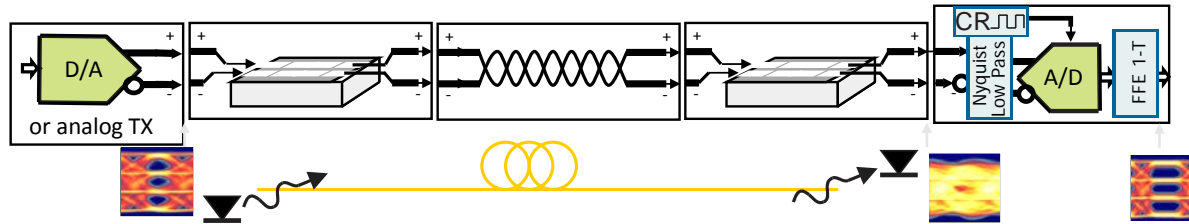
The receiver rule: more BW is better (keeps the eye more open)



The links as we know them from lower loss systems.
Equalization was low key or (optical systems) none



What's the DUT doing: the Receiver for PAM4 at 53 GBd (aka 100 Gb/s) does sample at Nyquist. The extra bandwidth beyond that is not that useful* as it's past Nyquist.



- Today the receivers for 53+ GBd are an A/D that samples at the symbol rate... (53 GS/s for a 53 GBd signal) ... and the Nyquist is then 26 GHz ... energy beyond 26 GHz is aliased* and thus not fully in control of the DSP
- For this and other reasons, the receiver is rolled off just past Nyquist.
- Thus the measurement system should not measure past what the receivers will be able to see. i.e. the measurement bandwidth ought to be similar to what the Rx does.

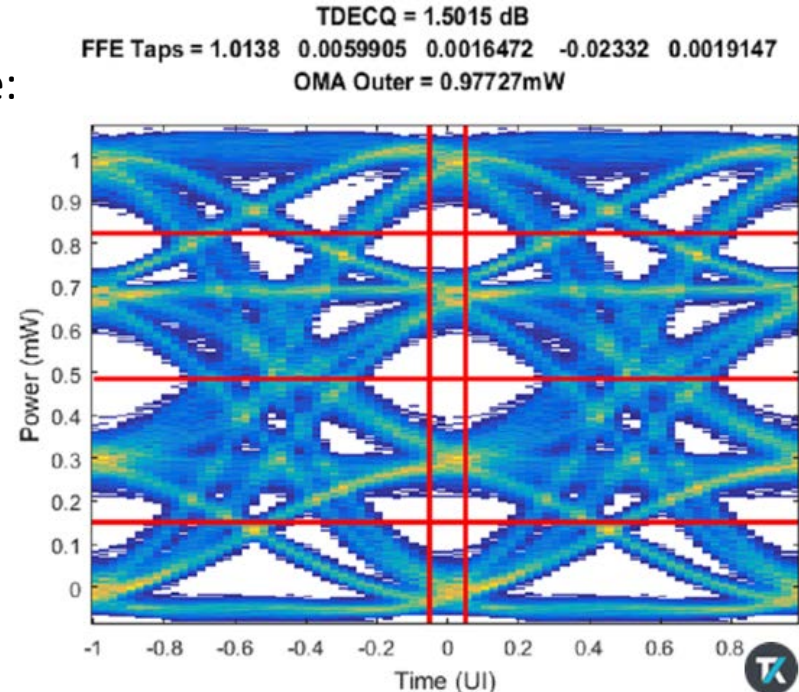
*Since we sample in-phase the alias is not as bad as in asynchronous systems.
And: there's (typically) is an analog boost (CTLE) *before* sampling... *not* aliased.



Ethernet changed the measurement bandwidth significantly to match what the RX sees: to measure a 26 GBd signal, use 13 GHz scope BW 4th order Bessel-Thomson filter, with controlled roll-off)

And you have to get the bandwidth right! Since:

- Higher bandwidth will improve the eye opening. You might get false 'good' on bad DUT.
- Lower bandwidth than the required $\frac{1}{2}$ of the symbol-rate-frequency is (i.e. 13 GHz for 26 GBd of the 50 Gb/s link) will worsen the TDECQ, and increase the number of false 'fail' DUTs.
- Opposite will happen for the RX test (where the oscilloscope measures up the stressors)



Conclusion

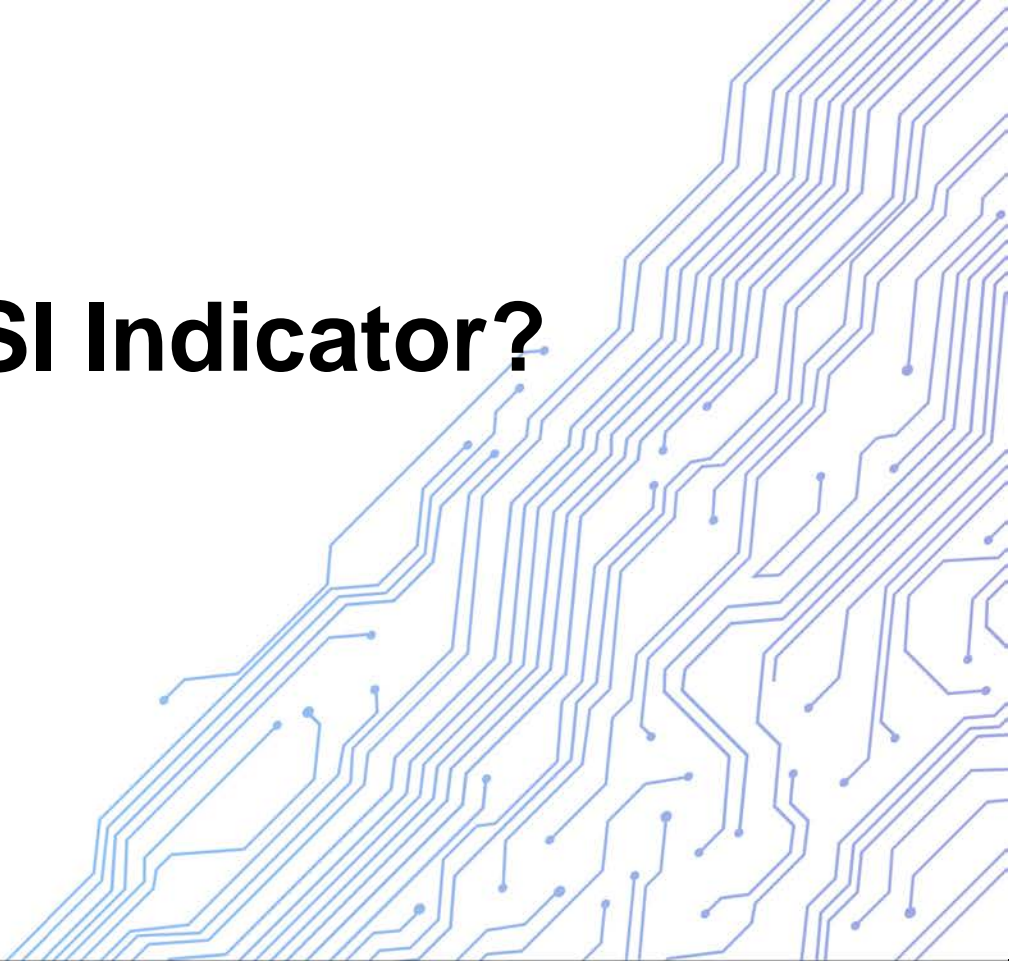
- The measurement bandwidth is critical for correct TDECQ measurement.
- Unlike in NRZ, where the measuring device (oscilloscope) doesn't close the eye*, the bandwidth of the oscilloscope limits the
- This is true for the measurement of the TX, and...
- ... the measurement of the RX, since the stressed eye source is measured with the same (oscilloscope) measurement bandwidth

*about 1% closure is due to the B-T in NRZ (0.75x filter)



SNDR as a good SI Indicator?

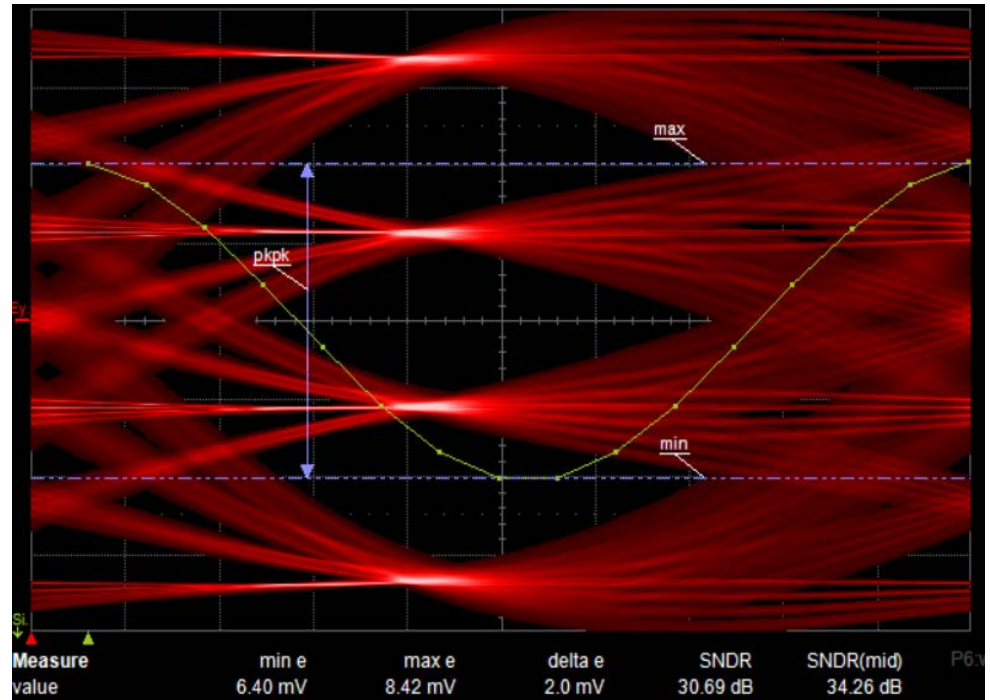
Marty Miller, Teledyne-LeCroy



Signal to Noise and Distortion

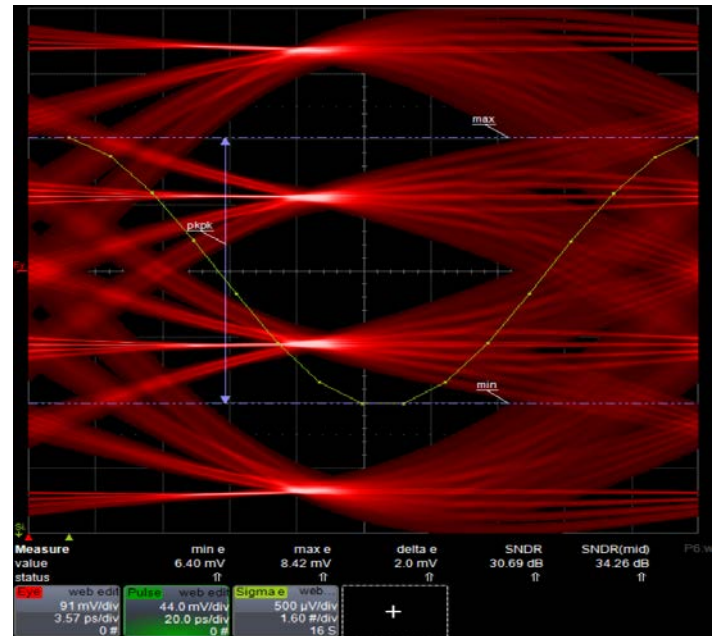
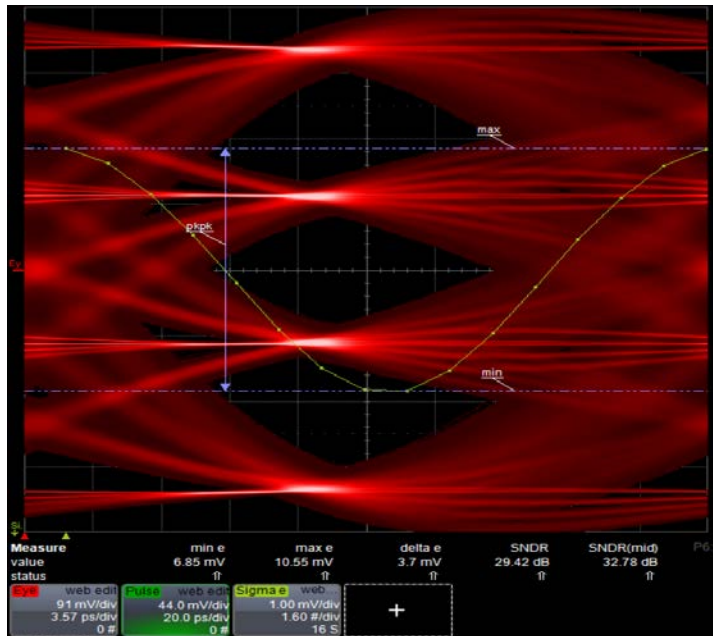
- Calculated from a QPRBS13
 - “linear fit” -> Pulse

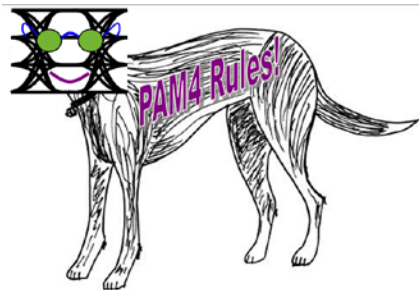
$$SNDR = 10 \log_{10} \left(\frac{P_{\max}^2}{\sigma_e^2 + \sigma_n^2} \right) \quad (\text{dB})$$



Why not a SNDR (mid) using error at center?

- Jitter affects RMS fit error at 0 & 1UI (500fs and 50fs Rj)





Panel Discussion

