DesignCon® 2014

Optimizing On Die Decap in a System at Early Stage of Design Cycle

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UBM Tech

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Disclaimer:

The scope of approach presented is limited to decap related to IOs only

Motivation

- When do we need On Chip Decap (OCD) for IO interface?
- Is adding OCD for an IO interface always beneficial?
- Does OCD requirement vary with system topology?
- How soon the estimation of OCD in a design can be done?

Agenda

- Background
- Determine the need for OCD
  - Understand Transmission line effect on power noise
  - Understand power noise effect on far end timing
- Predicting the OCD value
  - Effect of OCD on System PDN
  - Effect of power noise on system timing
- Validation of methodology
- Steps to predict optimum OCD
- Scope of Future work

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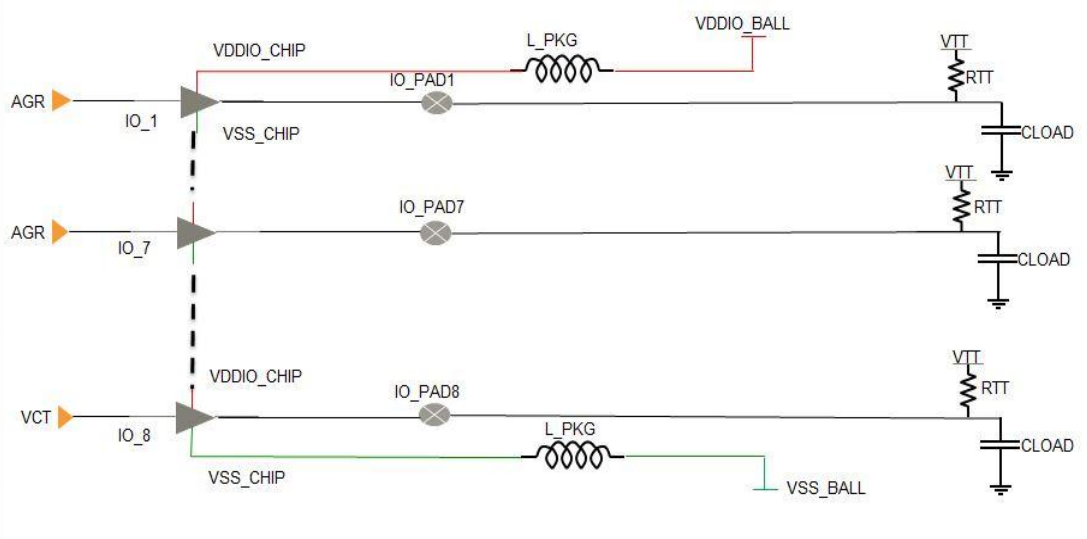
SSO setup with lumped load at IO PADs

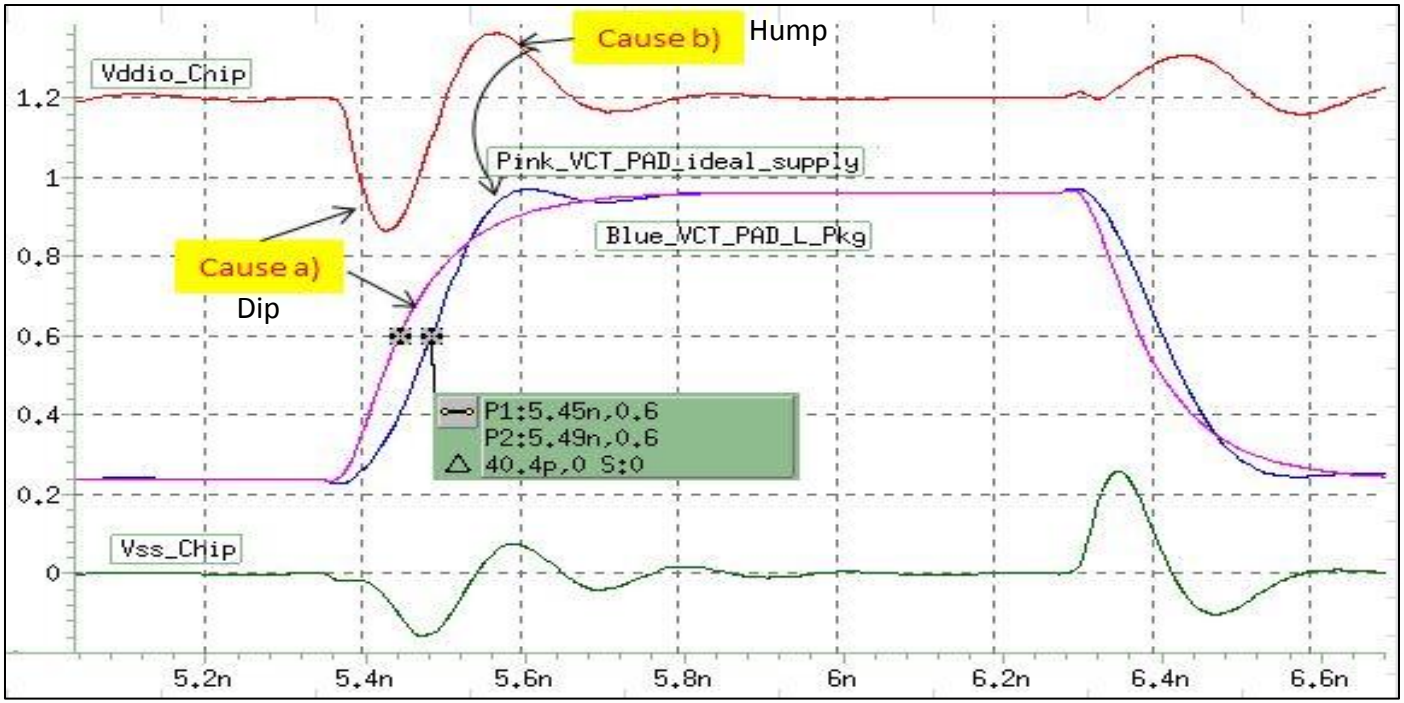
- Seven Aggressor IOs (AGR), One Victim IO (VCT)
- Both aggressor and victim IOs are having pseudo random pattern
- All AGRs having same pattern and is different than VCT



CLOAD = 2pf, 16pf
RTT = 50 ohms
IO_Drv = 33 ohms
L_PKG = 0.21nH
VDDIO_BALL = 1.2V
VTT = 0.6V

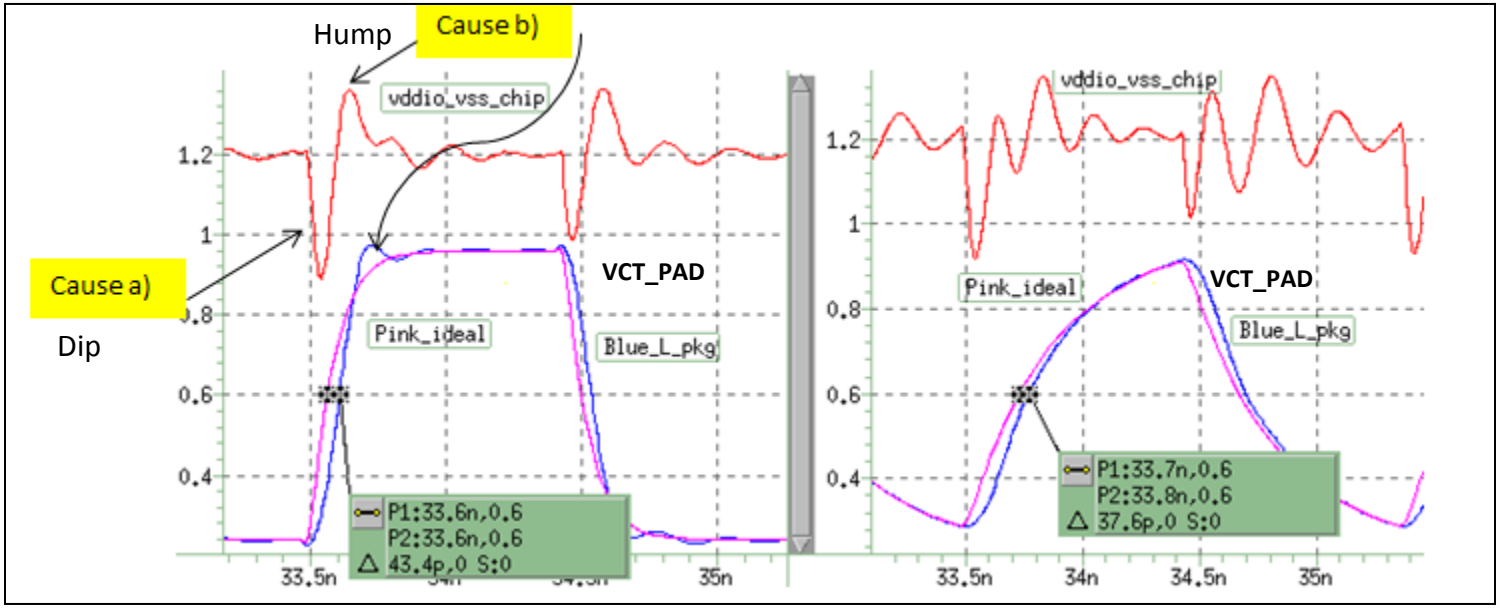
Two effects of Power Noise

- Consider a 0 →1 transition of aggressors, this causes a droop (cause a) in power followed by a hump (cause b)due to inversion of di/dt while Cload is getting charged *(For details, refer to back-Up slides #37)*
- Cause a) slows down the victim edges wherever droop hits the edge. This leads to period jitter over N-periods



Two effects of Power Noise

- Cause b) tries to make the edge fast and compensate for the effect of cause a).
- In case, load is small or rise time is fast, it is cause a) that is primarily responsible for distorting the edge as a delay.
- Cause b) affects in the latter portion of rise, it can affect mainly slow rising edges.



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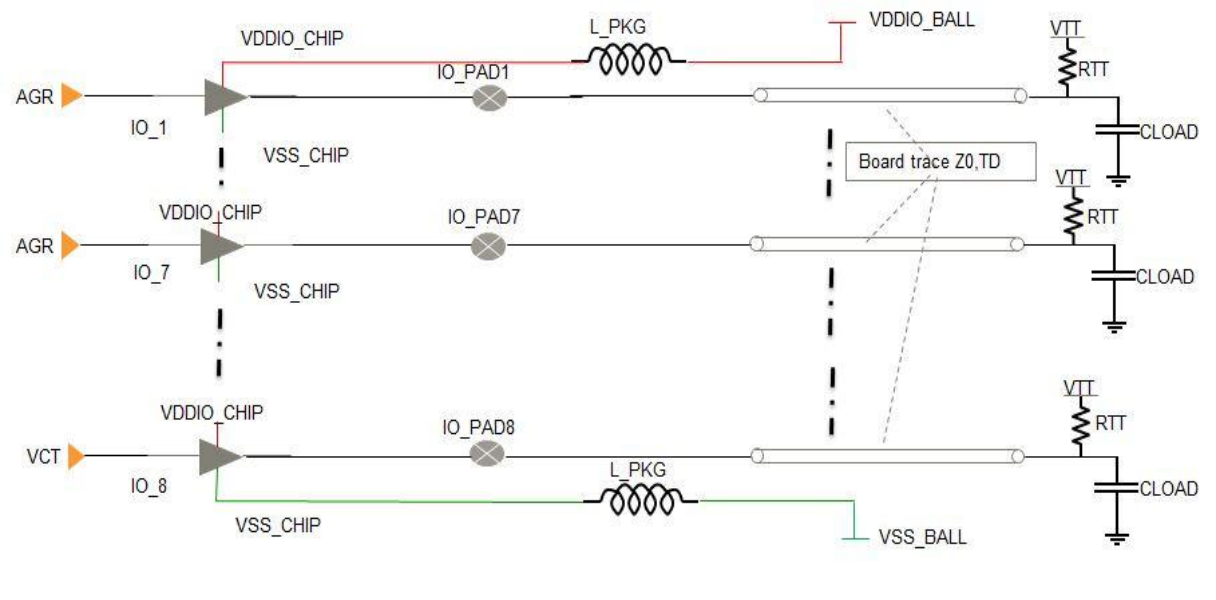
SSO Jitter in a setup with Transmission line

- The main goal is to see how to quantify SSO jitter in presence of transmission line
- To quantify SSO jitter, we first need to see how power noise gets modulated in presence of transmission line
- From previous section, cause (a) corresponds to first voltage droop during any transition
- Considering the fact that droop in supply occurred due to cause (a) we will mainly focus on voltage droop effects in the following slides

SSO setup in presence of transmission line

- In the same setup as used in previous section, a transmission line of Z0 = 50 ohms and length (TD) in terms of UI is varied.

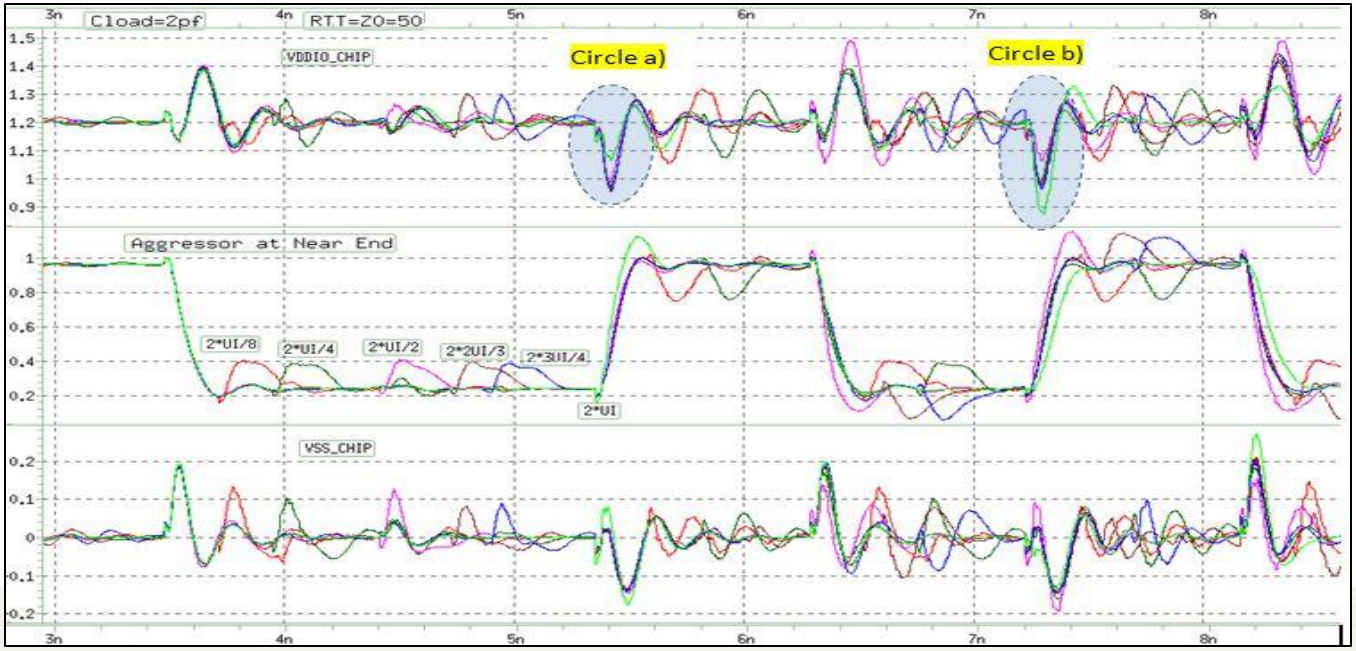
- Power Noise need to be measured at different TD values and different load conditions (Cload=2pf, 16pf and RTT=50 ohms, 120 ohms).



CLOAD = 2pf, 16pf
RTT = 50 ohms, 120 ohms
IO_Drv = 33 ohms
L_PKG = 0.21nH
VDDIO_BALL = 1.2V
VTT = 0.6V
Data Rate = 1067Mbps
1 UI = ~937ps
Z0 = 50 ohms

Power Noise in presence of transmission line

- If length of transmission line TD=x.UI, the noise generated at near end will occur after 2*x.UI time the transition occurred
- For TD << UI/2, transmission line will not modulate this power noise
- For TD ~ UI/2, the modulated power will be least
- For TD ~ UI, Power noise is worst and equals to power noise when Cload is connected directly at IO Pad
  - This can be generalized as TD ~ (1+N/2)*UI where N is an integer



Summary of Power Noise

Modulation of Power Noise at edges (0101…)				
	RTT=Zo=50		RTT=120, Zo=50	
	Cload =2pf	Cload = 16pf	Cload =2pf	Cload =16pf
TD	Droop (mV)	Droop (mV)	Droop (mV)	Droop (mV)
First edge	229	229	270	270
UI/8	220	224	262	228
UI/4	212	160	260	150
UI/2	120	100	80	120
2UI/3	224	301	160	308
3UI/4	228	308	180	352
1UI	328	361	376	424

Overall Worst Case Power Noise				
	RTT=Zo=50		RTT=120, Zo=50	
	Cload = 2pf	Cload = 16pf	Cload = 2pf	Cload =16pf
TD	Droop (mV)	Droop (mV)	Droop (mV)	Droop (mV)
First edge (Cload @ IO PAD)	360	409	397	443
UI/8	256	262	303	277
UI/4	252	278	300	286
UI/2	245	256	267	295
2UI/3	255	310	275	326
3UI/4	267	319	298	352
UI	358	395	391	442

- Power noise will always be less than lumped Cload at IO Pad unless TD ~ (1+N/2)*UI where N is an integer
- Higher Cload causes transmission line to modulate power noise much earlier depending on the pattern *(See Backup slide # 38 for details)*
- With 120 ohms RTT, For TD > UI/2, the modulation of power noise reduces as now there will be initially –ve reflection due to Cload and then +ve reflection because of RTT (120) being higher than Z0 (50) *(See Backup slide # 39 for details)*
- Above table can also be explained using load transformation [1]. For TD ~ UI/2 (λ/4), load will be inverted, for TD ~ UI (λ/2), far end load appears at near end

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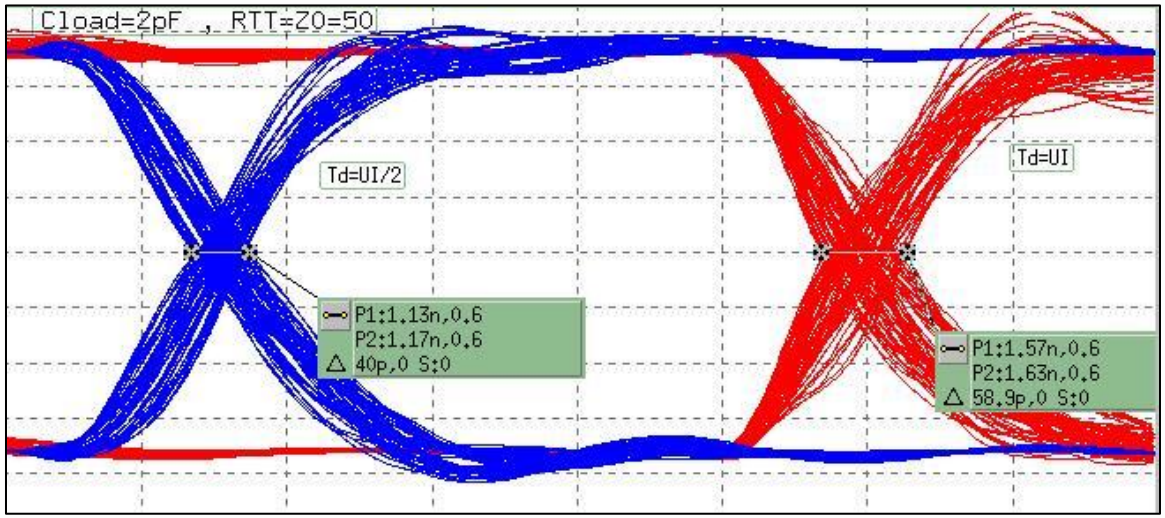
SSO Jitter due to Power noise generated by transmission line of two different lengths

- 50% increase in jitter at Cload=2pf, with increase in transmission line length Td from UI/2 to 1UI



Effect of far end Cload on SSO Jitter

- To see the effect of Cload on SSO jitter we will consider a test case where droop has highest difference between Cload of 2pf and Cload of 16pf; So we take a case when TD=2UI/3 and measure the jitter at Cload

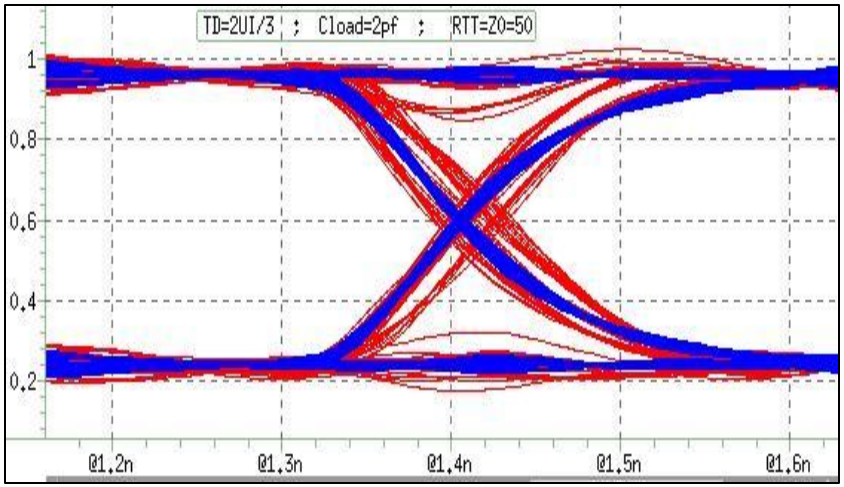
	RTT=Zo=50		RTT=Zo=50	
	Cload =2pf		Cload =16pf	
TD	Droop (mV)	SSO Jitter[1] at Cload (ps)	Droop (mV)	SSO Jitter[1] Cload(ps)
2UI/3	224	43	301	4

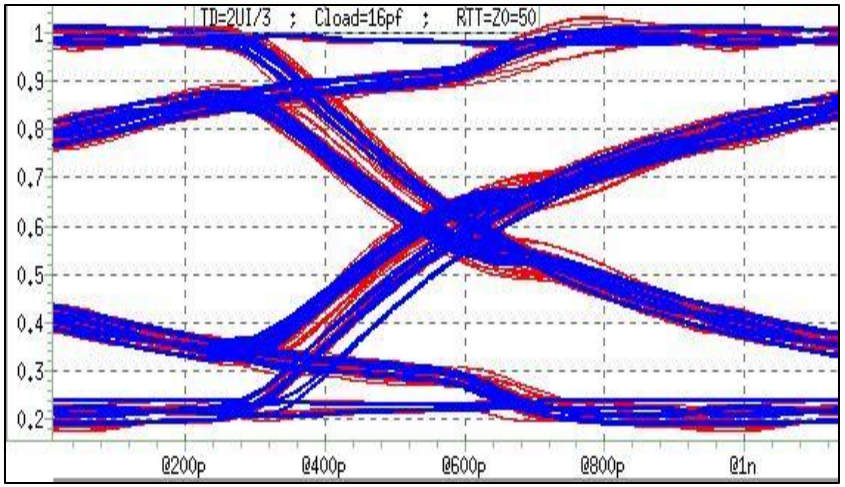
- We can see that although the droop on 16pf load is high but the SSO jitter at Cload is negligible – explained in next slide

Note 1: SSO Jitter is the delta increase in jitter due to power supply noise.

Effect of far end Cload on SSO Jitter

- Below (left) is the eye diagram of victim signal in a lightly loaded (Cload=2pf) system and (right) is the Eye diagram of victim signal in a heavily loaded (Cload=16pf) system





- Difference in SSO jitter at Cload is because of the fact that effective rise time at load is given by equation $T_{\text{rise composite}} = \left(T_1^2 + T_2^2 + \cdots + T_N^2\right)^{1/2}$ [3]
- With higher Cload, the effect of degradation in rise time has lesser impact at far end compared to near end

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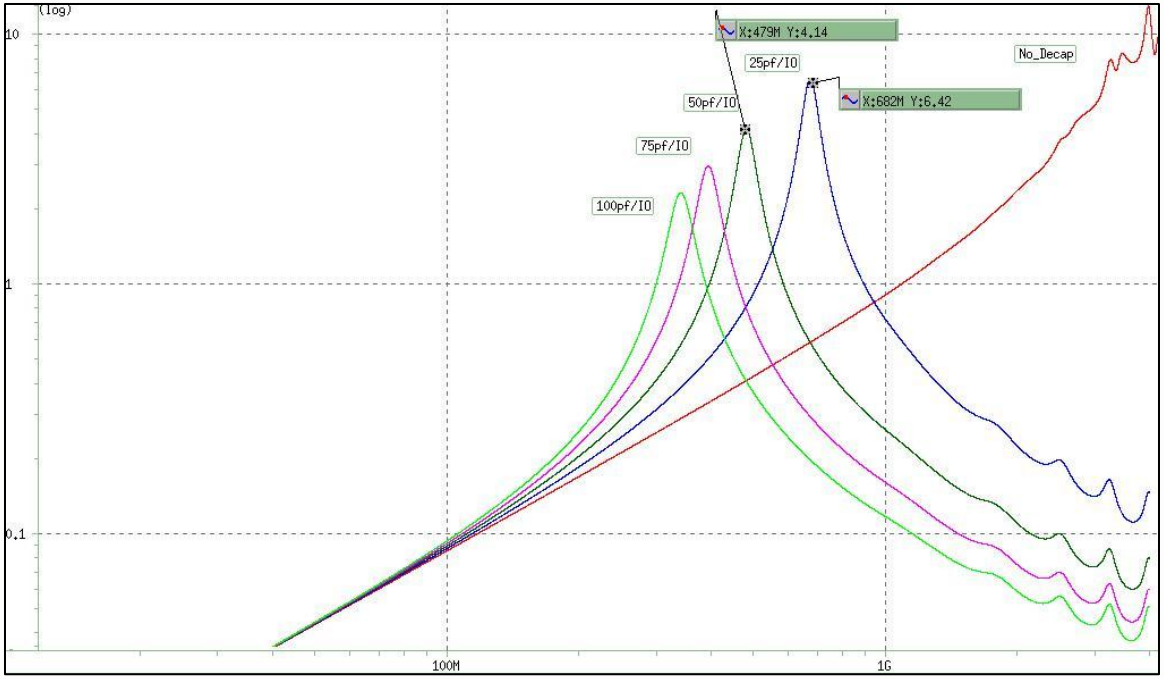
Effect of OCDs on PDN

- System Z11 seen from Die side with different value of OCD



- Adding decaps lower the impedance at high frequency but brings the resonance peak to the lower frequency

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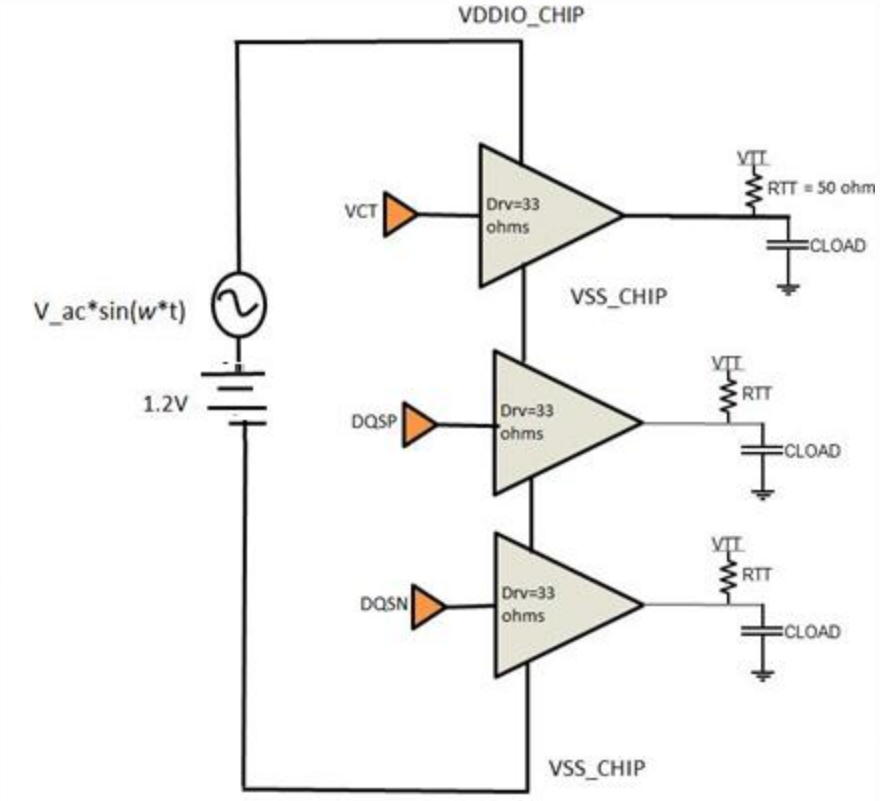
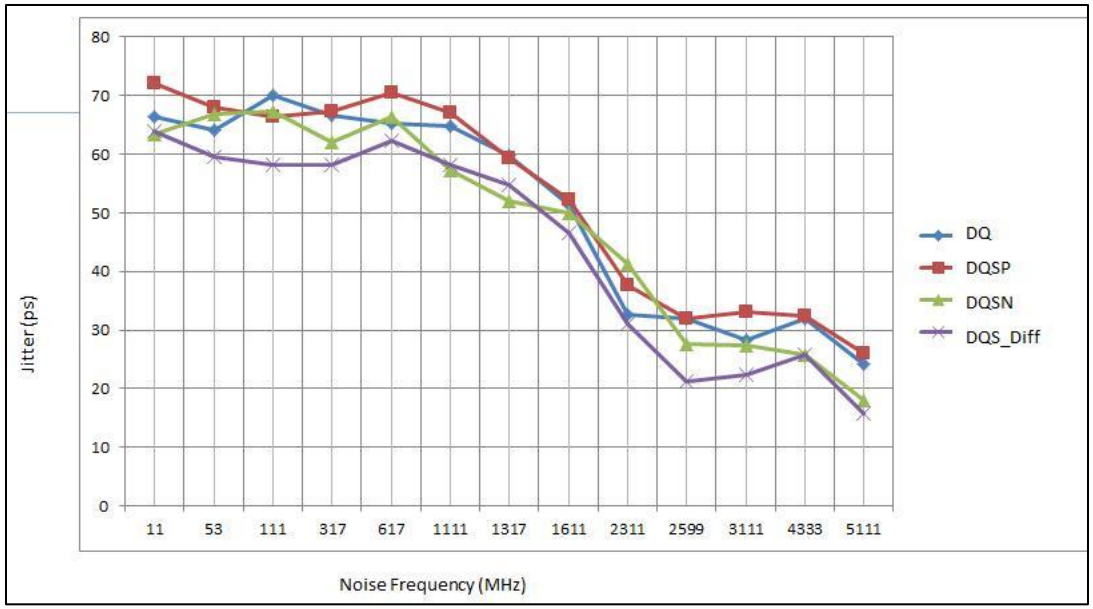
Effect of pdn generated noise on Timing

- PDN generated noise can be considered as forced voltage noise across IO supply
- Setup to see effect of voltage noise of different frequencies on a lumped Cload:



Effect of pdn generated noise on Timing

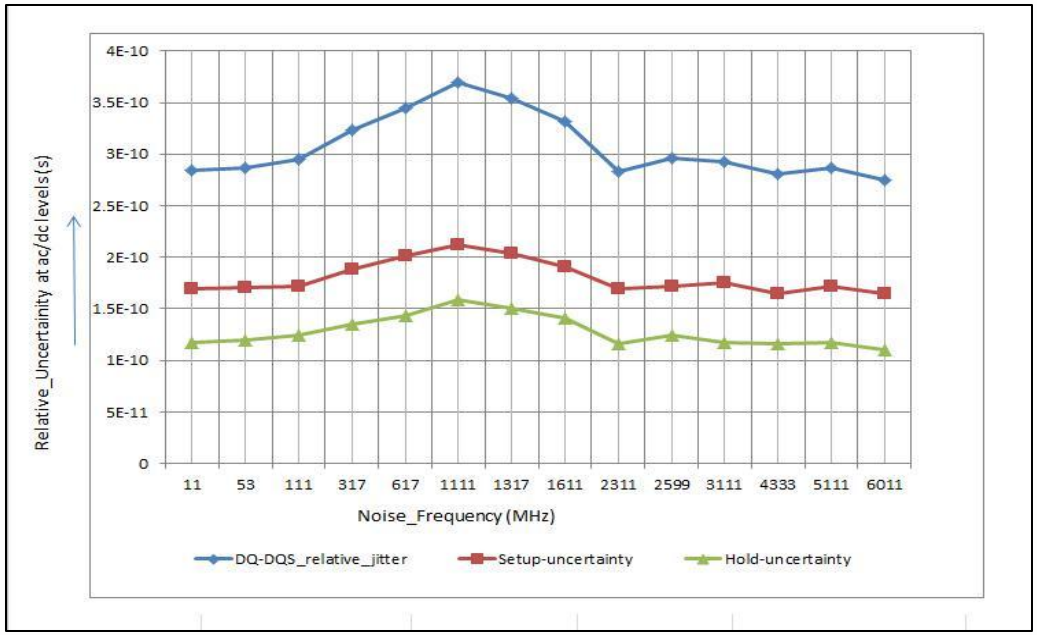
- Pk-Pk Jitter vs. input sinusoidal Noise of 100mV amplitude at different frequencies



- IO intrinsic stray capacitance is the main reason as the curve doesn't change much at different data rates *(see Backup slide #40 for details)*

Effect of pdn generated noise on Timing

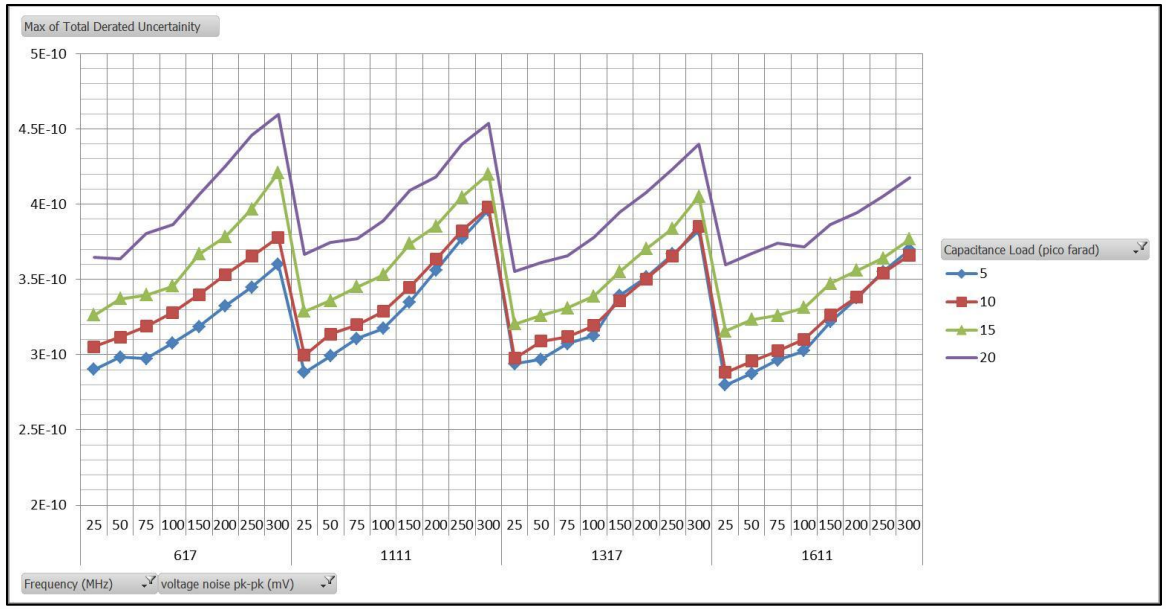
- Relative Jitter between DQ and Differential DQSP/DQSN



- Strobe is 90 degree phase shifted w.r.t data, so the mid-range frequencies close to data rate will see highest relative jitter
- Since data rate considered here is 1067 Mbps, the relative jitter increases up to 1067 MHz of noise frequency. After that as standalone jitter decreases (as shown in fig.10) the relative jitter also starts decreasing quickly

Effect of Decap on Timing

- To see if there is any effect of Cload w.r.t noise, we swept Cload from 5pf to 20pf



- There is only constant offset of jitter between different load conditions
- Change of jitter w.r.t change in voltage noise is almost linear and is independent of Cload

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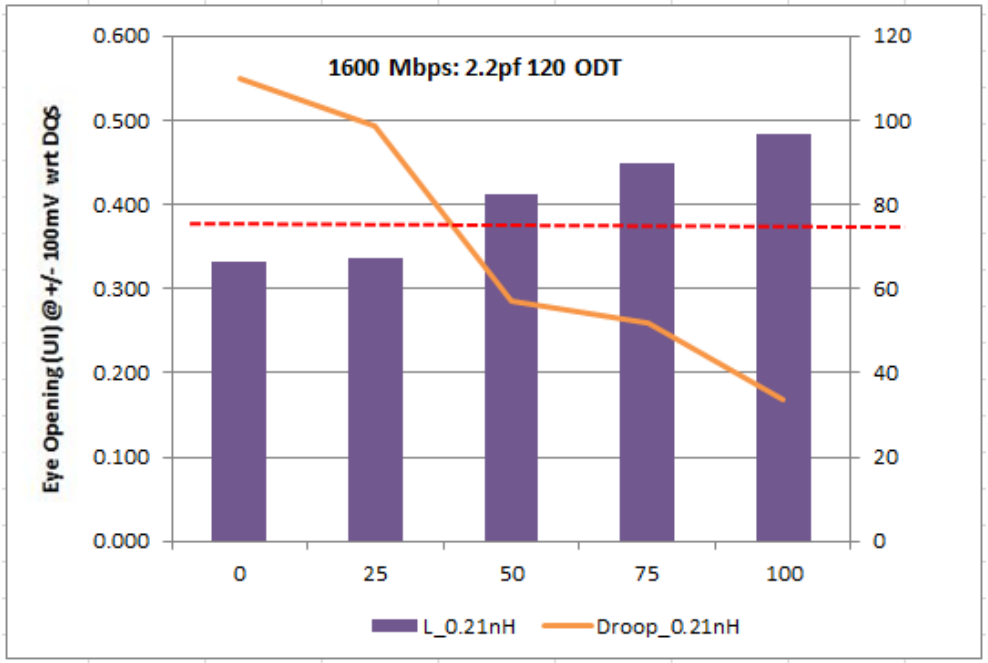
SSO simulations on actual system with lighter Cload (2.2pf) @ 1600Mbps

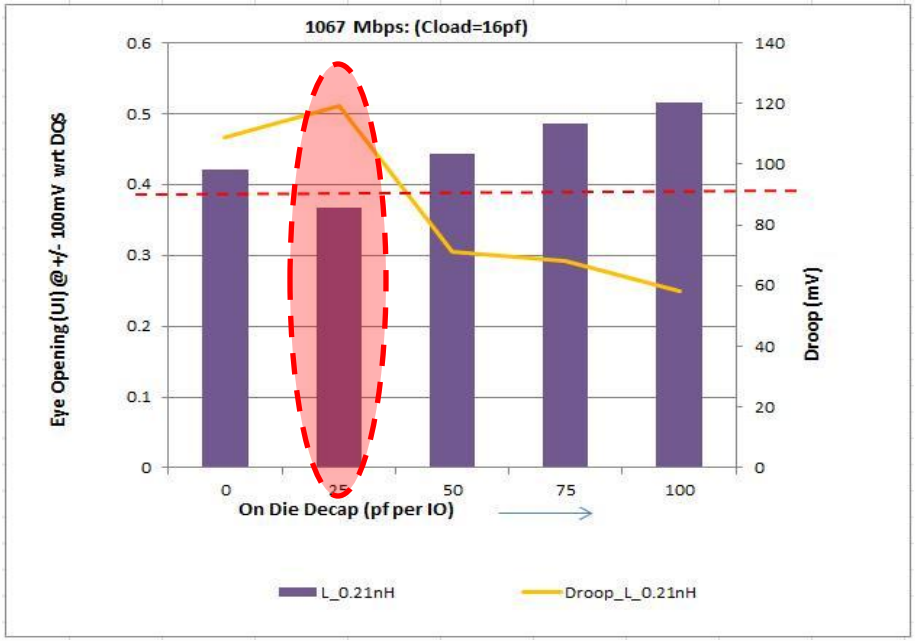
- On an actual system with Cload of 2.2pf @ 1600Mbps, RTT=120 ohms, TD=1.35UI, L_pkg=0.21nH, OCD value from 0pf/IO to 100pf/IO was swept



- Since the Cload is low, we see that Eye opening is directly proportional to droop

SSO simulations on actual system with heavier Cload (16pf) @ 1067 Mbps

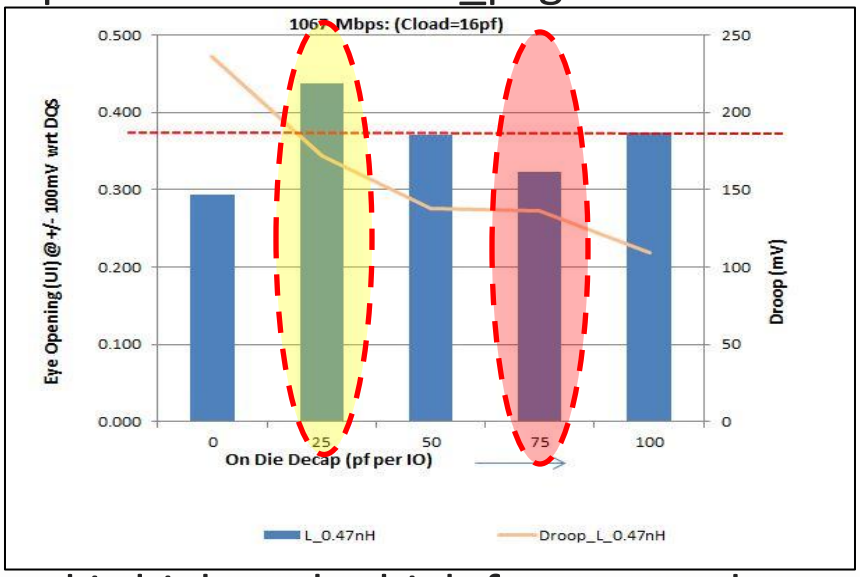
- On an actual system with Cload of 16pf @ 1067Mbps, RTT=50 ohms, TD=0.63UI



- In previous section (PDN plot), for the value of 25pf/IO, the resonance peak comes at 682Mhz. Using 50pf/IO, the resonance comes to 479MHz
- Also seen that for 1067Mbps data rate, the resonance caused by 682MHz peak lie in the noise-jitter curve where it has more impact than any other OCD value

Heavy Cload (16pf) @ 1067 Mbps with package of higher loop inductance

- Same setup as in previous slide but L_pkg increased from 0.21nH to 0.47nH



- As L_pkg increased is higher, the high frequency droop (L.di/dt) will be higher
- Adding decaps is reducing voltage droop
- Due to higher L_pkg, and with 25pf/IO decap, z11 resonant peak comes below 300MHz, so its effect on jitter is less
- Adding decap more than 25pf/IO shows mixed trend in Eye opening (anomaly to be studied as part of *future work*)

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Steps to follow to decide OCD value

1. Understand transmission line length effect (Ref Slide 16)
   - For lightly loaded systems, transmission line length of delay UI/2 will give the least droop at edges and hence least jitter; So for systems having this kind of characteristics, doesn't need big amount of decap if the concern is interface timing only

2. Understand Cload effect on timing delay (Ref Slide 18)
   - If Cload is high and power noise doesn't show significant increase (because of transmission line length or IO architecture), then effect of power noise on jitter will be very less and can be judged by a percentage increase in delay of edges; If this delay is negligible, the decap can be totally avoided without any impact on timing

3. Understand the effect of Noise Spectrum on Jitter (Ref Slide 20-25)
   - If the system configuration doesn't meet the requirement of above two steps to decide on OCD value, or in case of OCD is required to avoid glitch on asynchronous signal (not for timing), PDN curve should be plotted along with noise to jitter / relative uncertainty curve
   - If FFT of current from any previous design is available, the pdn noise prediction can be more accurate
   - Decap value should be chosen such that value of jitter shouldn't exceed direct jitter specs such as period jitter, pulse width distortion along with relative uncertainty between data and strobe

4. Understand OCD trend (Ref Slide 27-28)
   - Lastly, if current FFT or noise-jitter plot is not available, SSO simulations by sweeping OCD values on the required system is to be done – verifying droop, jitter and relative uncertainty for reliable operation of the system

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Future Work

- The effect of cause (b) mentioned in slide #9 should be studied in detail so that optimum decap value can be predicted more accurately
- Relation between power noise and frequency domain is to be proven by taking FFT of currents
- Different IO architectures need to be considered like IOs where pre-driver dominates the L.di/dt, delay between pre-driver and driver switching, linearity of IO etc.

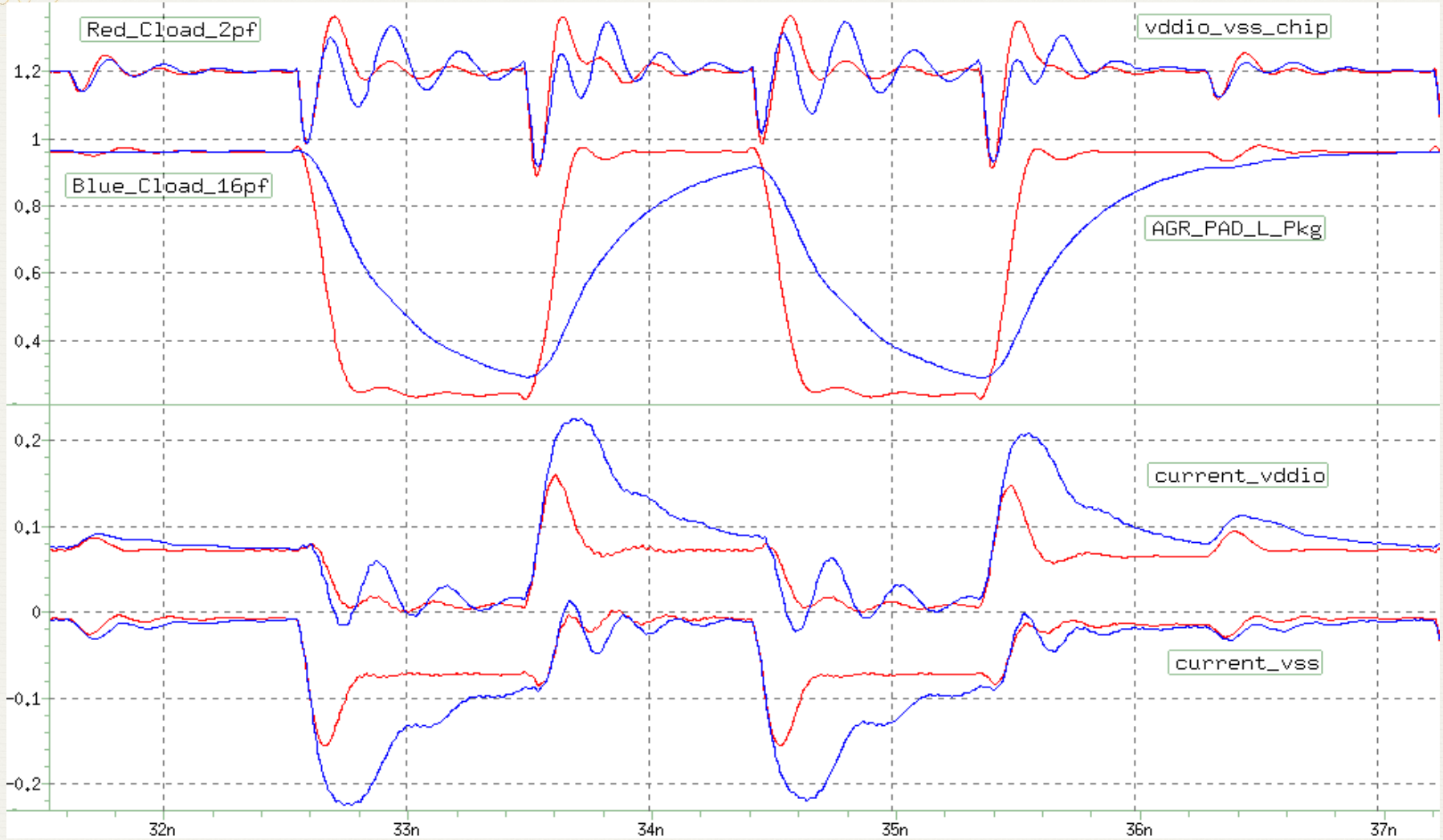
References

- [1] William H. Hayt, “Engineering Electromagnetics - Sixth Edition”, The McGraw Companies
- [2] James R. Andrews, “Time Domain Reflectometry (TDR) and Time Domain Transmission (TDT) Measurement Fundamentals”, Application Note AN-15Copyright November 2004
- [3] Johnson and Graham, “High-Speed Digital Design: A Handbook of Black Magic”, Prentice-Hall, 1993
- [4] Istvan Novak, “Power Distribution Network Design Methodologies”, Professional Education International, Inc.
- [5] Iliya Zamek, “Modeling FPGA Current Waveform and Spectrum and PDN Noise Estimation”, DesignCon 2008

Q&A

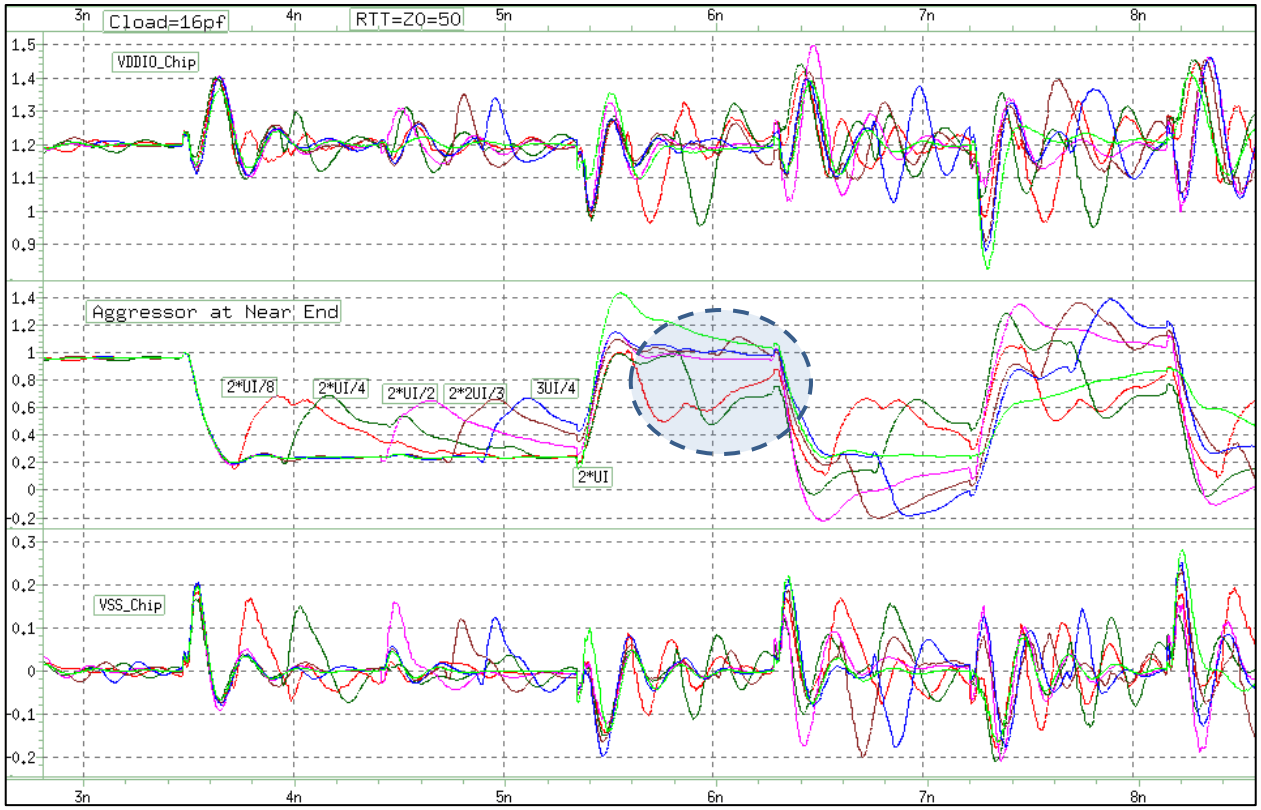
Backup

Current and Power Noise at two different load conditions



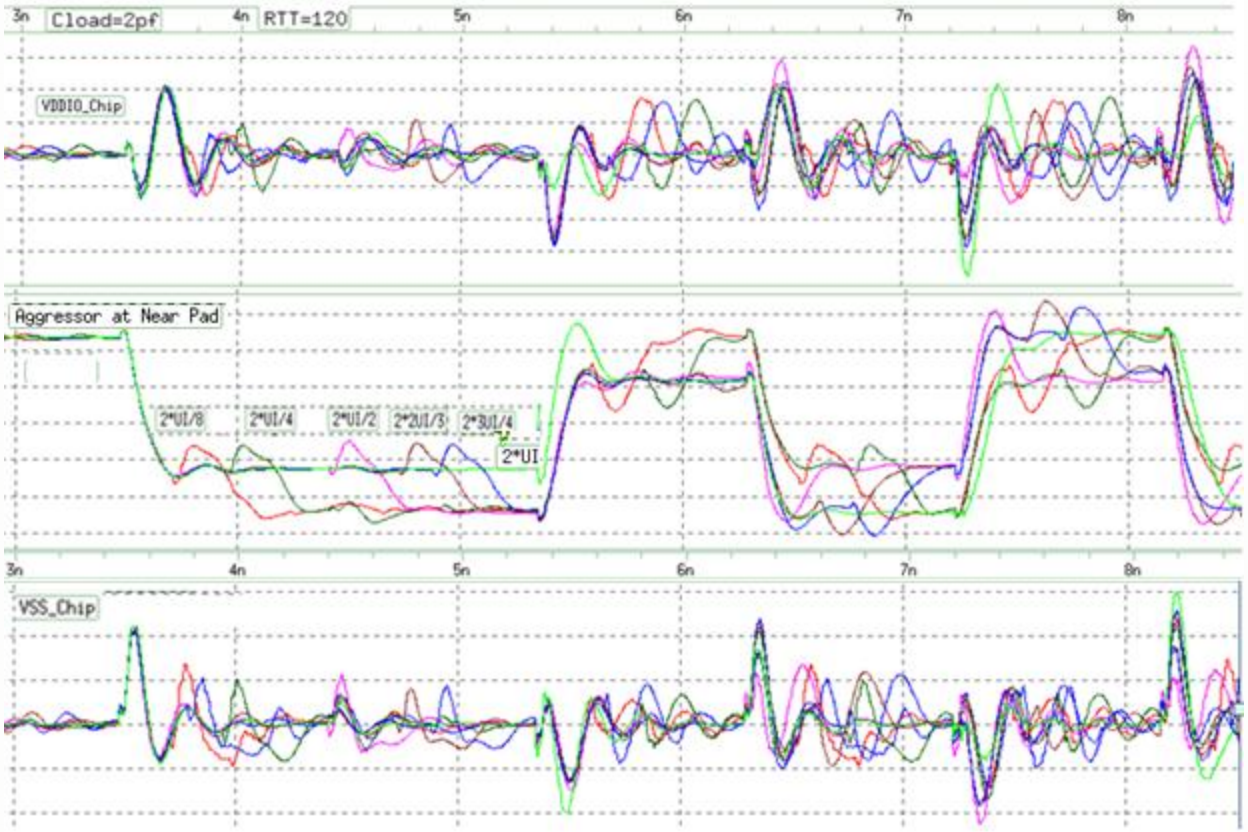
Power Noise in presence of transmission line (Higher Cload=16pf)

- Higher Cload causes transmission line to modulate power noise much earlier depending on the pattern. As shown in encircled area TD <=UI/4

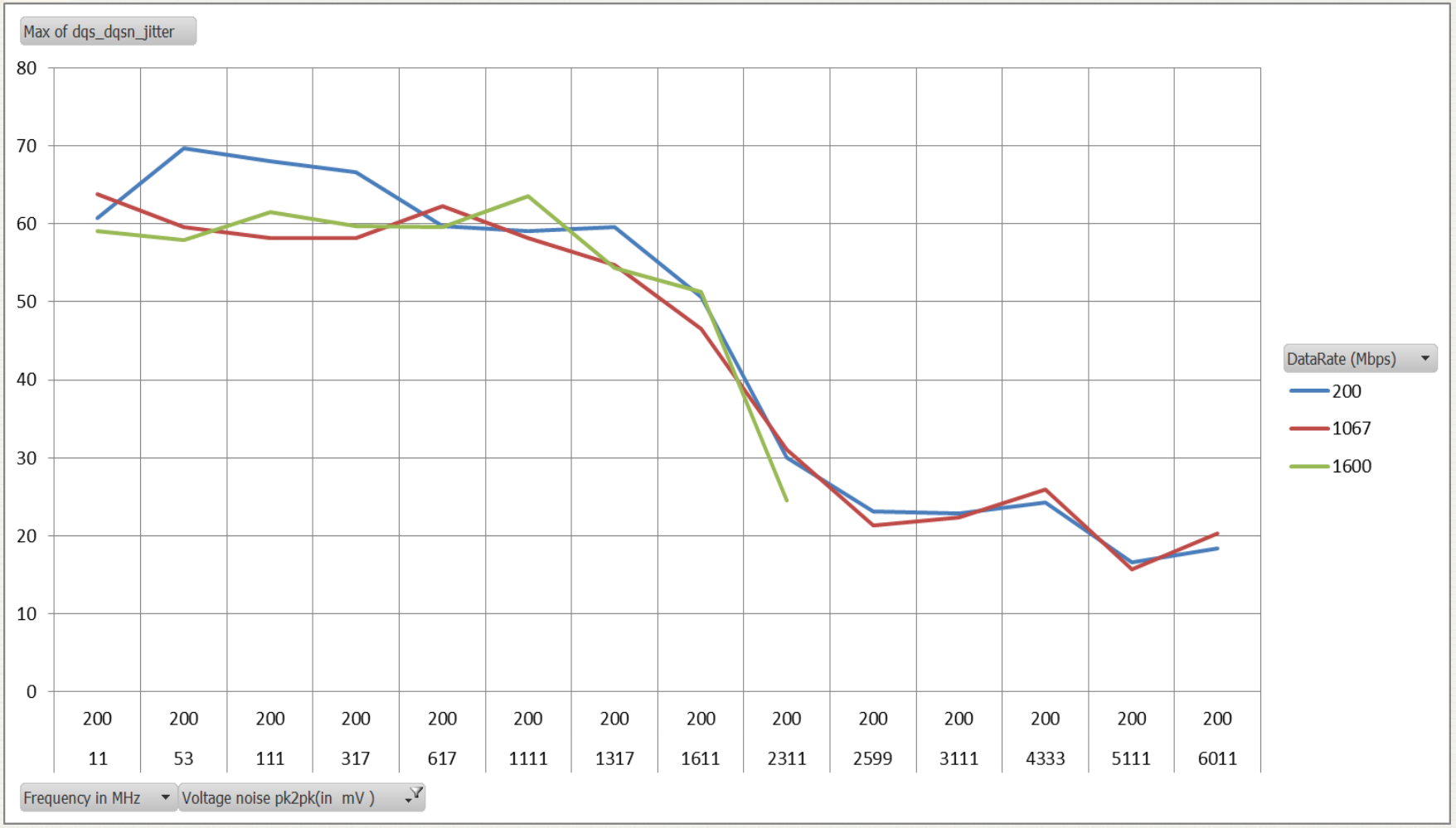


Power Noise in presence of transmission line (Higher RTT=120 ohms, Cload=2pf)

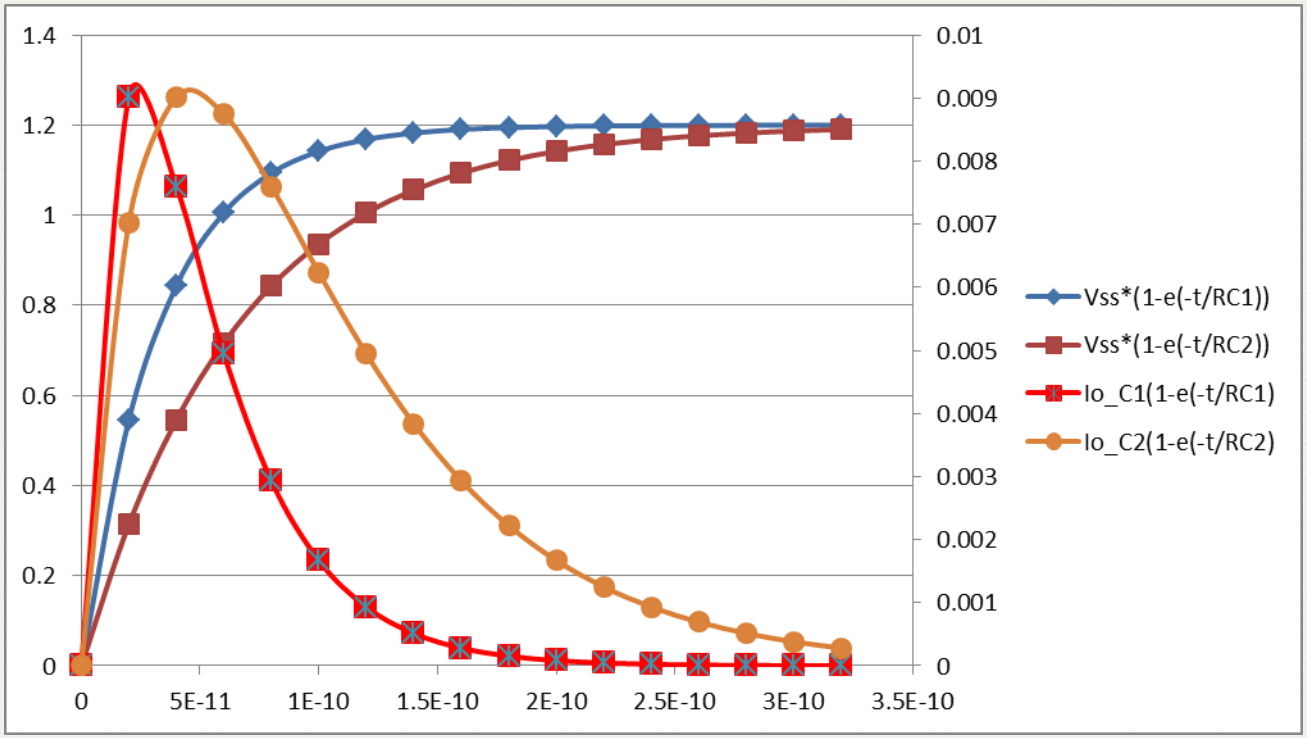
- With 120 ohms RTT, For TD > UI/2, the modulation of power noise reduces as now there will be initially –ve reflection due to Cload and then +ve reflection because of RTT (120) being higher than Z0 (50).



Jitter vs Power Noise @ different data rates

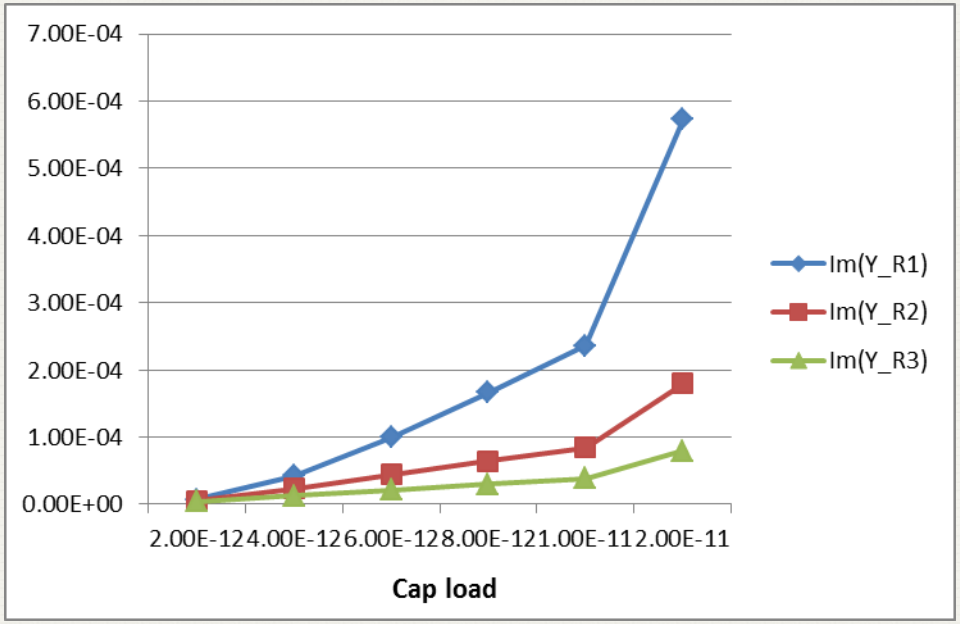


Current and Voltage relationship during charging



R	C1	C2
33	1.00E-12	2.00E-12
Vss	RC1	RC2
1.2	3.3E-11	6.6E-11

Current dependency on cap load and driver resistance



Drv_R1	Drv_R2	Drv_R3
18	33	50

Thank You