

## Method for Troubleshooting Power Integrity Problems in Programmable Logic Device Electronic Systems by Embedded Measurement of Power Distribution Impedance

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# Outline

Overview of Power Distribution Networks (PDN)

PDN Failure Mechanisms

PDN Troubleshooting Techniques

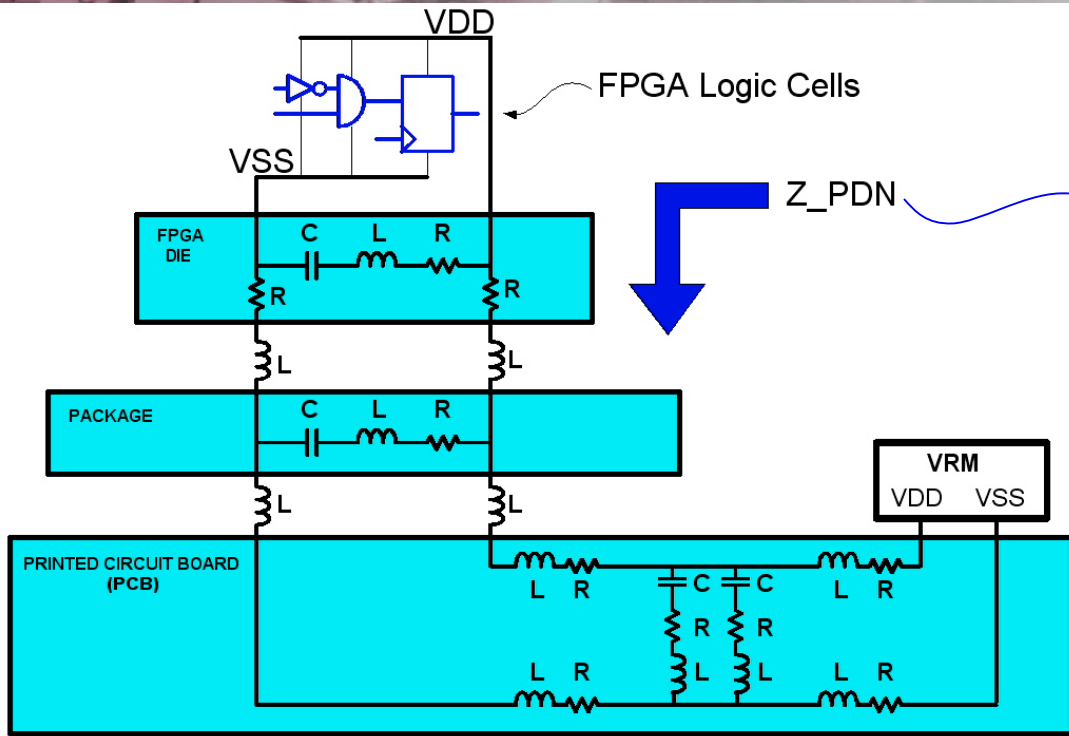
Proposed PDN Troubleshooting Method

Embedded On-Die PDN Impedance Measurement

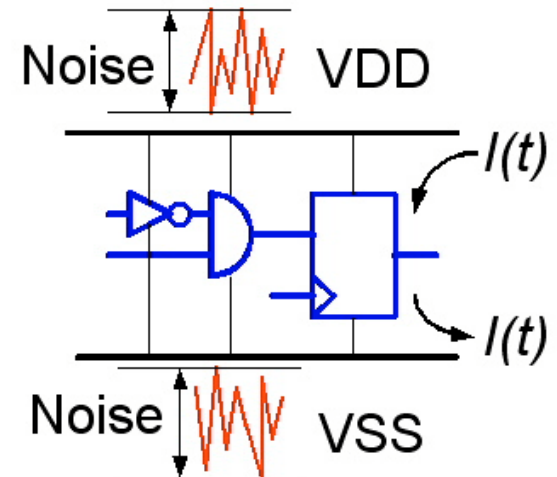
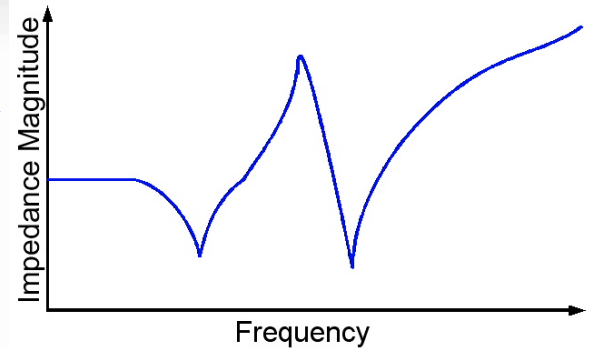
Case Study Implemented in a Spartan 3A FPGA

Conclusions

# Overview of Power Distribution Networks



## PDN Impedance



Transient currents flowing through PDN impedance generate noise on power supply rails

# PDN Failure Mechanisms

## PDN Failure Types

### Total PDN Failure

- Easy to detect
- Can be addressed using standard troubleshooting techniques

### PDN Performance Degradation

- System level performance degradation
- System level “indirect” failures
- Sometimes failures are intermittent
- Hard to detect
- Difficult to troubleshoot

# PDN Failure Mechanisms

## PDN Failure Types

### Total PDN Failure

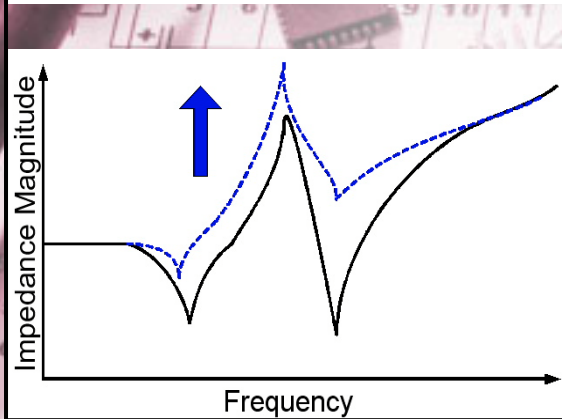
- Easy to detect
- Can be addressed using standard troubleshooting techniques

### PDN Performance Degradation

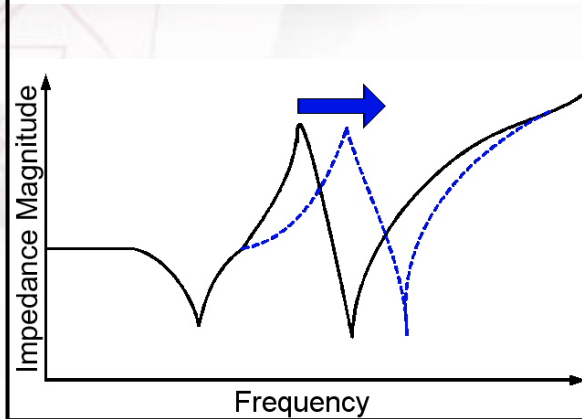
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- Difficult to troubleshoot

# PDN Performance Degradation

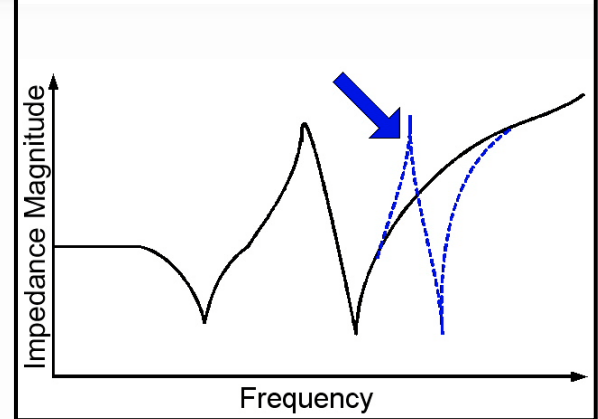
Increased impedance at some frequencies



Existing resonance peaks may shift in frequency



Additional resonance peaks may appear

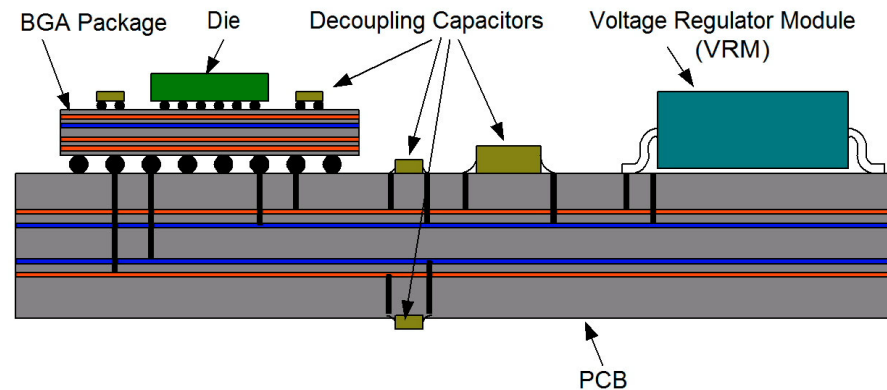


- The increase in PDN impedance increases the noise on power supplies
- New or frequency shifted resonance peaks may now coincide with chip operating frequencies generating significant supply noise

# Troubleshooting PDN

These types of problems and especially open circuit capacitors, open vias or solder joints, and increased series resistance are in general hard to identify using common test instruments due to:

1. redundant / parallel power supply current paths
2. multiple decoupling capacitors connected in parallel

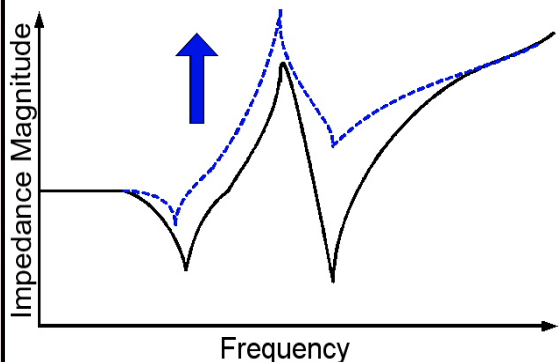




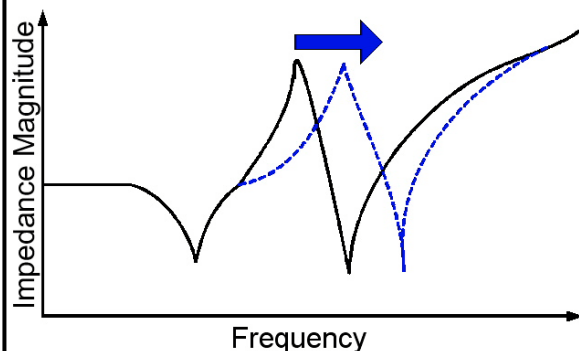
# Troubleshooting PDN - What are we looking for?

We want to be able to detect any increase in PDN impedance and the frequency location and magnitude of resonance peaks.

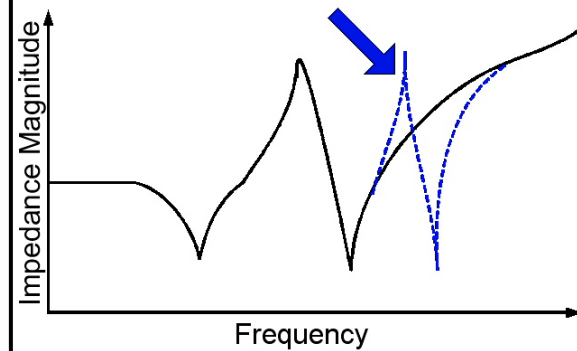
Increased impedance at some frequencies



Existing resonance peaks may shift in frequency



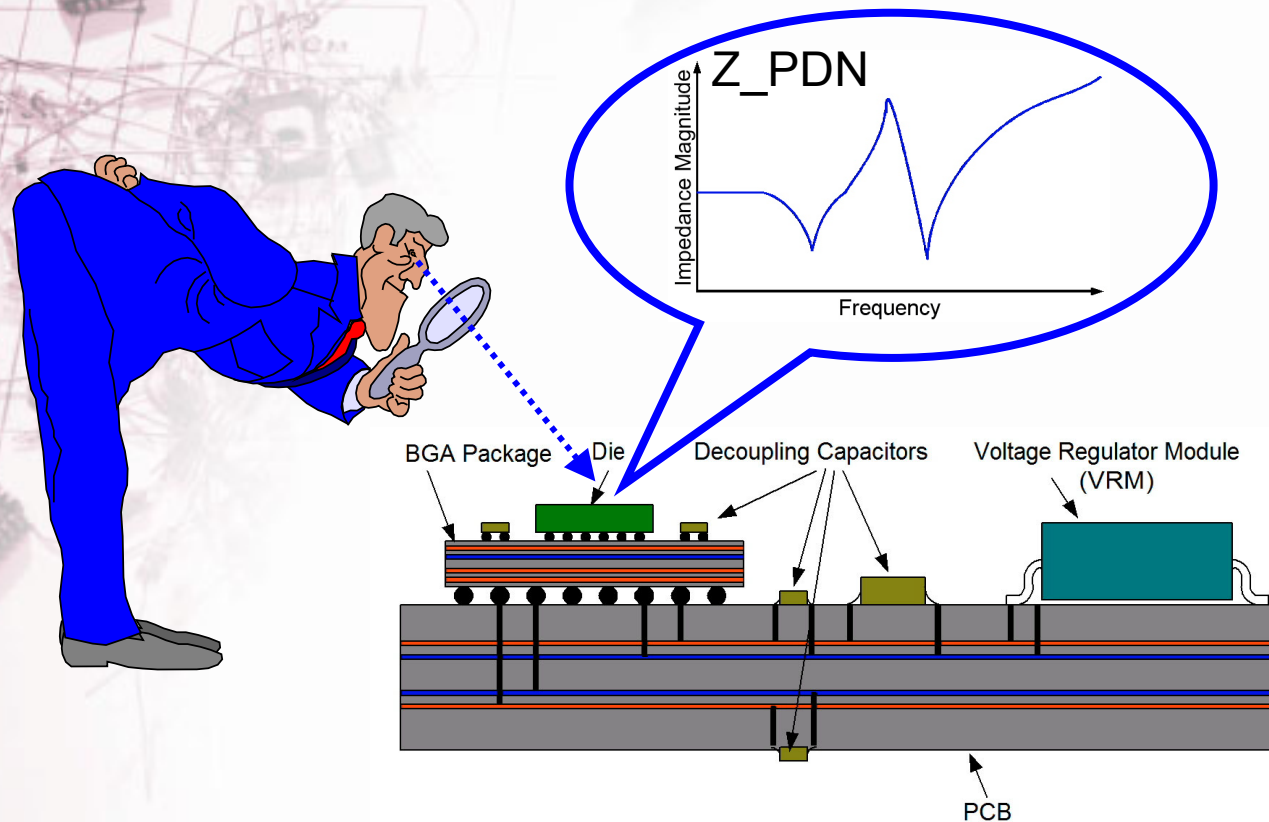
Additional resonance peaks may appear





# Troubleshooting PDN - What do we need?

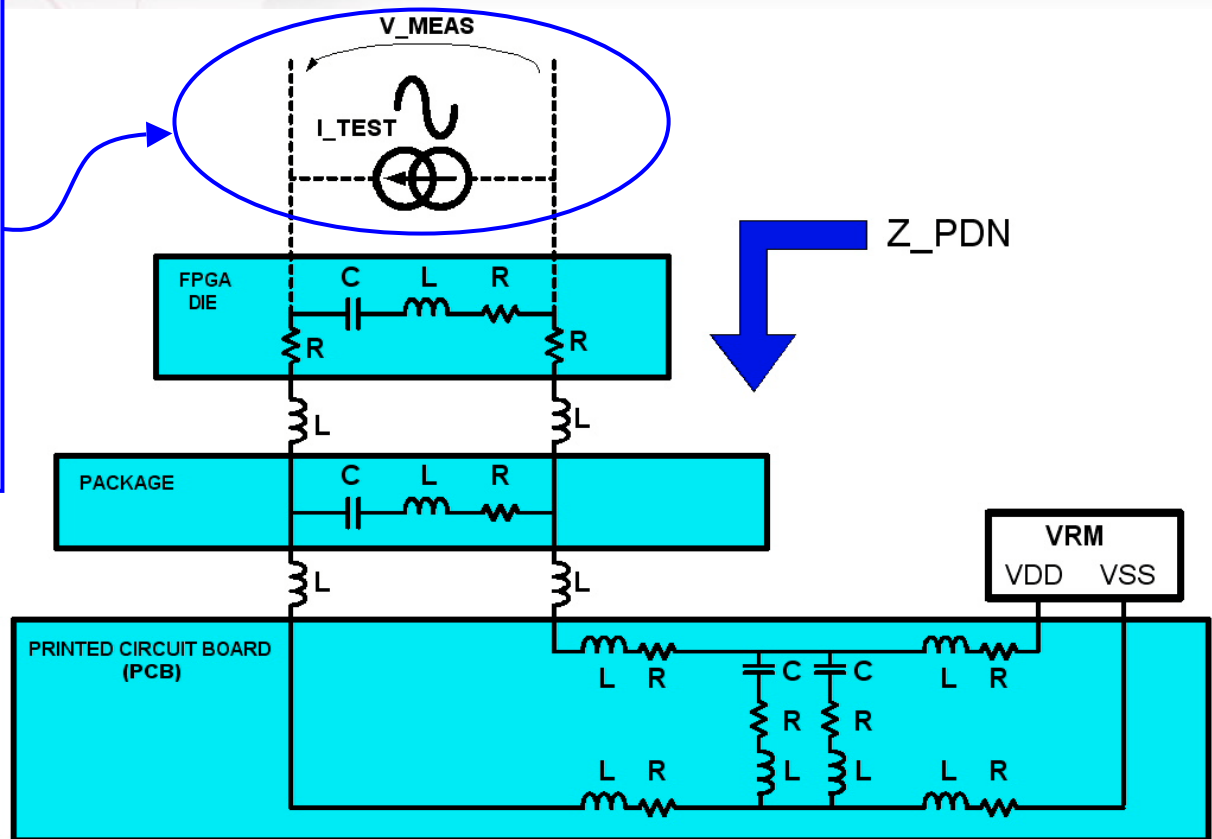
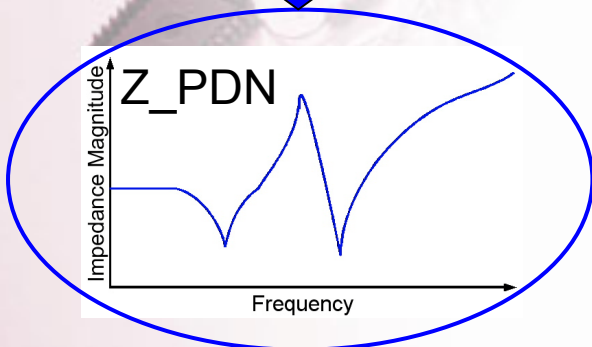
We need to get access to the PDN impedance frequency profile as seen by the logic circuits on the FPGA / PLD die.



# Proposed PDN Troubleshooting Technique

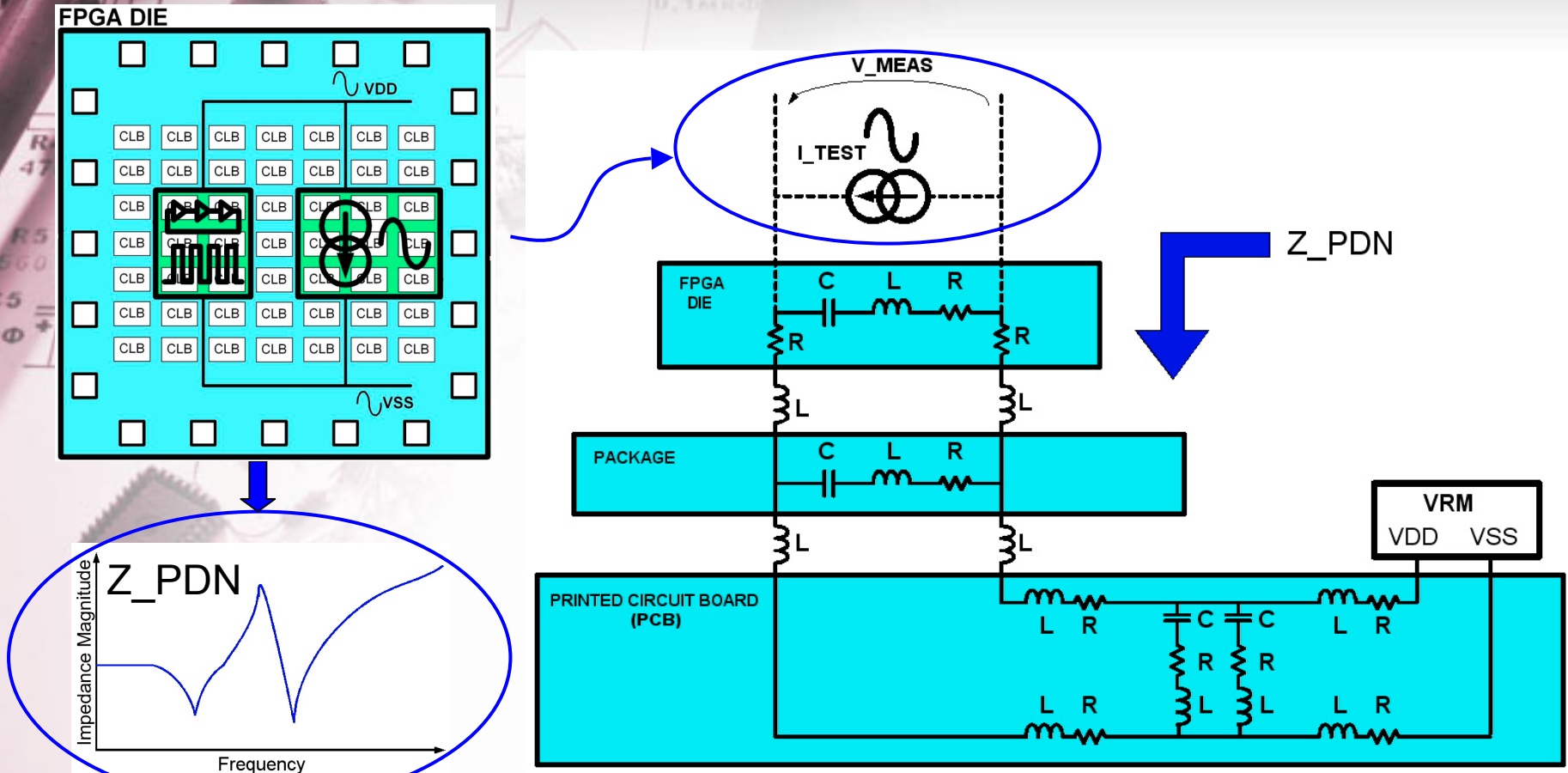
## AC Steady State Analysis

AC steady state analysis connects a sinusoidal current source to the measured port and records the voltage drop while sweeping the sinusoidal current frequency



# Proposed PDN Troubleshooting Technique

## AC Steady State Analysis



(patent pending technology)

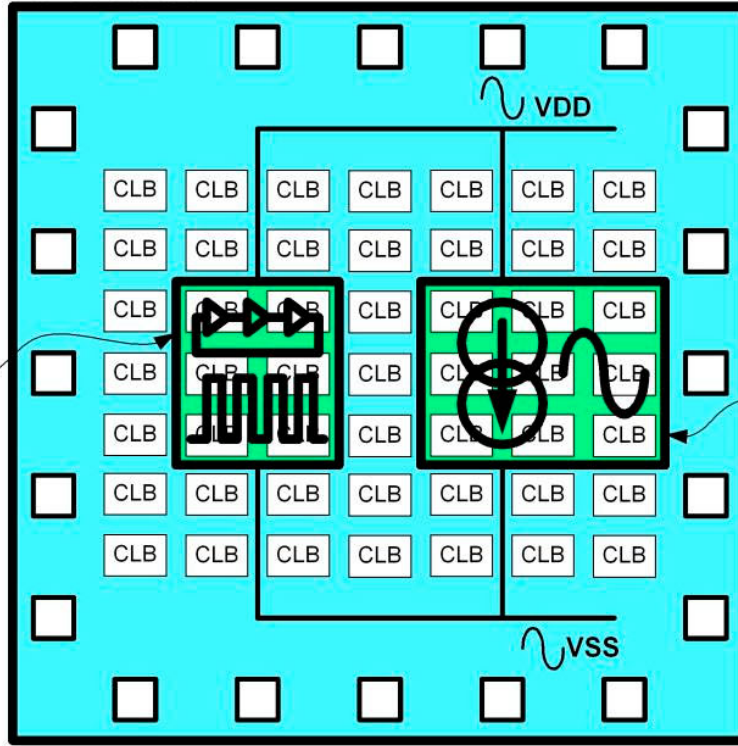
# Proposed PDN Troubleshooting Technique

## FPGA / PLD Implementation

### FM MODULATED RING OSCILLATOR

A group of FPGA logic blocks is configured to form a ring oscillator

### FPGA DIE

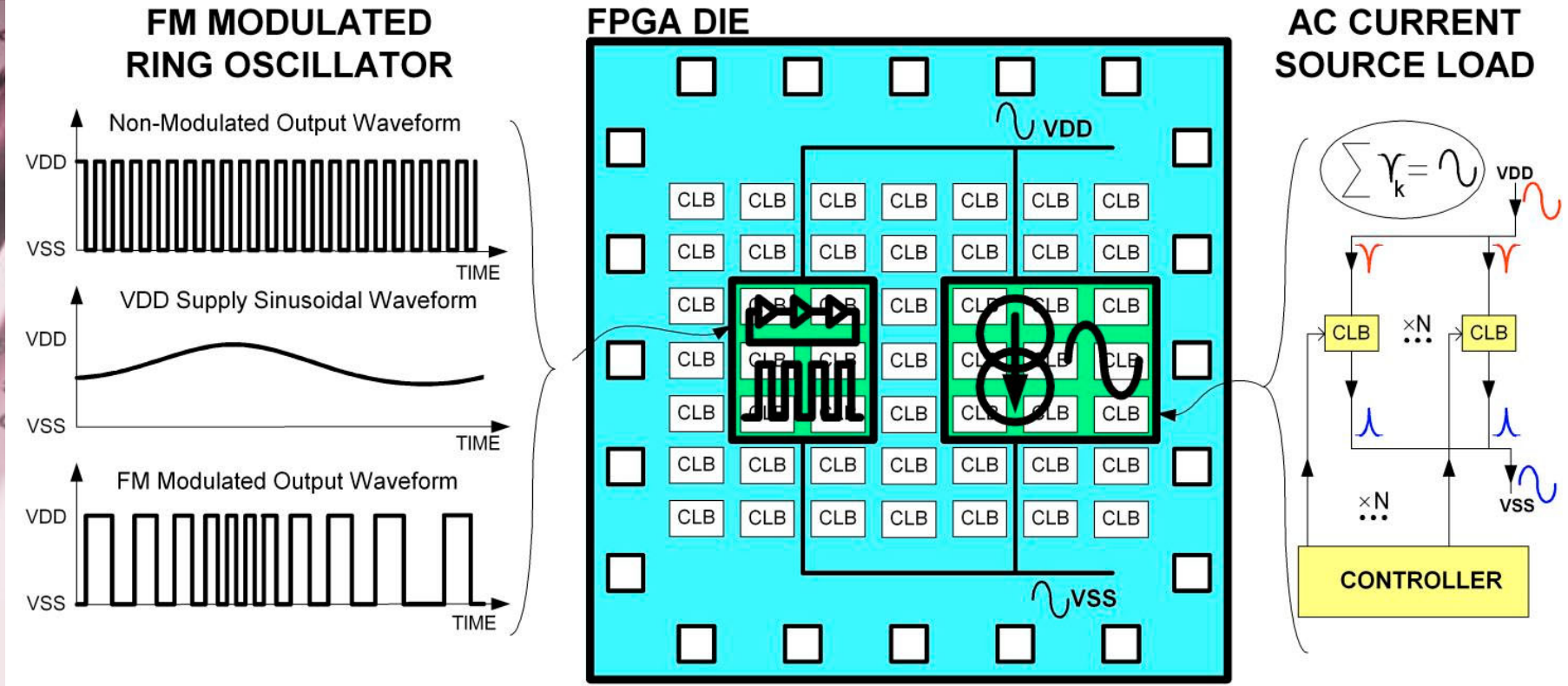


### AC CURRENT SOURCE LOAD

A group of FPGA logic blocks is configured to function as a sinusoidal current source

(patent pending technology)

# Proposed PDN Troubleshooting Technique

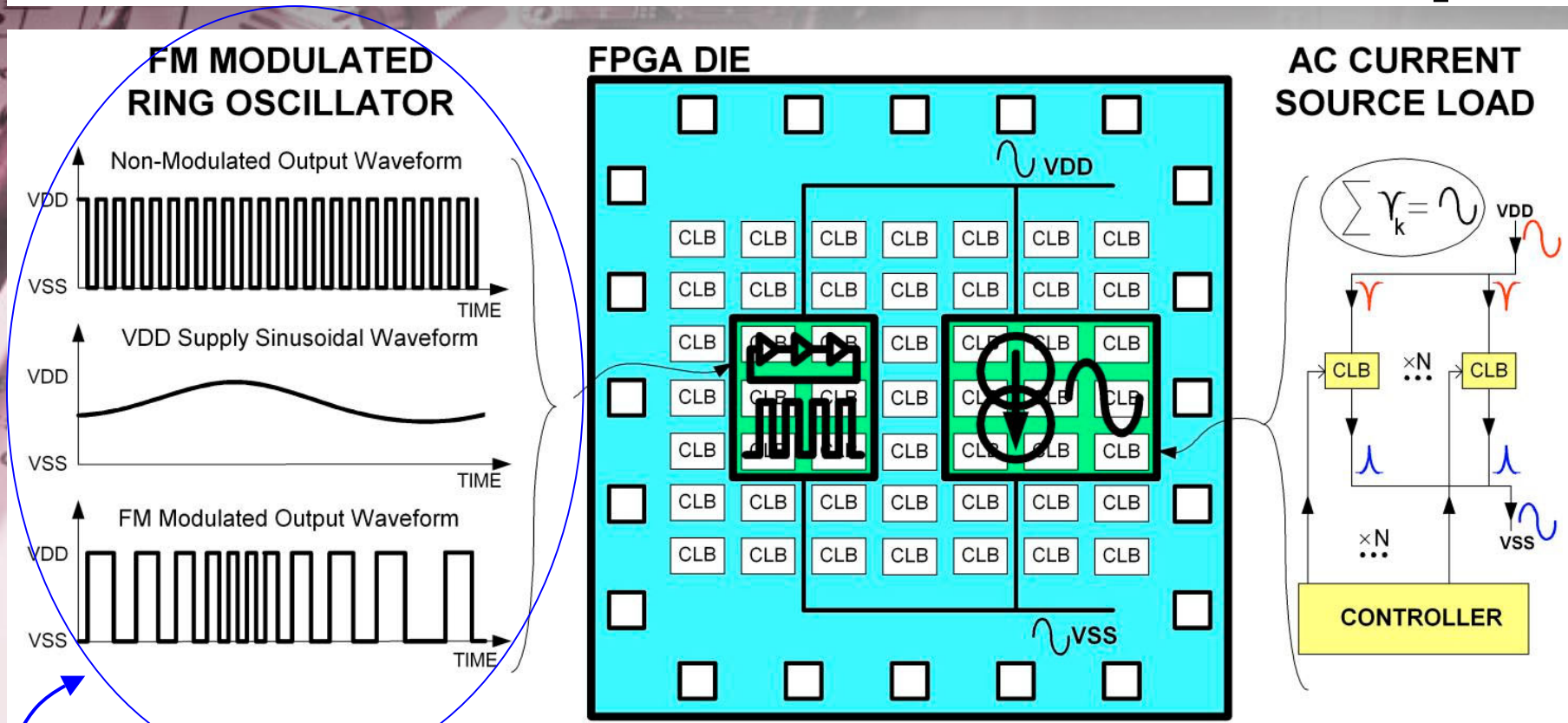


The sinusoidal current flows through the power distribution network and generates sinusoidal variation of the on-die power supply voltage

(patent pending technology)



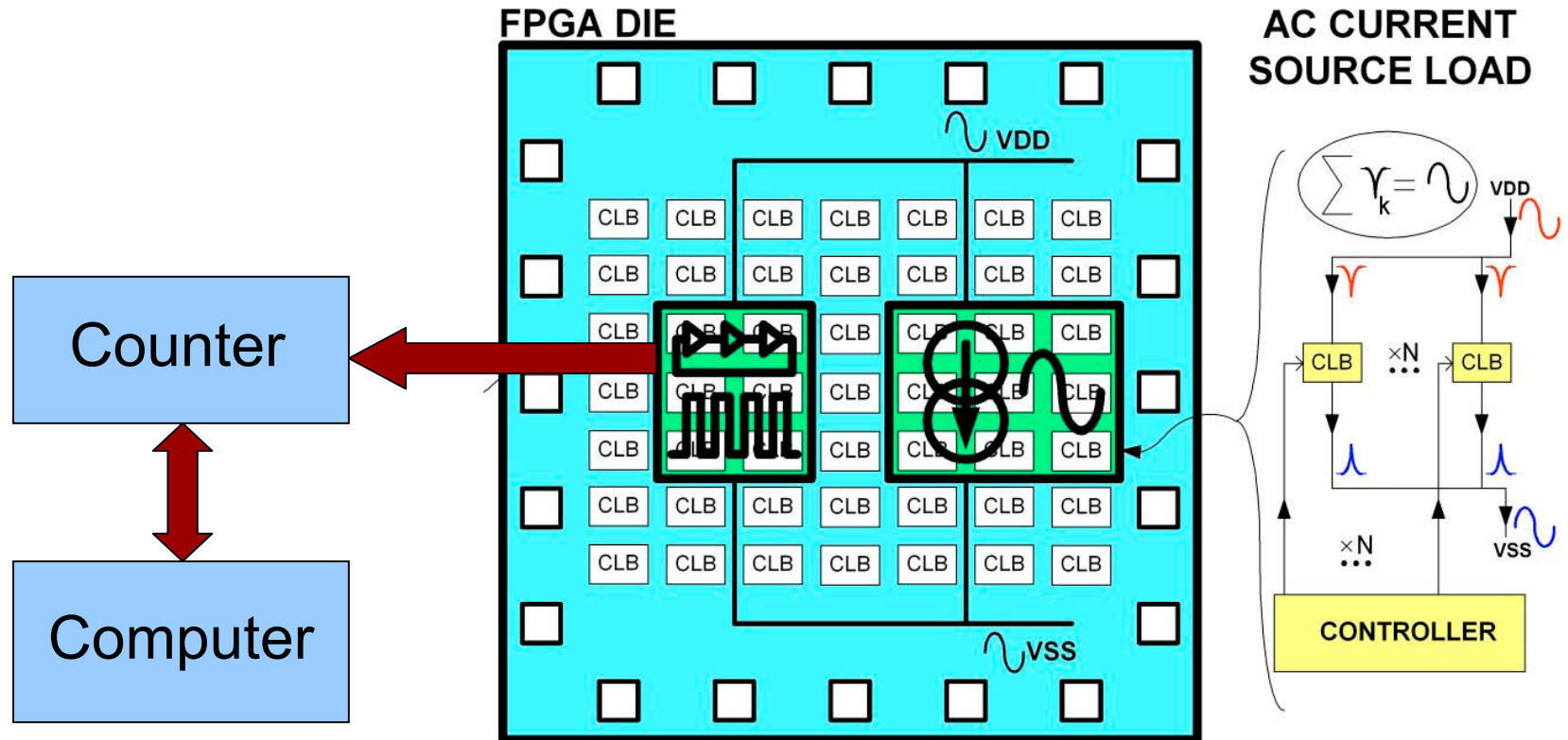
# Proposed PDN Troubleshooting Technique



The sinusoidal variation of the voltage supply modulates the frequency of the ring oscillator

(patent pending technology)

# Proposed PDN Troubleshooting Technique



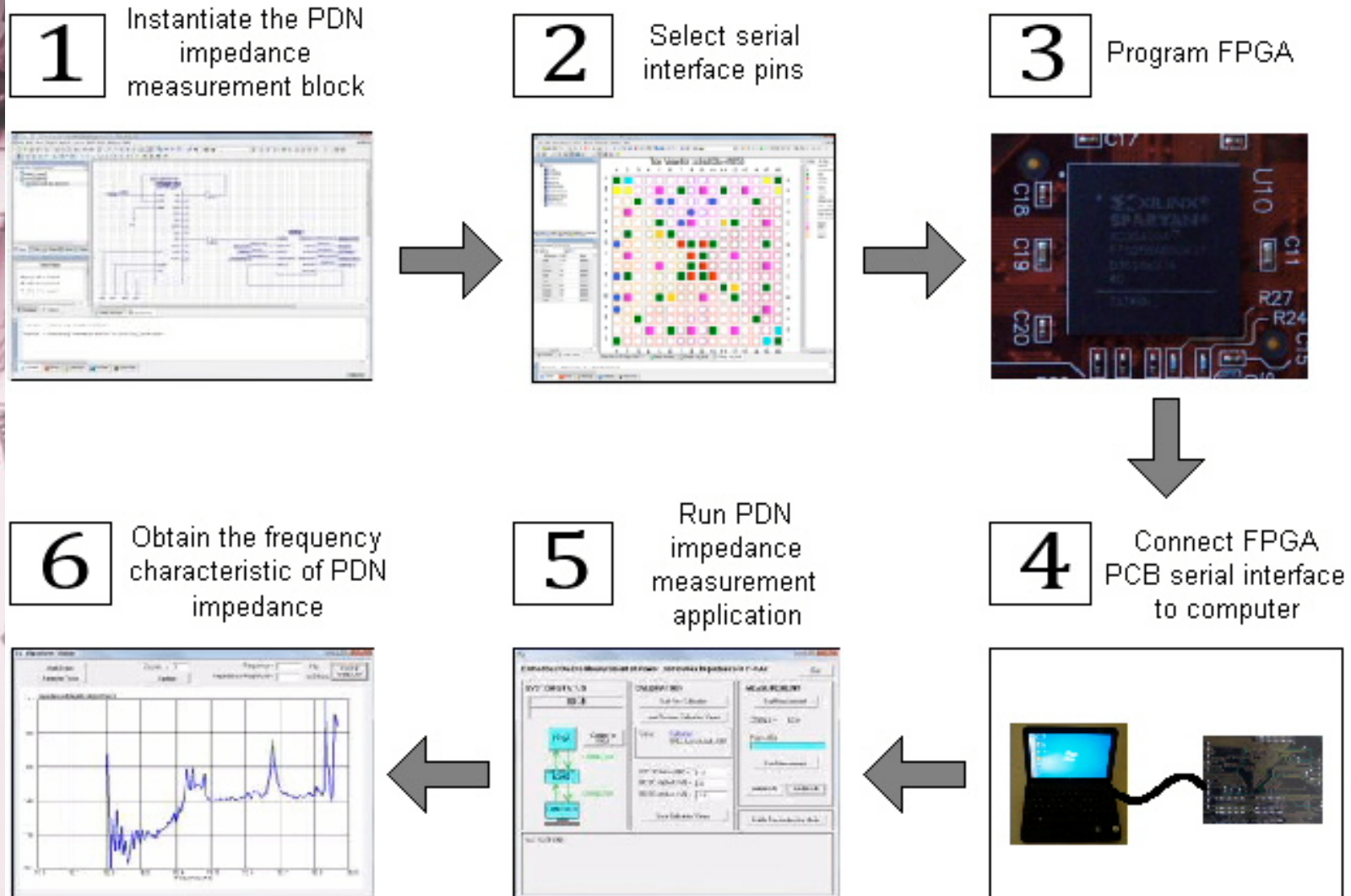
A counter circuit measures the frequency of the ring oscillator

PDN impedance is calculated from the average frequency deviation

(patent pending technology)



# Device Configuration and Measurement Process



# Case Study

- The proposed PDN troubleshooting technique has been implemented in a Spartan 3A FPGA on a test board
- PDN impedance frequency profile has been measured at frequencies up to 500MHz
- Various PDN failure mechanisms have been intentionally induced in the test board
- The proposed PDN troubleshooting technique has been used to detect each induced PDN failure mechanism

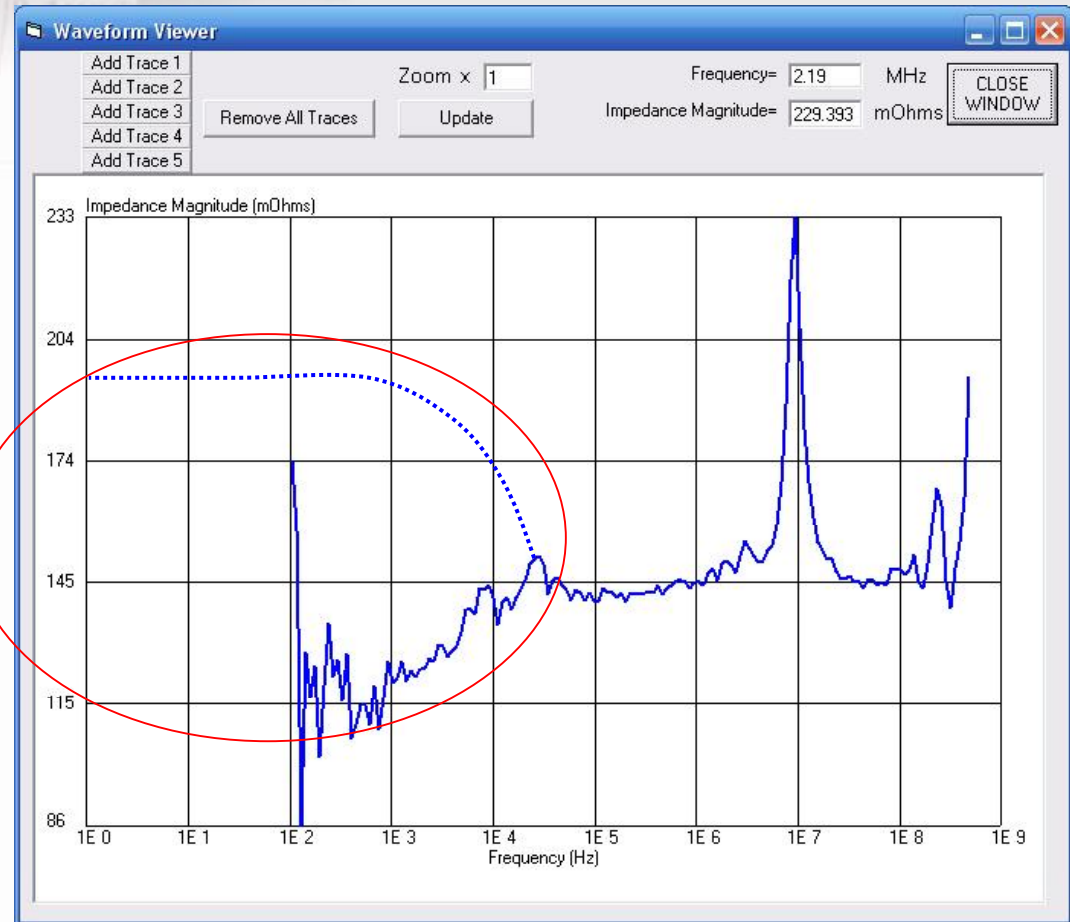
# Case Study

## Measured on-die PDN impedance frequency profile

Measurement up to 500MHz

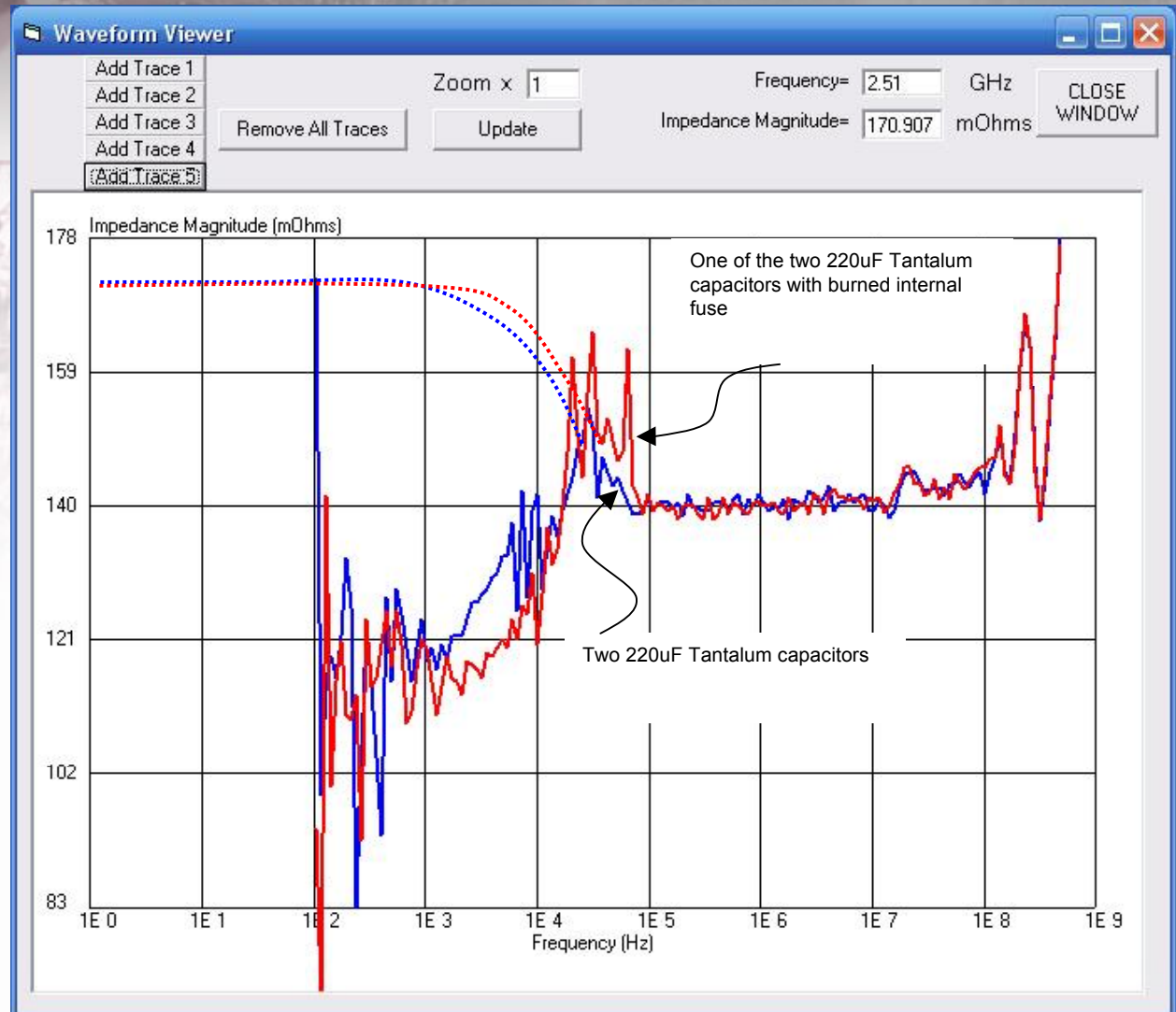
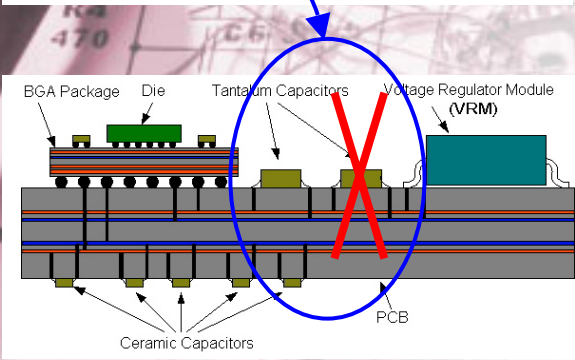
Not accurate below 20kHz

Accuracy can be extended below 20kHz with the expense of increased measurement time

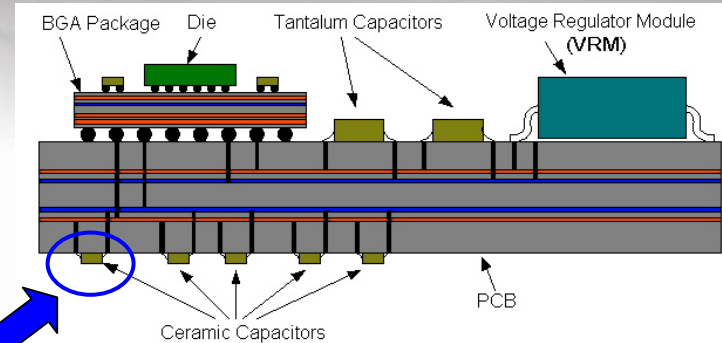


# Detecting Tantalum Capacitors with Burnt Internal Fuse

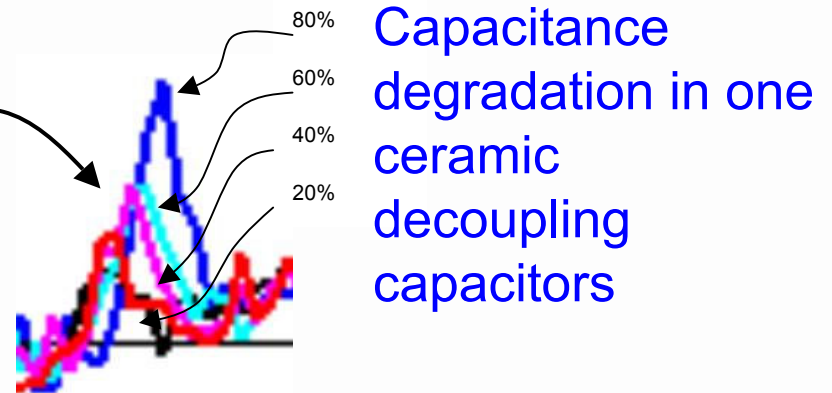
One of the two 220uF Tantalum capacitors with burnt internal fuse



# Detecting Capacitance Degradation in Ceramic Capacitors

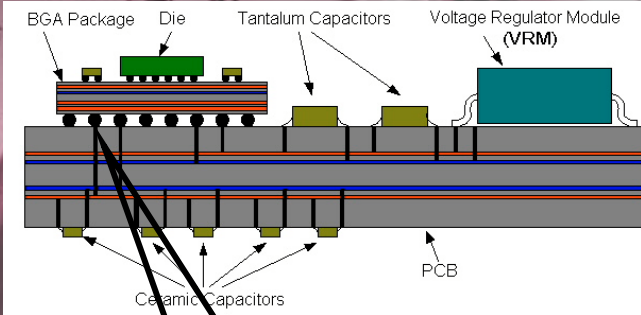


Capacitance degradation in one ceramic decoupling capacitor

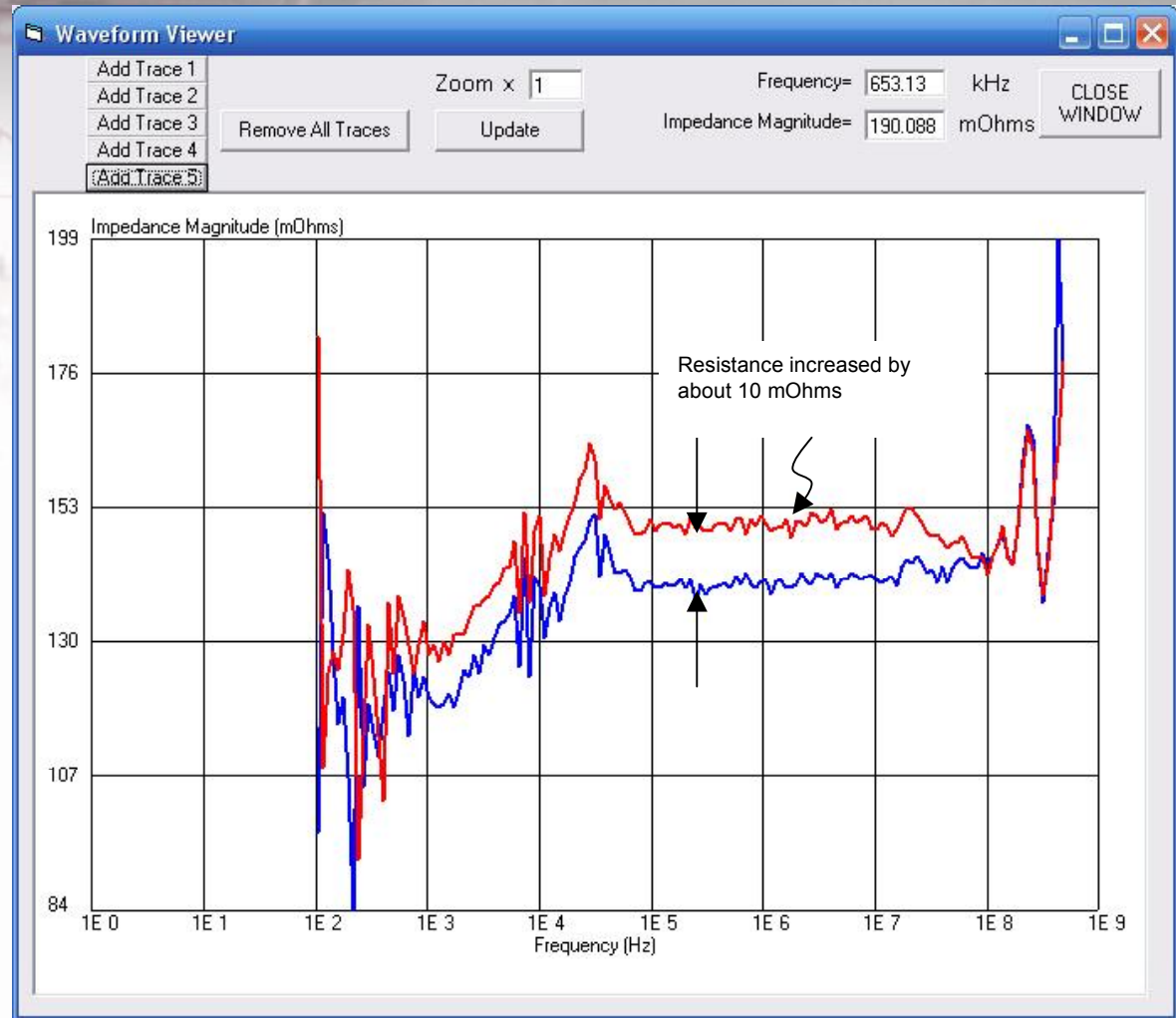




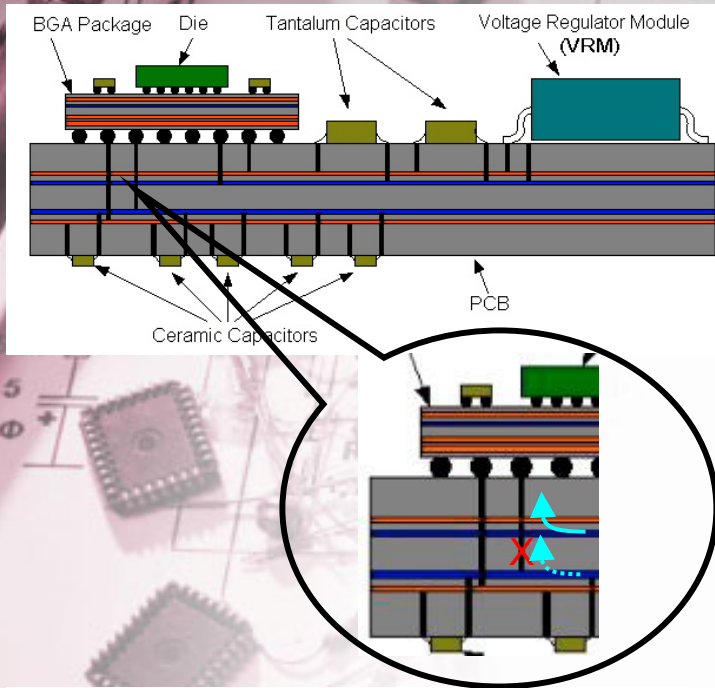
# Detecting Increased Series Resistance of PDN Interconnects



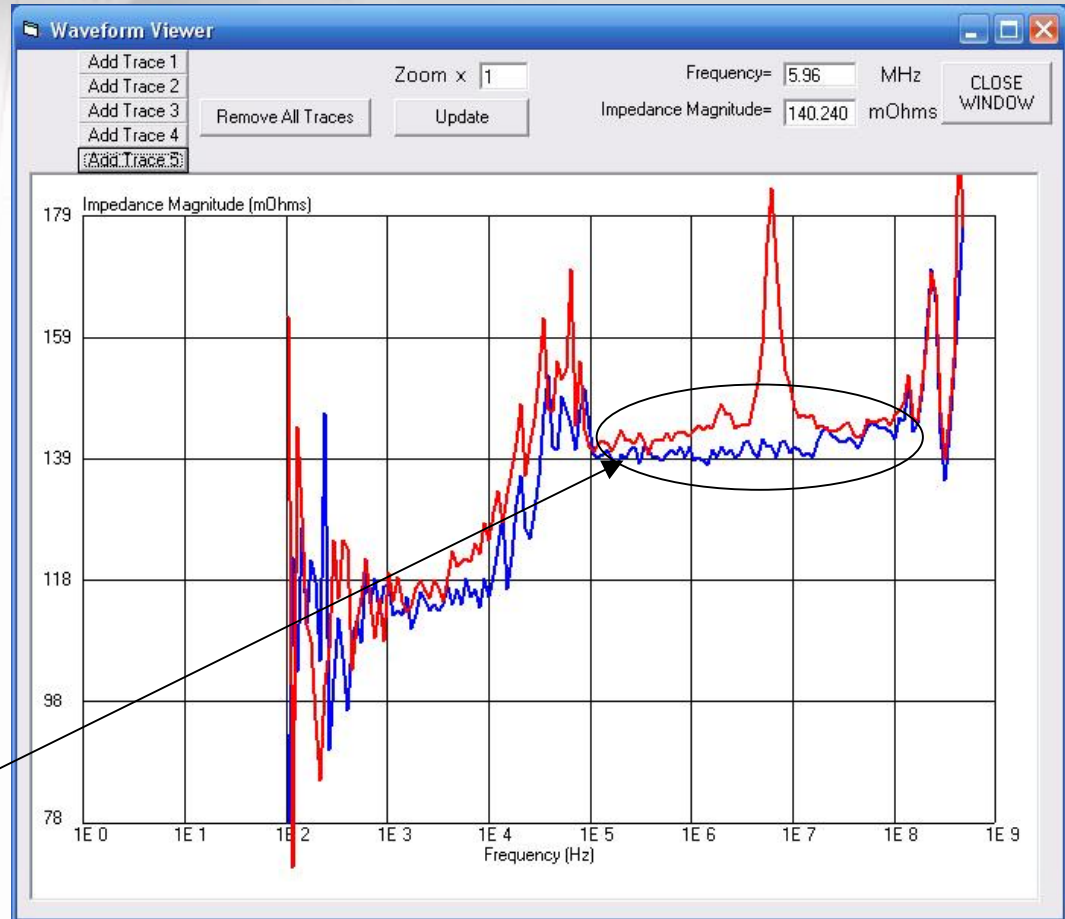
Increased resistance induced in the PDN interconnect path by cutting open a redundant current path



# Detecting Increased Loop Inductance



Induced open interconnect path divert transient currents flow increasing loop inductance





# Test Case Summary

PDN failure mechanisms detected by the proposed method:

- Tantalum capacitors with burnt internal fuse
- Capacitance degradation in ceramic capacitors
- Increased series resistance of interconnects
- Increased PDN loop inductance

# Conclusions

- Low cost PDN troubleshooting method for PLD devices
- Uses only common logic blocks and can be implemented in most existing PLDs (FPGA, CPLD, ...)
- PLDs can be temporarily configured in PDN troubleshooting mode and then reconfigured back to their intended functionality
- Can be easily implemented in existing production test floors and in product support/repair environments
- Allows remote PDN troubleshooting in systems installed in the field or in hardly accessible areas
- Evaluation on a FPGA test case has shown how this method can identify typical PDN failure mechanisms