

Electromagnetic Interference Simulations for Wide-Bandgap Power Electronic Modules

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Abstract—A simulation methodology that incorporates cosimulation techniques using ANSYS EM tools is proposed to predict radiated and conducted electromagnetic interference (EMI) from power electronic modules. The radiated EMIs for a coplanar wire bonded and wire bondless power electronic modules are simulated and compared. The instantaneous power-levels conducting through the power devices in the wire bonded power module are significantly higher than those for the wire bondless power electronic module due to parasitic circuit element imbalance. These power-levels occur for a very short duration at the turn-ON and turn-OFF of the devices and can be considered as a potential source of radiated EMI emissions. Through the cosimulation technique, it is shown that the wire bondless power electronic module has a better electromagnetic compatibility (EMC) compliance compared with that of the coplanar wire bonded power electronic module. Conducted EMI measurements and simulations are also performed to predict the conducted EMI and validate the simulation methodology. The proposed cosimulation technique can be implemented during the initial design phase of power modules to reduce significant time to physically test module-level EMC/EMI.

Index Terms—Electromagnetic interference (EMI), power electronic modules, simulation methodology.

I. INTRODUCTION

FAST switching, power dense, and compact power electronic modules or power modules are in great demand for modern power electronic systems. In these power modules, wide-bandgap power semiconductor devices, such as silicon carbide (SiC) and gallium nitride, are increasingly being used for efficient fast switching and continuous operation at high temperatures. Recently, many research efforts are focused to understand the characteristics of these devices as well as utilize these fast switching devices in high power density modules for various applications [1]–[12]. Because of the high dv/dt and di/dt slew rates in these wide-bandgap power semiconductor devices, they generate significant electromagnetic compatibility (EMC) concerns [13]–[15]. As such, it is necessary in the early design phase of these power modules to address electromagnetic interference (EMI). Mitigation of EMI in power converters using improved layout techniques has

been discussed in [13] and [16]–[18]. Various mathematical and numerical modeling approaches have been reported to understand EMI sources and generation mechanisms to predict both conducted and radiated EMI in power convert systems in [29]–[33]. However, their approaches are limited by overly simplified device models and circuit approximations, which eventually prevent precise prediction of EMI. The simulation methodology proposed in this paper directly addresses both radiated and conducted EMI, taking into consideration the nonideal transient characteristics during the switching operation and corresponding power-levels through each device. Typically, the EMI/EMC test for the power module is performed after the physical prototyping of the power module in an anechoic chamber [14]. Physical prototyping of the power modules to test for EMI issues can be a very long and costly engineering process. As such, a coherent simulation methodology to predict the EMI issues early in the design process is desired. In this paper, a simulation methodology that incorporates cosimulation techniques using ANSYS EM tools is proposed to predict the radiated and conducted EMI. The proposed simulation methodology is validated using radiated and conducted EMI measurements using a simple near-field measurement technique with near-field EM probes and line impedance stabilization network (LISN).

The magnitude of the current conducting through the physical traces during switching operation, parasitic circuit elements, and physical characteristics of the power semiconductor devices are important parameters that govern the switching characteristics of the power device [19], [20]. These parameters are also important considerations to predict the EMI in a power module. The proposed simulation methodology commences with a static current conduction simulation on the power module layout using ANSYS MAXWELL [26]. Subsequently, a frequency-dependent parasitic extraction of the physical traces on the power module is performed using ANSYS Q3D extractor [28]. The frequency-dependent parasitic model is then dynamically linked to ANSYS SIMPLORER. Using physical model characteristics from device manufacturer's data sheet, the electrical characteristics of the power semiconductor device are reproduced using ANSYS SIMPLORER's built-in semiconductor device characterization tool [27]. A frequency-dependent parasitic model-based circuit schematic of the power module is then constructed. From ANSYS SIMPLORER, the waveforms from transient simulations are then imported to ANSYS High Frequency Structure Simulator (HFSS) [28] to perform a full-wave 3-D EM field simulation to analyze the radiated

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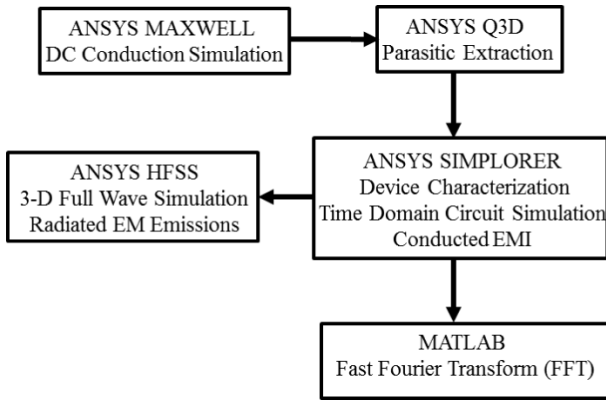


Fig. 1. Flowchart of the simulation methodology.

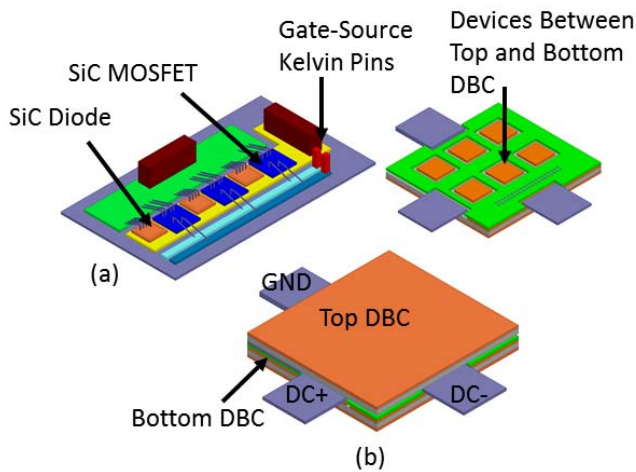


Fig. 2. (a) Coplanar wire bonded power module. (b) Wire bondless power module.

EMI. Furthermore, conducted EMI simulation is performed in ANSYS SIMPLORER incorporating the LISN model. The time-domain line voltages of the LISN are recorded and mathematically converted to frequency-domain using fast Fourier transform (FFT) in MATLAB. A flowchart of the simulation methodology is shown in Fig. 1.

II. DESIGN AND LAYOUT OF POWER MODULE

To illustrate the simulation methodology, a simple power module of a single switching position of a half-bridge topology consisting of three 1200 V 36-A power MOSFETs (CREE part number CPM2-1200-0080B) in parallel with three 1200 V 20-A antiparallel SiC Schottky barrier diodes (CREE part number CPW4-1200-S020B) is used. Fig. 2(a) and (b) shows the layout of a coplanar wire bonded and wire bondless power modules, respectively. In the wire bonded power module, the power MOSFETs and the antiparallel Schottky barrier diodes are positioned side by side as shown in Fig. 2(a). The overall dimensions of the coplanar wire bonded power module are 19.5 mm \times 34 mm. Electrical connection is achieved using multiple 127- μ m aluminum wire bonds to increase the current-handling capability and to reduce the parasitic inductance of the current path. For the wire bondless power

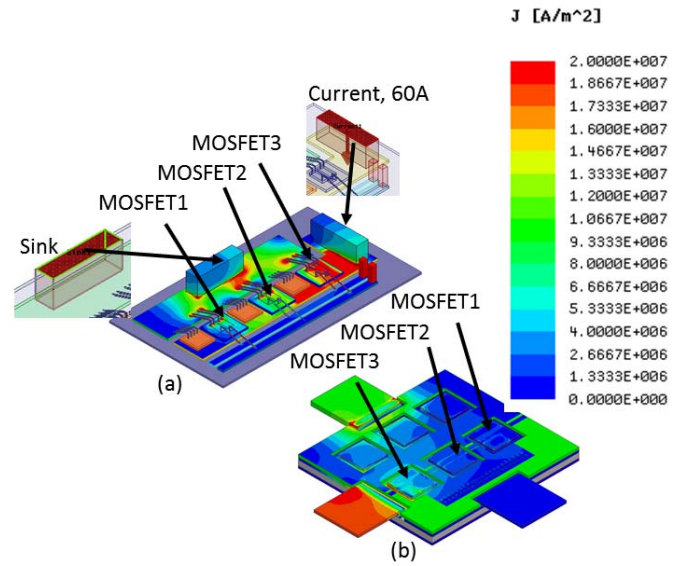


Fig. 3. DC conduction simulation. (a) Wire bonded module. (b) Wire bondless module.

module shown in Fig. 2(b), the copper plate of the upper direct bond copper (DBC) substrate provides the electrical connection between the source, drain, and gate of the power devices through solder balls. The positive power supply (dc+), ground (GND), and the gate terminals are extended outside the power module to facilitate easier access to the input/output terminals. The overall module dimensions of the wire bondless power module are 19 mm \times 19 mm. As can be seen, the overall module size for the wire bondless power module is reduced by 45% compared with that of the wire bonded power module. The reduction of the overall module size plays a significant role in reducing the parasitic inductance [21], which in turn, reduces EMI by reducing the switching noise of the power modules. The wire bondless power module can be designed to facilitate top and bottom current-carrying conductors to cancel the magnetic fields by the opposing current directions to reduce EM emissions [22], [23]. However, this is not easily accomplished for the wire bonded power module.

III. STATIC CURRENT DISTRIBUTION ANALYSIS

Static current conduction simulation for the two module structures is performed using ANSYS MAXWELL. The dc conduction simulation is performed to understand the current density distribution on the power modules. For dc conduction simulation, a 60-A current excitation is assigned to the dc+ terminal. The current path is defined from the dc+ terminal to the GND terminal, which acts as the current sink. The power MOSFETs and the antiparallel diodes are assumed to be switched ON and OFF alternatively. Fig. 3(a) and (b) shows the current density of the wire bonded and wire bondless power modules, respectively. As can be seen from the current density simulation of Fig. 3(a), the power device MOSFET3 has the highest current density compared with the other two MOSFETs in the layout. Also, MOSFET2 has a higher current density compared with that of MOSFET1.

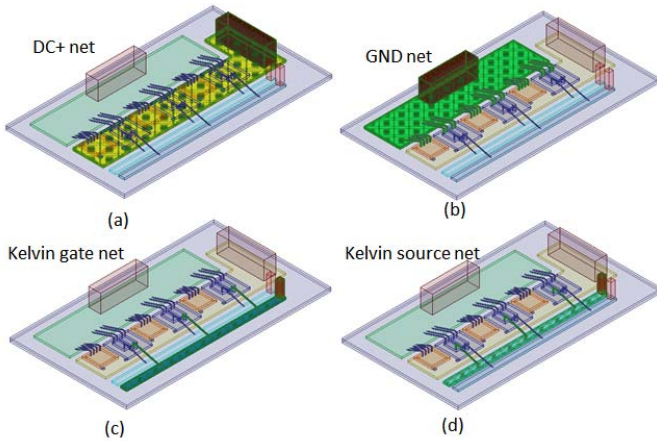


Fig. 4. Conducting nets in ANSYS Q3D for parasitic analysis (coplanar wire bonded module).

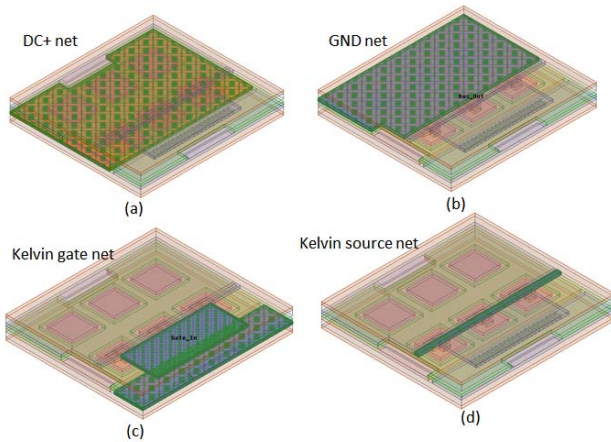


Fig. 5. Conducting nets in ANSYS Q3D for parasitic analysis (wire bondless module).

This imbalance in current density can be explained by the proximity effect of the power devices to the dc+ terminal.

As can be seen from the current density plot of Fig. 3(b), MOSFET3 has a slightly higher current density compared with MOSFET2 and MOSFET1, whereas MOSFET2 and MOSFET1 have approximately similar current density distribution. As such, the imbalance in current density in the wire bondless module is reduced compared with that in the wire bonded power module. The imbalance in current density has a direct impact on the power-levels through each of the devices in power module, which will be evident from the power-level simulations.

IV. PARASITIC EXTRACTION

The parasitic extraction for the power module is performed using ANSYS Q3D. To perform the parasitic extraction simulations, various current conducting nets are assigned in accordance with the switching sequence of the power module. For our case study, i.e., for a switching position with three MOSFETs in parallel, there are primarily three conducting nets that are of interest, the dc+, GND, and the gate-source loop nets. Figs. 4 and 5 show the conducting nets for the

wire bonded and wire bondless power modules, respectively. The dc+ conducting nets in Figs. 4(a) and 5(a) consist of the inductance paths from the dc+ terminal to the drain of the SiC power MOSFETs and the cathode of the Schottky barrier diodes. The GND nets consist of the inductance paths from the source of the MOSFET to the GND terminal as shown in Figs. 4(b) and 5(b). The gate-source loop inductance is divided into two parts, one going from the gate of the devices to the Kelvin gate terminal and the other from the source of the power MOSFETs to the Kelvin source terminal. After assigning the desired conducting nets, a frequency sweep is performed to extract the frequency-dependent parasitic inductance. The frequency of interest for the frequency sweep is determined by the rise time of the time-domain signal. The SiC power MOSFETs have a rise time of 31 ns [$t_r + t_{d(ON)}$] according to the data sheet provided by the manufacturer. For a time-domain waveform with a rise time of 31 ns, we assume that six samples within that time step are required to fully capture the signal in the frequency-domain. Therefore, the maximum frequency sweep for the parasitic is

$$F_{\text{Max}} = \frac{1}{5.16 \text{ ns}} = 200 \text{ MHz.} \quad (1)$$

The parasitic inductance for the wire bondless power module is significantly less over the frequency range for all the assigned nets compared with that of the coplanar power module. The effect of these parasitic inductances on the switching performance of the power devices will be discussed in Section VI.

V. DEVICE CHARACTERIZATION

The transient response and voltage and current overshoots of the power devices during turn-ON and turn-OFF primarily contribute to EMI. As such, ANSYS SIMPLORER simulations are performed to understand the transient behaviors of these switching devices. A frequency-dependent parasitic model (RLC) of the device is imported and dynamically linked from ANSYS Q3D to construct the circuit schematic of the power module in ANSYS SIMPLORER. The devices used to build the power module are characterized using the SIMPLORER's device characterization tool with parameters from the manufacturer's data sheet. ANSYS SIMPLORER's dynamic semiconductor characterization tool takes the dynamic measurement and nominal operating point conditions as inputs [27]. CREE's 1200 V 36-A power MOSFETs (CPM2-1200-0080B) and 1200 V 20-A Schottky barrier diodes (CPW4-1200-S020B) are used in this paper. The transfer and output characteristics are then fitted in SIMPLORER against several data points obtained from the data sheet of the device.

VI. CIRCUIT AND SYSTEM SIMULATION

After the device characterization, the circuit schematic of the power module is constructed for the frequency-dependent parasitic model using the characterized power devices in SIMPLORER. To test the transient switching behaviors of an inductive switching, a test circuit is constructed for the power

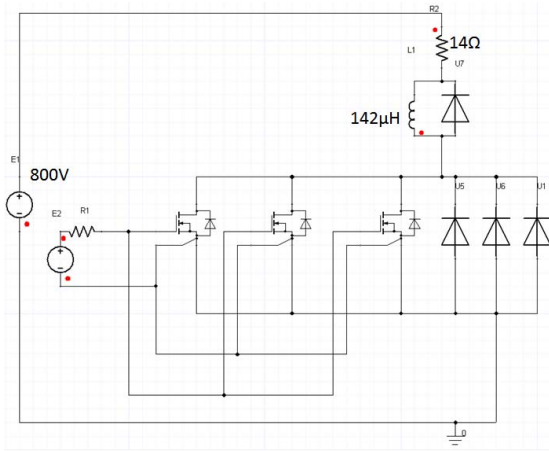


Fig. 6. Circuit schematic for switching simulations (without parasitic inductance).

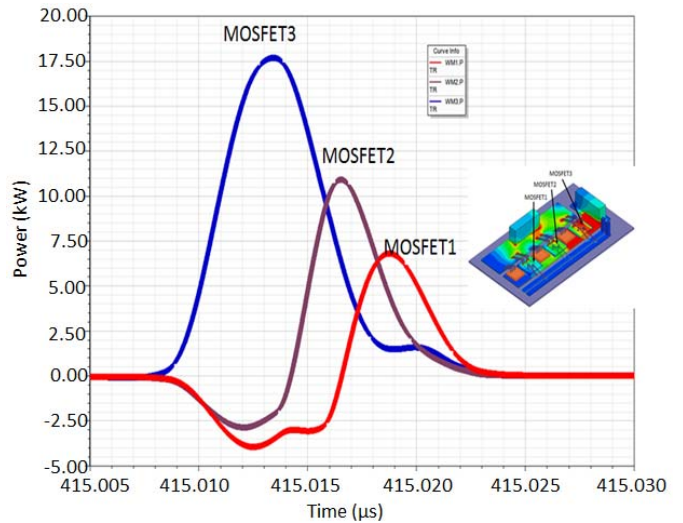


Fig. 8. Instantaneous power through paralleled power MOSFETs (coplanar wire bonded module).

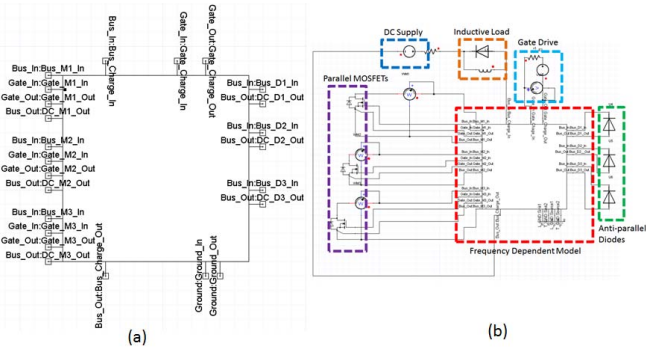


Fig. 7. (a) Frequency-dependent circuit model. (b) Circuit schematic built around frequency-dependent parasitic model.

module with circuit parasitics. Fig. 6 shows the simplified circuit schematic for the switching simulation. The input dc voltage for the simulation is chosen to be 800 V. The inductive load for the inductive switching test is chosen to be 142 μ H, which is the same value given in the manufacturer's data sheet for the inductive test circuit condition. The duty cycle and the switching frequency for the simulations are 50% and 50 kHz, respectively.

Fig. 7(a) shows the frequency-dependent parasitic model that is imported from ANSYS Q3D, while Fig. 7(b) shows the circuit model, derived from the parasitic model, used to study the switching behaviors of the power modules. As can be seen from Fig. 7(b), the three paralleled MOSFETs and the three antiparallel diodes are all connected to the different pins in the parasitic model. The inductive load, dc supply, and the gate driver circuitry are added to complete the switching system. To obtain the drain current, drain-source voltage, and the instantaneous power waveforms through the power devices at turn-ON and turn-OFF, a watt meter is connected to each of the power MOSFETs as shown in Fig. 7(b).

Figs. 8 and 9 show the instantaneous power-levels conducting through the MOSFETs at a single switch-ON instance for the wire bonded and wire bondless power modules, respectively. As can be seen from the power-level plot in Fig. 8, MOSFET3 carries the highest power-level compared

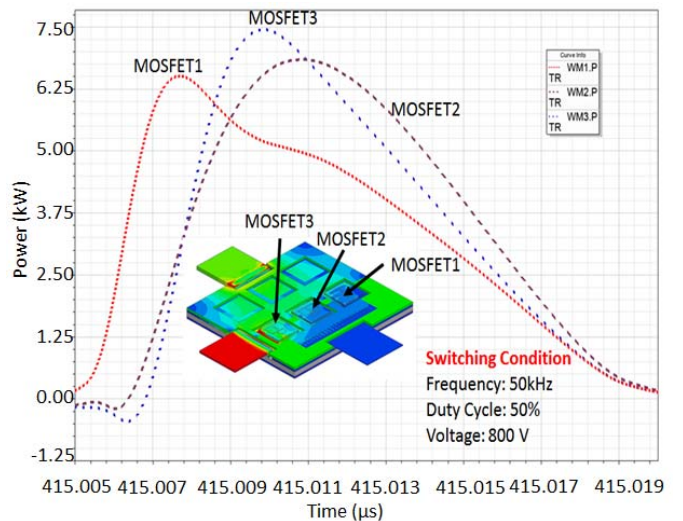


Fig. 9. Instantaneous power through paralleled power MOSFETs (wire bondless module).

with those of MOSFET2 and MOSFET1, which is consistent with the dc conduction simulation performed in Section III. As shown, an instantaneous power of 17.5 kW is conducting through MOSFET3 in the wire bonded power module for a very short duration of time at the turn-ON of the device and can be considered as a potential source of EMI. The instantaneous power-levels conducting through the devices in the wire bonded power module are significantly higher than those in the wire bondless power module as shown in Fig. 9.

In order to understand the radiation behaviors of the power module, time-domain instantaneous power waveforms are converted to frequency-domain waveforms using FFT. Fig. 10(a) and (b) shows the spectral power distribution of the time-domain instantaneous power waveform for a single switching (turn-ON) instance for the wire bonded and wire bondless power modules, respectively. From these spectral plots, it can be observed that most of the higher power-level frequencies are between 10 and 200 MHz, whereas the power-level above 200 MHz is very small.

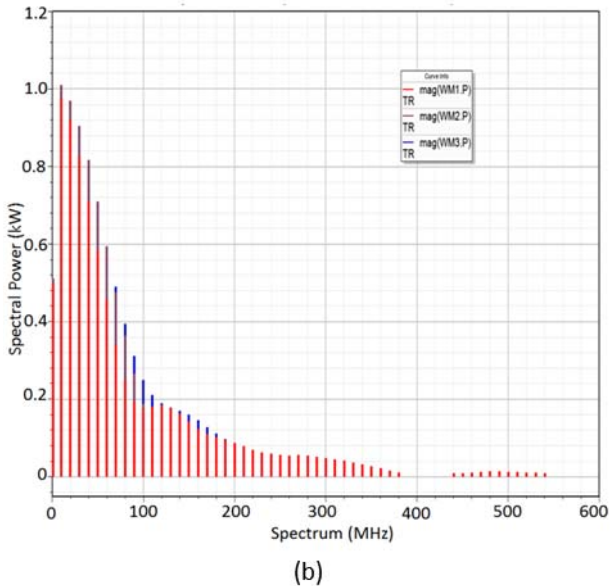
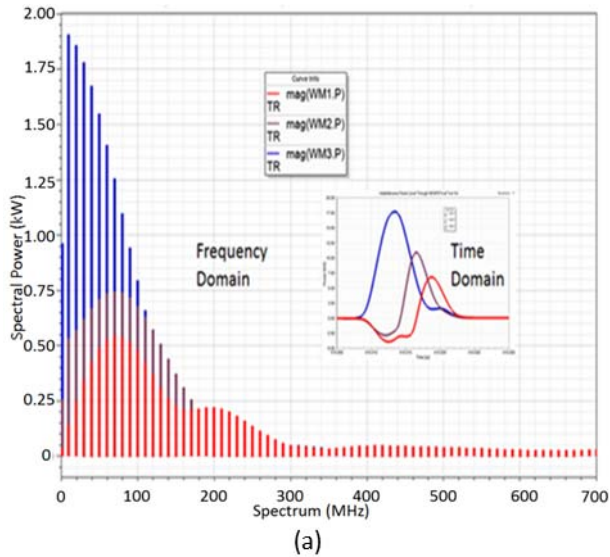


Fig. 10. Spectral power-levels through power MOSFETs. (a) Wire bonded module. (b) Wire bondless module.

VII. FULL-WAVE SIMULATION

The frequency-domain spectral power amplitudes are given as inputs for the ANSYS HFSS to perform 3-D full-wave EM simulations in order to analyze radiated fields from the power modules. In ANSYS HFSS, a driven modal solution is performed to simulate the electric field strength. The power-levels are assigned to the device location on the physical layout using lumped ports. The lumped ports are assigned between the drain and source of the power MOSFETs.

Fig. 11 shows the electric field strength in volts per meter at different spectral frequencies of 10, 100, and 200 MHz. From Fig. 10, it is evident that the power-levels conducting through each MOSFET gradually decreases as frequency increases. The electric field strength also follows the same pattern and decreases as the power-levels are decreasing at higher frequencies. As can be seen from Fig. 11, the electric

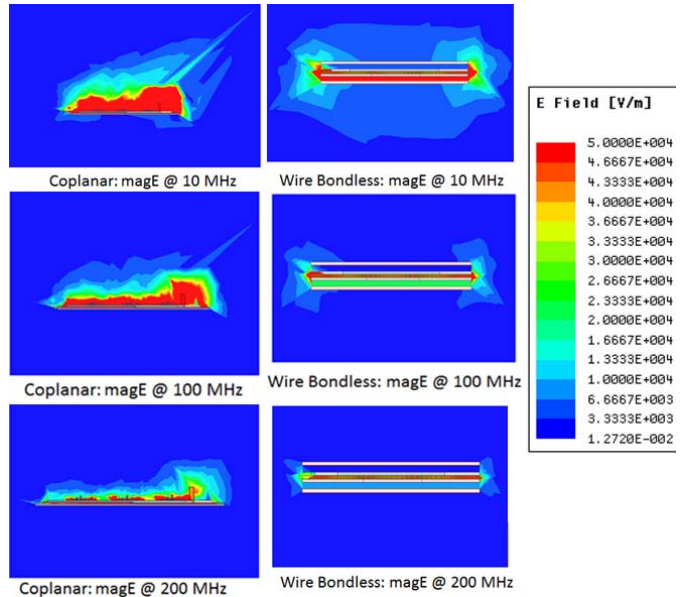


Fig. 11. E-field strength at different frequencies for wire bonded and wire bondless modules.

field is highly localized for wire bondless power module compared with wire bonded power module. The high power-levels due to the parasitic imbalance in wire bonded power module for a very short duration of time contribute toward higher electric field. On the contrary, the wire bondless power module utilizes the top and bottom DBC substrates to form a forward and return current path laid on top of each other in opposing directions. As such, the opposing current paths cancel the magnetic fields to yield a shielding mechanism to suppress the fields. As mentioned before, the dimensions are 19.5 mm × 34 mm and 19 mm × 19 mm for the wire bonded and wire bondless power modules, respectively. The frequency of interest is between 10 and 200 MHz, which corresponds to wavelength ranging from 30 to 1.5 m. Since the largest conductor should be at least λ/4 wavelength to yield effective radiation, both wire bonded and wire bondless modules itself will not radiate efficiently because the largest metallic conductor dimensions for both the modules are much smaller than their quarter wavelengths. However, in reality, power modules are part of larger power electronic systems surrounded by larger metallic objects that might radiate the electric field emitted from the power modules. Therefore, for EMC compliance, it is important to suppress the electric field as close as possible to the power modules.

The wire bondless power module structure with the top and bottom DBC substrates provides a shielding mechanism to suppress the fields within the module structure. The shielding effectiveness can be calculated from the skin depth of the confined metal. The skin depth of the metal is given as [24], [25]

$$\text{Skin depth, } \delta = \frac{1}{\sqrt{\pi f \mu \sigma}} \quad (2)$$

where δ is the skin depth of the metal, f is the frequency, μ is the magnetic permeability, and σ is the conductivity of the metal. The copper layer thickness for the top and bottom

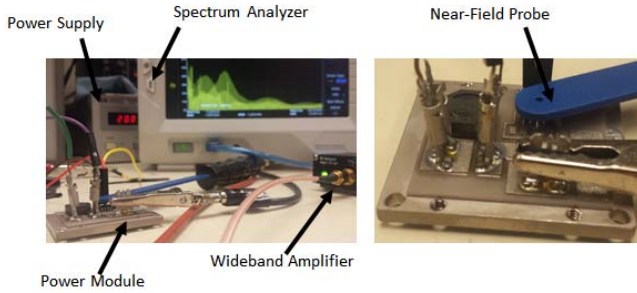


Fig. 12. Test setup for near-field measurement.

DBC substrates is $304.8\text{-}\mu\text{m}$. At 10 MHz, the calculated skin depth for copper is approximately $20.3\text{-}\mu\text{m}$ assuming that the conductivity of copper is 5.7×10^7 S/m. The total shielding effect can be found by summing the absorption and reflection losses given by the following expressions [24], [25]:

$$\text{Absorption loss, } A(\text{dB}) = 20 \log e^{-\frac{t}{\delta}} \quad (3)$$

where t is the thickness of the copper layer and δ is the skin depth of copper

$$\text{Reflection loss, } R(\text{dB}) = 20 \log \frac{\eta_0}{4\eta_s} \quad (4)$$

where η_0 is the intrinsic free space wave impedance and η_s is the intrinsic impedance of copper.

The intrinsic impedance of copper is given by [24], [25]

$$\eta_s = \sqrt{\frac{2\pi f \mu}{\sigma}}. \quad (5)$$

From the above expressions, the reflection and absorption losses for the $304.8\text{-}\mu\text{m}$ copper are calculated to be 98 and 127 dB, respectively. Therefore, the total shielding effectiveness for the DBC substrate is 225 dB in any one direction. As such, wire bondless power modules will provide better EM compliance compared with wire bonded power module.

VIII. RADIATED EMI VALIDATION

In this section, a simple validation process of our simulation methodology is performed. To verify the simulation methodology, a single-device power module is fabricated using a 1200 V 36-A SiC power MOSFET (CPM2-1200-0080B) from CREE, similar to the device used for simulation. The test setup includes a power supply (HP-E3630A), a function generator (HP-33120A), a spectrum analyzer (Rigol-DSA 815), and a near-field EMC probe kit (Tekbox-TBPS01-TBWA2), as shown in Fig. 12. The near-field EMC probe kit consists of four EMC probes with three H-field probes of different loop diameters and one E-field probe. As the measurement is carried out on coplanar current-carrying traces, the H-field probes are most sensitive to the radiated emissions from the power module. The near-field EMC probe is positioned just above the power module to capture the maximum field strength from the switching test. The EMC probe is connected to the spectrum analyzer through a 40 dB wideband preamplifier to increase the dynamic range of the measurement. Three different H-field probes with 20-, 10-, and 5-mm diameter

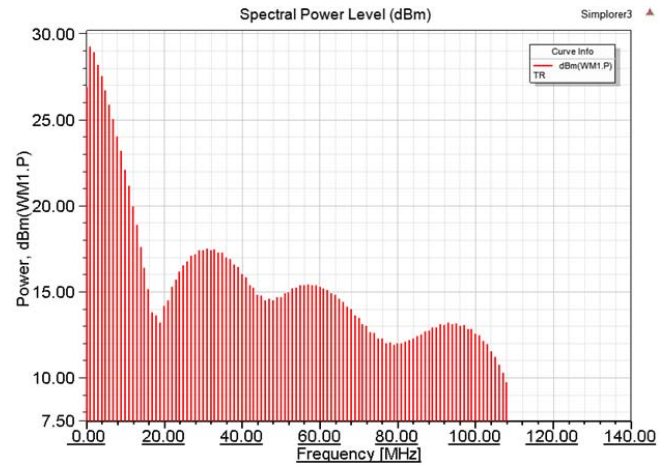


Fig. 13. Simulated spectral power for the fabricated single-device module.

are initially used to choose the most sensitive probe to the radiated fields. It is observed that the 5-mm-diameter probe is most sensitive to the radiated fields and can locate precisely the source of the radiated emissions, which is mostly concentrated in the switching loop of the power device. The dimension of the supply and terminal leads are carefully chosen so that they are not self-radiating objects at the frequencies of interest. The device is switched at 50 kHz using a gate-source voltage V_{GS} of 20 V. The dc supply voltage provided for the switching test is 20 V. The resolution bandwidth for the spectrum analyzer is set at 1 MHz. The unit of measurement for the spectrum analyzer is set to measure in millivolts with a reference level of 100 mV. The impedance of the spectrum analyzer is 50Ω . In order to maintain consistency, the impedances of all the cables connecting the near-field EM probes and the wideband amplifier to the spectrum analyzer are chosen to be 50Ω . As discussed earlier, the frequency range of interest is up to 200 MHz; as such, the frequency range for the spectrum analyzer is set from 10 kHz to 200 MHz.

To verify the measurement results, a simulation-based study is performed on the fabricated power module using the same simulation methodology discussed earlier. Fig. 13 shows the simulated spectral power distribution in decibel-milliwatts (dBm) for the fabricated power module under similar test conditions discussed above. In order to compare the spectrum analyzer measurement and SIMPLORER simulation, the simulated unit in dBm is converted to milliwatts and subsequently to millivolts using the following equation assuming that the impedance of the measurement is 50Ω :

$$\text{Power (mW)} = \frac{|V|^2}{50 \Omega}. \quad (6)$$

Fig. 14 shows the comparison between the simulation (top) and the measurement data (bottom). As can be seen from the measurement and simulation results, the spectral spikes occur at similar frequencies, even though the amplitudes for the measurement results are several orders of magnitude lower than those from simulation. It should be mentioned here that the measurement with the near-field EM probe were performed at a distance away from the power module. On the contrary, the

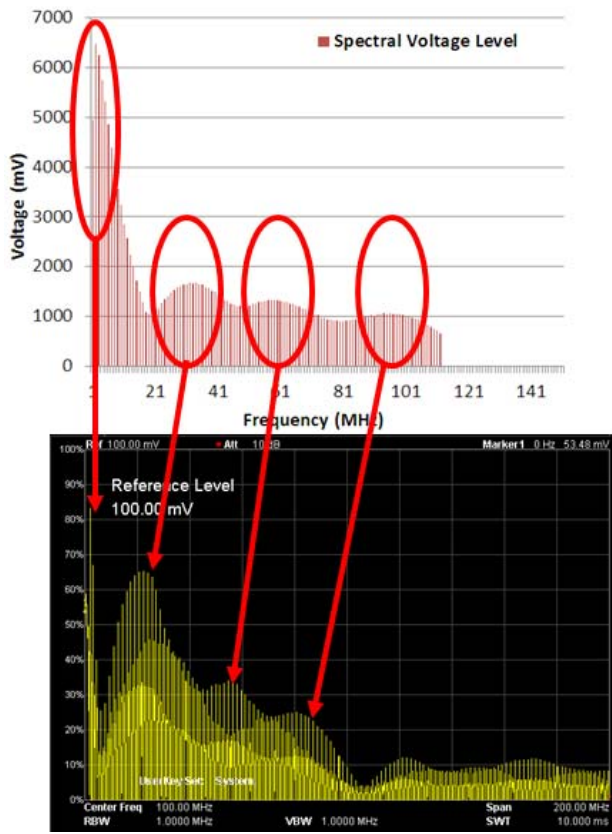


Fig. 14. Comparison between simulation (top) and measurement (bottom).

simulation results are spectral power-levels conducting directly through the devices. As the near-field probe is placed above the power module at some distance, the power-levels gradually diminish since the radiated power captured by the EM probe strongly depends on its sensitivity and distance from the power module. As such, the magnitude captured by the EM probe is lower. Since the frequency spikes in the simulation and measurement occur at similar frequencies, these measurements validate the simulation methodology.

IX. CONDUCTED EMI SIMULATION AND VALIDATION

In order to perform conducted EMI measurements and validation of the simulation methodology, a single-device power module consisting of CREE’s 1200 V 36-A SiC power MOSFET (CPM2-1200-0080B) is fabricated. The power module is first designed using ANSYS EM tools and simulated for its conducted EMI response. The frequency-dependent parasitic extraction of the power module is performed using ANSYS Q3D, and subsequently a switching simulation is performed using the frequency-dependent parasitic model and the characterized SiC power MOSFET in ANSYS SIMPLORER. The clamped inductive switching test is performed on the fabricated power module under 20 V input dc voltage. Fig. 15(a) and (b) shows the drain-to-source voltage waveforms under clamped inductive switching recorded from measurement and simulation, respectively. As can be seen, the simulated switching waveform matches with the measured waveform both in transient and the steady state.

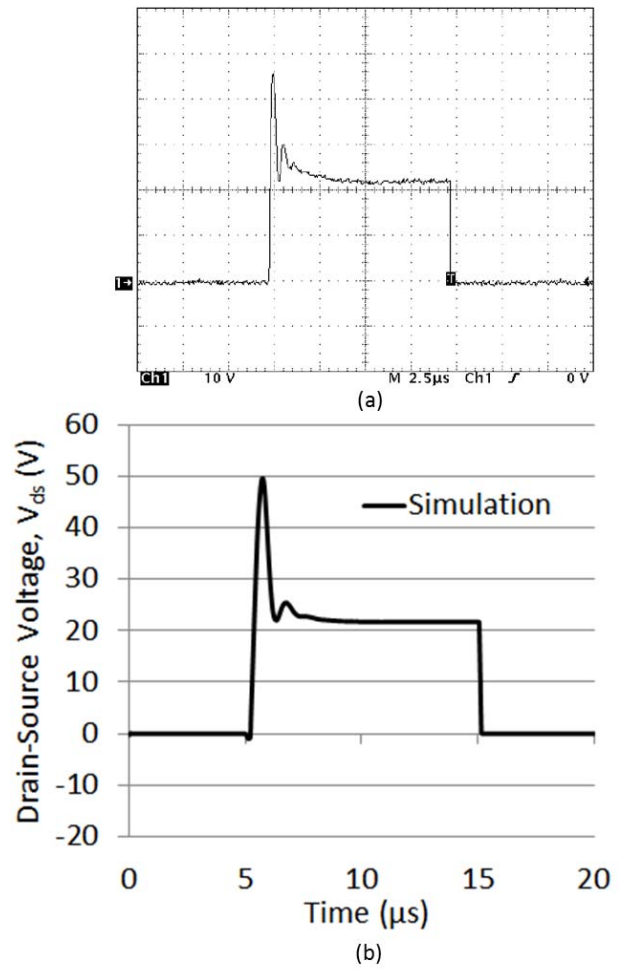


Fig. 15. Switching waveform. (a) Measurement. (b) Simulation.

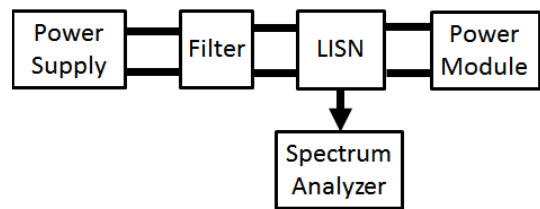


Fig. 16. Conducted EMI measurement setup.

An LISN is implemented to simulate and measure the conducted EMI per CISPR22 [34]–[38]. The circuit model for the LISN is taken from the manufacturer’s (ETS-LINDGREN, model-3810/2 LISN) provided user manual [39]. Fig. 16 shows the setup for the conducted EMI simulation and measurement. A power-line filter (CORCOM F7129) is introduced in between the power supply and LISN in order to filter any noise coming from the power supply. The power module under test is kept on a nonconductive wooden table, and the LISN is placed under the table and grounded properly according to the standards. The output of the LISN is fed to the spectrum analyzer to observe the conducted EMI noise.

Figs. 17 and 18 show the voltage-levels at the two lines (line and neutral) of the LISN under the operating conditions monitored on oscilloscope. These voltage waveforms are fed into

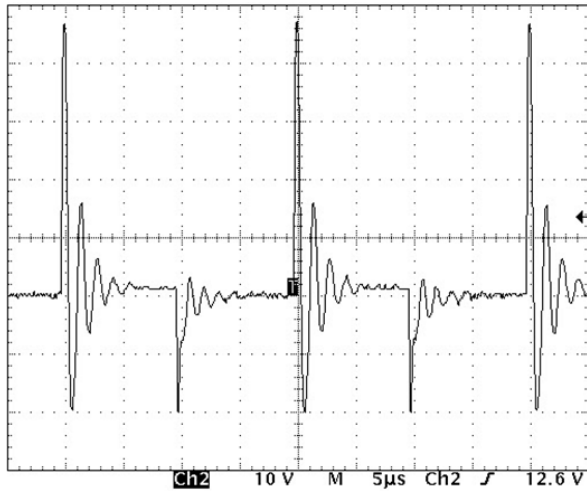


Fig. 17. Voltage-level at line of LISN monitored from oscilloscope.

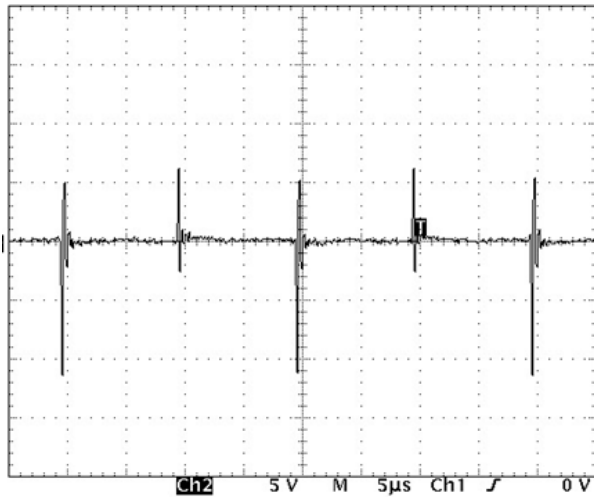


Fig. 18. Voltage-level at neutral of LISN monitored from oscilloscope.

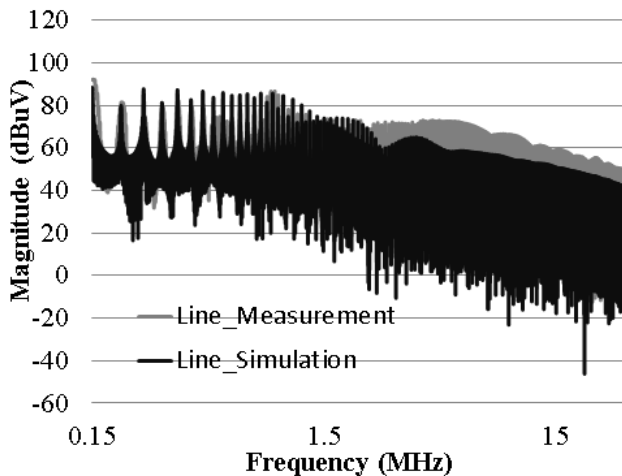


Fig. 19. Simulated and measured voltages at LISN line.

the spectrum analyzer to obtain the frequency-domain spectral distribution of the line and neutral voltages of the LISN.

Figs. 19 and 20 show the comparison between the simulated and measured spectral distribution of the line voltages

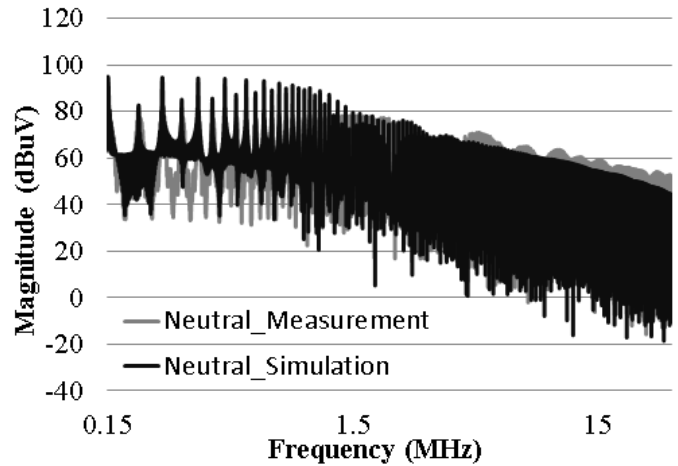


Fig. 20. Simulated and measured voltages at LISN neutral.

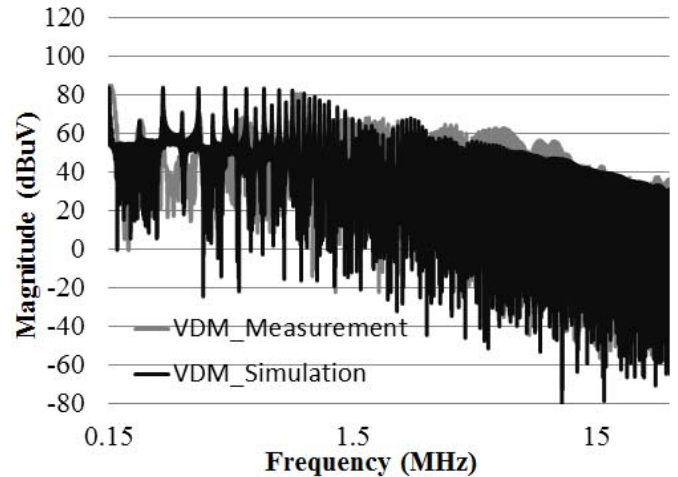


Fig. 21. Differential mode noise.

from 150 kHz to 30 MHz. For the simulated spectrum, the voltages at two lines are first simulated using the frequency-dependent parasitic model, cable configuration, and LISN model in ANSYS SIMPLORER. The FFTs of the time-domain waveforms are then performed using MATLAB to achieve the frequency-domain response. As can be seen from Figs. 19 and 20, the simulated and measured spectra of the line voltages closely match in magnitude and spectral shape.

Figs. 21 and 22 show the comparison of the simulated and measured differential and common mode LISN voltages. The differential and common mode voltages are mathematically separated using the following equations:

$$V_{DM} = (V_{Line} - V_{Neutral})/2 \quad (7)$$

$$V_{CM} = (V_{Line} + V_{Neutral})/2. \quad (8)$$

As can be seen, the simulated differential and common mode voltages match well with the measured results.

From Figs. 19–22, we can observe that the magnitudes of the low-frequency spikes are similar. However, at higher frequency, around 20–30 MHz, the simulation amplitudes are about 8–10 dB μ V lower than that of the measurement. This

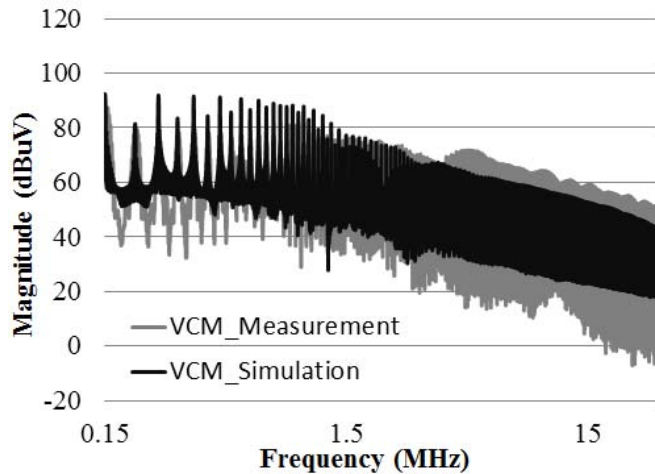


Fig. 22. Common mode noise.

can be attributed to the round-OFF error of the FFT conversion. The correlation coefficient between the simulation and measurement is 0.73. The coefficient of determination (R^2) is calculated to be 53%. As such, 53% of the variation in the measurement results can be explained by the linear relationship between simulation and measurement, which is deemed acceptable given the highly nonlinear behavior of the conducted EMI noise.

X. CONCLUSION

A simulation methodology that incorporates cosimulation techniques using ANSYS EM tools is proposed to predict both radiated and conducted EMI from power electronic modules. The radiated EMIs for a coplanar wire bonded and wire bondless power modules are simulated and compared. The instantaneous power-levels conducting through the power devices in the wire bonded power module are significantly higher than those for the wire bondless power module due to parasitic imbalance. These power-levels occur for a very short duration of time at turn-ON of the devices and can be considered as a potential source of radiated EMI emissions. It has been demonstrated that a wire bondless power module shows a greater EMC compliance compared with a traditional wire bonded power module. Moreover, the simulation methodology used to reach this conclusion has been validated using a simple near-field EMC measurement technique with EMC probes and a spectrum analyzer. The conducted EMI simulation for a single-device power module was performed using the proposed simulation methodology. The simulation results were compared with the measurement results, and they show good agreement in shape and magnitude. As such, the simulation methodology proposed for radiated and conducted EMI can be incorporated into the initial design phase of the power modules to reduce the design cycle and costly engineering process to test for EMI/EMC.

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