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COM and Reference Transmitter/Receiver/Package for 106/112Gbps Long-Reach and Chip-to-Chip Links

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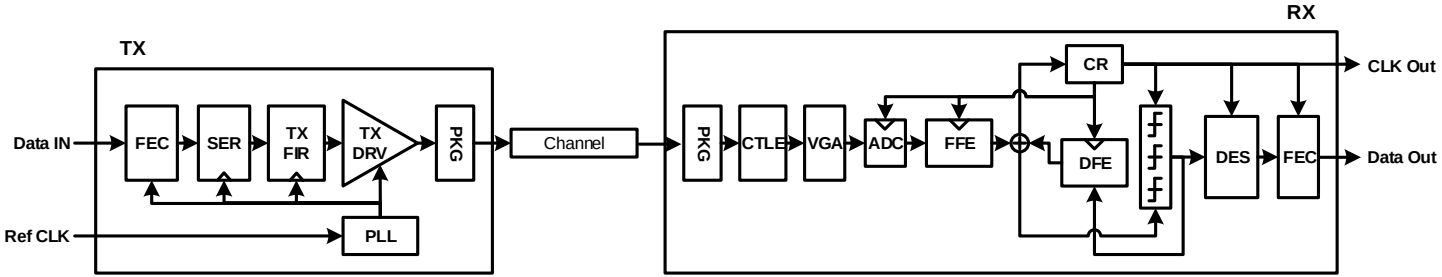
Agenda

- **Overview of serial link technologies at *106/112Gbps***
- **IEEE 802.3 *106Gbps* Ethernet and OIF CEI *112Gbps* tasks**
- **Evolutions of SerDes electrical specifications and COM baseline model**
- **Observations and next steps**

Overview of Serial Link Technologies for *106/112Gbps (KR/C2C)*



- **Transition of SerDes and EQ architecture at 106/112Gbps**
  - Analog-based ⇒ ADC-based
  - DFE heavy ⇒ FFE heavy
  - FEC's impacts on BER gain/latency and dependency on EQ types/characteristics
- **Effectiveness of EQ schemes under PPA (Power, Performance, and Area) matrix***
  - PPA drives the choice of EQ schemes
  - Analog performance is essential to ADC-based SerDes design
  - FFE is efficient in EQ performance and area
  - DFE is effective especially for the first few taps and under noisy conditions

Note: H. Wu, M. Shimanouchi, and M. Li, "Effective Link Equalizations using FIR, CTLE, FFE, DFE, and FEC for Serial Links at 112 Gbps and Beyond", DesignCon 2018, Santa Clara, CA.

IEEE 802.3 *106Gbps* Ethernet and OIF CEI *112Gbps*

Standards	Data Rate & Modulation	Subclass	Applications
IEEE 802.3ck	106.25Gbps, PAM4	KR	Backplane (up to 2 connectors)
		CR	Cable
		C2C	Chip-to-Chip (up to 1 connectors)
		C2M	Chip-to-Module
OIF CEI 5.0	72Gbps-116Gbps, PAM4	LR	Long Reach
		MR	Medium Reach
		VSR	Very Short Reach
		XSR	Extra Short Reach

- **~2 years in working**
- **Follows IEEE 802.3 50Gbps Ethernet and OIF CEI 56Gbps frameworks**
  - Divided into KR/CR/C2C/C2M (Ethernet) and LR/MR/VSR/XSR (OIF CEI) subclasses based on reaches and topology
  - Use COM (Channel Operating Margin) Methodology for channel and device spec. settings and compliance tests
    - *Exceptions: C2M and VSR/XSR subclasses*
- **Will focus on IEEE 802.3ck KR/C2C and OIF CEI 5.0 LR/MR in this paper**
  - Link performance is evaluated end-to-end at the slicer in the receiver

Evolutions of Electrical Spec. and COM Baseline Models

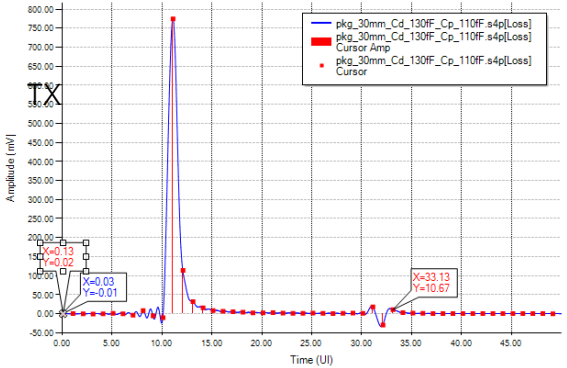
- **COM is a figure of merit (FOM) which is a ratio between available signal amplitude and broad-sense noises, from uncompensated channel effects, crosstalk, device jitter and noise, and amplitude distortions**

$$COM = 20 \times log_{10}(\frac{A_s}{A_{ni}})$$

- **COM methodology and its parameters bind the channels the standards can support and the *assumed SerDes capabilities* that can support the intended channels**
- **Due to the advancement of *106/112Gbps* SerDes architectures, the phrase "*assumed SerDes capabilities*" became one of the major study and discussion points during 802.3ck and OIF CEI 5.0 development processes. For example:**
  - Do we need to develop COM for ADC-based SerDes architecture?
  - Will an ADC-based SerDes have same EQ capabilities as an analog-based SerDes, e.g. if they have the same amount of FFE/DFE taps?
  - What about FEC performance differences between ADC-based and analog-based SerDes'?

Phase 1: *What channel can be supported at 106/112Gbps?* *(~May 2018)*

- **Initial *106/112Gbps* channel data from Intel, Samtec, TEC**
  - Channel models with projected/scaled materials and connector characteristics
- **Initial reference device characteristics**
  - Scaled from *53/56Gbps*: TX Rise/Fall time, TX/RX die capacitance (C_d), RX input noise (σ_0)
  - Kept same with 53/56Gbps: Package (C_p, *T-line*), TX nonlinearity (*TX RLM*), noise (SNR_{TX})
  - Added/Modified *106/112Gbps* SerDes features
    - *Long FFE (12-28 taps) and short DFE (1 tap)*
    - *EQ adaptation using LMS-based algorithm*
- **Findings**
  - *106/112Gbps* packages (C_d, *30mm T-line, and* C_p) will consume *>5dB* insertion loss
  - Reflections caused by the reference packages are at *22-23UI* away from the main cursor location
  - Determined that
    - *Maximum channel insertion loss is ~28dB at 26.56/28GHz*
    - *~24 post-taps are needed for ISI/reflection compensation*



Single bit response of 30mm package at 56Gbd (from 3ck_02_0518.pdf)

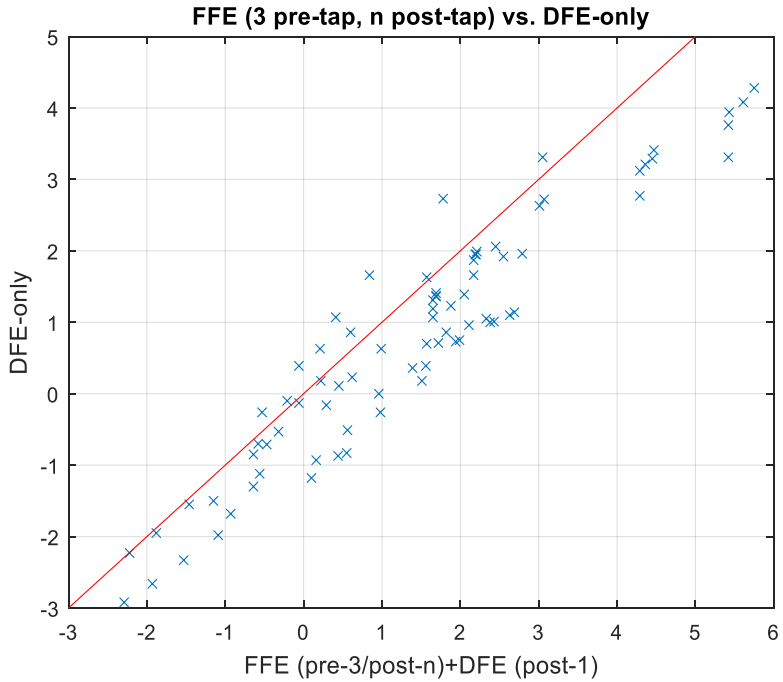
Phase 2: *Solution Space Differences?* *(~November 2018)*

- **In Phase 1, an ADC-based SerDes is assumed. Questions:**
  - Not all *106/112Gbps* SerDes' are ADC-based
  - FFE/DFE adaptation algorithms are implementation-dependent
  - Foresaw challenges in getting consensus regarding SerDes architecture and EQ adaptation methodology
- **Design Experiments with 3 receiver configurations**

Config #	Name	SerDes Architecture	Description
Config 0	**FFE-heavy/DFE-lite**	**ADC-based**	Long FFE with *3* pre-taps and *12~28* taps post-taps plus *1*-tap DFE
Config 1	**DFE-only**	**Analog-based / COM Ref. RX**	*12~28*-tap DFE
Config 2	**FFE-lite/DFE-heavy**	**Hybrid of ADC-based and Analog-based**	Lite FFE with *3* pre-taps and *no* post-taps plus *12~28*-tap DFE

Note: TX is with 2 pre-taps and 1 post-tap

Phase 2: *Solution Space Differences? (cont.)*

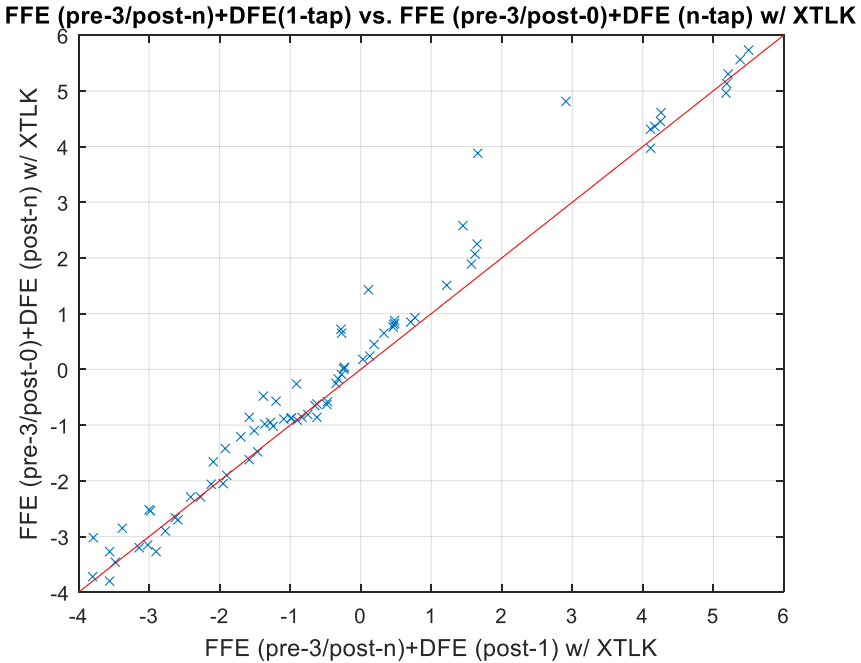


Config #	Name	SerDes Architecture
Config 0	FFE-heavy/DFE-lite	ADC-based
Config 1	DFE-only	Analog-based / COM Ref. RX

Mean Diff = 0.64dB (1.14dB for passing group)
FFE-heavy/DFE (1-tap) (Config 0) outperforms

Config 1 underperforms Config 0

Phase 2: *Solution Space Differences? (cont.)*



Config #	Name	SerDes Architecture
Config 0	FFE-heavy/DFE-lite	ADC-based
Config 2	FFE-lite/DFE-heavy	Hybrid of ADC-based and Analog-based

Mean Diff = -0.27dB (-0.10dB for passing group)
FFE-lite (3-pre/0-post)/DFE (n taps) (Config 2)
slightly outperforms

Config 2 is comparable to Config 0

Phase 2: *Solution Space Differences? (cont.)*

Comparisons among baseline ref. RX models

Config #	Baseline Ref. RX	Performance (w.r.t. *Config 0*)	Complexity	Notes
0	FFE-heavy (3-pre/n-post)/DFE (1-tap)	**High**	**High**	• Good performance • Complex COM model and standardization
1	DFE-only	**Low**	**Low**	• Low performance • Uses existing COM methodology
2	FFE-lite (3-pre/0-post)/DFE-heavy (n-taps)	**High**	**Low/Medium**	• Good Performance • Use existing 802.3/OIF-CEI and COM methodology

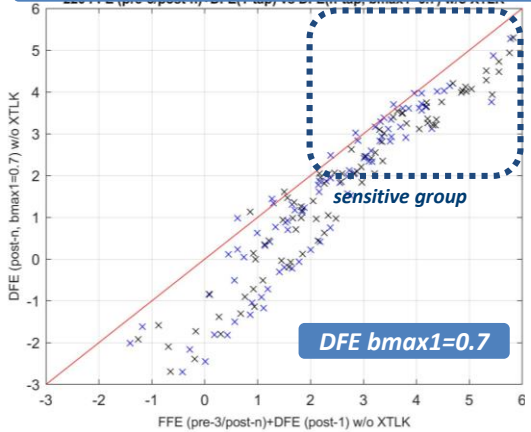
Phase 3: *Can we use a DFE-only baseline receiver to emulate an ADC-based receiver? (~March 2018)*

- **Previous studies (*in Phase 2*) showed Config 2 (FFE-lite/DFE-heavy) approximated well with ADC-based SerDes but task force argued that:**
  - It did not resemble a "*real*" SerDes design
  - It can potentially under-estimate the impact of noises
  - Still needs to develop methodology for calculating RX FFE pre-tap coefficients

- **Studies proposed to improve existing COM ref. receiver, i.e. DFE-only, to match ADC-based designs' performance**
  - Add TX pre-tap 3 in COM's ref. TX
  - Increase DFE coefficient limit, specifically tap 1, to 0.85 (from 0.75)

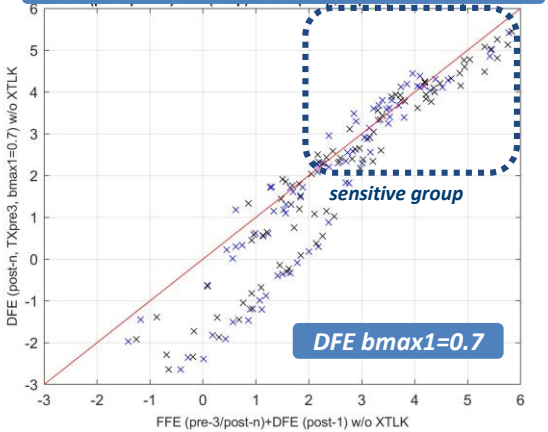
Phase 3: *Can we use a DFE-only baseline receiver to emulate an ADC-based receiver? (Cont.)*

Config 1 (Original: TX pre-2,& 2.5% step size)



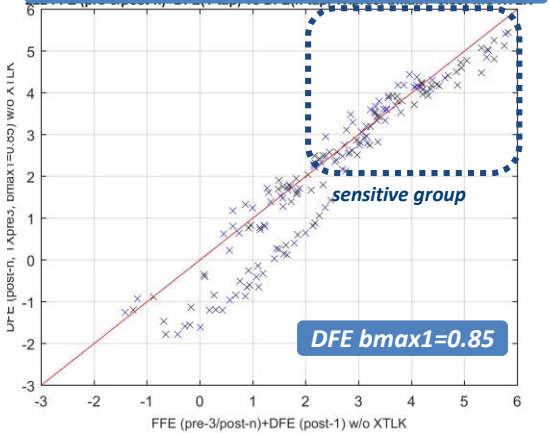
	Value	Note
Mean Diff	0.85	
Sensitive Group Mean Diff	0.65	
False Pass	1	0.59%
False Fail	16	9.41%

Config 1 (w/ TX pre-3 & 2% step size)



	Value	Note
Mean Diff	0.56	
Sensitive Group Mean Diff	0.24	
False Pass	3	1.76%
False Fail	8	4.71%

Config 1 (w/ TX pre-3 & 2% step size)



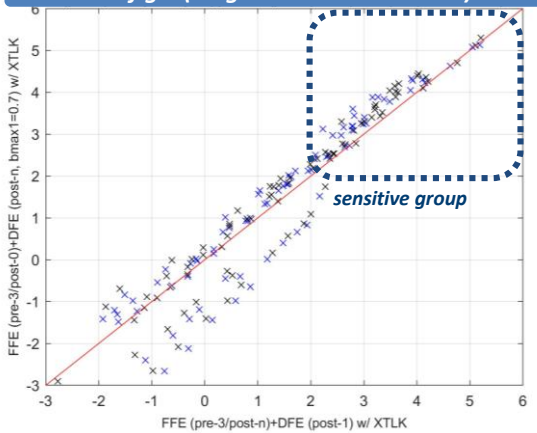
	Value	Note
Mean Diff	**0.33**	
Sensitive Group Mean Diff	**0.14**	
False Pass	**3**	1.76%
False Fail	**7**	4.12%

Original Config 1 is too pessimistic w.r.t. Config 0

Config 1 w/ $b_{max}(1)$=0.85 and TX w/ 3 pre-taps matches better with Config 0

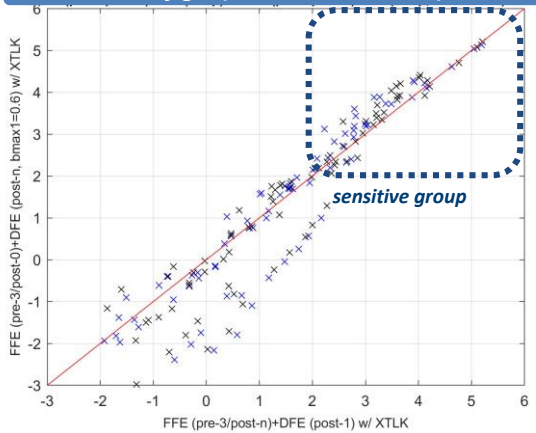
Phase 3: *Can we use a DFE-only baseline receiver to emulate an ADC-based receiver? (Cont.)*

Config 2 (Original: DFE bmax1=0.7)



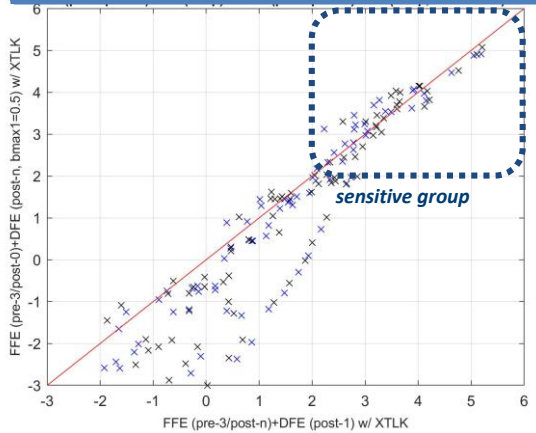
	Value	Note
Mean Diff	0.03	
Sensitive Group Mean Diff	-0.27	
False Pass	11	6.47%
False Fail	0	0.00%

Config 2 (w/ DFE bmax1=0.6)



	Value	Note
Mean Diff	0.29	
Sensitive Group Mean Diff	-0.14	
False Pass	9	5.29%
False Fail	0	0.00%

Config 2 (w/ DFE bmax1=0.5)

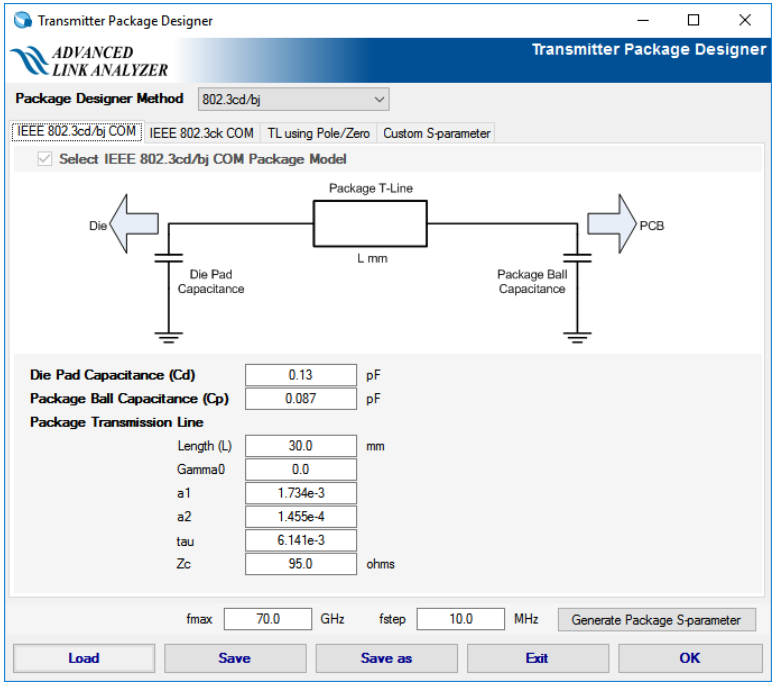


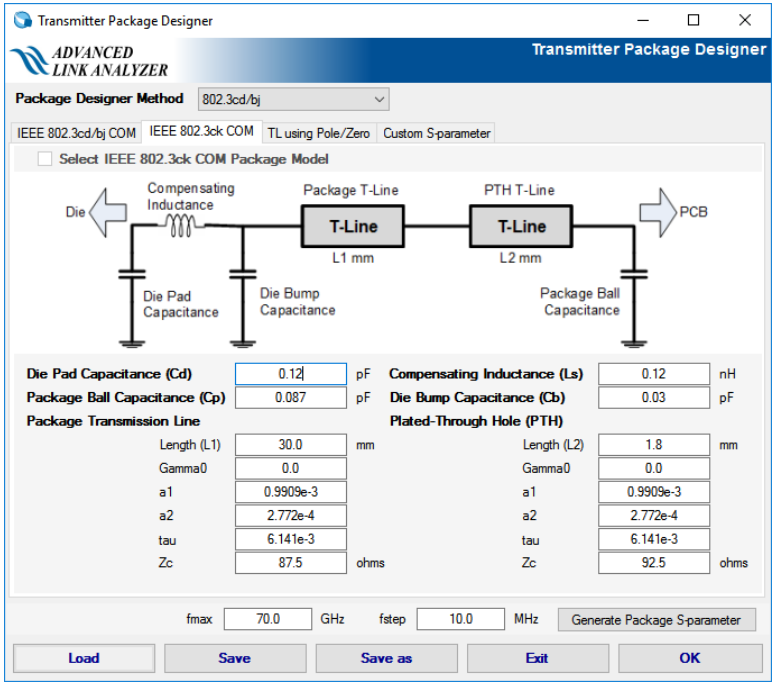
	Value	Note
Mean Diff	**0.81**	
Sensitive Group Mean Diff	**0.09**	
False Pass	**6**	3.32%
False Fail	**2**	1.18%

Original Config 2 is optimistic w.r.t. Config 0

Config 2 w/ $b_{max}(1)$=0.5 matches better with Config 0

Phase 3: *Can we use a DFE-only baseline receiver to emulate an ADC-based receiver? (Cont.)*





Phase 3: *Can we use a DFE-only baseline receiver to emulate an ADC-based receiver? (Cont.)*

- **Observations**
  - With improved package model, improved TX pre-tap 3, and extended DFE coefficient limit (0.85), DFE-only RX baseline model (Config 0) can approximate the performance of ADC-based SerDes design
  - With improved package model, improved TX pre-tap 3, and restricted DFE coefficient limit (0.5), FFE-lite/DFE-heavy RX baseline model (Config 2) can also approximate the performance of ADC-based SerDes design

- **802.3ck adopted DFE-only (Config 0) as COM RX baseline model**
  - Good match to ADC-based SerDes performance in terms of channel coverage
  - Can reuse existing COM model for standards use

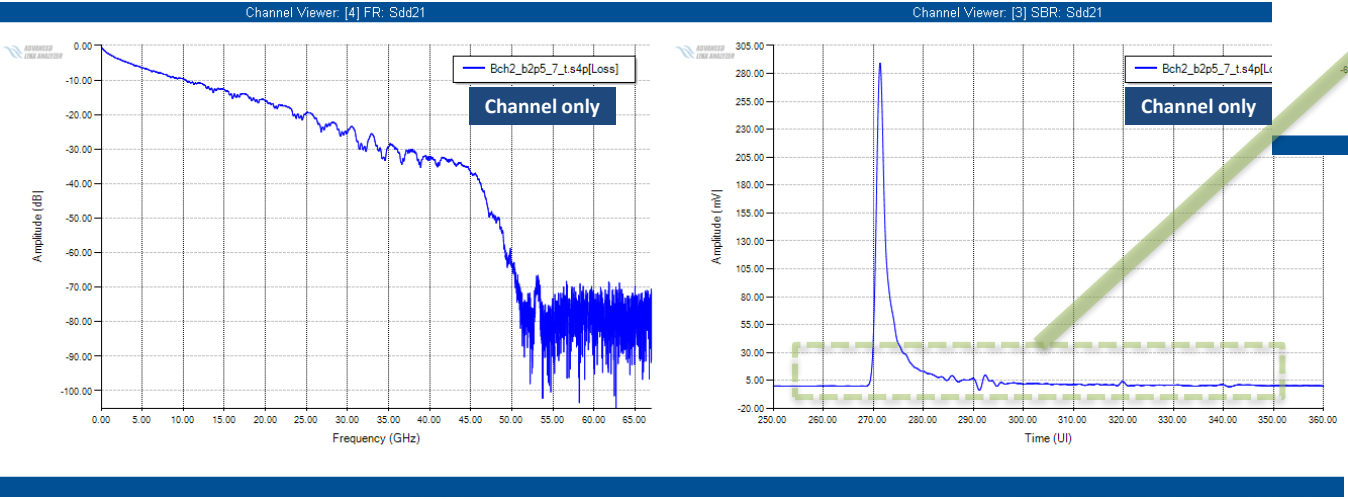
Phase 3: *Improve backplane channel coverage with floating tap DFE (~July 2019)*

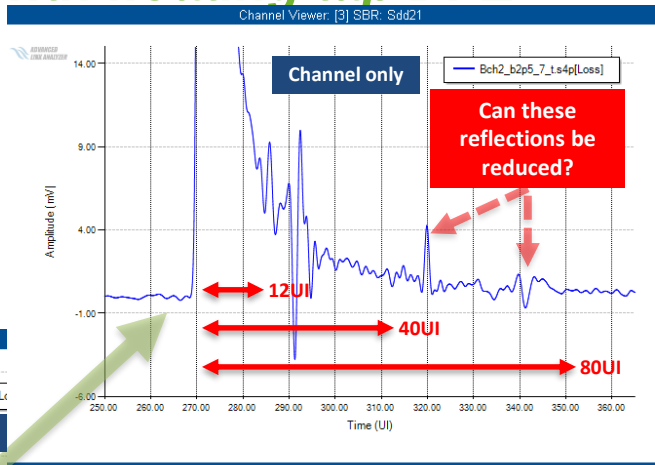
- **Issues**
  - Studies found many test channels requires >100 post taps to pass 3dB COM
  - Studies found that we do not need long consecutive EQ taps to pass 3dB COM

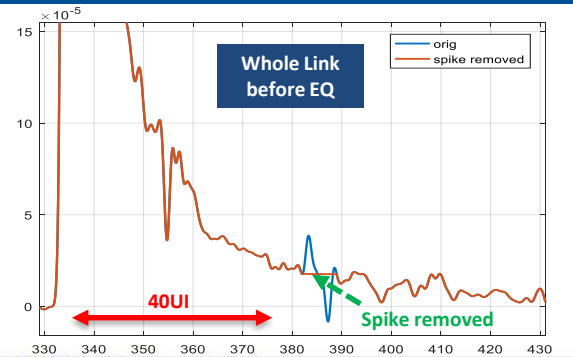
- **Studies/Actions**
  - Narrow down the channel list and eliminate bad/legacy channels
  - Use floating DFE taps

Evolutions of Electrical Spec. and COM Baseline Models

Phase 3: *Improve backplane channel coverage with floating tap DFE (cont.) (~July 2019)*







Summary of Latest 802.3ck and OIF CEI 5.0 Subclasses

Standards	Data Rate & Modulation	Subclass	Applications
IEEE 802.3ck	106.25Gbps, PAM4	KR	Backplane (~28dB IL, up to 2 connectors)
		CR	Cable (~28dB IL with ~2m cable)
		C2C	Chip-to-Chip (~20dB IL, up to 1 connectors)
		C2M	Chip-to-Module (~16dB IL between host and module)
OIF CEI 5.0	72Gbps-116Gbps, PAM4	LR	Long Reach (similar to 802.3ck KR)
		MR	Medium Reach (similar to 802.3ck C2C)
		VSR	Very Short Reach (similar to 802.3 C2M)
		XSR	Extra Short Reach (TBD)

Observations and Next Steps

- **SerDes technology is able to keep up with the increasing data rates. But**
  - w/ cost of increasing complexity and power consumption.
- **Packaging and channel are not able to scale with data rates due technologies and/or cost**
  - Usable channel insertion loss is reduced to ~28dB.
- **Channel characteristics becomes more challenging**
  - Drives up the complexity of equalization and subsequently drives up the power consumption.
- **COM baseline device specifications are de-coupled from actual SerDes architectures and designs**
  - COM baseline specifications just represent the capability of a SerDes
- **Burst error due to DFE is likely to be less than the COM baseline RX implied**
  - COM's DFE-only baseline receiver has tap 1 coefficient limit of 0.85. In ADC-based SerDes designs, where tap 1 ISI is to be compensated by TX FIR, RX FFE and RX DFE, DFE tap 1 coefficient will likely to be much lower.
- **TX FIR and RX FFE in ADC-based SerDes will reduce FEC performance**
  - Due to reduced SNR at receiver's slicer

Observations and Next Steps *(cont.)*

- **Burst errors caused by multi-tap DFE will be less likely to occur**
  - Because ADC-based SerDes designs usually have one or very few DFE taps.
  - This will simplify FEC modeling and performance analysis.

Next Steps

- **Need more theoretical researches and correlation studies in the interactions among TX FIR, FFE, DFE, and FEC**
- **HSIO industry and standard bodies need to start embracing ADC and FFE effects in the specification setting and compliance test methodologies**

Thank you!

QUESTIONS?