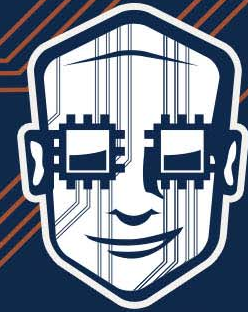


**DESIGNCON<sup>®</sup> 2015**



**100 GB/S ETHERNET - 100GBASE-CR4  
TEST POINTS AND TEST FIXTURES**

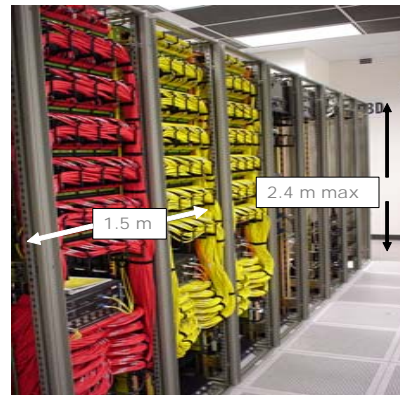


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## IEEE 802.3bj – 100GBASE-CR4

- IEEE Standard for Ethernet Amendment 2: Physical Layer Specifications and Management Parameters for 100 Gb/s Operation Over Backplanes and Copper
- 100 Gb/s backplane and copper cable port type 100GBASE-CR4
- Passive twinaxial copper cable assemblies of lengths up to at least 5 meters
- Interconnection of switches and server's in equipment racks within the data center, computer room, and central office environments.

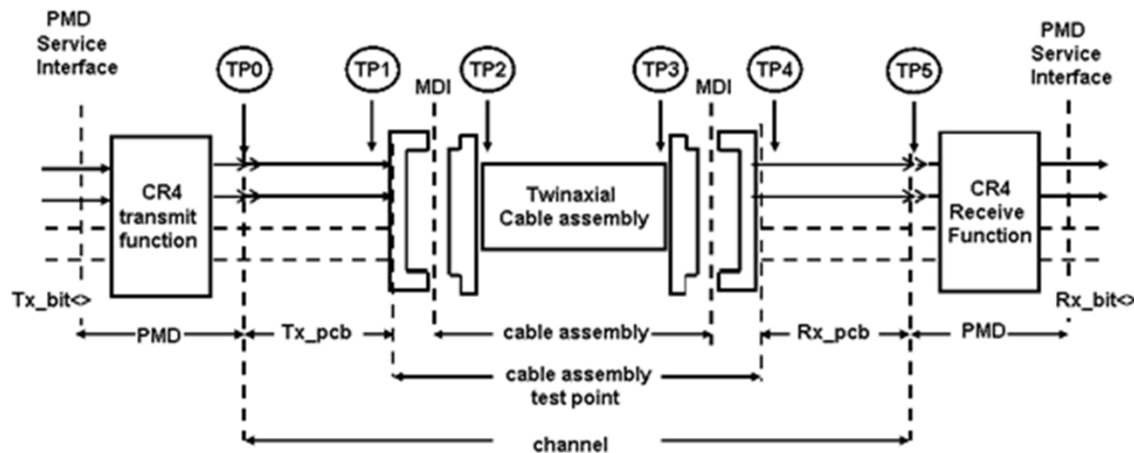


## Abstract

- Overview 100GBASE-CR4 test point specifications and test fixtures for testing;
  - transmitter and receiver signals
  - twinaxial copper cable assemblies
- Demonstration of achievability of conformance to the 100GBASE-CR4 test fixture s-parameter specifications;
  - HFSS models
  - vector network analyzer measurements

## Channel and link Definitions

- The channel is defined between the transmitter and receiver blocks to include the transmitter and receiver differential controlled impedance printed circuit board and the cable assembly.
- The Media dependent interfaces (MDIs) refer to the connector interfaces. 100GBASE-CR4 specifies the quad small form factor pluggable (QSFP28) plug and receptacle.



## Test Points and Descriptions

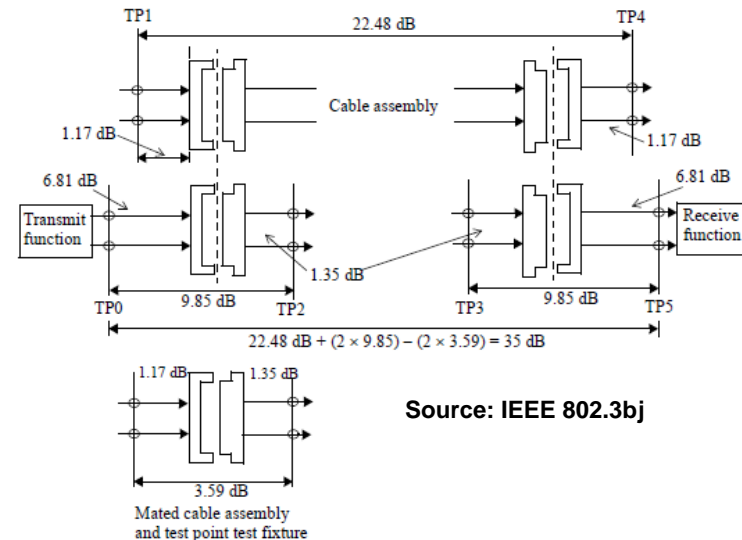
- For conformance testing five test points are standardized.

Test Points	Description
TP0 to TP5	The channel is defined between the transmitter and receiver blocks to include the transmitter and receiver differential controlled impedance printed circuit board and the cable assembly.
TP1 to TP4	All cable assembly measurements between TP1 and TP4. are performed with the test fixtures specified in 100GBASE-CR4.
TP0 to TP2 TP3 to TP5	A mated connector pair is included in both the transmitter and receiver specifications.
TP2	Transmitter parameters are measured at TP2 utilizing the test fixture specified in 100GBASE-CR4.
TP3	Receiver parameters are measured at TP3 utilizing the test fixture specified in 100GBASE-CR4.

# Channel Parameters and Insertion Loss Budgets

- TP0 and TP5 may not be accessible in an implemented system
- Information (not required for conformance) of channel transmission characteristics and insertion loss budgets provided in Annex's.

Parameter description	f(GHz)	Unit
Transmitter and receiver differential printed circuit board trace loss (host PCB insertion loss 6.81 dB @12.89 GHz)	$0.05 \leq f \leq 19$	dB
Channel Insertion Loss (6.81 dB @12.89 GHz)	$0.05 \leq f \leq 19$	dB
Maximum channel insertion Loss (35 dB @12.89 GHz)	$0.05 \leq f \leq 19$	dB
Minimum channel insertion loss (x dB @12.89 GHz)	$0.05 \leq f \leq 19$	dB
Channel operating margin (3 dB)		dB



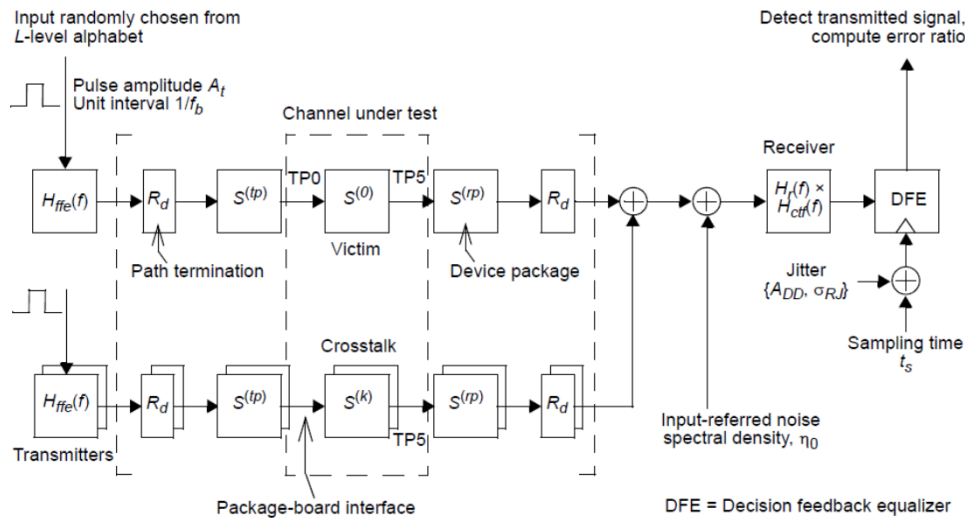
Source: IEEE 802.3bj

Insertion loss budget @ 12.89 GHz



# The Channel Operating Margin (COM)

- A figure of merit for a channel derived from a measurement of its scattering parameters. COM is related to the ratio of a calculated signal amplitude to a calculated noise amplitude; channel operating margin (3 dB).



DFE = Decision feedback equalizer

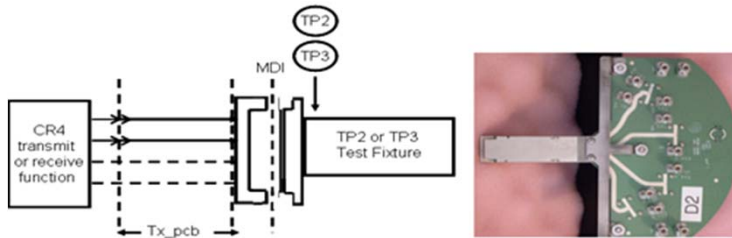
Source: IEEE 802.3bj

Parameter	Symbol	Value	Units
Signaling rate	$f_b$	25 781.25	GHz
Maximum start frequency	$f_{sb}$	0.05	GHz
Maximum frequency step	$\Delta f$	0.01	GHz
Device package model			
Single-ended device capacitance	$C_d$	$2.5 \times 10^{-4}$	nF
Transmission line length, Test 1	$L_1$	12	mm
Transmission line length, Test 2	$L_2$	20	mm
Single-ended package capacitance at package-to-board interface	$C_p$	$1.8 \times 10^{-4}$	nF
Single-ended reference resistance	$R_0$	50	$\Omega$
Single-ended termination resistance	$R_d$	55	$\Omega$
Receiver 3 dB bandwidth	$f_r$	$0.75 \times f_b$	GHz
Transmitter equalizer, minimum corner coefficient	$c(0)$	0.62	—
Transmitter equalizer, pre-cursor coefficient	$c(-1)$	-0.18	—
Minimum value		0	—
Maximum value		0.02	—
Step size			—
Transmitter equalizer, post-cursor coefficient	$c(1)$	-0.38	—
Minimum value		0	—
Maximum value		0	—
Step size		0.02	—
Continuous time filter, DC gain	$g_{DC}$	-12	dB
Minimum value		0	dB
Maximum value		1	dB
Step size			—
Continuous time filter, zero frequency	$f_z$	$f_b/4$	GHz
Continuous time filter, pole frequency	$f_p$	$f_b$	GHz
Transmitter differential peak output voltage	$A_v$	0.4	V
Victim	$A_v$	0.4	V
Facial aggressor	$A_v$	0.6	V
Near-end aggressor	$A_v$	0.6	V
Number of signal levels	$L$	2	—
Level separation mismatch ratio	$R_{LM}$	1	—
Transmitter signal-to-noise ratio	$SNR_{Tx}$	27	dB
Number of samples per unit interval	$M$	32	—
Decision feedback equalizer (DFE) length	$N_D$	14	UI
Normalized DFE coefficient magnitude limit, for $n = 1$ to $N_D$	$h_{max}(n)$	1	—
Random jitter, RMS	$\sigma_{RJ}$	0.01	UI
Dual-Delay jitter, peak	$A_{DD}$	0.05	UI
One-sided noise spectral density	$\eta_0$	$5.2 \times 10^{-6}$	V <sup>2</sup> /KHz
Target detector error ratio	$BER_D$	$10^{-9}$	—



## Transmitter and Receiver Parameters TP2/TP3

- The electrical transmit signals is defined at the output end of the mated connector (TP2) and all receiver measurements and tests are made at the input end of the mated connector (TP3).



Parameter	Subclause reference	Value	Units
Receiver input amplitude tolerance	92.8.4.1	1200 mV as measured at TP2	mV
Differential input return loss (min)	92.8.4.2	Equation (92-20)	dB
Differential to common-mode input return loss	92.8.4.3	Equation (92-21)	dB
Interference Tolerance	92.8.4.4	Table 92-8	—
Signaling rate, per lane	92.8.4.6	25.78125 ± 100 ppm	GBd
Unit interval (UI) nominal	92.8.4.6	38.787879	ps

Receiver characteristics at TP3 summary

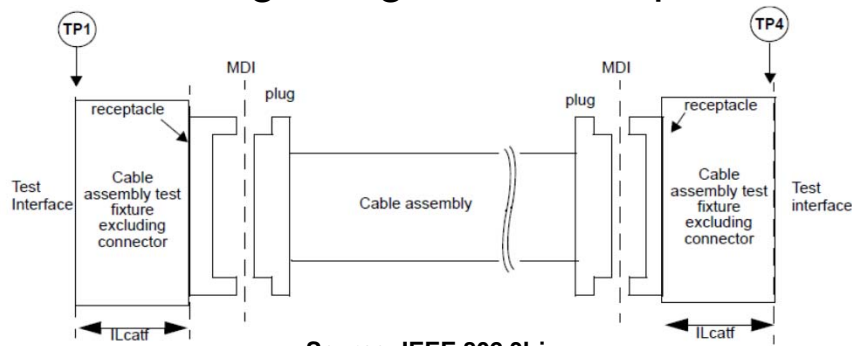
Source: IEEE 802.3bj

Parameter	Subclause reference	Value	Units
Differential peak-to-peak output voltage (max.) with Tx disabled	92.8.3.1	35	mV
DC common-mode voltage (max.)	92.8.3.1	1.9	V
AC common-mode output voltage, $v_{cmi}$ (max., RMS)	92.8.3.1	30	mV
Differential peak-to-peak voltage, $v_{di}$ (max.)	92.8.3.1	1200	mV
Differential output return loss (min.)	92.8.3.2	See Equation (92-1)	dB
Common-mode to differential mode output return loss (min.)	92.8.3.3	See Equation (92-2)	dB
Common-mode to common-mode output return loss (min.)	92.8.3.4	See Equation (92-3)	dB
Transmitter steady-state voltage, $v_f$ (min.)	92.8.3.5.2	0.34	V
Transmitter steady-state voltage, $v_f$ (max.)	92.8.3.5.2	0.6	V
Linear fit pulse peak (min.)	92.8.3.5.2	$0.45 \times v_f$	V
Transmitted waveform			
abs coefficient step size (min.)	92.8.3.5.4	0.0083	
abs coefficient step size (max.)	92.8.3.5.4	0.05	
minimum precursor full-scale ratio	92.8.3.5.5	1.54	
minimum post cursor full-scale ratio	92.8.3.5.5	4	
Signal-to-noise-and-distortion ratio (min.)	92.8.3.7	26	dB
Output jitter (max.)			
Even-odd jitter, peak-to-peak	92.8.3.8.1	0.035	UI
Effective bounded uncorrelated jitter, peak-to-peak	92.8.3.8.2	0.1	UI
Effective total uncorrelated jitter, peak-to-peak	92.8.3.8.2	0.18	UI
Signaling rate, per lane	92.8.3.9	25.78125±100 ppm	GBd
Unit interval nominal	92.8.3.9	38.787879	ps

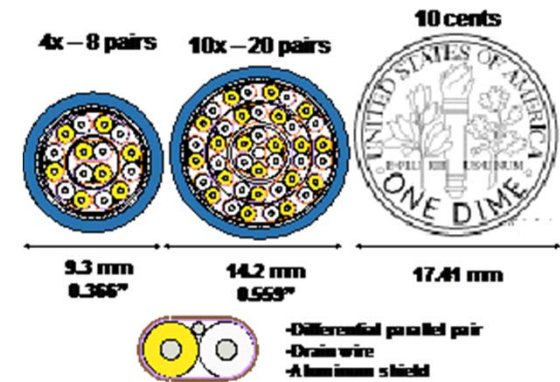
Transmitter characteristics at TP2 summary

## Cable Assembly Characteristics TP1/TP4

- The twinaxial copper cable assembly consists of shielded signal pairs utilized for differential signaling at 25 Gb/s per differential signal pair.



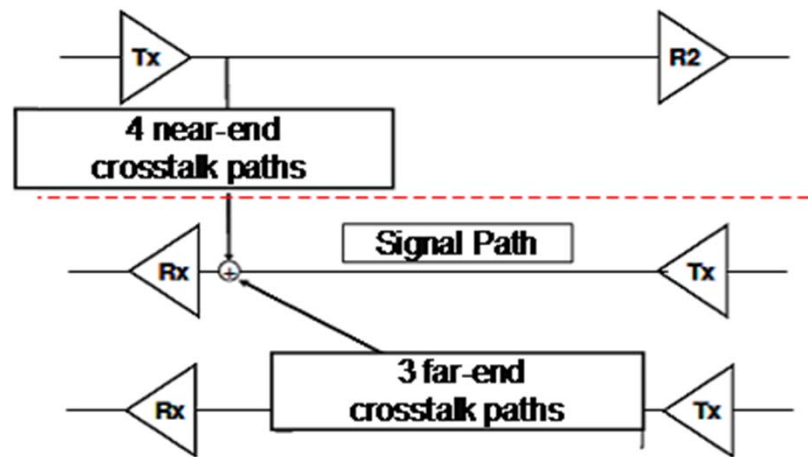
Source: IEEE 802.3bj



Parameter description	f(GHz)	Unit
Maximum Insertion Loss (22.48 dB)	@12.89 GHz	dB
Minimum Insertion Loss (8 dB @ 12.89 GHz)	$0.05 \leq f \leq 19$	dB
Minimum Return Loss	$0.05 \leq f \leq 19$	dB
Differential to common-mode return loss	$0.05 \leq f \leq 19$	dB
Differential to common-mode conversion loss	$0.05 \leq f \leq 19$	dB
Common-mode to common-mode return loss	$0.05 \leq f \leq 19$	dB
Common-mode to common-mode return loss	$0.05 \leq f \leq 19$	dB
Cable assembly Channel Operating Margin (3 dB)		dB

## Cable Assembly Channel (COM)

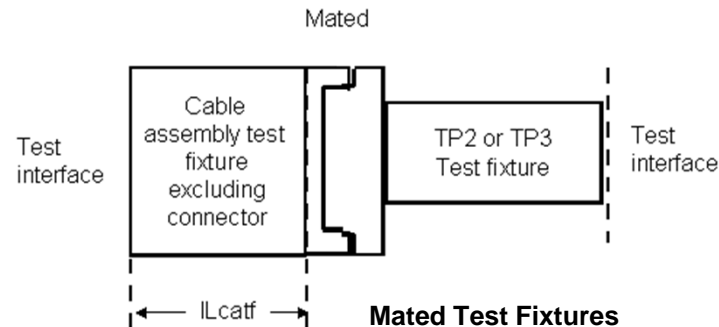
- The cable assembly Channel Operating Margin (COM) for each victim signal path (receive lane) is derived from measurements of the cable assembly victim signal path, the four individual near-end crosstalk paths, and the three far-end crosstalk paths that can couple into a victim signal path.



Cable assembly signal paths and crosstalk paths for COM

## Test Fixture Specifications

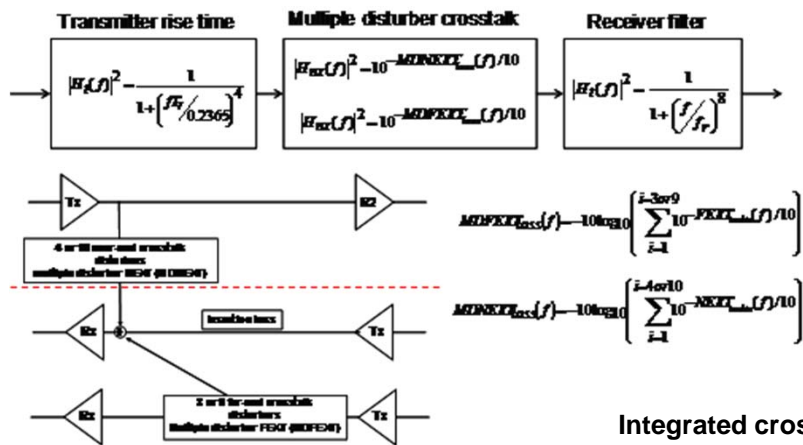
- Test fixtures specified in a mated state used for testing the transmitter, the receiver and cable assembly measurements
  - The TP2/TP3 test fixture also known in the industry as Host Compliance Board (HCB) is required for measuring the transmitter specifications at TP2 and the receiver return loss at TP3.
  - The cable assembly test fixture also known in the industry as Module Compliance Board (MCB) is required for measuring the cable assembly specifications at TP1 and TP4.



# Mated Test Fixtures Parameters

Parameter description	f(GHz)	Unit
Maximum insertion Loss	0.01≤f≤25	dB
Minimum Insertion Loss	0.01≤f≤25	dB
Minimum Return Loss	0.01≤f≤25	dB
Common-mode conversion insertion loss	0.01≤f≤25	dB
Common-mode return loss	0.01≤f≤25	dB
Common-mode to differential –mode return loss	0.01≤f≤25	dB
Integrated crosstalk noise		

Mated test fixtures parameters



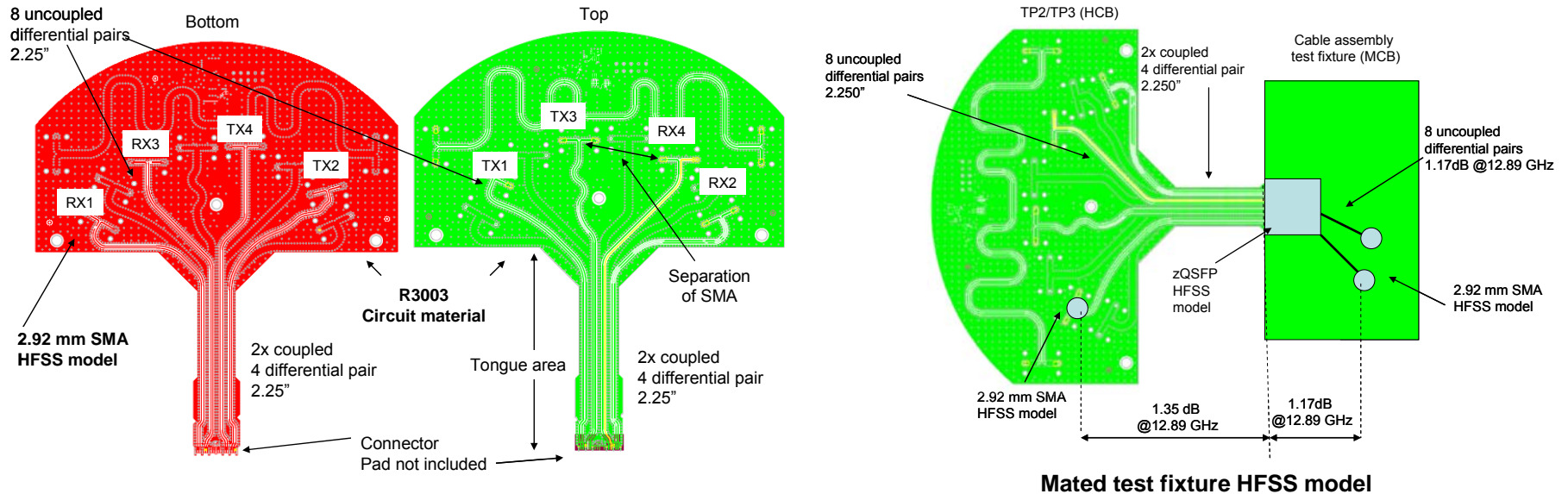
Description	Symbol	Value	Units
Symbol rate	$f_b$	25.78125	GBd
Near-end disturber peak differential output amplitude	$A_{nt}$	600	mV
Far-end disturber peak differential output amplitude	$A_{ft}$	600	mV
Near-end disturber 20% to 80% rise and fall times	$T_{nt}$	9.6	ps
Far-end disturber 20% to 80% rise and fall times	$T_{ft}$	9.6	ps

Source: IEEE 802.3bj

Integrated crosstalk noise (ICN)

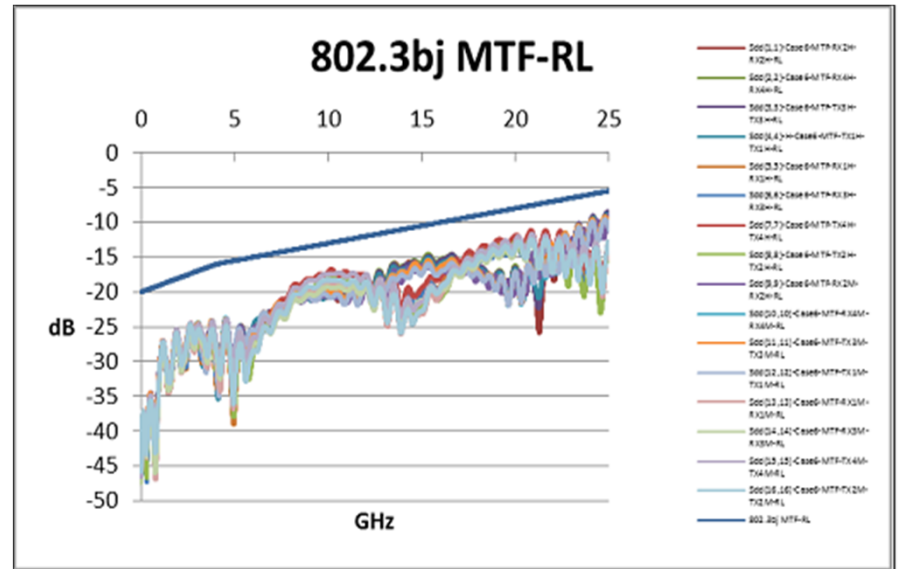
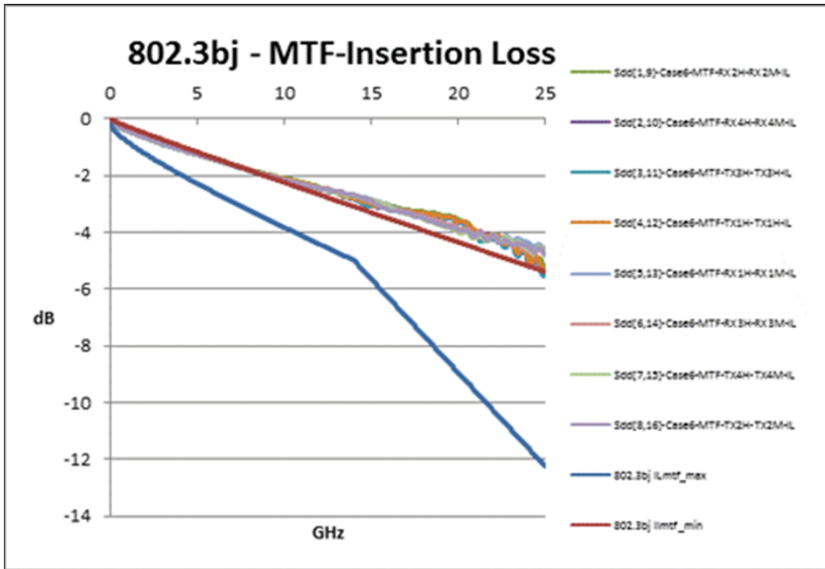
## TP2/TP3 (HCB) HFSS Model

- TP2/TP3 (HCB) test fixture insertion loss specification of 1.35 dB @12.89 GHz yields an insertion loss of approximately 0.3 dB/in @12.89 GHz.



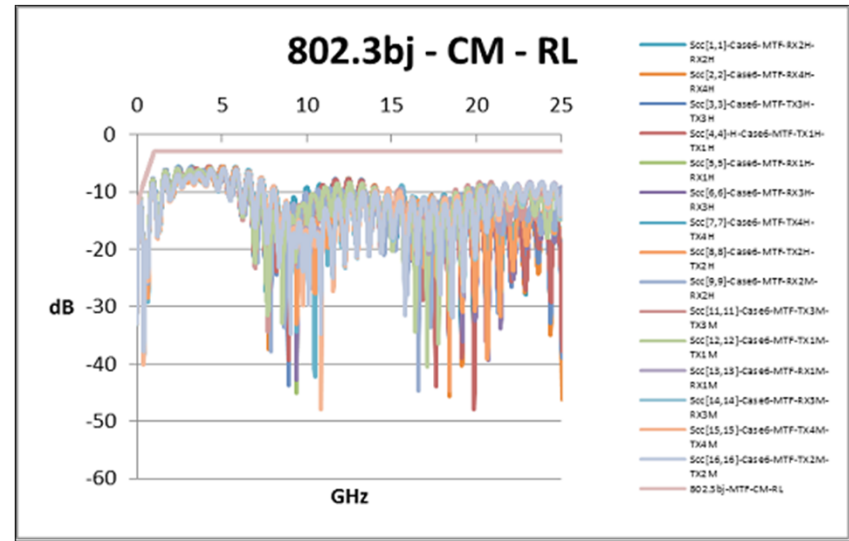
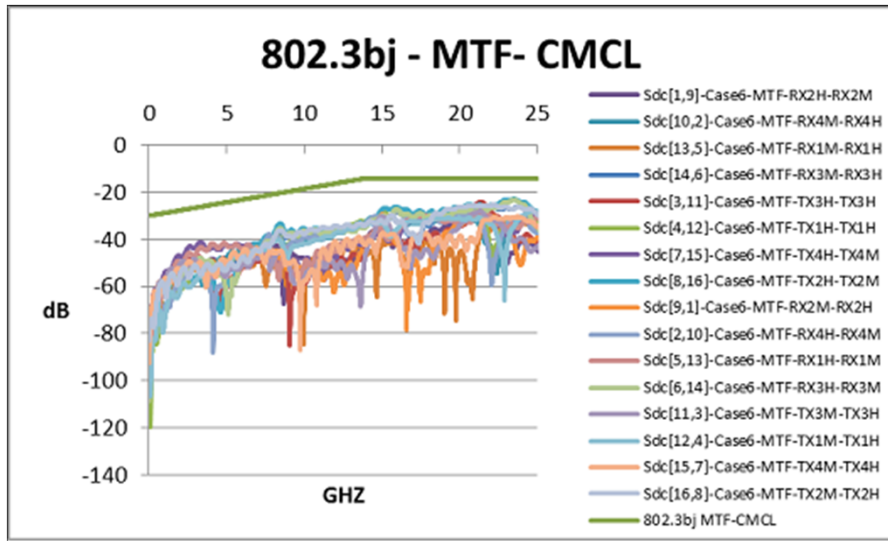


# Mated Test Fixture – HFSS Model

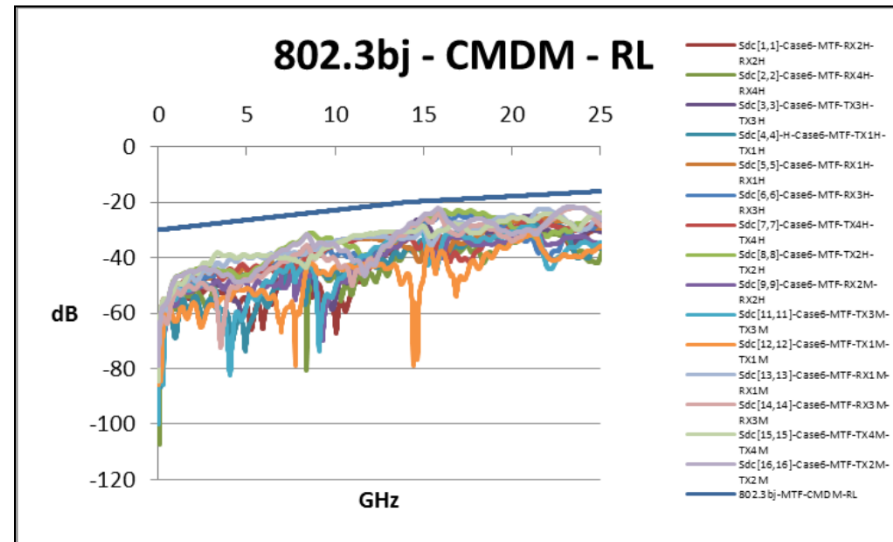




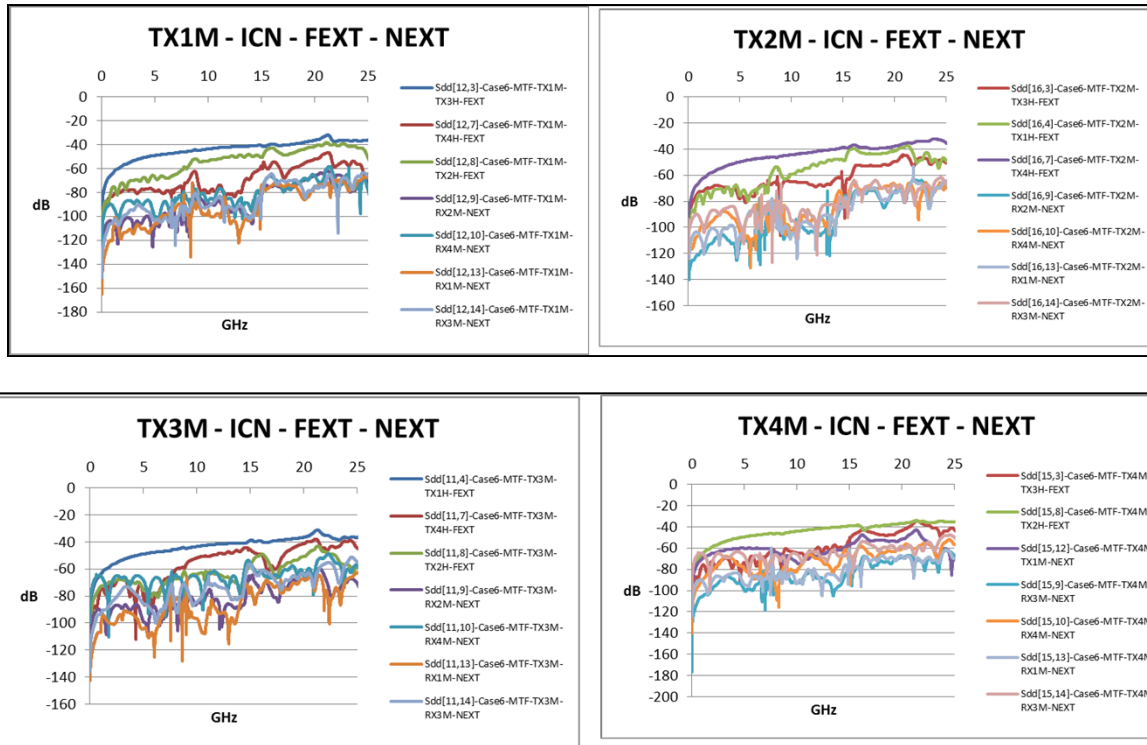
# Mated Test Fixture – HFSS Model



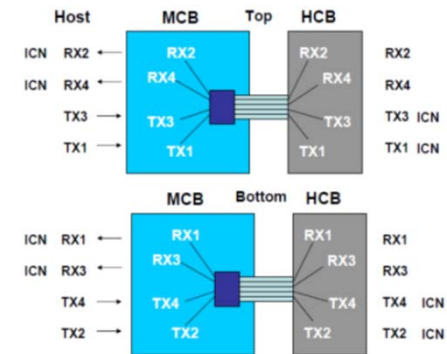
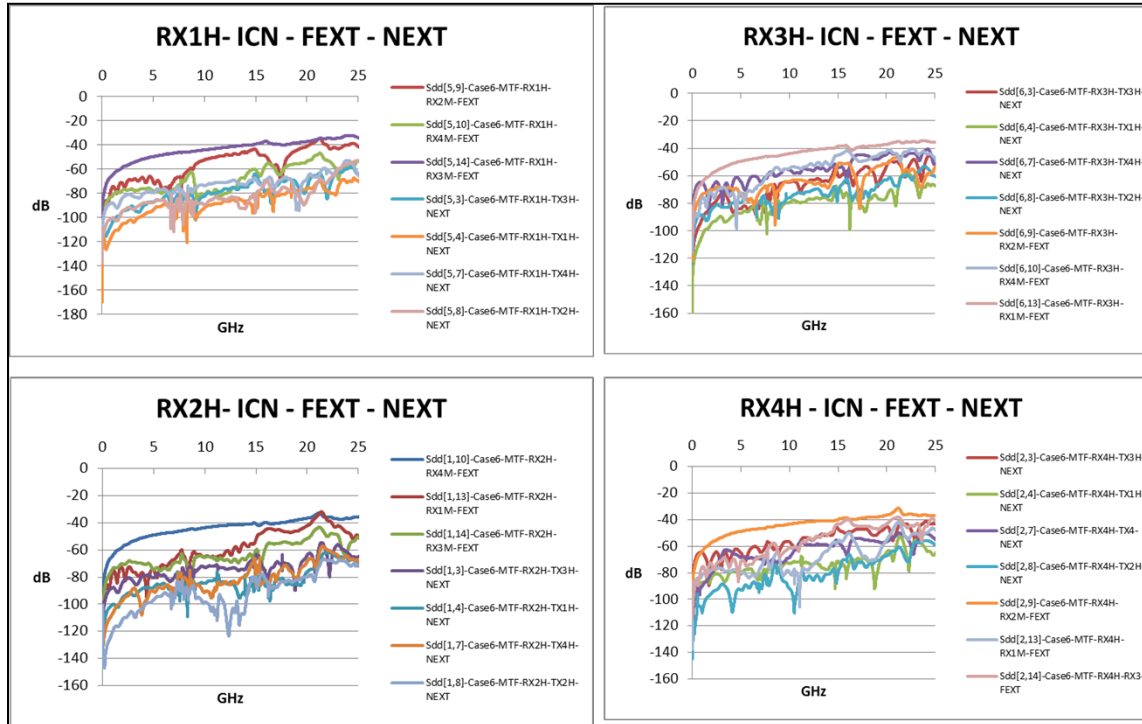
## Mated Test Fixture – HFSS Model



# Mated Test Fixture – HFSS Model



# Mated Test Fixture – HFSS Model

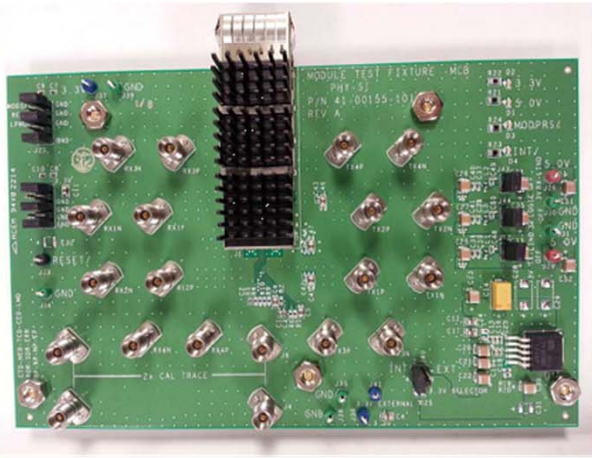


Parameter	100GBASE-CR4	Units
MDNEXT integrated crosstalk noise voltage	less than 1.8	mV
MDFEXT integrated crosstalk noise voltage	less than 4.8	mV

	RX1	RX2	RX3	RX4
MDNEXT ICN (mV)	0.11	0.10	0.73	0.81
MDFEXT ICN (mV)	2.91	2.80	2.95	3.01

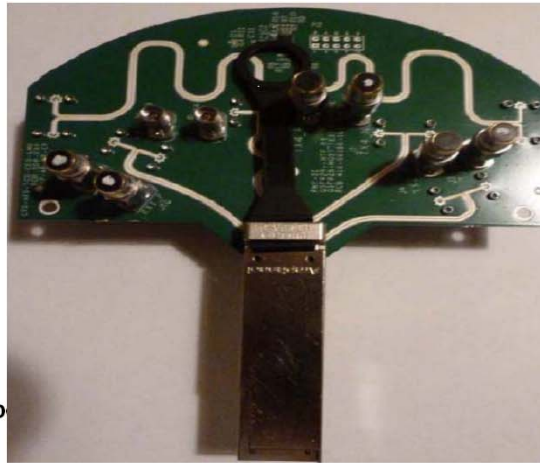
	TX1	TX2	TX3	TX4
MDNEXT ICN (mV)	0.07	0.07	0.30	0.30
MDFEXT ICN (mV)	2.90	2.94	2.99	2.84

## Test Fixtures



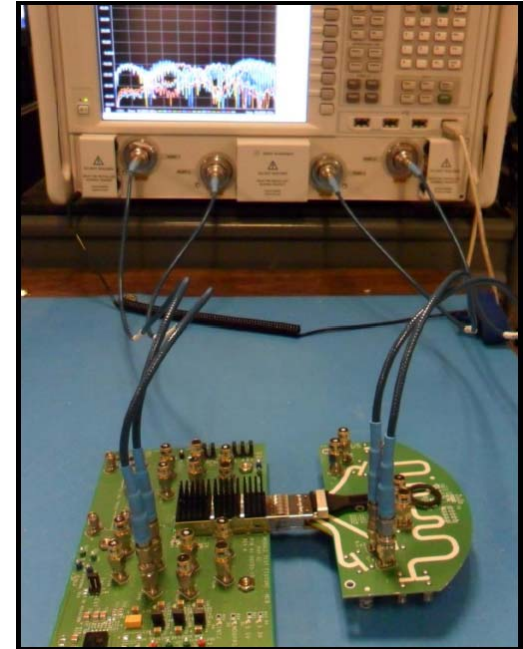
Module compliance board (MCB)

- Cable assembly test fixture
- Module test fixture
- TP1 to TP4 test fixture



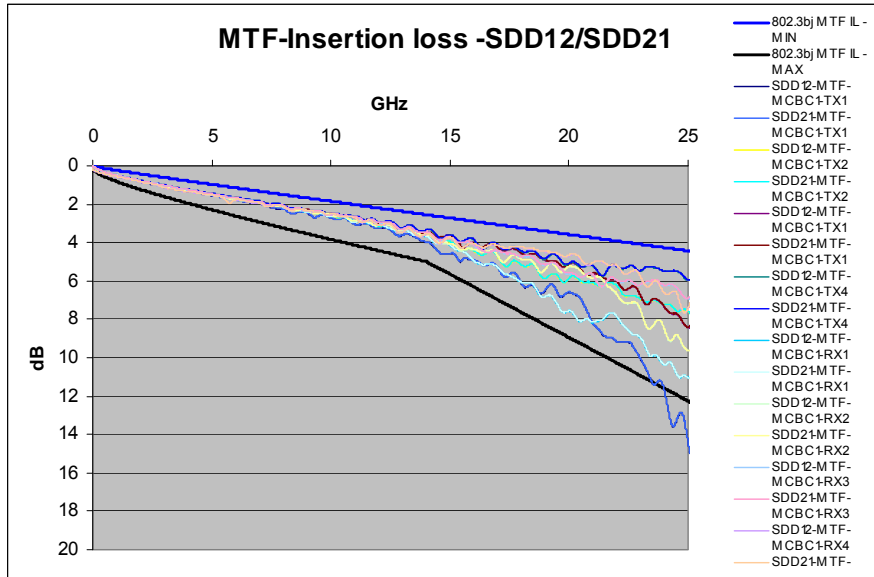
Host compliance board (HCB)

- TP2 or TP3 Test Fixture



PHY-SI Mated test fixtures measured at University of New Hampshire Interoperability Test Lab (UNH-IOL)

# Mated Test Fixture – Measurements

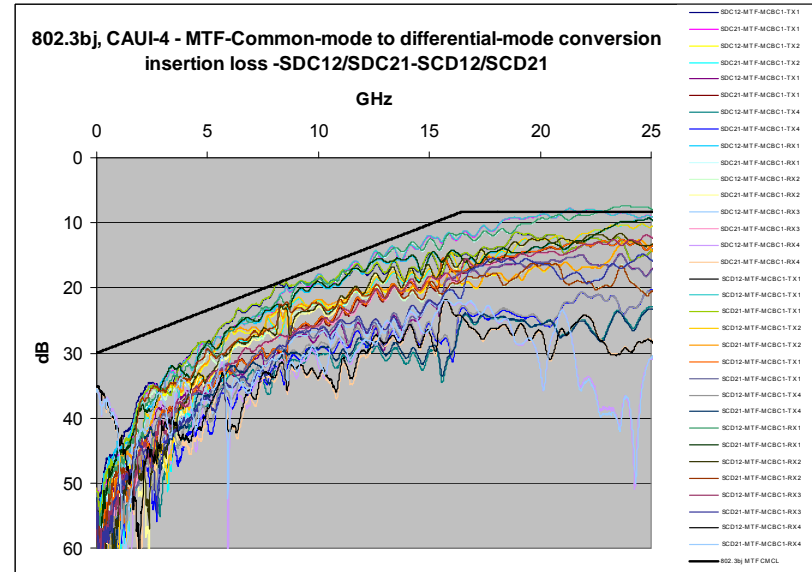
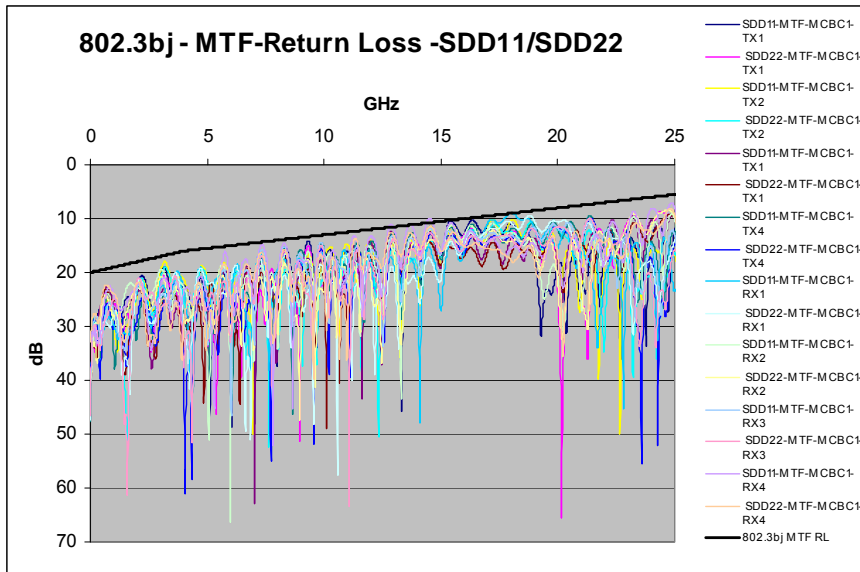


FOM<sub>ILD</sub> is calculated according to 93A.4 with  $f_b=25.78125$  GHz,  $T_r=9.6$  ps, and  $f_r=0.75 \times f_b$ . The fitted insertion loss and insertion loss deviation are computed over the range  $f_{min}=0.01$  GHz to  $f_{max}=25$  GHz. FOM<sub>ILD</sub> shall be less than 0.13 dB.

Lane	FOM <sub>ILD</sub> (dB)
TX1	0.075
TX2	0.045
TX3	0.039
TX4	0.044
RX1	0.067
RX2	0.046
RX3	0.042
RX4	0.053

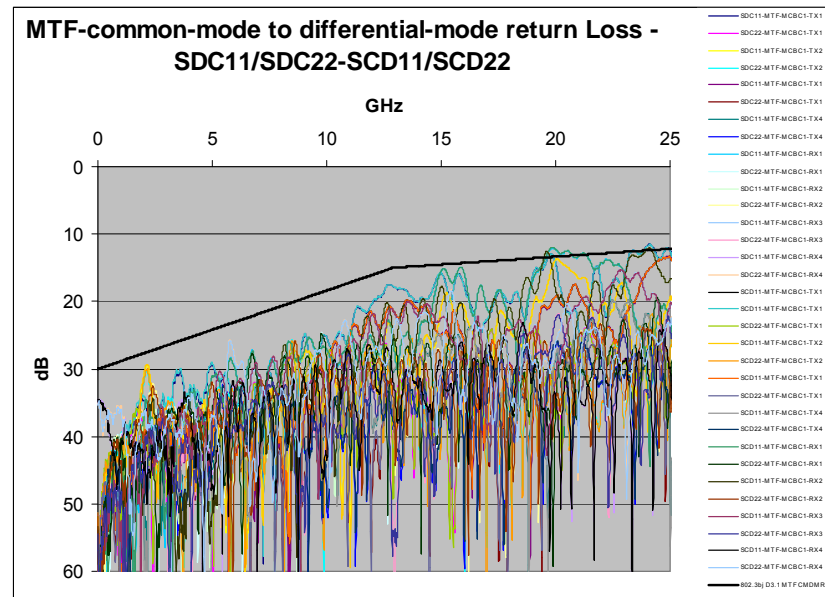


# Mated Test Fixture – Measurements

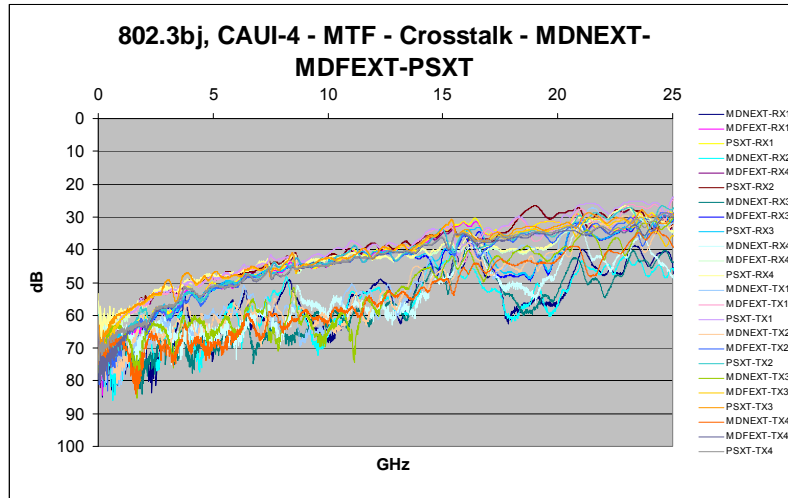




# Mated Test Fixture – Measurements



# Mated Test Fixture – Measurements

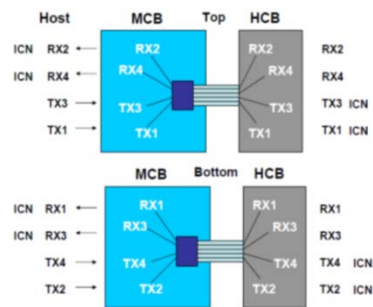


Description	Symbol	Value	Units
Symbol rate	$f_b$	25.78125	GBd
Near-end disturber peak differential output amplitude	$A_{nt}$	600	mV
Far-end disturber peak differential output amplitude	$A_{ft}$	600	mV
Near-end disturber 20% to 80% rise and fall times	$T_{nt}$	9.6	ps
Far-end disturber 20% to 80% rise and fall times	$T_{ft}$	9.6	ps

Parameter	100GBASE-CR4	Units
MDNEXT integrated crosstalk noise voltage	less than 1.8	mV
MDFEXT integrated crosstalk noise voltage	less than 4.8	mV

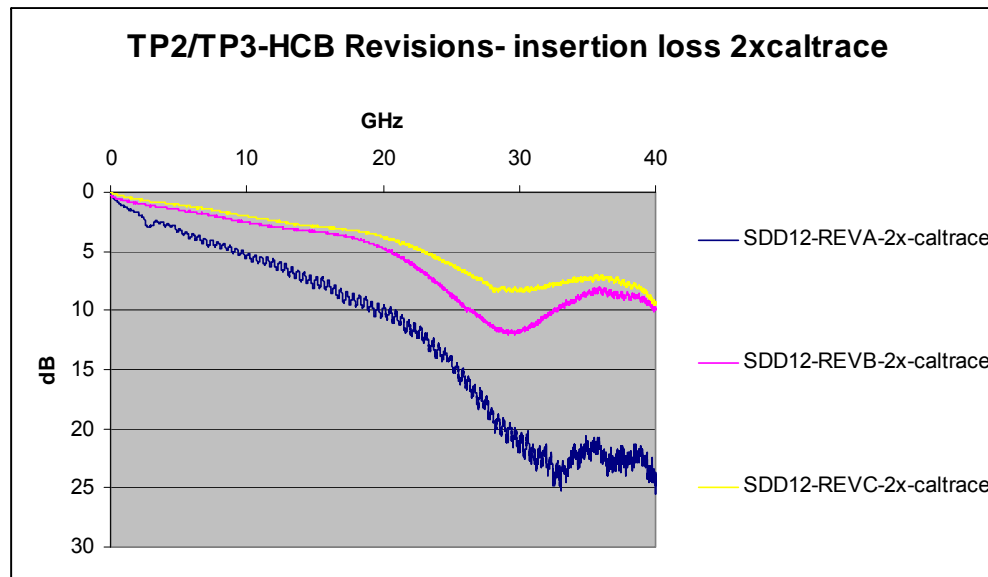
	RX1	RX2	RX3	RX4
MDNEXT ICN (mV)	1.08	0.95	1.00	0.95
MDFEXT ICN (mV)	3.72	4.09	2.77	3.01

	TX1	TX2	TX3	TX4
MDNEXT ICN (mV)	1.39	1.13	1.11	0.81
MDFEXT ICN (mV)	4.17	3.19	3.74	3.00



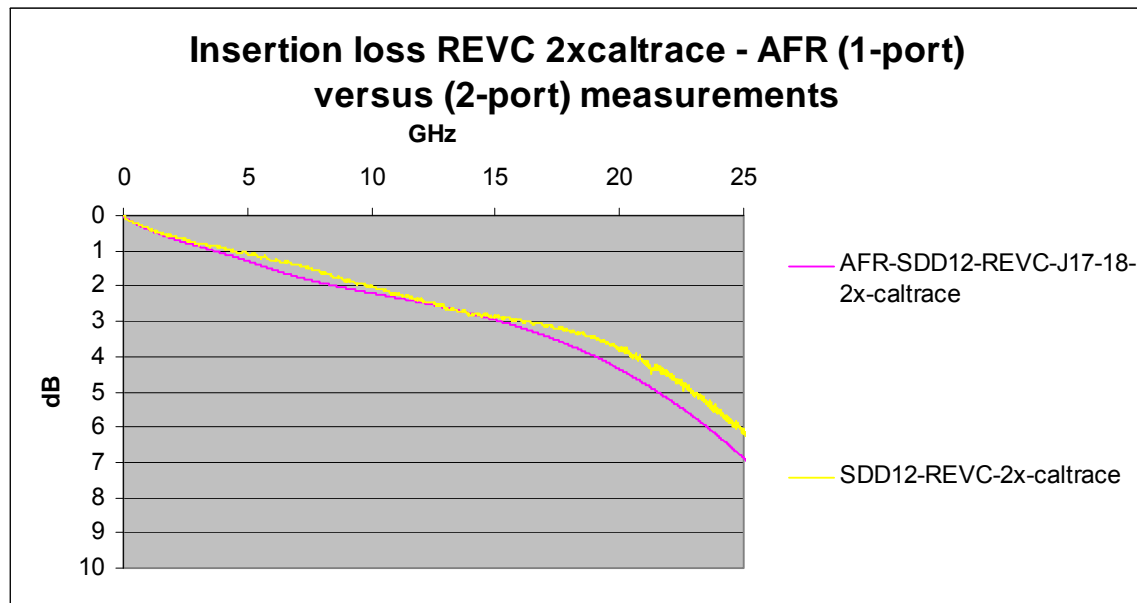
## 2x Calibration Trace – Measurements

- Three revisions of the PHY-SI TP2/TP3 HCB test fixture improvements; transmission line structure, PCB materials, plating over copper, differential and ground trace geometries, ground plane stitching symmetry, proximity of solder mask to differential trace placement and tightly controlled PCB fabrication tolerances.



## Automatic Fixture Removal (AFR) Software

- Viability of open ended test fixture measurements (i.e., tested in an unmated state) was explored using Keysight's physical layer test software (PLTS) automatic fixture removal (AFR) software.



## Summary

- Overview 100GBASE-CR4 test point specifications and test fixtures
- The achievability of meeting the 100GBASE-CR4 test fixture s-parameter specifications was demonstrated in HFSS models as well as by vector network analyzer measurements
- Test fixture measurement results were presented and compared to the s-parameter specification limits.
- Revisions of the PHY-SI TP2/TP3 HCB test fixture design depicting insertion loss improvements based on design attributes were illustrated.
- Considerations for the viability of open ended test fixture measurements (i.e., tested in an unmated state) was explored using Keysight's physical layer test software (PLTS) automatic fixture removal (AFR) software.

## Acknowledgements

- The authors thank Curtis Donahue-University of New Hampshire Interoperability Test Lab (UNH-IOL) and Arnav Shah-Cisco Systems for the for the laboratory measurements and O.J. Danzy-Keysight Technologies for assistance with PLTS AFR.