Electronics Desktop: PAM4 Signaling for Circuit Analyses

Modern high speed serial designs are increasingly looking to PAM4 signaling to overcome some of the limitations of NRZ binary. ANSYS Electronics Desktop has added support for PAM4 signaling in the circuit QuickEye, VerifEye, and IBIS-AMI analyses. This feature includes support for PAM4 via additional options in transmitter components and new post processing capabilities to analyze multi-level signaling.

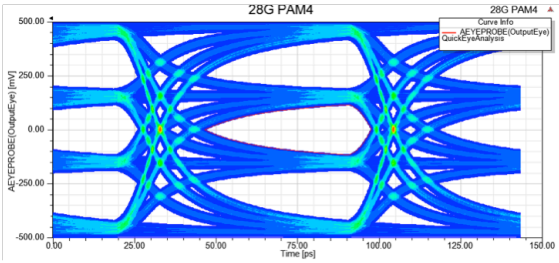

Figure 1 – 28 Gb/s PAM4 Eye Diagram

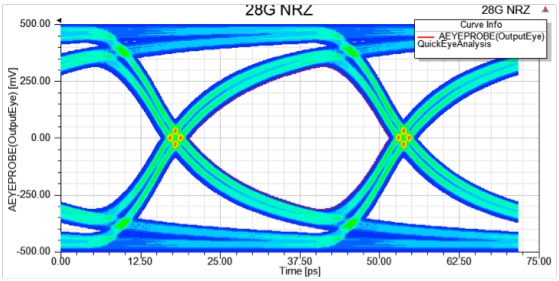

Figure 2 – 28Gb/s NRZ Eye Diagram

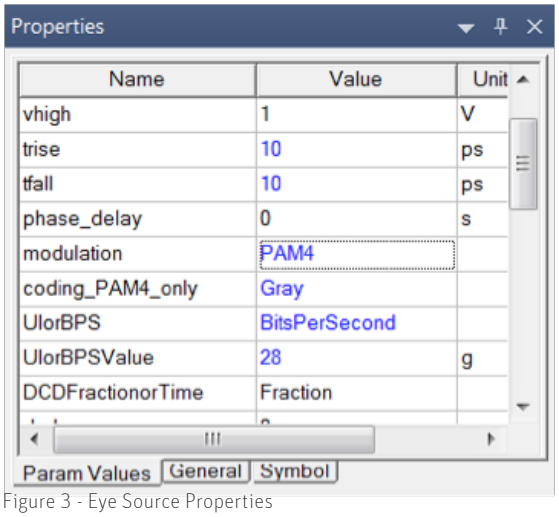

Figure 3 - Eye Source Properties

Introduction

PAM4, also known as 4-level pulse amplitude modulation, is a method of encoding two binary bits into a single symbol mapped to one of four logic levels. When transmitted with the same unit interval (UI), PAM4 transmits twice as much data as Non-Return to Zero (NRZ) binary. Similarly, if transmitting at the same data rate, PAM4 will use a UI twice as large as what is used for NRZ. This is shown in Figures 1 and 2 where at 28Gb per second, PAM4 signaling uses a 71.4ps UI and NRZ uses a 35.7ps UI.

PAM4 Setup in AEDT

PAM4 signaling can be set in Ansys Electronic Desktop (AEDT) in the Eye Source component as well as in IBIS-AMI transmitter components (assuming that the underlying AMI executables support PAM4 signaling). These components have a new property (Figure 3) called “Modulation,” which allows you to select either PAM4 or NRZ signaling.

Additionally, there is a second new property called “Coding” which, in the case of PAM4 signaling, enables you to select gray or linear coding of the PAM4 symbol mapping. Gray coding is generally preferred for PAM4 signaling as it eliminates the double-bit error when crossing the center threshold in linear coding.

PAM4 Results

When plotting eye results for PAM4 signaling, there is an additional dialog box for setting the threshold voltages at the receiver (Figure 4). As opposed to NRZ which has a single center threshold, PAM4 has three threshold voltage values to separate the four logic levels. These values may come from a specification or some other outside source that the user can enter manually. If not overridden by user input, AEDT will try to automatically choose these values based on the received eye data.

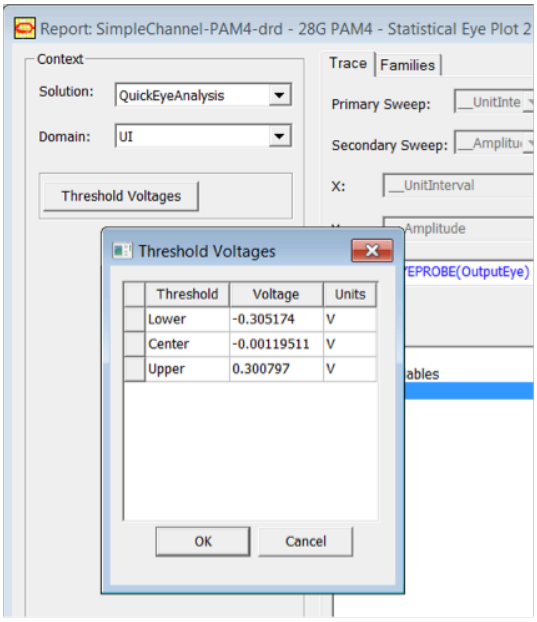

Figure 4 - Threshold Voltage Value Entry

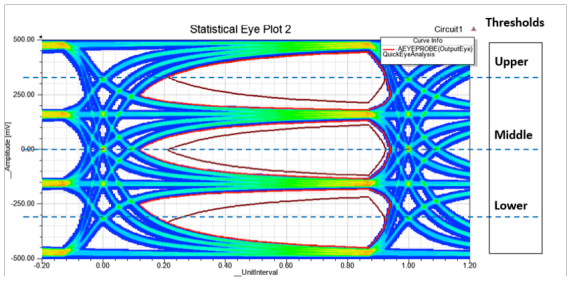

Figure 5 - PAM4 Eye with Threshold Values Illustrated

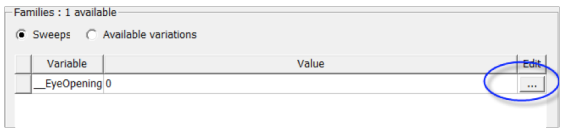

Figure 6 – Families Tab

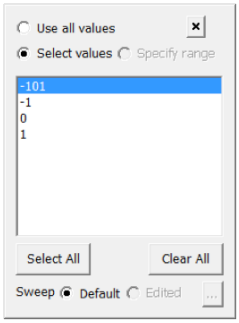

Figure 7 - New Family Values

The dark red inner eye contour shown in the middle of each of the three eyes is referred to as the "consolidated eye contour." This is the minimum inner eye contour that is produced by superimposing the upper, lower, and middle eyes around a common midpoint. In Figure 5 you can see how the upper half of the upper eye contour, and the lower half of the lower eye contour are the limiting factors in the consolidated eye contour for that example.

When reporting bathtub plots, there are now four variations in the Families tab (Figures 6 and 7) for PAM4 based simulations.

When plotting the individual bit error rate bathtub curves for timing data, note that the three bathtub curves will have a common midpoint (Figure 8), as they are correlated in time with each other. However, the three individual voltage bathtubs (Figure 9) will be offset from one another, preserving the voltage spacing in the eye diagram. In that case the bathtub curve for the lower eye appears as the leftmost one in the eye diagram, the center eye in the middle, and the upper eye as the rightmost bathtub.

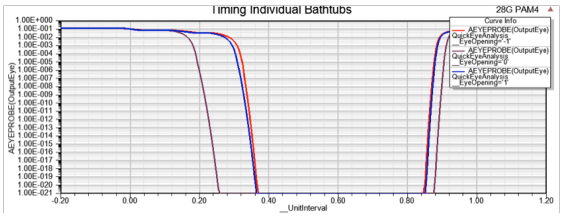

Figure 8 - Timing Bathtub

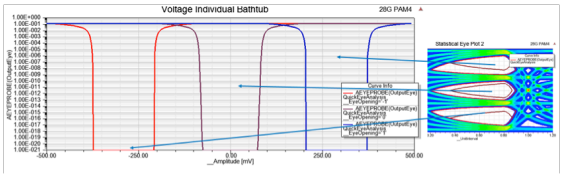

Figure 9 - Voltage Bathtub with Offsets Illustrated

ANSYS, Inc.
Southpointe
2600 ANSYS Drive
Canonsburg, PA 15317
U.S.A.
724.746.3304
ansysinfo@ansys.com

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