Using Via Fences for Crosstalk Reduction in PCB Circuits

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***Abstract*— Crosstalk is one of the major signal integrity concerns at high-speed and high-frequency electronic circuits. Via fences or in another term guard traces are increasingly used to alleviate this problem as dense interconnect layouts emerge. In this paper, first the effect of loading of a via fence on signal transmission in a microstrip line is investigated through parametric studies. Subsequently, a via fence structure is designed and optimized to reduce coupling between two adjacent traces. Additionally, experimental results, while compared with fullwave simulations, are presented to demonstrate crosstalk reduction.**

***Index Terms*— Via fence, guard trace, crosstalk, coupled PCB microstrip, signal integrity.**

I. Introduction

Due to the advancements in electronic packaging technology [1], [2], a new paradigm of electronic system design has emerged to compactly integrate multi-functional electronic circuits. Further component and packaging miniaturization has resulted in dense routing topologies, which are prone to signal integrity problems such as crosstalk. Traditionally, guard traces, which are microstrip lines grounded by a few plated via holes, are employed in minimizing crosstalk between adjacent conductor paths in PCBs [3], [4]. Often the spacing between the vias are chosen arbitrarily or based on the routing and fabrication convenience. However, this design parameter has shown to be a determining factor in improvement or degradation of crosstalk immunity [3], [5]. It has been observed that at frequencies pertinent to the occurrence of resonance between the vias, coupling between the lines become stronger [3], [5]. A similar architecture, called via fences, has been utilized in LTCC technology and multichip modules, which exploits a similar design but with higher number of grounding via holes [6]. Via fences have demonstrated effective crosstalk reduction over a wide frequency band, tens of GHz as opposed to few hundred MHz observed in the guard trace structures, 589MHz bandwidth is reported in [7].

Therefore, in this paper, application of via fence structures in PCB lines for crosstalk reduction is investigated. For this purpose, initially, the loading of a via fence on a single microstrip line is studied through a set of fullwave finite element method (FEM) simulations. Design parameters such as number of via holes, via spacing, diameter of the via, and spacing between the via fence and the line are varied in this parametric study. Then, near-end and far-end coupling between

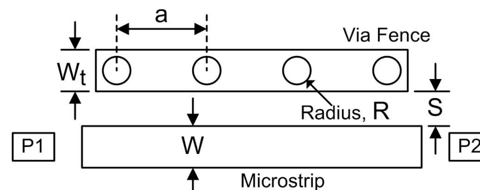

Fig. 1. A typical microstrip line adjacent to a via fence

two FR4 PCB microstrip lines with and without an interleaving via fence is evaluated. Finally, two test structures are fabricated and characterized through S-parameter measurements to validate the effectiveness of the designed via fences for crosstalk reduction.

II. Loading of a Via Fence on a Single Microstrip Line

The geometry of the structure understudy is presented in Fig. 1. A microstrip line of width W and a via fence or guard trace of with W_t are separated by the spacing S. The guard trace is connected to the bottom ground plane through a number of plated via holes of radius R with the via spacing a. For all studied cases, a FR4 laminate ($\epsilon_r = 4.4$ and $tan\delta = 0.02$) is used as the substrate with the substrate thickness of 1.575mm. W is chosen to be 3mm, which yields a characteristic impedance of 50Ω. The width of the guard trace is the same as the width of the microstrip line, and the via hole radius is chosen to be 0.762mm. The lengths of the microstrip line and the via fence are chosen to be 50mm and 48mm, respectively. The length of via trace is chosen shorter for convenience in definition of ports in fullwave simulations.

In the first case study, the effect of number of via holes on a via fence is examined. Parametric simulations are performed for 2, 3, 4, 5, and 12 via holes, which are separated with equal distances on the via fence. The corresponding via spacings (a) are 46, 23, 15.33, 11.50, and 4.18mm. The resulting S-parameters are shown in Fig. 2. It is observed that the resonances in the magnitudes of S_{21} can be related to the via spacing. For example, in the 2 via-hole case, when $\lambda/2 = 46mm$ (via spacing) and $\epsilon_{eff} \approx 3.4$, the corresponding resonance frequency of 1.77GHz is obtained. This prediction matches with the frequency of occurrence of S_{21} minima in Fig. 2(b). As the number of via holes increases, these

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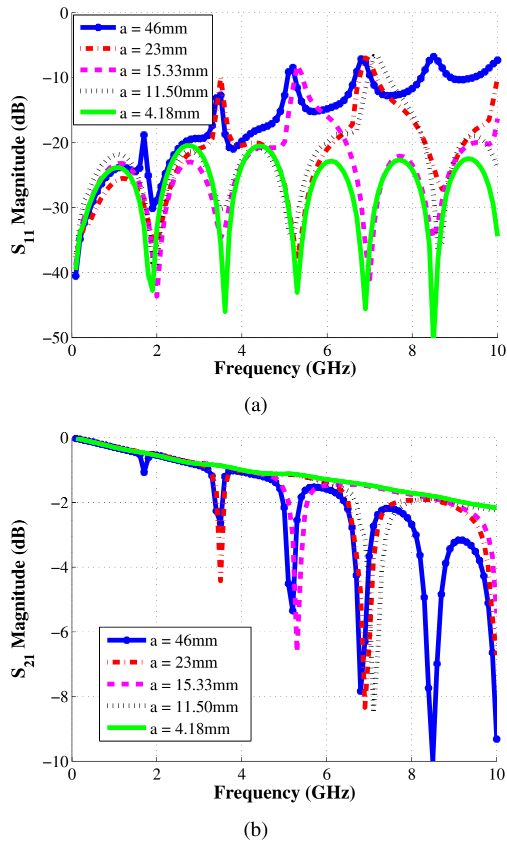

Fig. 2. Inspecting the effect of changing number of via holes and via spacing on loading of the via fence on the signal line when S = 1mm (a) Magnitudes of S_{11}. (b) Magnitudes of S_{21}.

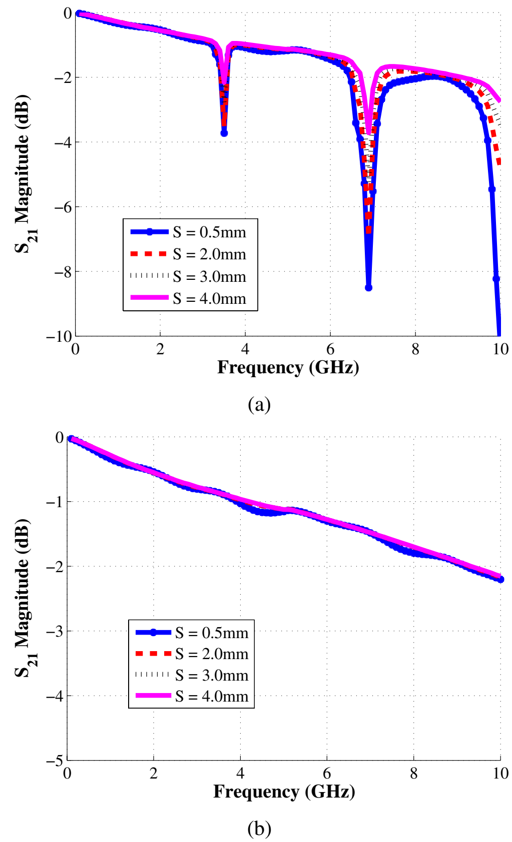

Fig. 3. Inspecting the effect of changing line spacing on loading of the via fence on the signal line. (a) Magnitudes of S_{21} for 3 vias. (b) Magnitudes of S_{21} for 12 vias.

resonances occur at higher frequencies. Hence, the bandwidth of the via fence increases, which is observed in the case of 12 via holes ($a = 4.18mm$) where there is a smooth transmission over the range of 10GHz.

Next, the effect of spacing between the microstrip line and the via fence is investigated. The cases with 3 and 12 via holes are simulated for the line spacings (S) of 0.5, 2.0, 3.0, and 4.0mm. The corresponding S_{21} parameters are shown in Fig. 3. It is observed in the 3-via case that the resonances (minima in S_{21} signature) become weaker as the line spacing increases. In the case of 12 vias, it is observed that the change in line spacing does not affect the magnitudes of S_{21} significantly other than a small ripple in the insertion loss when S = 0.5mm, as shown in Fig. 3(b).

In the final parametric study, the simulations are performed for different via diameters, *i.e.*, D/W_t = 0.169, 0.339, 0.677, and 0.847, where W_t is fixed to 3mm and D is the diameter of the via hole. The S_{21} parameters as shown in Fig. 4 are obtained for via fences containing 3 and 12 vias. In Fig. 4(a), it is observed that the resonances are shifted towards lower frequencies, as D/W_t decreases. Additionally, a wider resonance is also observed when D/W_t is much smaller than the via fence width. This effect is much more pronounced for the case of D/W_t = 0.169. In the case of 12 via holes, the resonances are predicted to appear at much higher frequencies. Therefore, no changes can be observed over the range of 10GHz. However, a small resonance starts to appear at 9.1GHz for the smallest via diameter (D/W_t = 0.169).

From parametric simulations, it can be concluded that in designing a via fence number of vias, via spacing, line spacing, and via size are important parameters with various impacts on signal integrity. In order to achieve a wide band performance, the via fence must contain many via holes with small spacing so that the resonances appear at very high frequencies. As well, the diameter of the via should be comparable to the width of the via fence for efficient grounding. In the next section, it will be shown that employing via fences to reduce crosstalk will render ineffective if proper design guidelines are not observed.

III. Crosstalk Between Adjacent Microstrip Lines

The crosstalk performances of three microstrip configurations as shown in Fig. 5 are investigated in this section. The first geometry shown in Fig. 5(a) comprises two microstrip lines without any interleaving via fence. The width of each line (W) is 3mm, and the spacing between the lines (S_t) is 3.508mm. The second structure is the same microstrip-line structure but contains also a via fence with 3 via holes, as shown in Fig. 5(b). The via fence has the following dimensions: a = 48mm, R = 0.762mm, and W_t = 2mm. The last test case has the same specifications as the second

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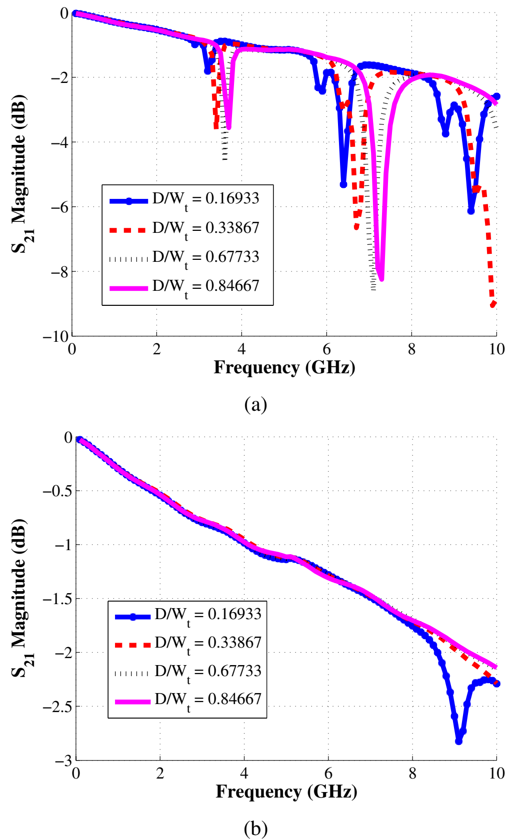

Fig. 4. Inspecting the effect of changing via diameter on loading of the via fence on the signal line when S = 1mm. (a) Magnitudes of S_{21} for 3 vias. (b) Magnitudes of S_{21} for 12 vias.

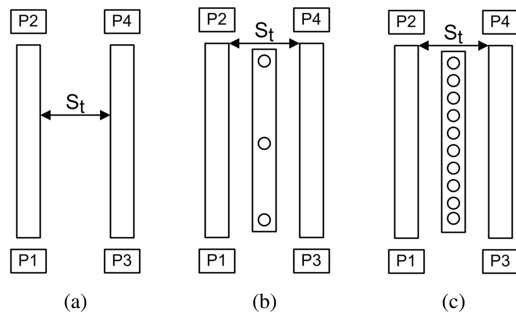

Fig. 5. Studied coupled microstrip line geometries (a) Without a via fence. (b) With a via fence containing 3 vias. (c) With a via fence containing 12 vias

case, except that the number of vias is 25 and a = 4mm. The substrate is FR4 with a thickness of 1.575mm. The total length of each microstrip line is 100mm while the length of the via fence is 98.476mm.

From fullwave simulations, the S-parameters of these coupled structures are generated as presented in Fig. 6. It can be observed that the transmission (S_{21}) and far-end coupling (S_{41}) coefficients of the microstrip lines with a via fence containing 3 vias is even worse than those of the microstrip lines of Fig. 5(a) with the same S_t. However, a significant improvement in transmission and crosstalk immunity is obtained when the via fence contains 25 vias, as shown in Fig. 6. Therefore, it can be deduced that to isolate two adjacent signal lines, effective shielding can be achieved only if a properly designed via fence is used. Otherwise, the signal transmission can be degraded rather than improved. Increasing the number of vias has demonstrated to result in minimal loading on signal lines (shown in Section II) and to offer improved crosstalk immunity. Therefore, it can be concluded that design rules for electromagnetic bandgap (EBG) and periodic structures can be employed to provide a more systematic design guideline for via fences. An example of application of the EBG design concepts in realization of a conductor wall embedded in PCB substrates are presented in [8].

IV. Experimental Results

To investigate the coupling between microstrip lines experimentally, two test structures shown in Figs. 7(a) and 7(b) were fabricated using a FR4 substrate with the substrate thickness of 0.508mm. Each microstrip line has a characteristic impedance of 50Ω, *i.e.*, W = 0.97mm. The spacing between the microstrip lines is 7.57mm. In the via fence, the via spacing and via radius are 2.54mm and 0.762mm, respectively. The total length is 100mm. For each test structure, standard SMA connectors are connected to port 1 and 4. Ports 2 and 3 are each terminated by a 52Ω surface mount resistor to create an approximate matched termination. In addition, both structures are simulated by a FEM solver. Measured and simulated far-end couplings (S_{41} parameters) are depicted in Fig. 8. It is observed that the far-end crosstalk is reduced when the via fence is placed between the coupled lines. Small ripples in the measured S_{41} parameters are caused by the mismatched terminations. The discrepancies between the simulations and measurements can be attributed to fabrication errors, and not including the effect of frequency-dependent dielectric loss and the thickness of conductors in simulations.

V. Conclusion

Improving the crosstalk immunity between adjacent printed circuit board signal traces has become a necessity in modern and highly integrated electronic systems. Conventionally, via fences are utilized for this purpose. However, it was shown in this paper that the proper design of these interleaving traces is in fact the crucial factor in achieving this goal rather than the mere placement of them between the adjacent signal lines. To investigate the determining variables in the design of a via fence, parametric study on the effects of various geometrical features of trace is conducted herein. The considered parameters are number of vias in a via fence, spacing between the via trace and the signal line, and the via diameter. This study demonstrates that the via fence can be utilized across a wider bandwidth when the number of plated via holes in the trace is increased. Moreover, it is found that wider spacing between the vias result in further degradation of signal transmission characteristics in the active line. The diameter of the via should be comparable to the width of the trace in order to maintain the signal integrity within the bandwidth of interest.

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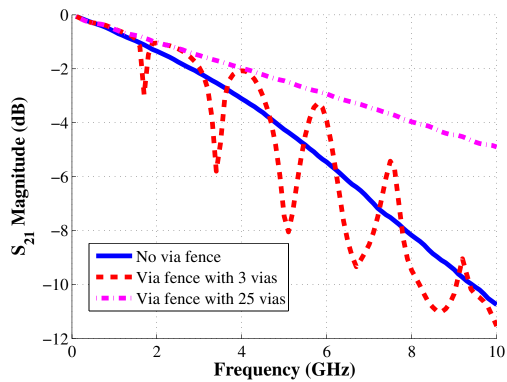
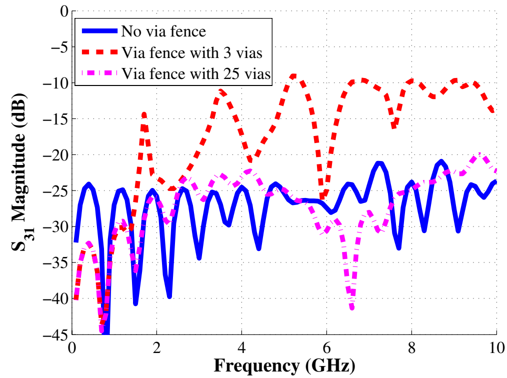


(a)



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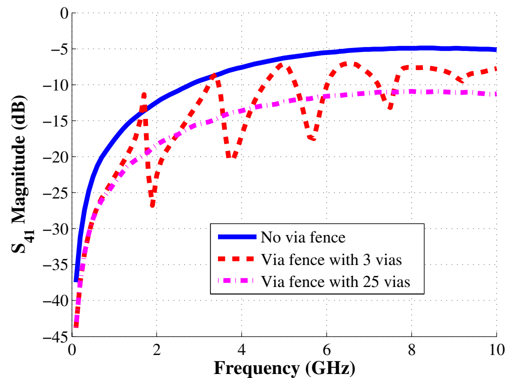

(c)

Fig. 6. Simulated S-parameters of the coupled microstrip line structures shown in Fig. 5. (a) Magnitudes of S_{21}. (b) Magnitudes of S_{31}. (c) Magnitudes of S_{41}.

To investigate the crosstalk reduction between adjacent lines by using a via fence, a few test structures are studied. Fullwave simulations of these structures confirm the earlier conclusion about the required number of vias in a via fence. Finally, two coupled microstrip lines are fabricated, and characterized by S-parameter measurements to validate the concluded design guidelines and simulation results.

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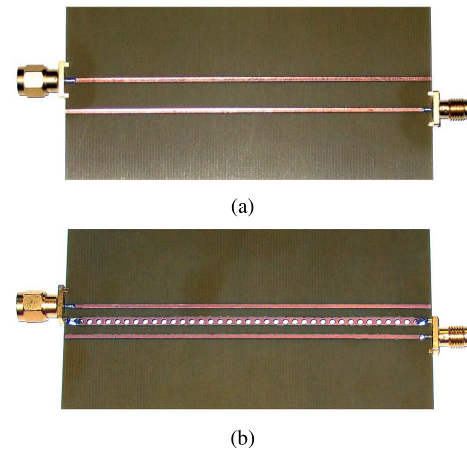

(a)

(b)

Fig. 7. Photographs of the coupled microstrip test structures. (a) Without a via fence. (b) With a via fence.

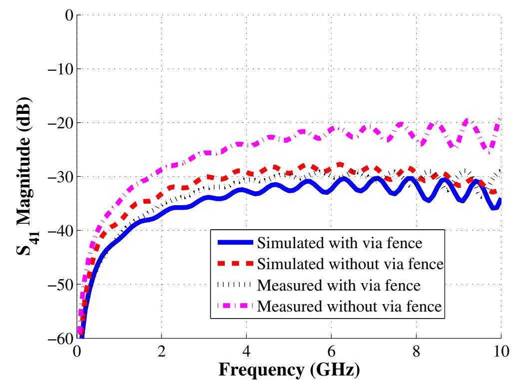

Fig. 8. Magnitudes of S_{41} for the structures shown in Fig. 7(a) and Fig. 7(b) from simulations and measurements.

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