高速電路阻抗量測
及
電路模型應用

Agenda

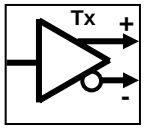
- TDR resolution and accuracy
- Differential transmission line
- How to make test coupon
- Other TDR/TDT measurement

Impedance and Signal Integrity Issues

- Control of characteristic impedance is becoming more important as digital system designers seek faster speeds. Mismatches and variations of impedance cause reflections that add to system noise and jitter, especially with fast signals. This can lead to data and logic errors and severe, hard-to-identify reliability problems.

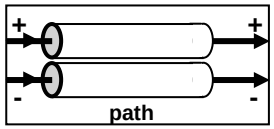
eSerial: the **basic blocks** of the serial DATA link

Transmitters

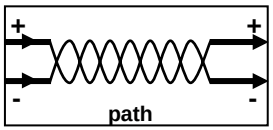


Differential
Transmitter

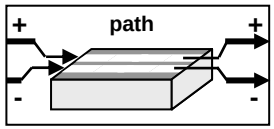
Interconnects (paths)



Dual-coax
differential cable

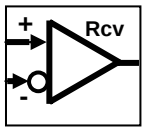


Twisted-pair
differential cable



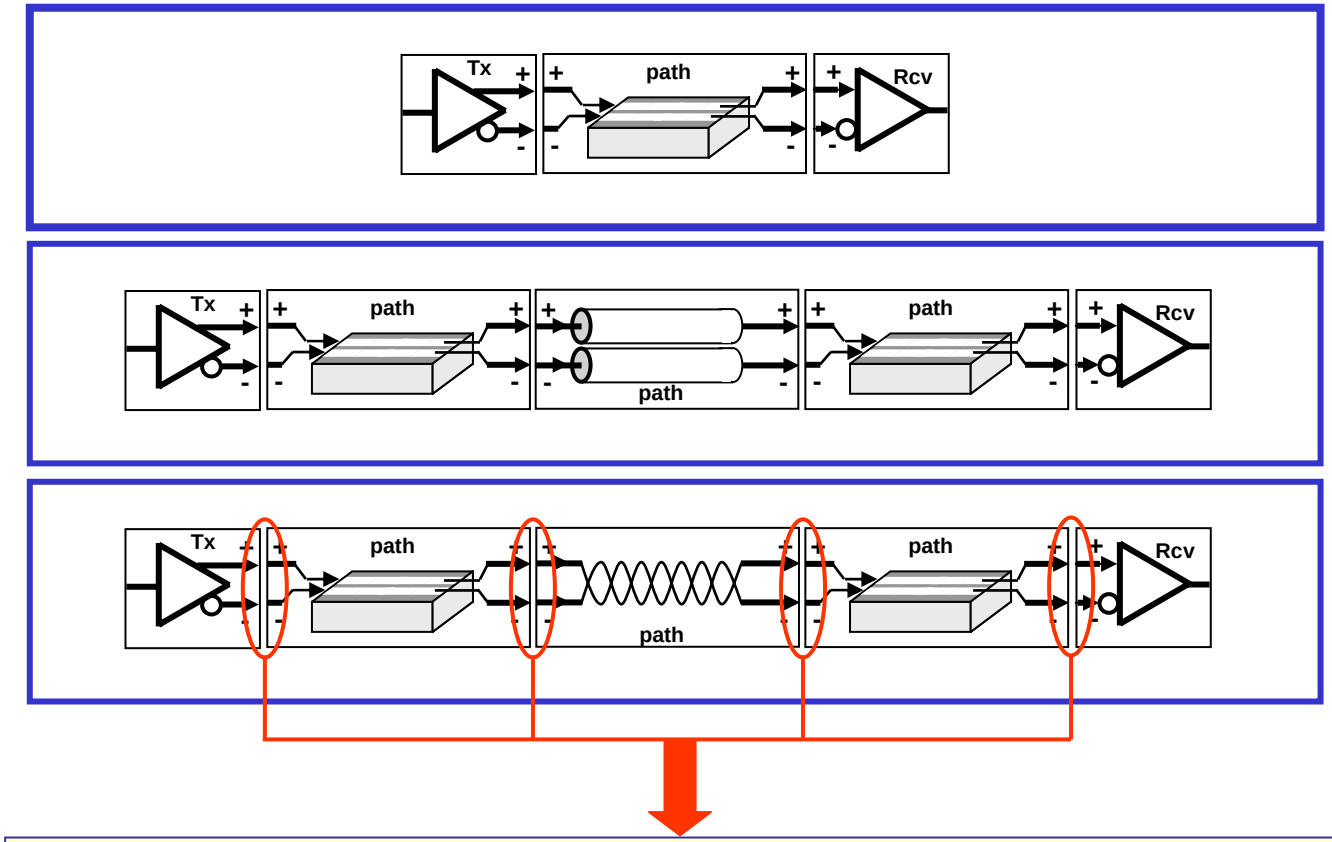
Coupled-pair traces
on **circuit board**
(backplanes)

Receivers



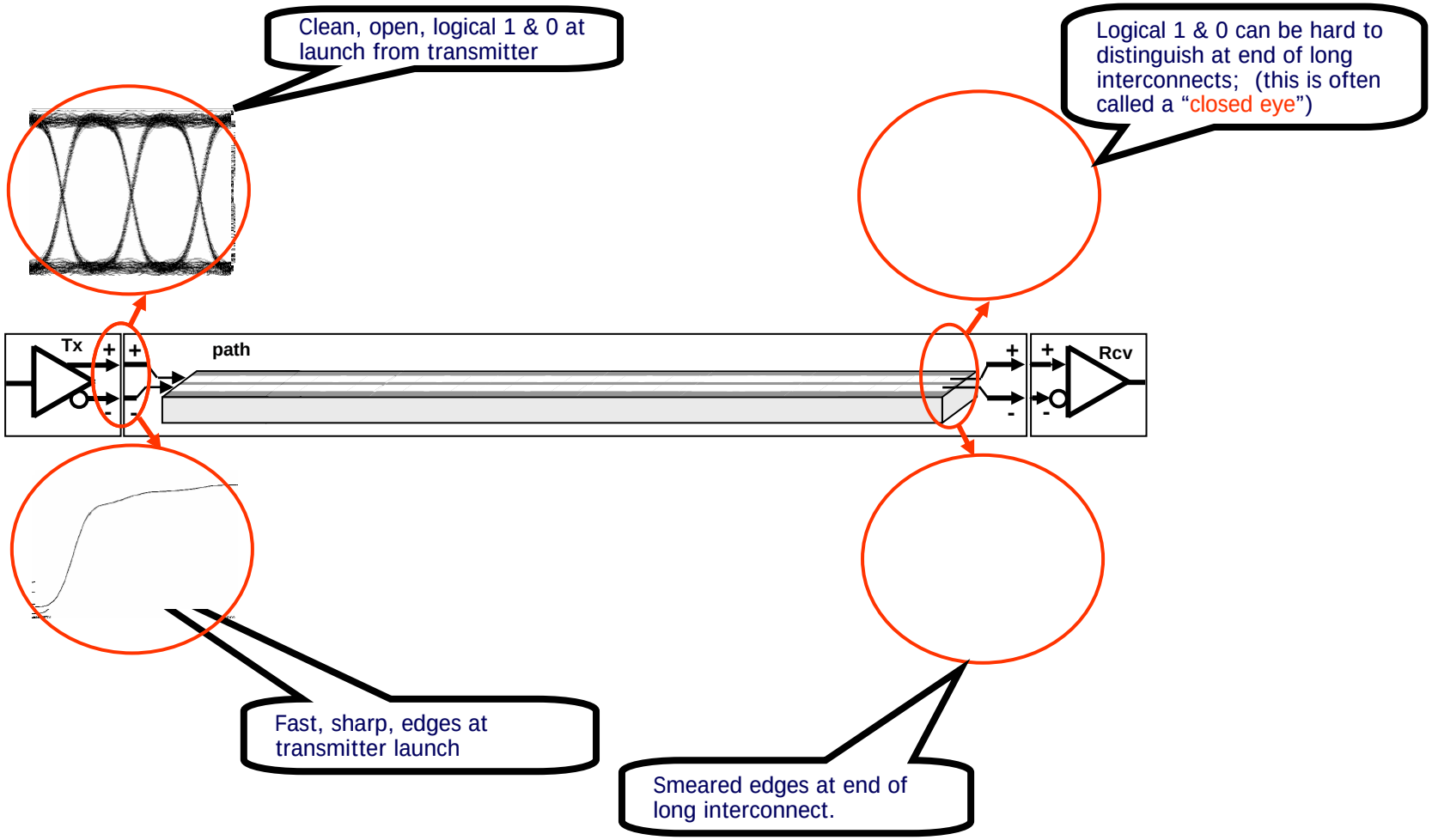
Differential
Receiver

eSerial: DATA is *generally* transmitted across the interconnect without any clock in parallel



- *Transition points often involve combinations of **solder joints**, **circuit board vias**, and **connectors**: these all can have substantial effect on the total link performance.*

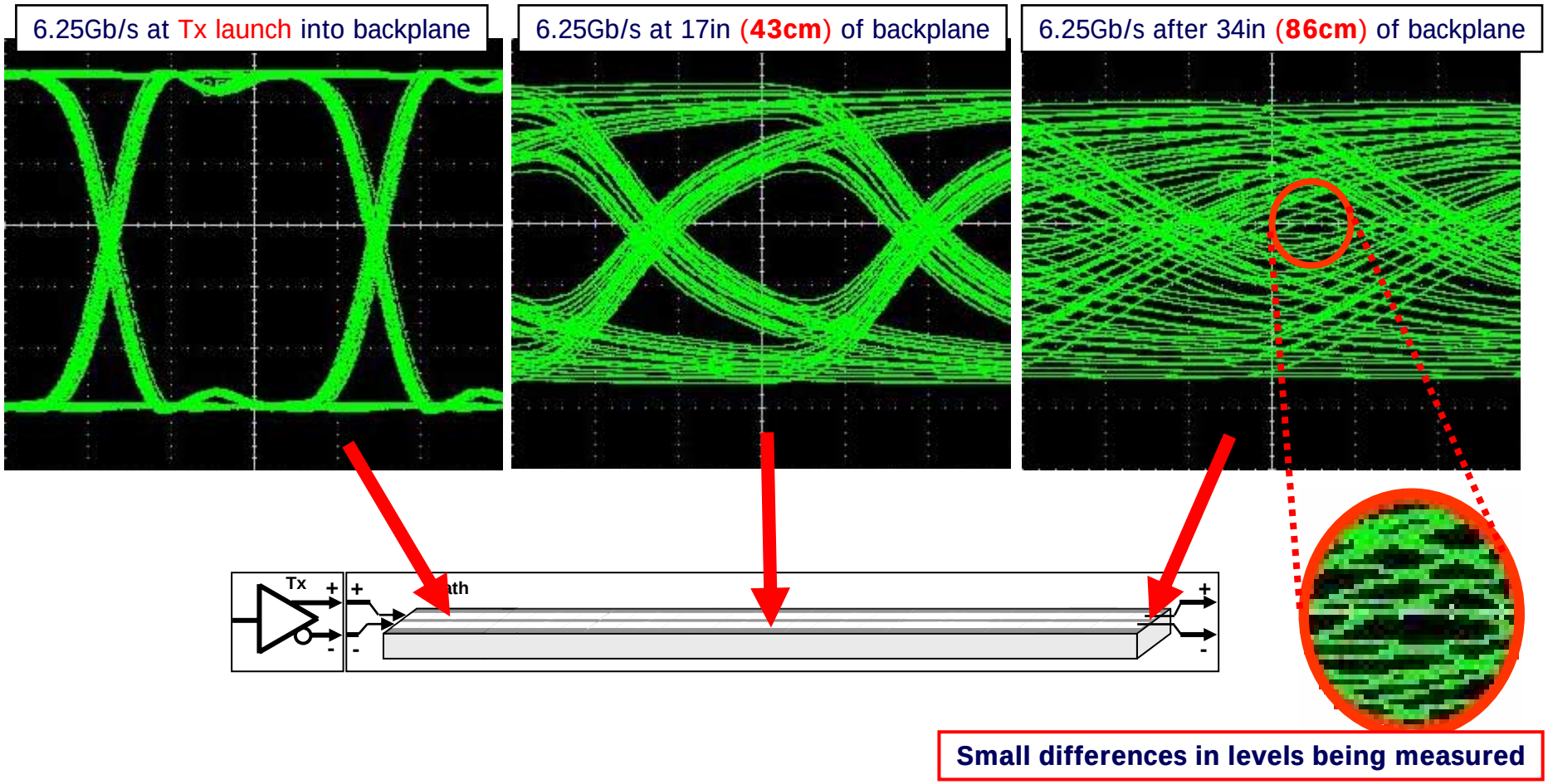
eSerial Interconnect: Loss The faster the data rate and the longer the interconnect, then the more loss in the signal



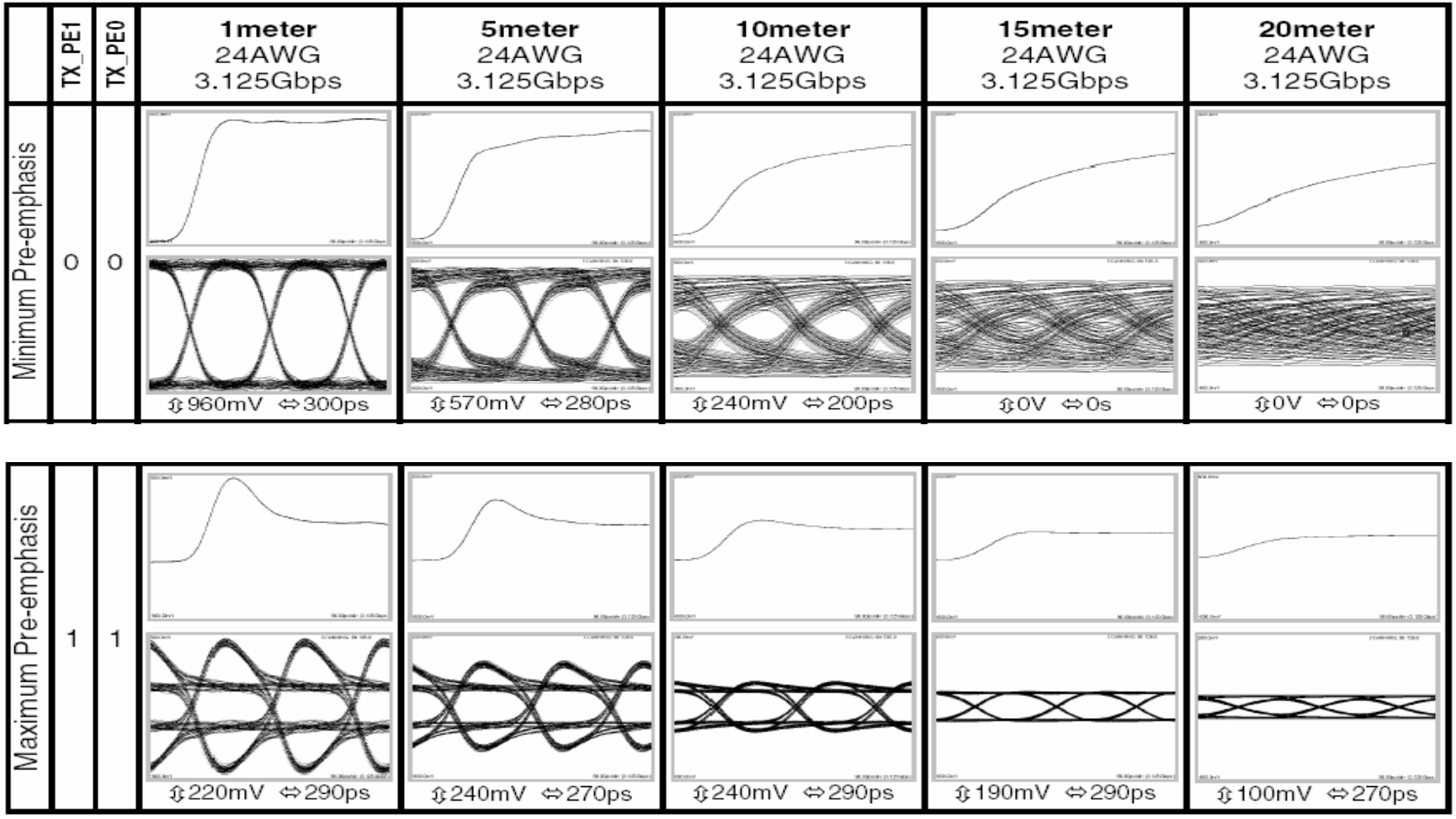
Click here to go to a detailed backup slide showing pre-emphasis methods used to help overcome interconnect loss and ISI effects.

Reference Maxim Note HFDN-27.0 (Rev. 0, 09/03)

eSerial Interconnect: Precision Low noise, higher resolution, best fidelity often needed by designer:



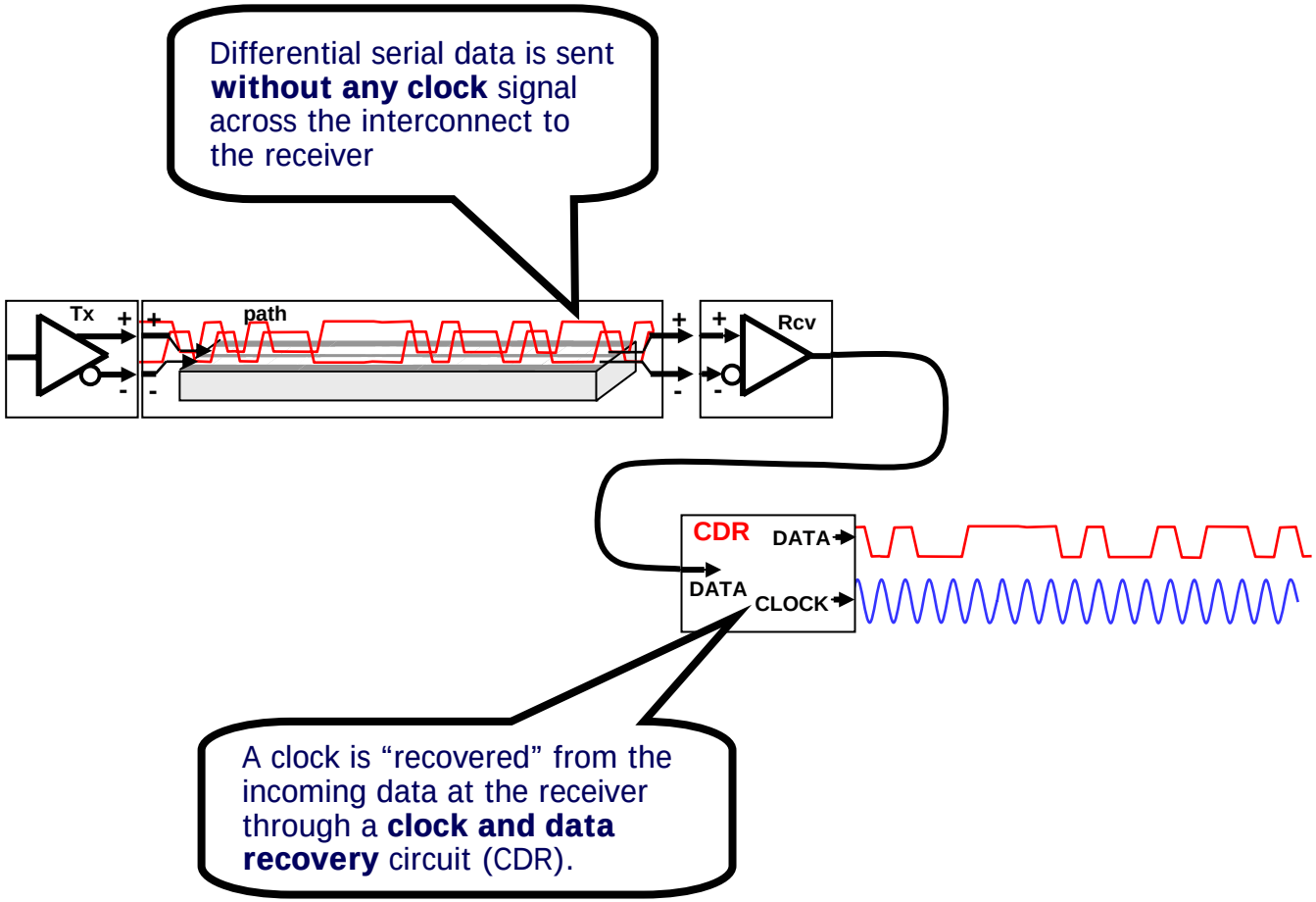
Effects of active Pre-emphasis & the need to characterize the pre-emphasis bit



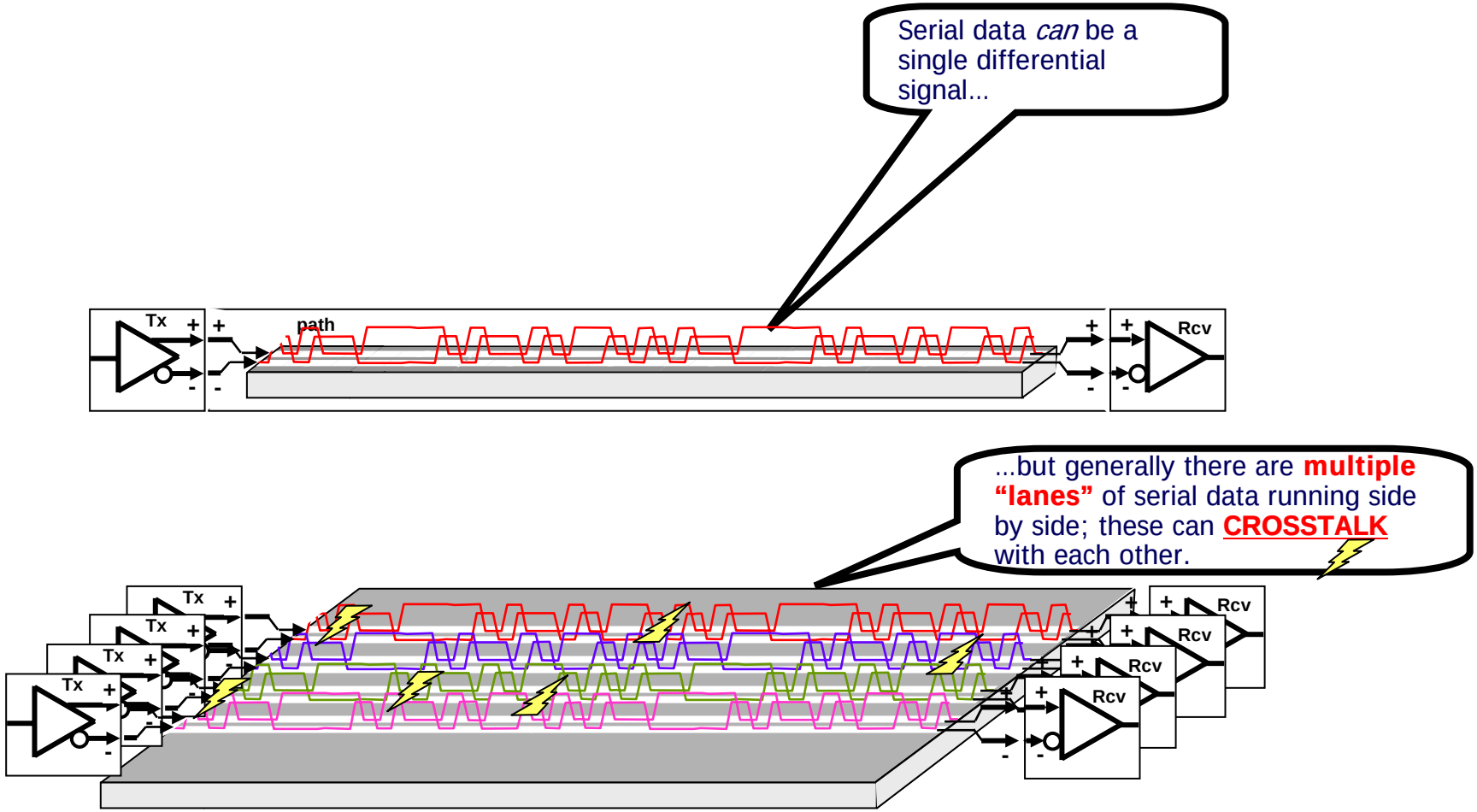
Reference Maxim Note HFDN-27.0 (Rev. 0, 09/03)

Click here to return to original slide

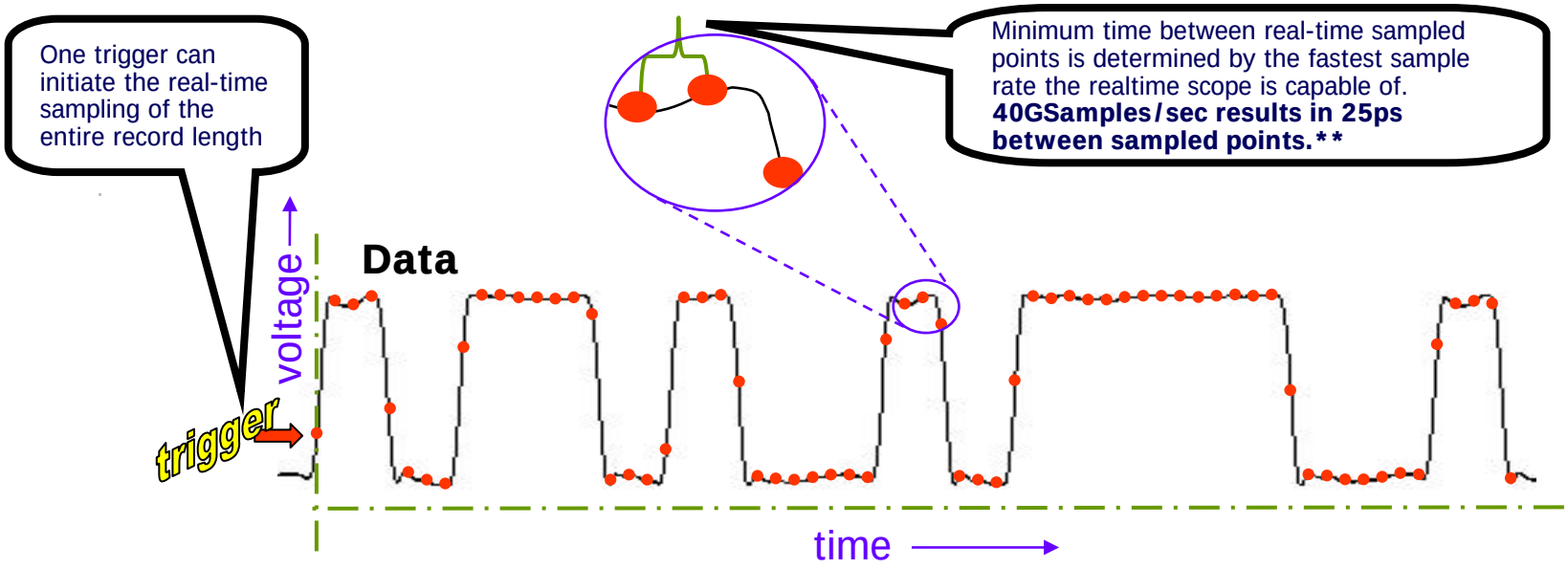
eSerial: Clockless Signal includes both data and clock



eSerial Crosstalk: In many cases there are multiple “lanes” of serial data.



ET-RT Basics:
RT architecture - trigger on data and sample in real-time

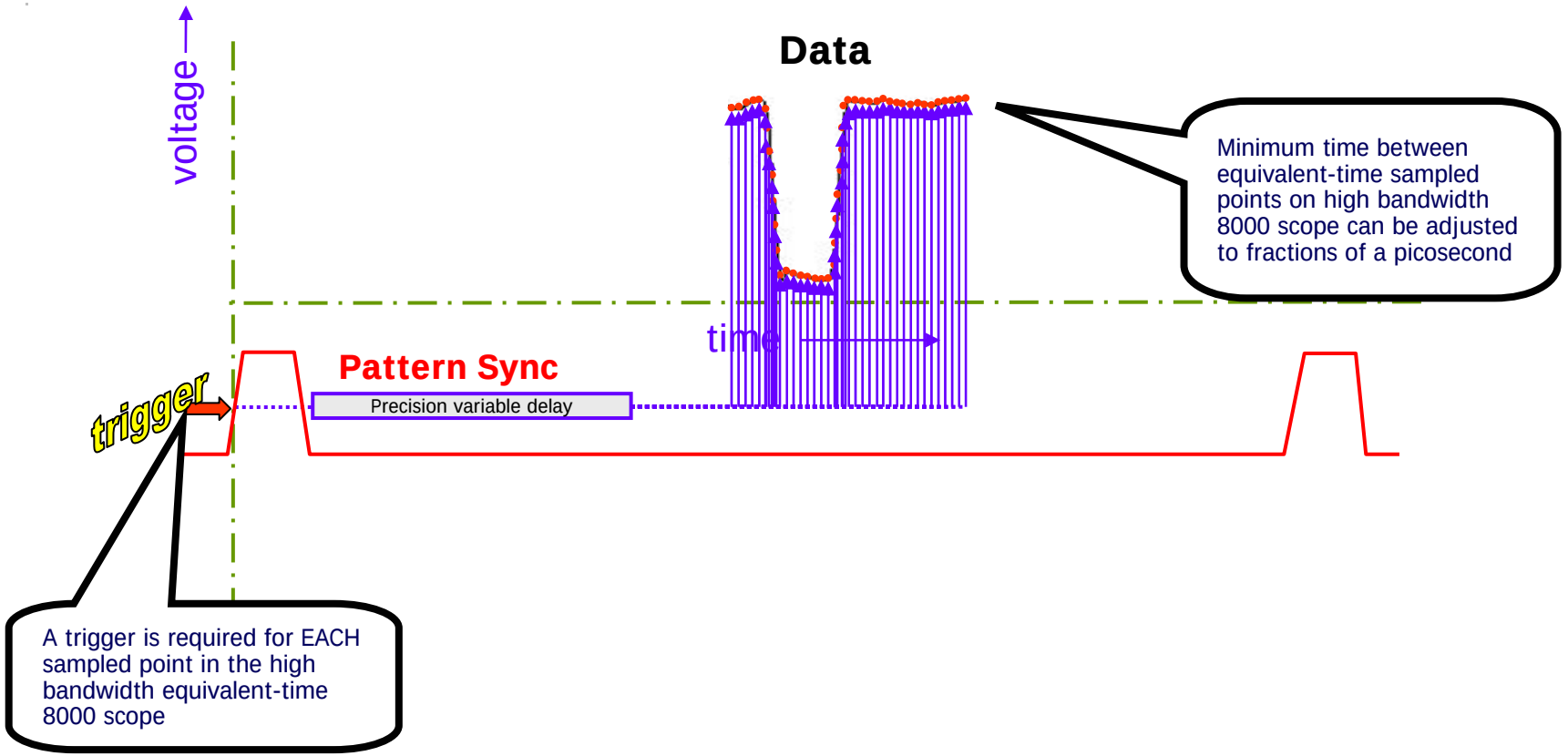


- *A realtime scope does not require a separate signal to trigger: the signal under test can act as the trigger for initiating fast real-time sampling to acquire a waveform.*

– **Maximum resolution is higher through interpolation

ET-RT Basics:

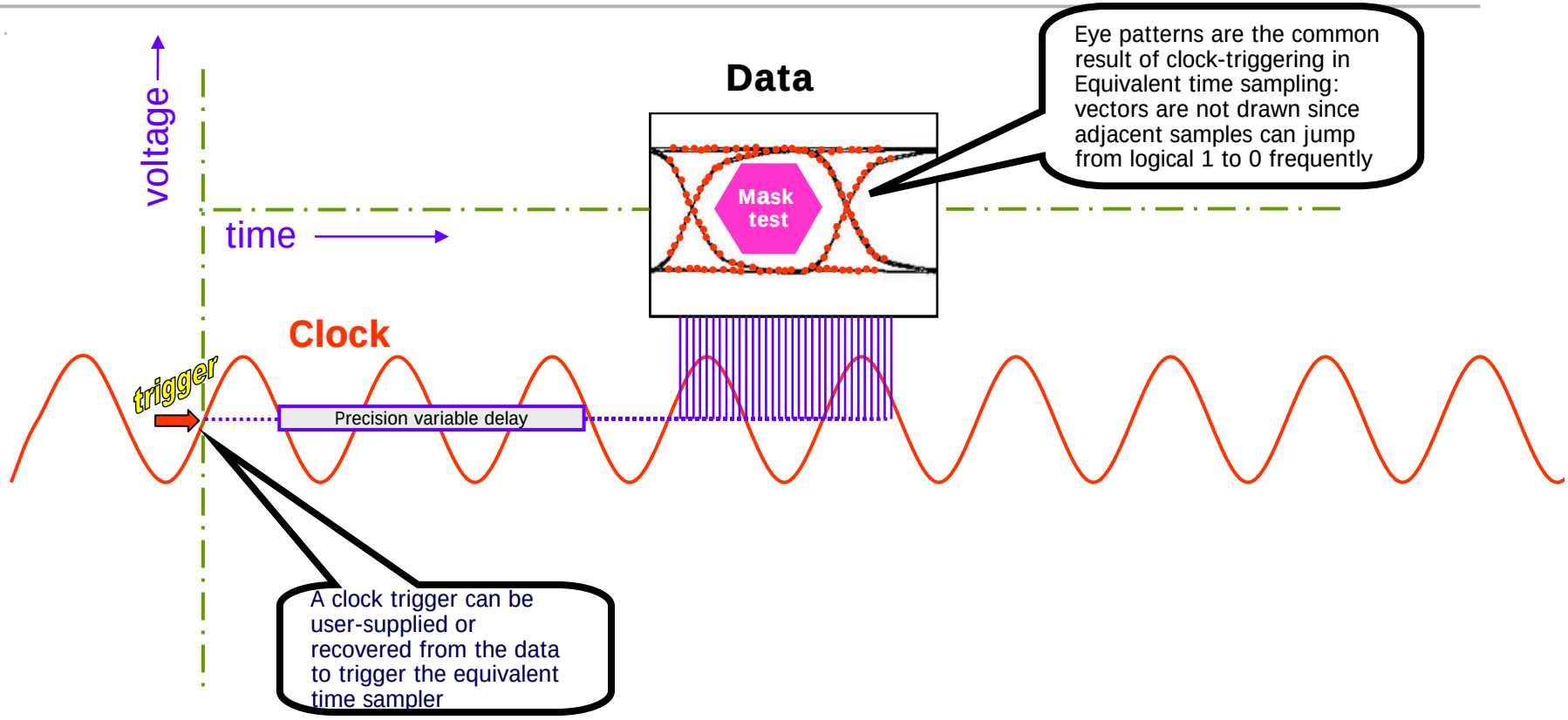
ET - one-sample-per-trigger, repetitive pattern required for pulse streams



- *An equivalent-time 8000 series sampling oscilloscope requires a trigger signal: this is generally a user-supplied clock, a recovered clock, or a pattern sync signal synchronous to the signal.*

ET-RT Basics:

ET – one-sample-per-trigger, non repetitive pattern ok for mask test



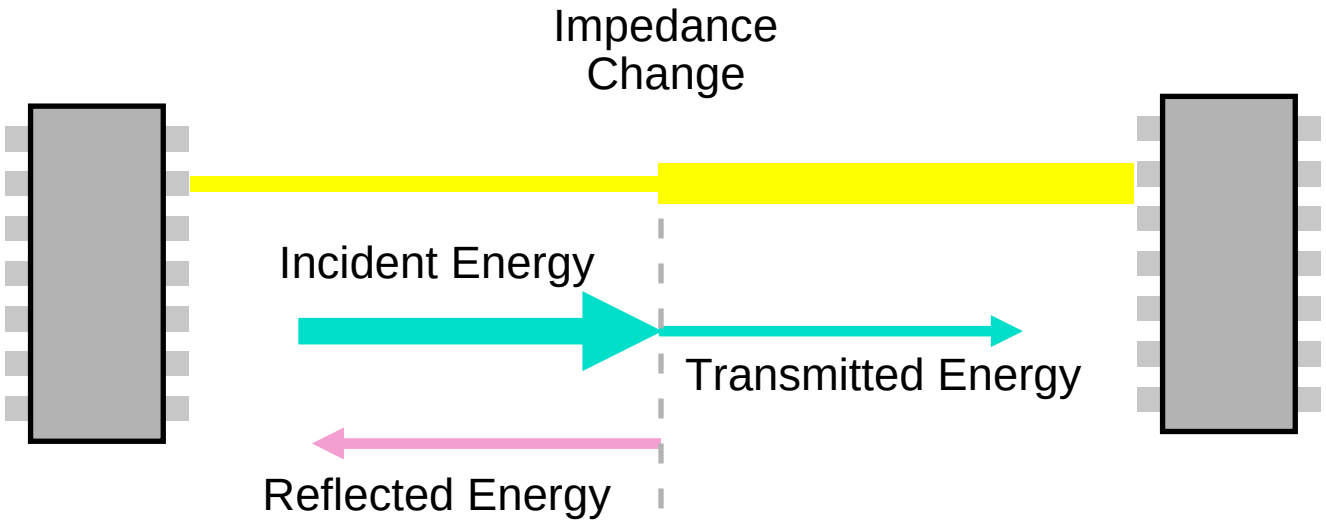
- *When a clock signal is used to trigger the equivalent-time 8200 scope the sampled DATA signals generally create EYE PATTERNS (between clock triggers the sampled DATA could be either a logical 1 or 0)*

Impedance Measurement with TDR

- Time Domain Reflectometry - a measure of reflection in an unknown device, relative to the reflection in a standard impedance.
- Compares reflected energy to incident energy on a single-line transmission system.
  - Known stimulus applied to the standard impedance is propagated toward the unknown device
  - Reflections from the unknown device are returned toward the source
  - Known standard impedance may or may not be present simultaneously with the device or system under test

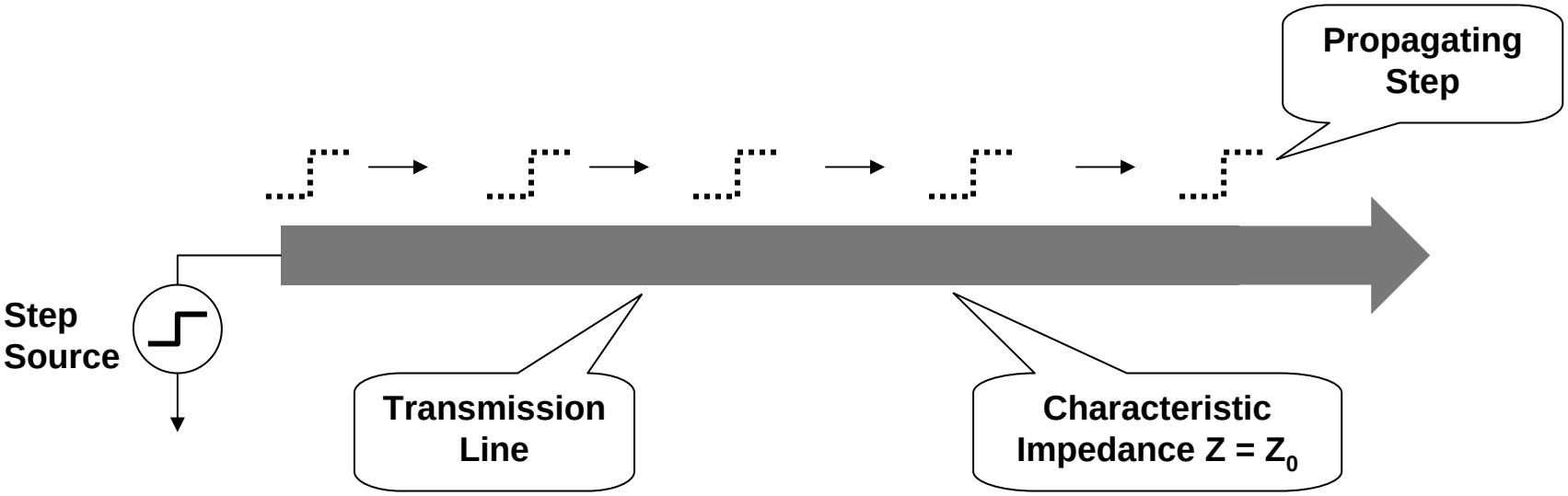
TDR Overview

- At high-speeds, interconnect limits system performance.
- It is desirable to characterize and model interconnect to predict the performance early in the design phase.



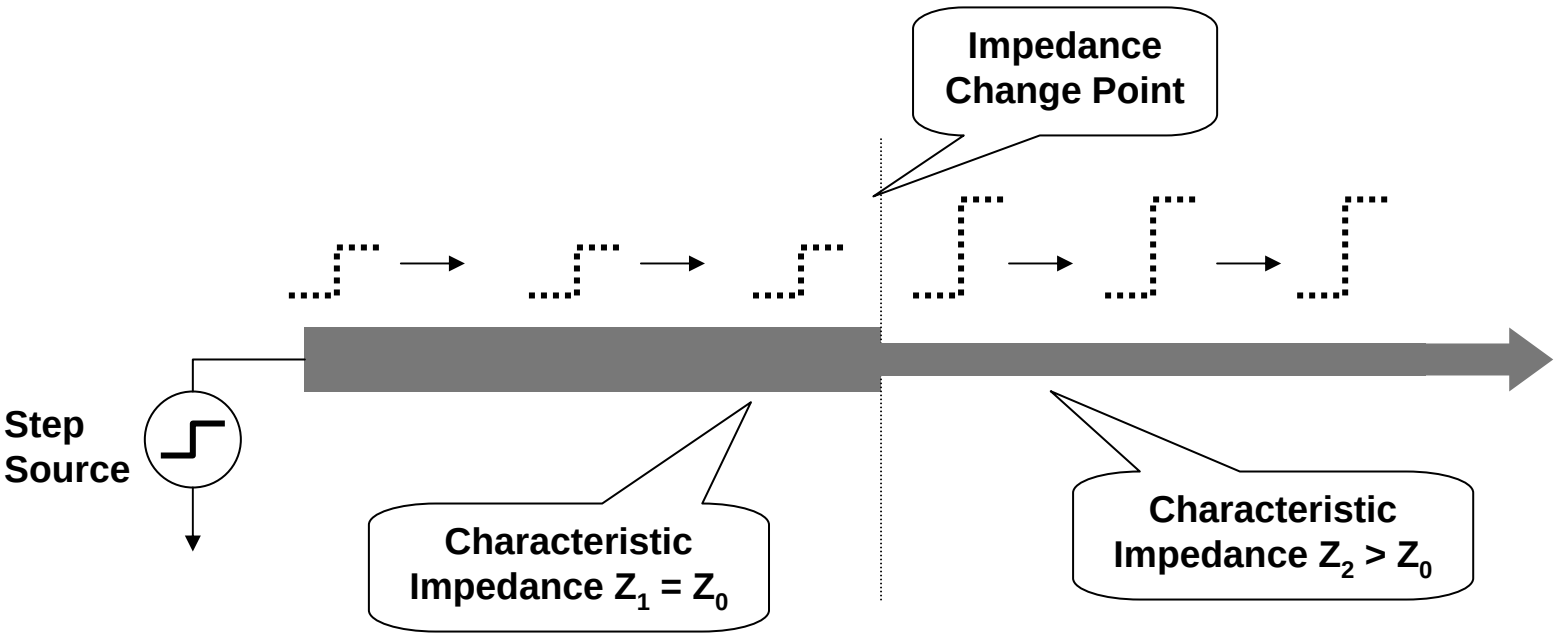
TDR Fundamentals – Applied Step Signal

- Starting with a transmission line with a characteristic impedance Z equal to Z_0
- A fast rise-time step signal is applied at the transmission line input point
- The step signal will propagate down the line



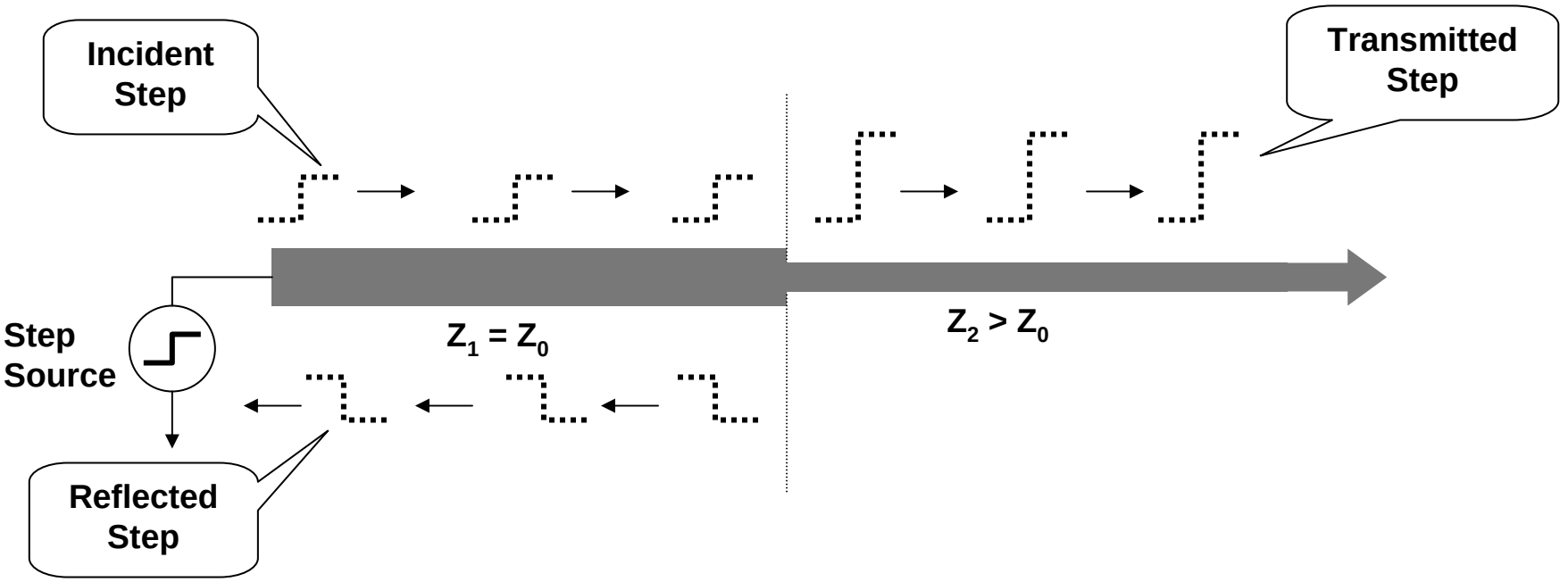
TDR Fundamentals – Impedance Change

- An impedance change in the transmission line will cause a change in the amplitude of the propagating step



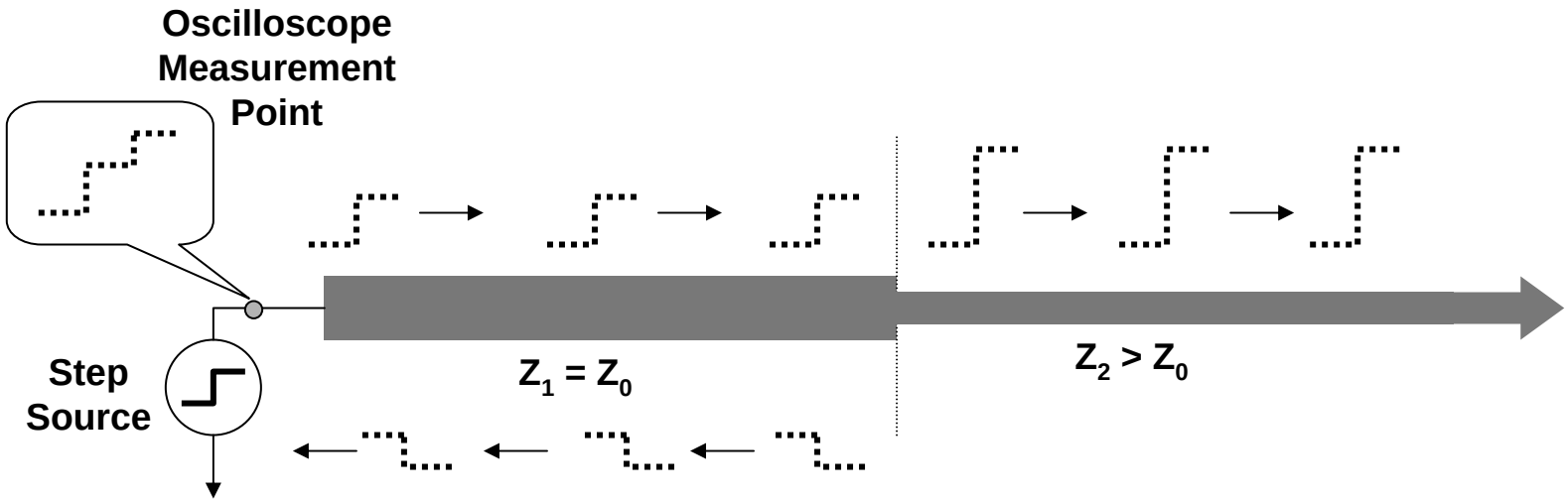
TDR Fundamentals – Transmitted and Reflected Signals

- The change in impedance causes some of the energy to be reflected back to the source
- The remainder of the energy will be transmitted

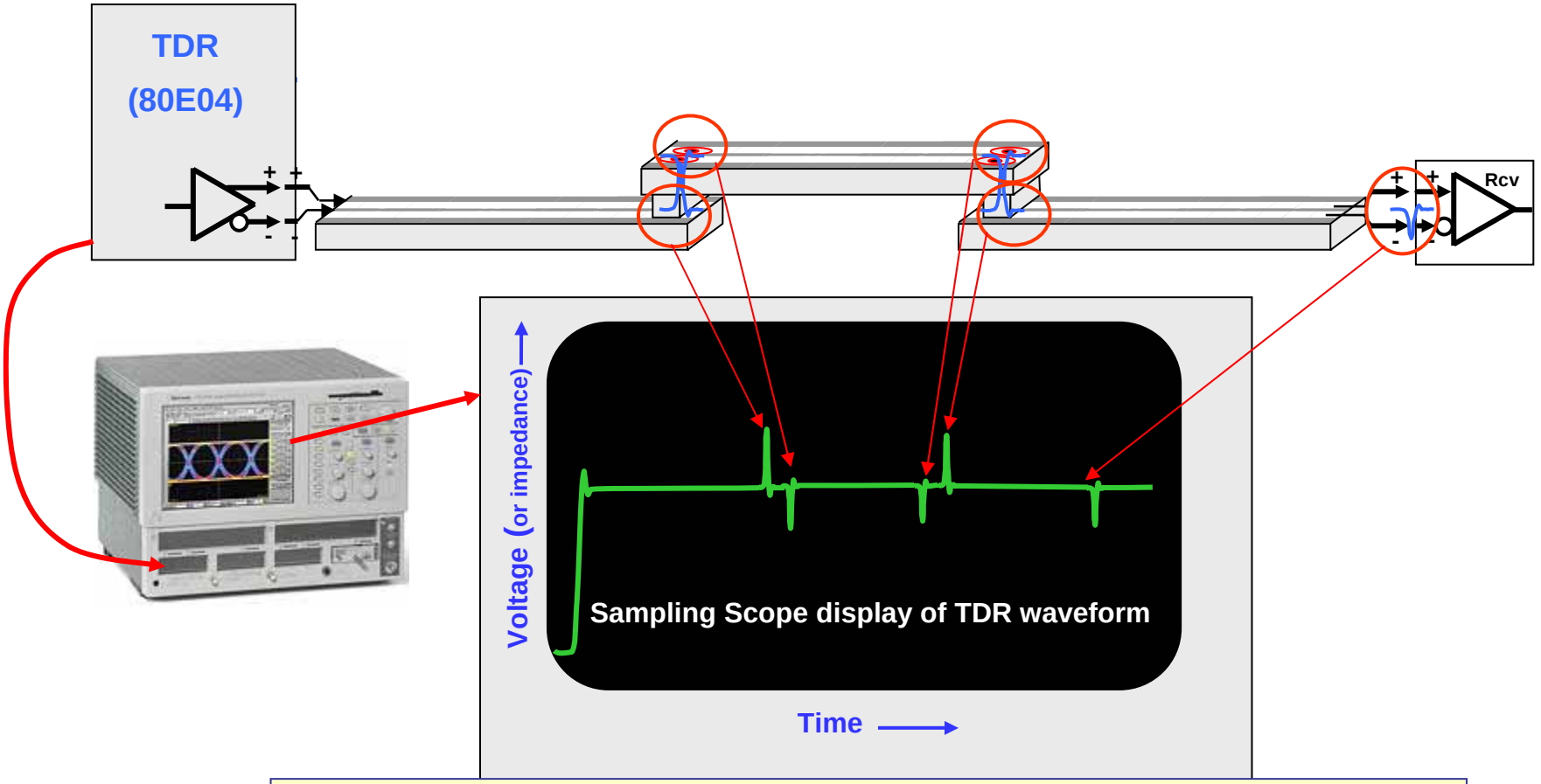


TDR Fundamentals – Oscilloscope Monitoring

- Use an oscilloscope to monitor the transmission line signal at the step source input point
- The oscilloscope waveform will show the combined sum of the incident and reflected propagating signals in proper time sequence

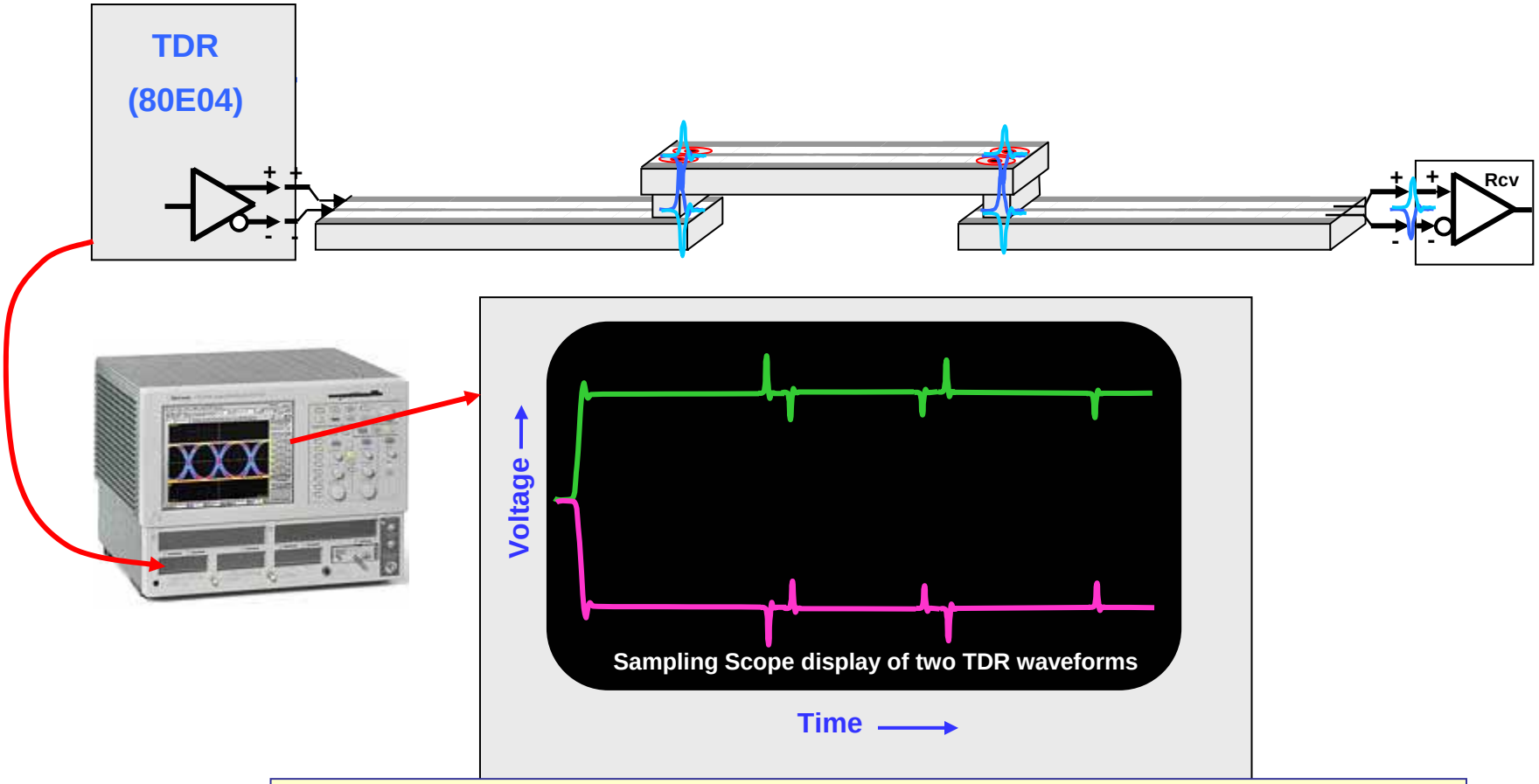


eSerial: Interconnect itself Characterized using Time Domain Reflectometry (**TDR**)



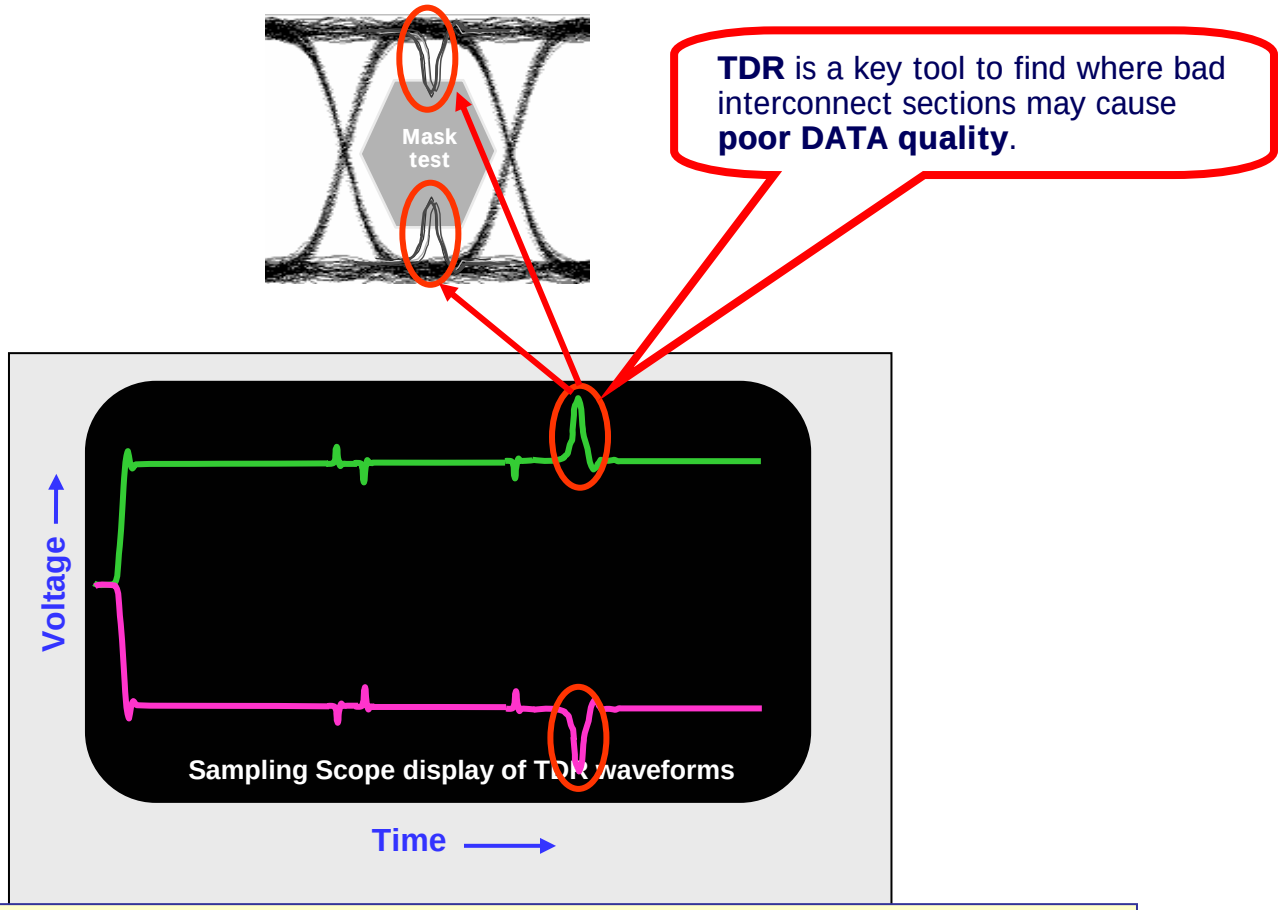
- *TDR on an Equivalent Time scope is used to measure the quality of the serial data interconncet: A step is generated and returning reflections are sampled (**it's like radar for serial data cables and boards**)*

eSerial: Differential TDR is used on differential interconnects.



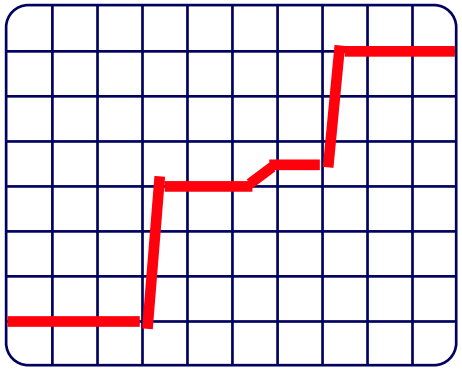
- *Two TDR sampling channels allow the differential impedance between the DATA+ and DATA- eSerial paths to be measured.*

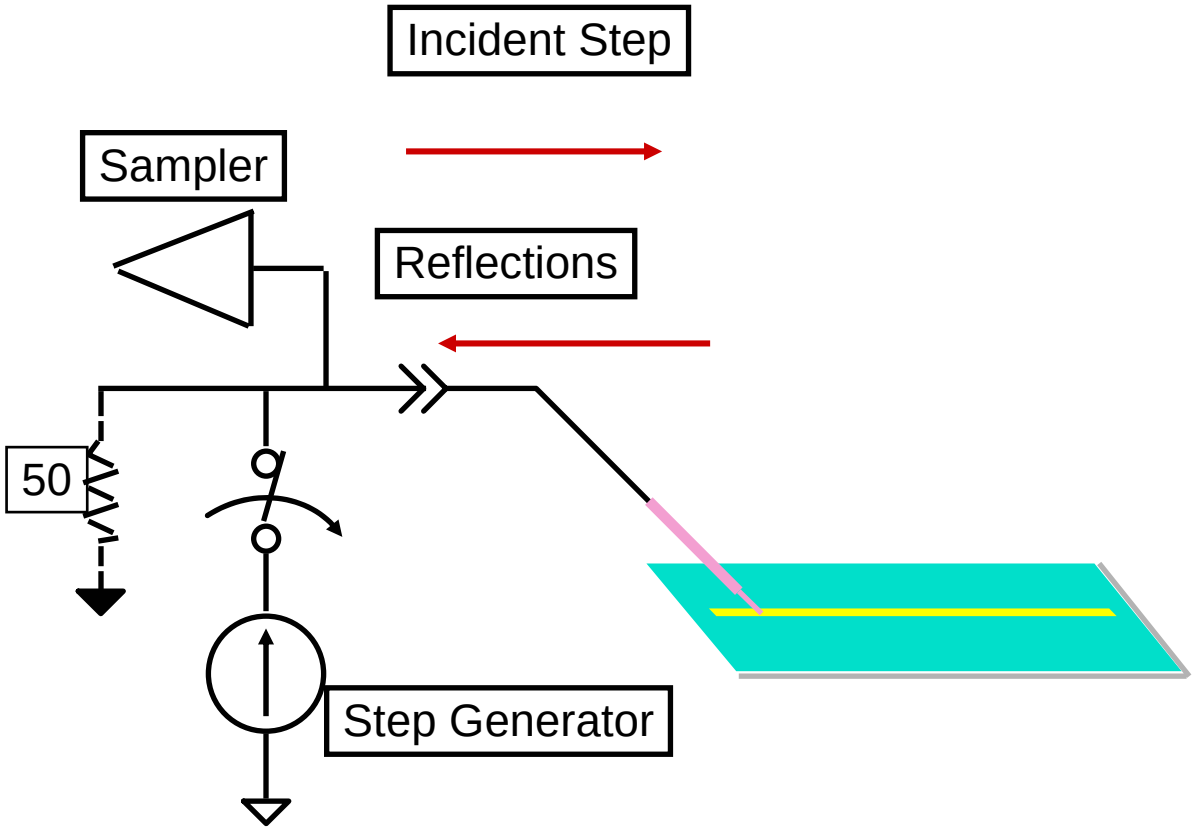
eSerial: TDR is commonly used in design and manufacturing test of eSerial Interconnects



- *TDR can test passive eSerial Interconnect to characterize where poor quality will exist when Gbit DATA is sent through it.*

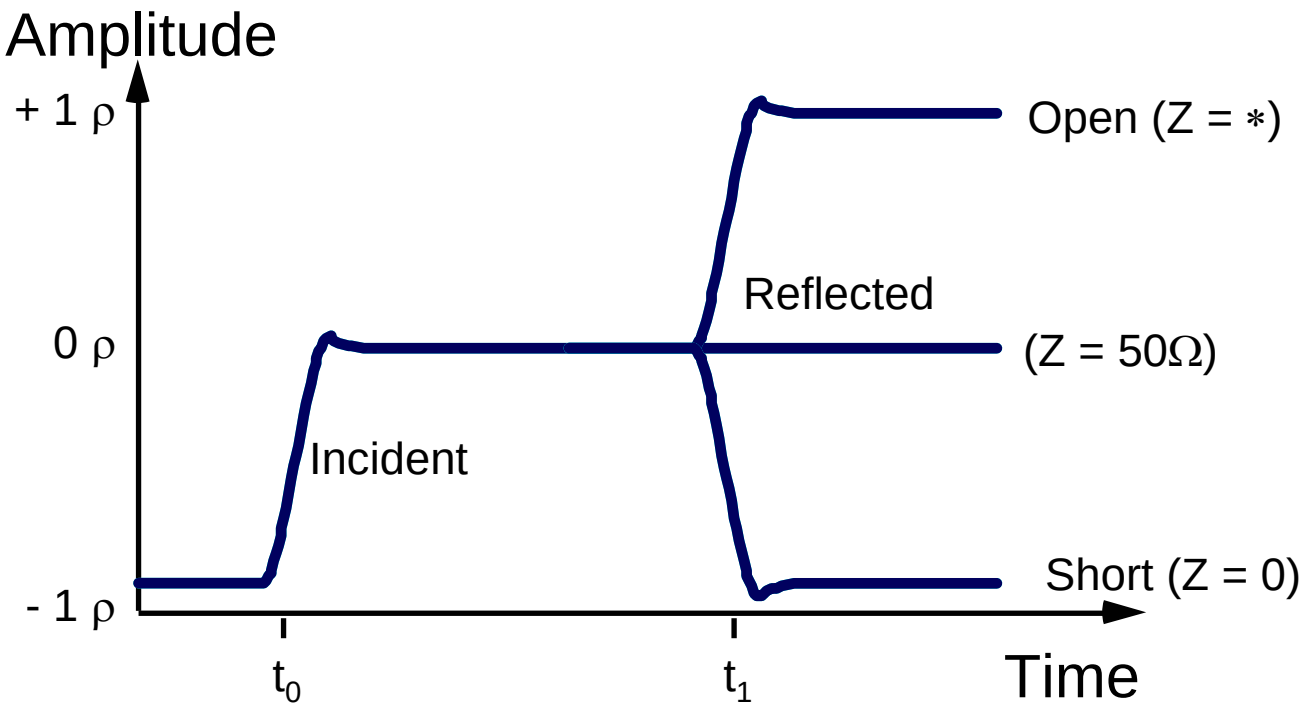
TDR Overview - Typical System



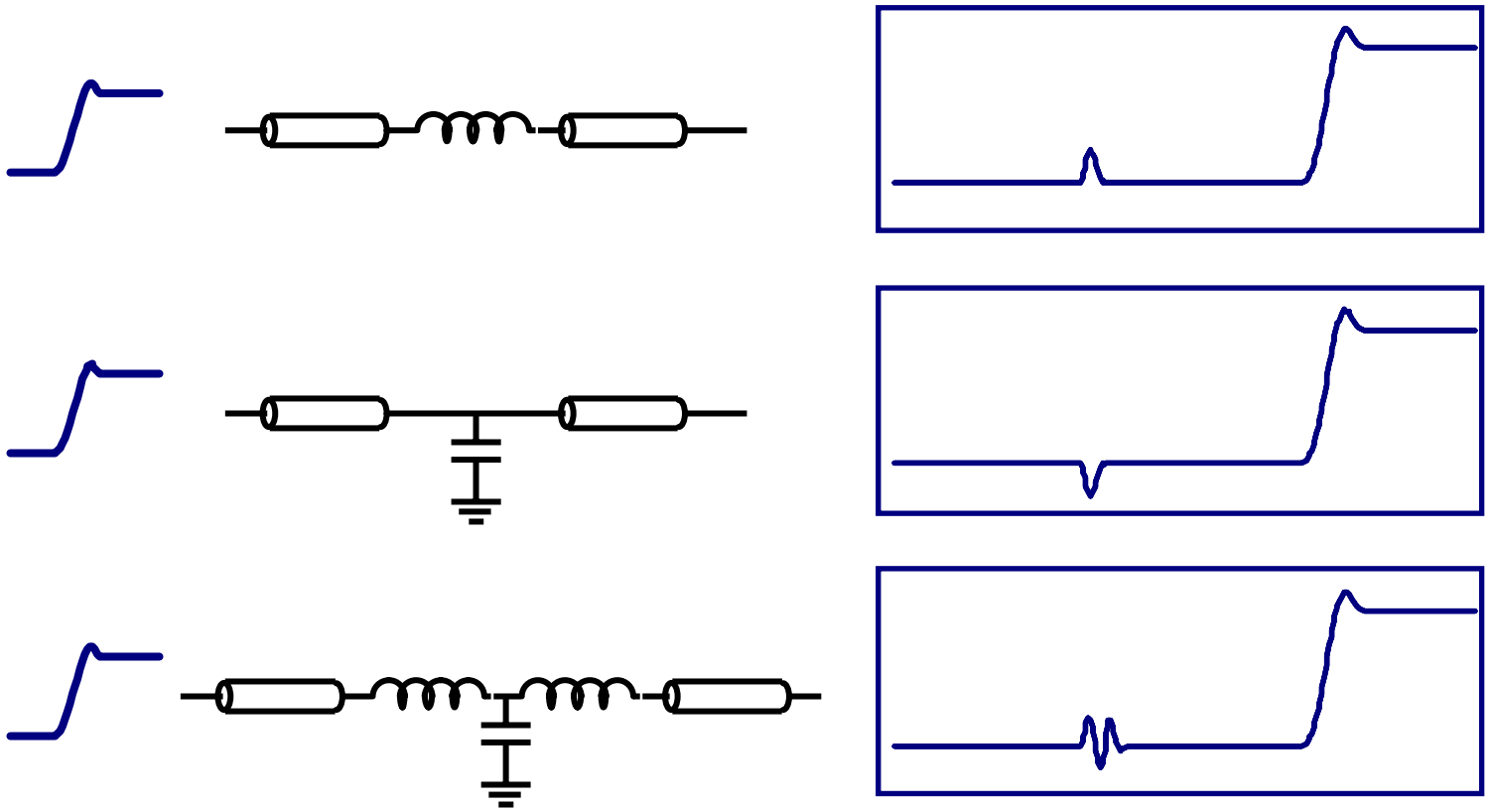


TDR Overview

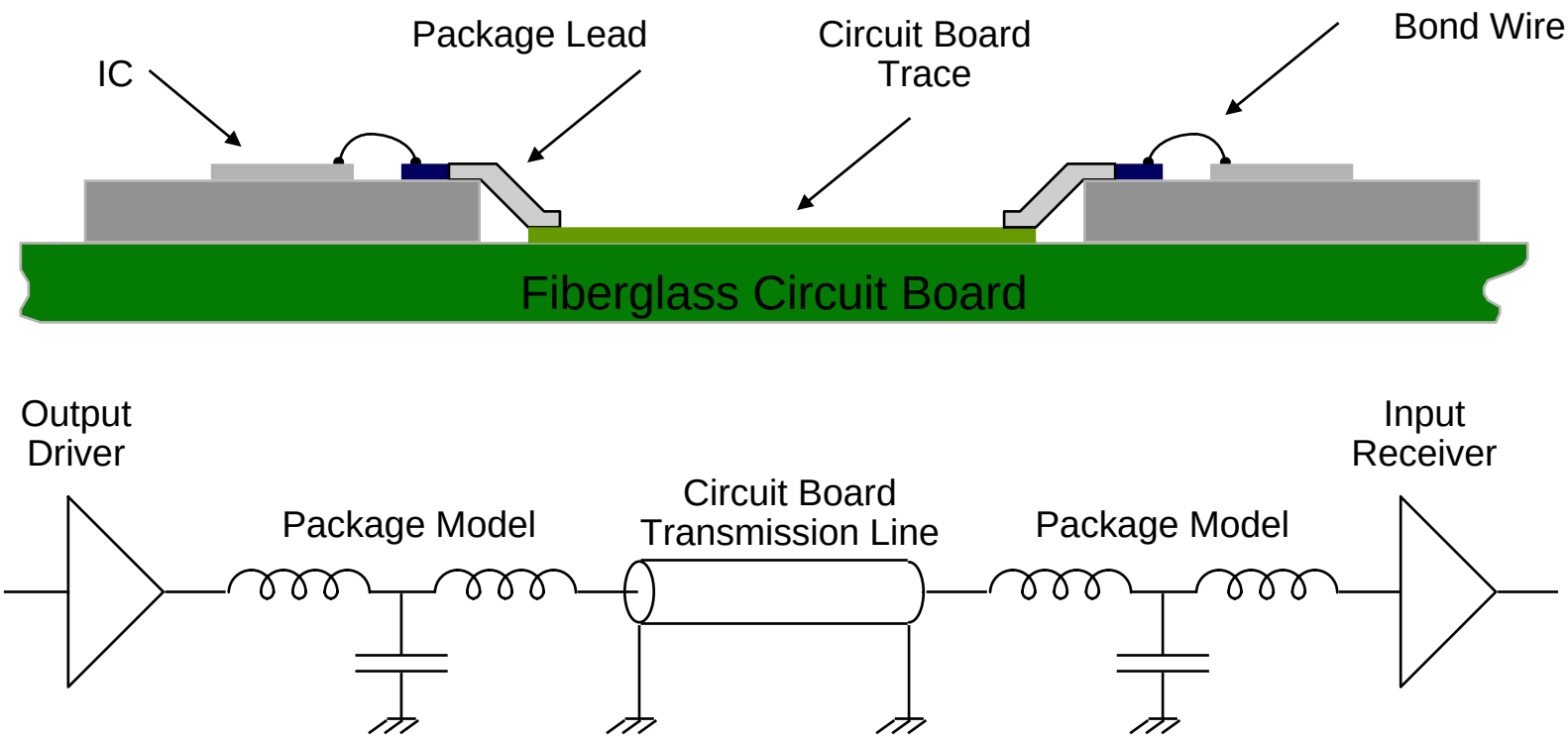
TDR Waveforms - Open, Short and 50Ω Termination



TDR Overview - Lumped Discontinuities



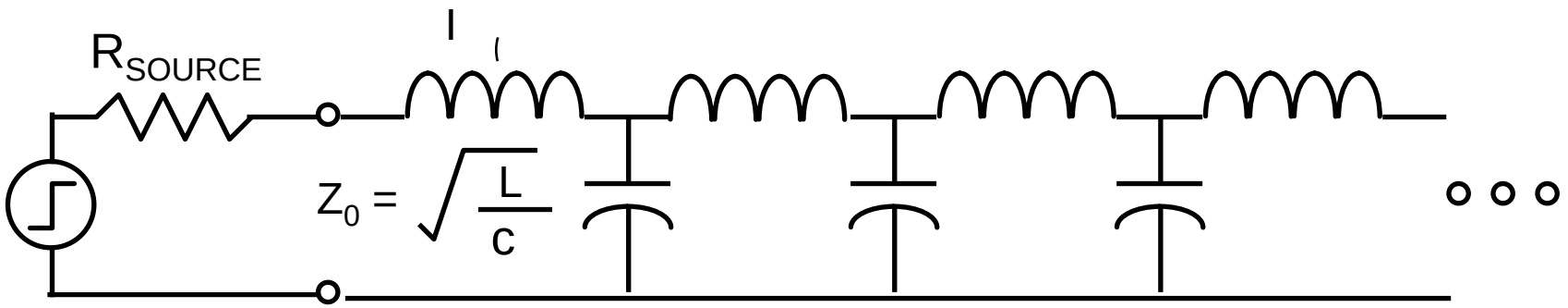
System Performance Limited by Interconnect between ICs



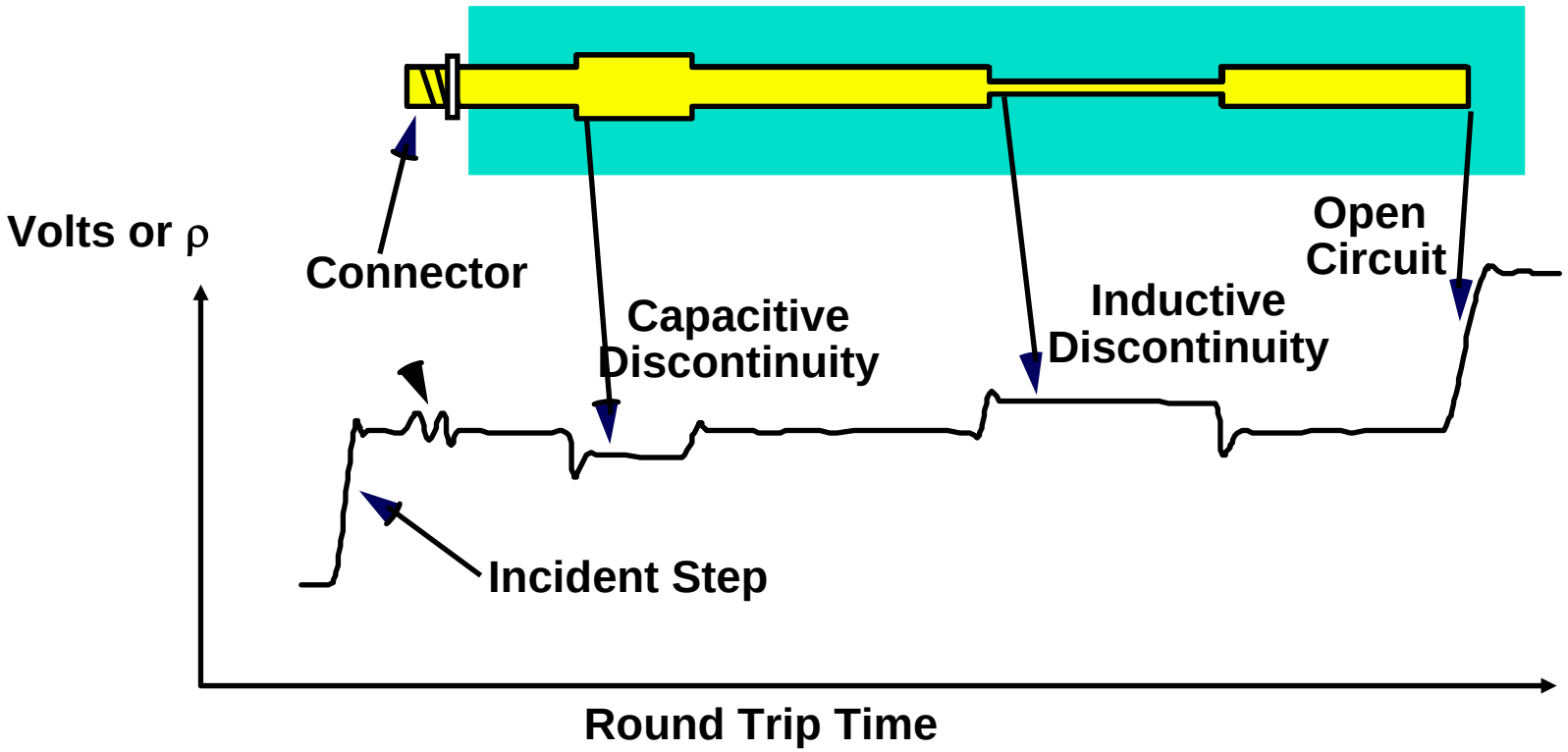
GOAL: Predict performance by simulating the interface between ICs

Ideal Transmission Line

- Amount of current is a function of the voltage and the characteristic impedance.
- While the step is propagating, z_0 and r_{source} form a voltage divider.
- Termination determines what happens at the end of the transmission line and what energy, if any, is reflected.

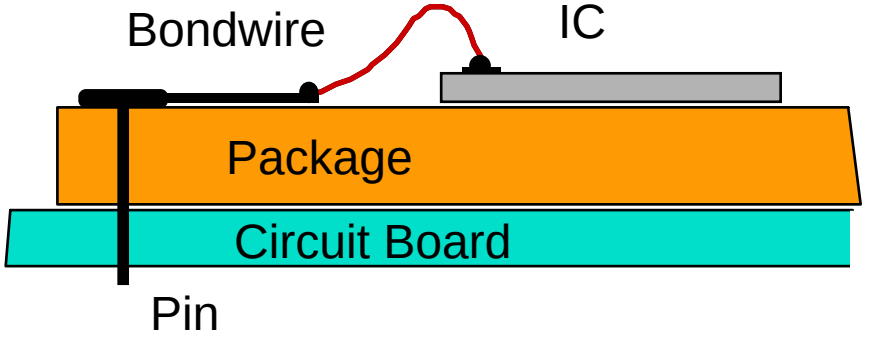


TDR Overview - Microstrip Discontinuities

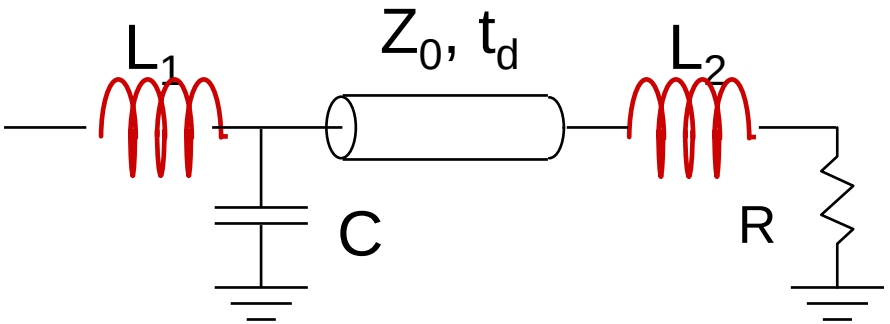


IC Package Example

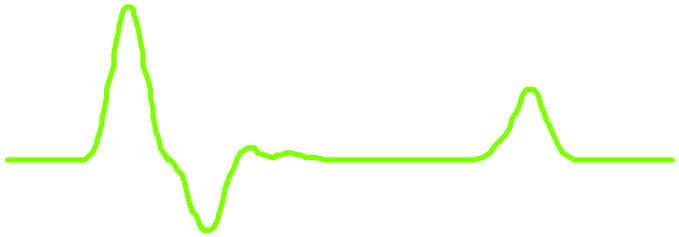
Physical Structure



Equivalent SPICE Model



TDR Trace



TDR Overview - Reflection Coefficient and Impedance

$$\textbf{Rho } (\rho) = \frac{\textbf{Reflected Amplitude}}{\textbf{Incident Amplitude}} = \frac{Z_T - Z_0}{Z_T + Z_0}$$

$$= Z_0 \frac{1 + \rho}{1 - \rho}$$

Where Z_T represents the trace impedance

Z_0 is a known impedance
(the characteristic impedance of the TDR system)

ρ is measured by the oscilloscope

TDR Overview - Measuring Impedance

$$\text{Rho } (\rho) = \frac{\text{Reflected Step}}{\text{Incident Step}}$$

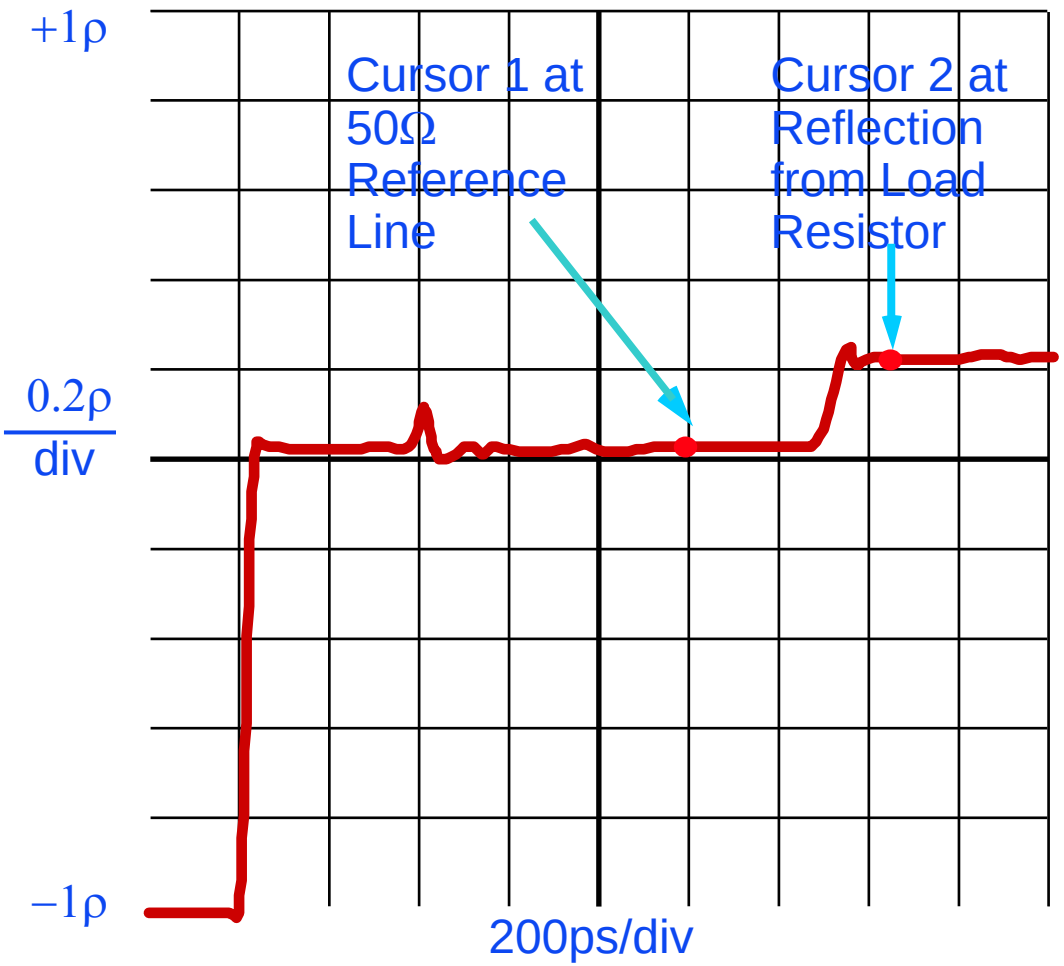
$$= \frac{1 \text{ Division}}{5 \text{ Divisions}}$$

$$= 0.2$$

$$R_{Load} = Z_0 \frac{1 + \rho}{1 - \rho}$$

$$= 50 \frac{1 + .2}{1 - .2}$$

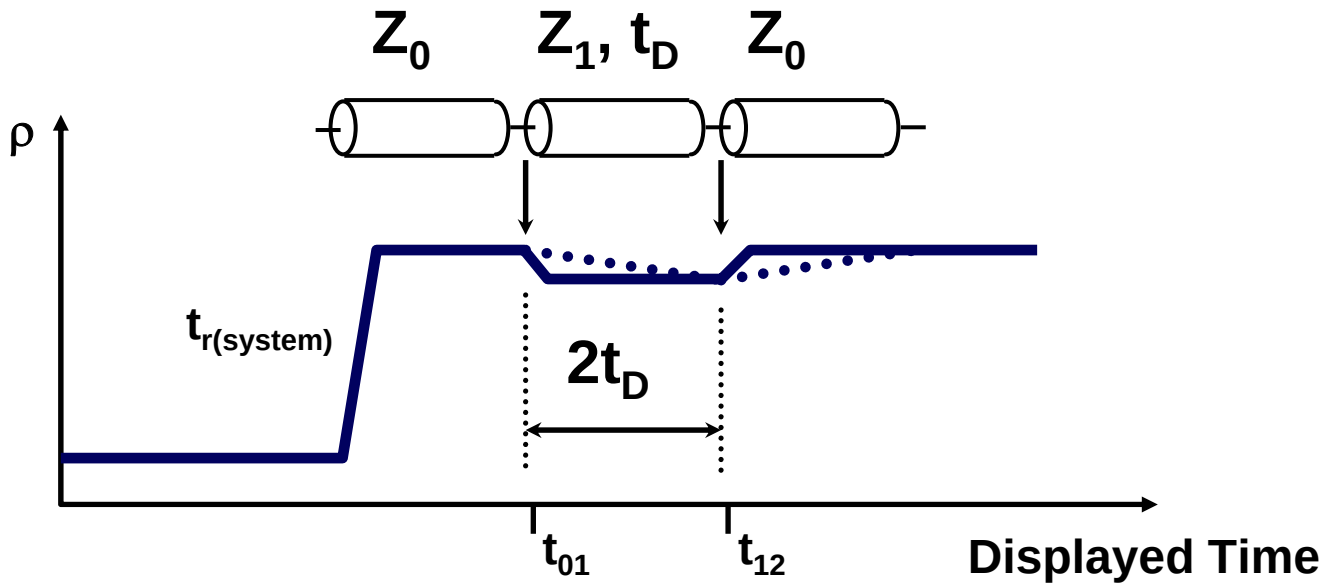
$$= 75\Omega$$



TDR Resolution

- No TDR Measurement is Ideal
  - Risetime limited on TDR Measurement Device
  - Interconnect Limited by Parasitics
- TDR Reflection will last as least as long as the Incident Edge
- Insufficient TDR Resolution
  - Rounds out Edges from Discontinuities
  - Causes Two Closely Spaced Discontinuities to be Smoothed Together
  - May Lead to Mis-Interpretation of TDR Reflection
  - May Lead to Inaccurate Impedance Readings

TDR Resolution Limitations

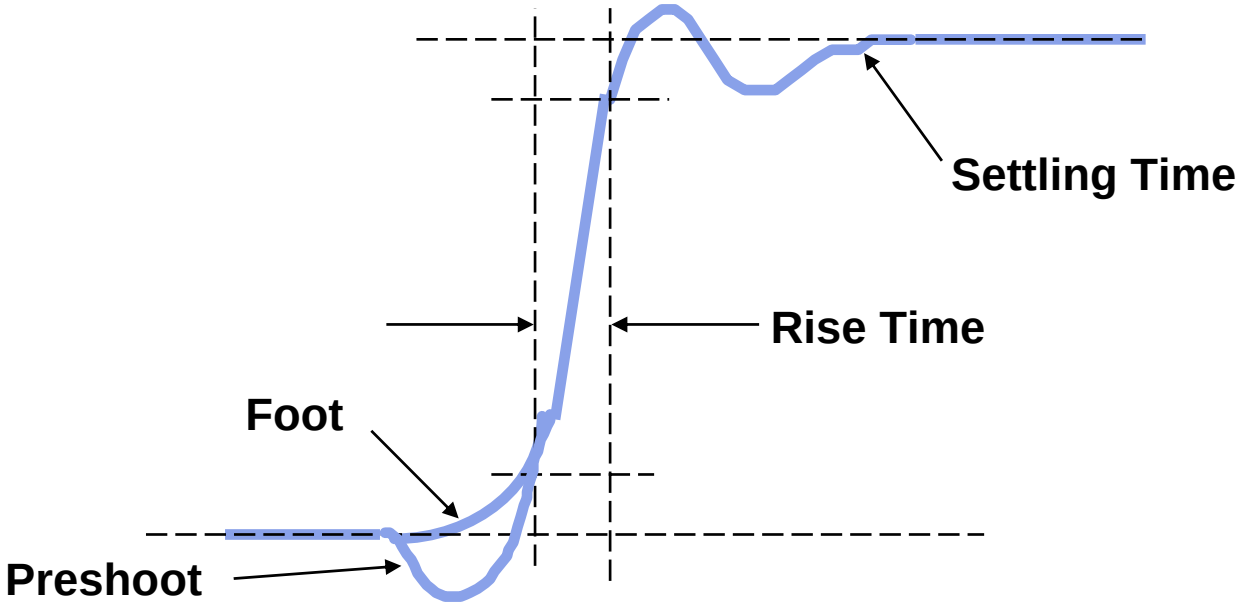


- TDR resolution is related to system risetime
  - Reflections last as long as the incident step and display as long as the system risetime

$$T_{(resolution)} = \frac{1}{2} T_{R(system)}$$

TDR Resolution

- Resolution Factors
  TDR Edge
  - Rise Time
  - Settling Time
  - Foot and Preshoot
- Resolution Factors
  Interconnect
  - Cable quality
  - Connector quality
  - Launch quality



TDR Resolution

- Rule of Thumb:
  - Two Discontinuities will be Indistinguishable if Separated by less than Half the System Rise Time
- System Rise Time is Characterized by Fall Time of Reflected Edge from Ideal Short at Test Point
- System Rise Time Approximated by:

$$T_{R(system)} = \sqrt{T_{R(stepgen)}^2 + T_{R(sampler)}^2 + T_{R(interconnect)}^2}$$

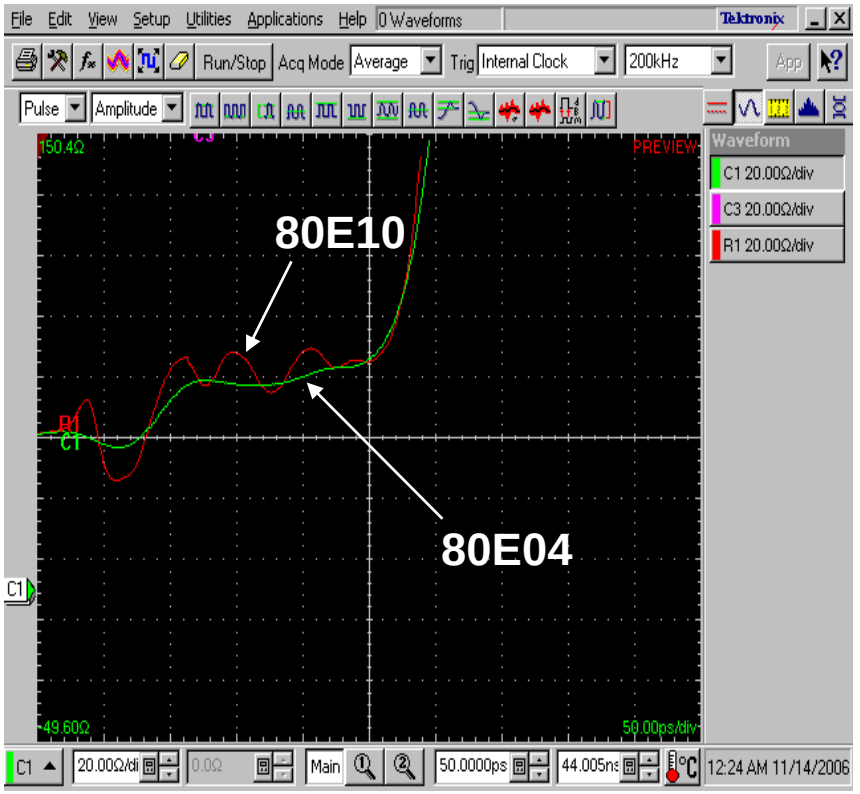
TDR Resolution

80E04 TDR Reflected Rise Time is <35 ps at Front of Sampling Head

Resolution = 35 ps /2 = 17.5 ps

- Air: 5.25 mm
- Fiberglass/epoxy circuit boards: ~3 mm
- Alumina microcircuits: ~2.5 mm

- 80E08 TDR reflected Rise time is<20ps
- 80E10 TDR reflected Rise time is<12ps



Waveform compare result

TDR Accuracy Factors

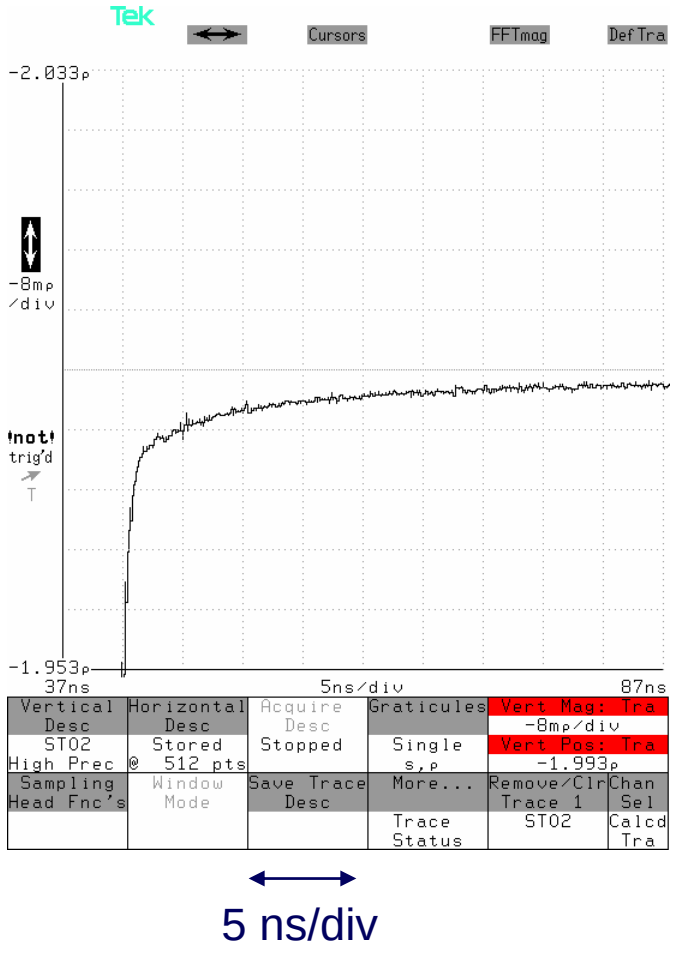
- Test System
  - Launch Parasitics
  - Cable Losses
  - Multiple Reflections
  - Interface Transmission Loss

TDR Accuracy - Test System

- Launch Parasitics
  - Effects are like those of Aberrations in Step and Sampler
  - May not be repeatable
- Cable Losses
  - Apparent Z Increase over Time
  - From Interconnect or DUT
  - Caused mostly by Skin Effect
  - Times Involved can be Very Long

Cable Losses

TDT response of 1 meter RG-58



0.8%/div

100%

5 ns/div

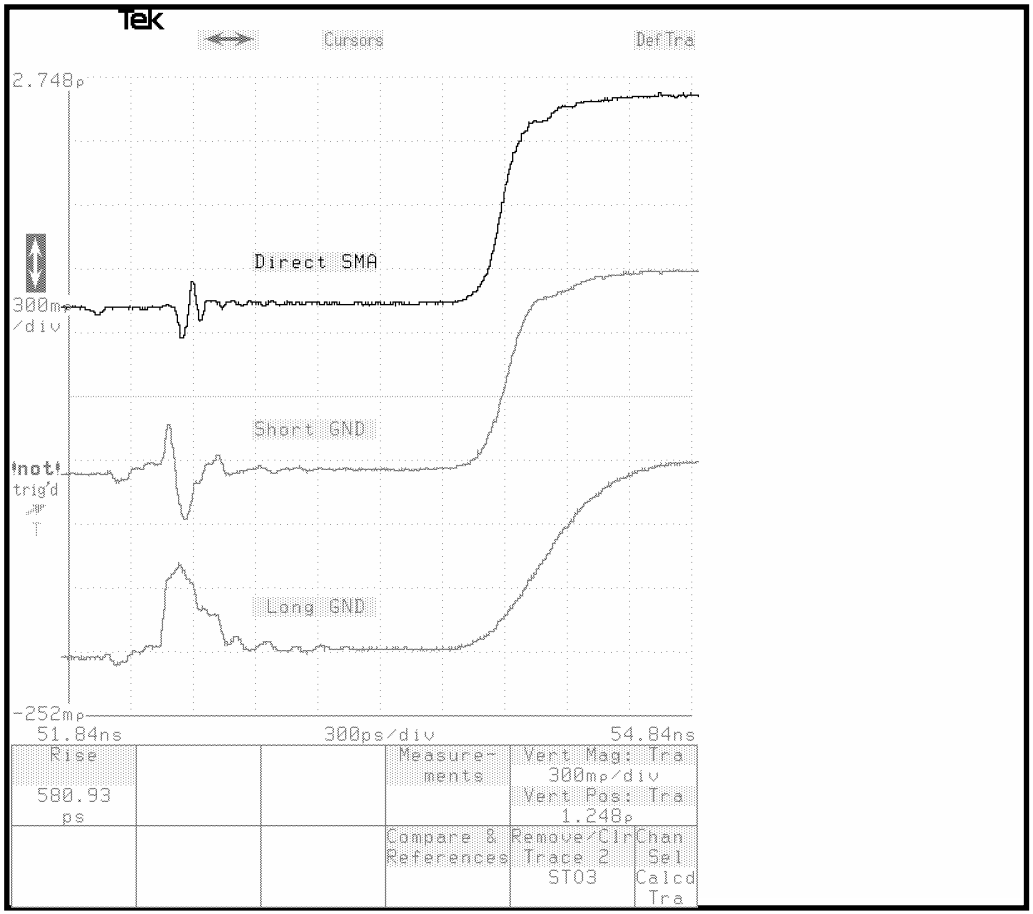
TDR Accuracy - Test System

- Multiple Reflections
  - Can Appear Anywhere in a Waveform
  - Can Look Like Anomaly or Z-shift
  - Are Predictable
  - Might be Controllable
- Interface Transmission Loss

Launch Parasitics

- The goal is to launch a fast rise time signal and maintain fidelity
- Considerations:
  - Small ground loop
  - Minimum crosstalk
  - Reliable physical connection to the DUT
  - Distance from the ground plane

Launch Parasitics

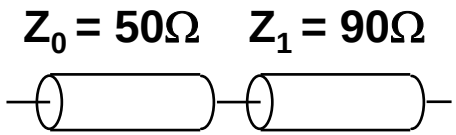


TDR Accuracy - Test System

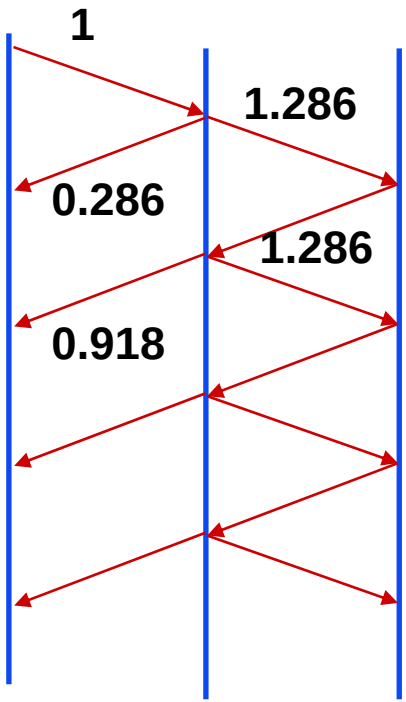
- Interface Transmission Loss
  - Only a Portion of Energy in Step Striking Interface is Transmitted
  - Only a Portion of Reflection Passing Back Through an Interface is Returned to Source
  - Reduction is Significant when Impedances at Interface are Substantially Different (e.g. 50 and 90 Ω)

Interface Transmission Loss

Effect of Multiple Impedance Discontinuities

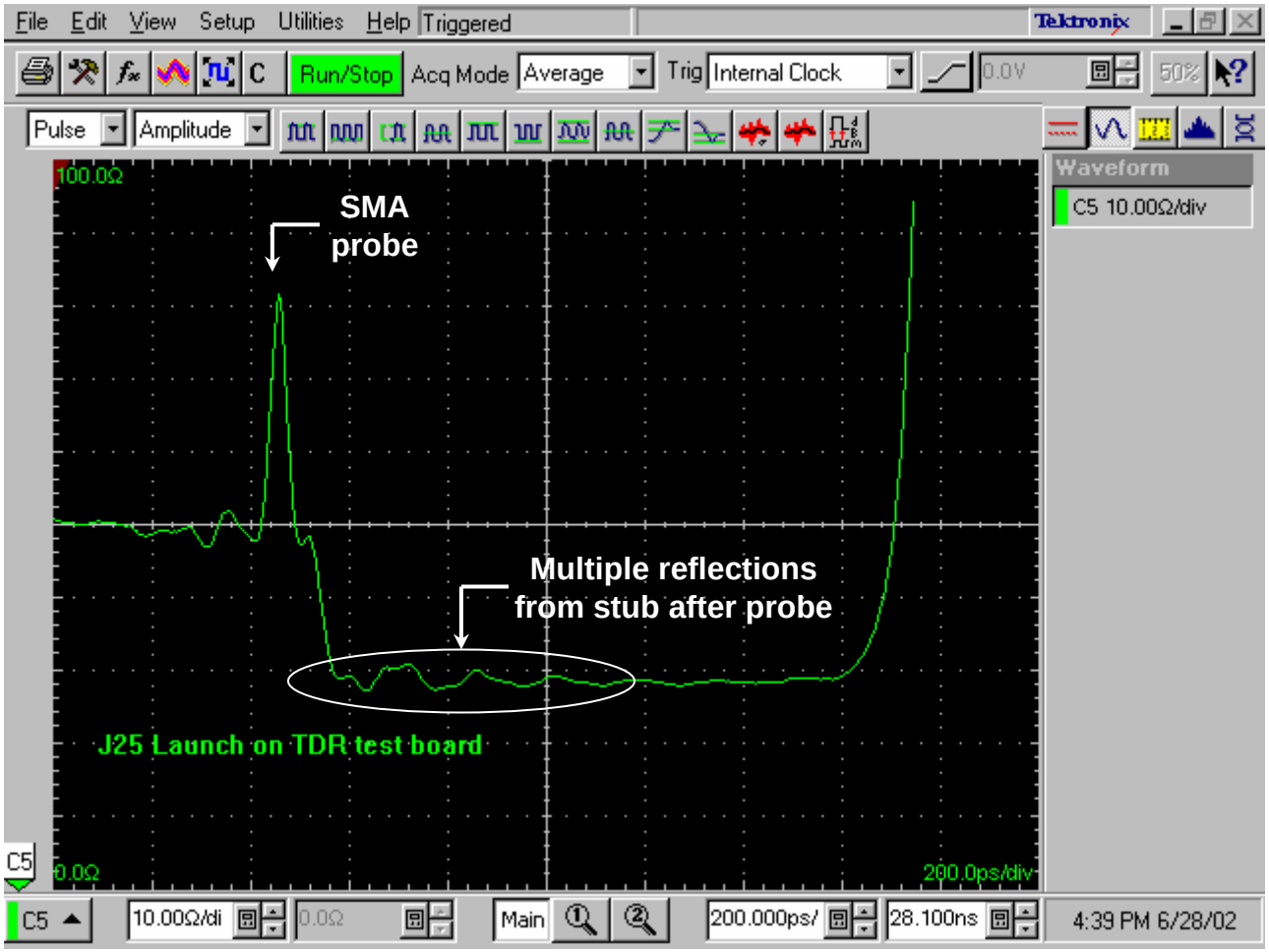


(Open)



$\rho = 0.918$ in a 50 Ω system is 1170 Ω !

Multiple Reflection Issues



Interface Transmission Loss

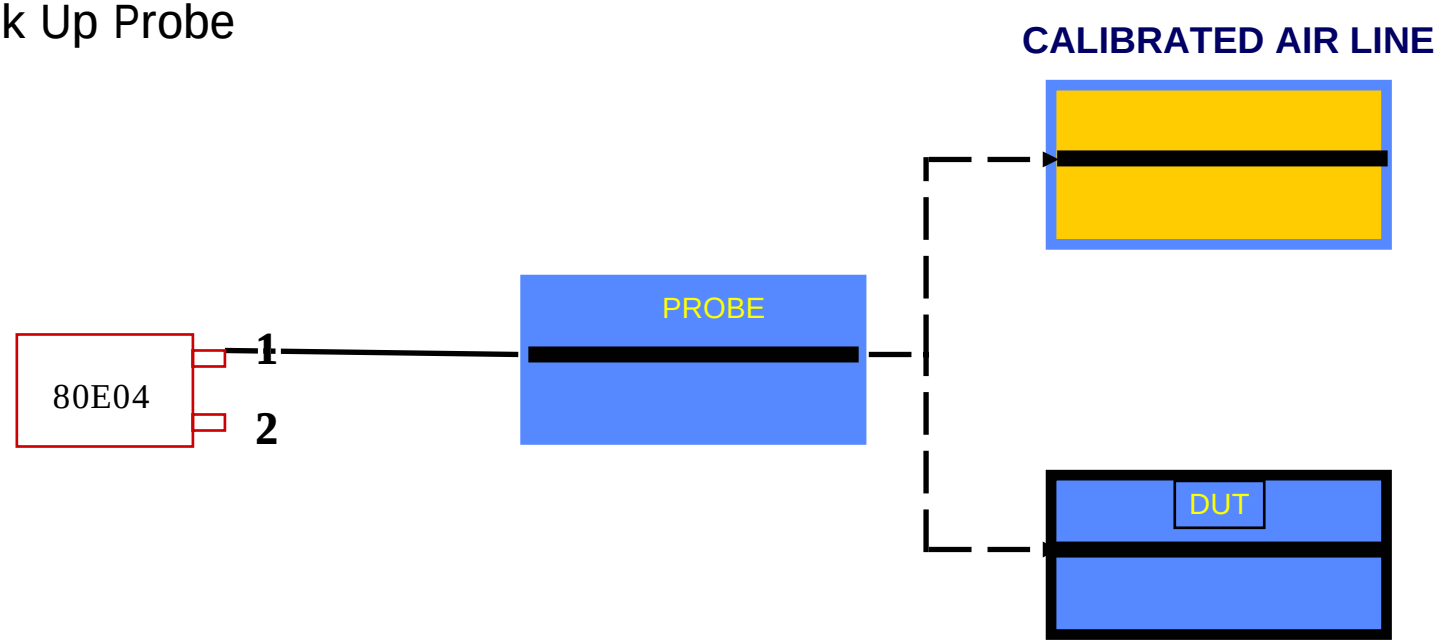
- Effects are Linear
- Can be Deconvolved (Iconnect)
- Impedance Readings can be Corrected
- Can Calibrate Once and Subsequent Measurements Corrected

TDR Accuracy Improvement
IPC - TM - 650 Method

- Eliminates These Errors
  - Step / Sampler Offset
  - Step Generator Amplitude Error
  - Sampler Gain Error (Single Gain Setting)
  - Most Aberration Errors
  - Long Term Drift / Temperature Effects
  - Skin - Effect Loss Errors
  - Interface Transmission Loss

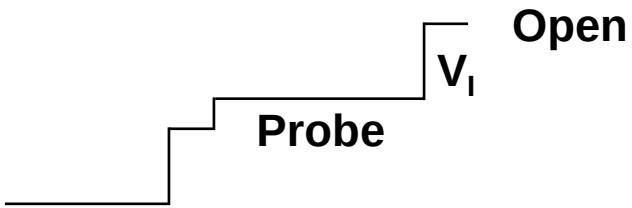
TDR Accuracy Improvement - Steps:

- Preliminary Steps
  - Preset TDR
  - Turn off Rho Cal
  - Turn off Baseline Correct
  - Hook Up Probe

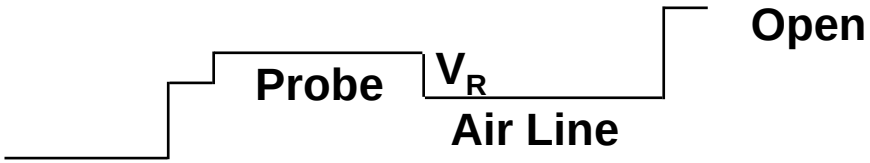


TDR Accuracy Improvement - Steps:

- Measure Probe Impedance with Air Line
  - Disconnect Air Line and Measure Size of Step Incident on Air Line V_I, as Modified by Passing Back to Sampler.



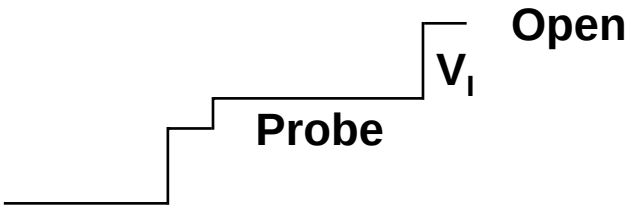
  - Re-connect Air Line and Measure size of Step Reflected from Air Line V_R, as Modified by Passing Back to Sampler.



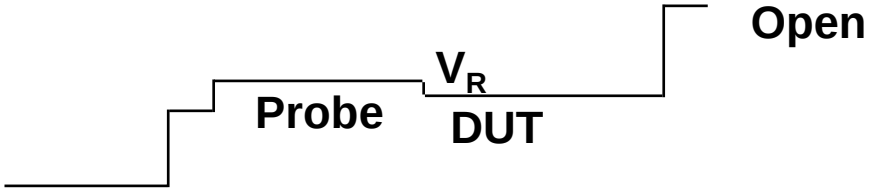
  - Calculate Z_{PROBE}: $Z_{PROBE} = Z_{AIRLINE}(V_I - V_R) / (V_I + V_R)$

TDR Accuracy Improvement - Steps:

- Measure DUT Impedance
  - Disconnect DUT and Measure Size of Step Incident on DUT V_I, as Modified by Passing Back to Sampler.



  - Re-connect DUT and Measure size of Step Reflected from DUT V_R , as Modified by Passing Back to Sampler.



  - Calculate Z_{DUT}: $Z_{DUT} = Z_{PROBE}(V_I + V_R) / (V_I - V_R)$

TDR Accuracy Improvement - Advantages

- Reduces Problem to Three Critical Measurements
  - Probe (Secondary Standard) Impedance Z_{PROBE}
  - Incident Step at DUT V_I
  - Reflected Step from DUT V_R
- Uses Primary Traceable Standard (Air Line)
  - Can be Sent to Standards Lab (NIST)
  - Can Also Use Internal or "Golden" Standards

TDR Accuracy Improvement - Caveats

- Always Measure with Last Line or DUT Open Circuited
  - Eliminates Step Amplitude Change with Loading
- Always Measure Same Distance From Beginning of Step
  - Reduces Sensitivity to Aberrations, Dribble-Up
  - Reduces Chance of Measuring Re-reflections
- Minimize Probe / TDR Cable Length and Loss
- Use Short, Repeatable Connector Between Probe and Air Line or Probe and DUT

TDR Accuracy Improvement - Caveats

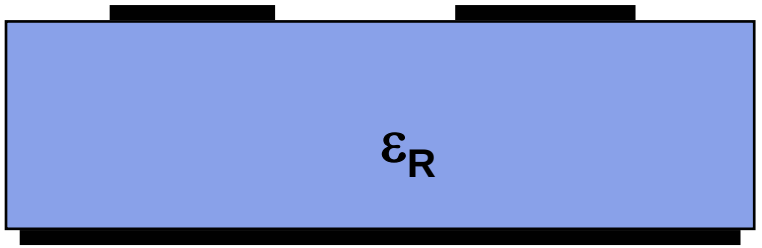
- Keep Probe Impedance and DUT Impedances Close to One Another
  - Keep Baseline and Topline on Same Screen
  - V_R will be Small, Making High Accuracy Possible
  - Sensitivity to Accuracy of V_R will be Very Low
- Keep Interconnect Impedance Between Probe and DUT Likewise Close
  - Avoids Re-reflection Problem

Agenda

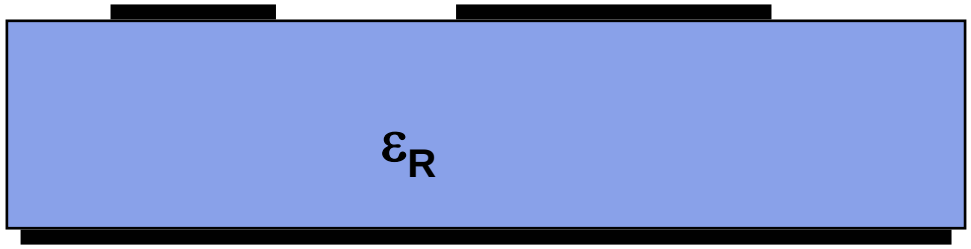
- TDR resolution and accuracy
- Differential transmission line
- How to make test coupon
- Other TDR/TDT measurement

Types of Coupled Lines

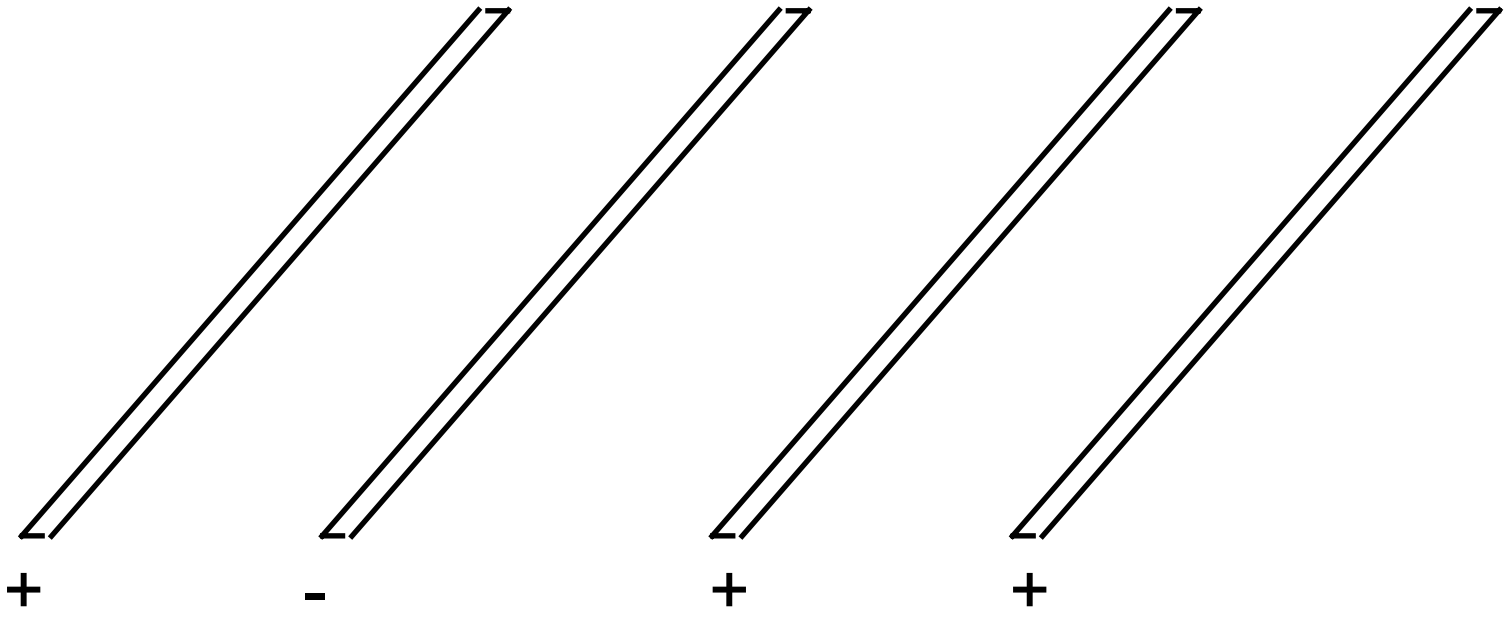
- Symmetric Coupled Lines - "Differential" or "Balanced"
  - Homogeneous
  - Inhomogeneous



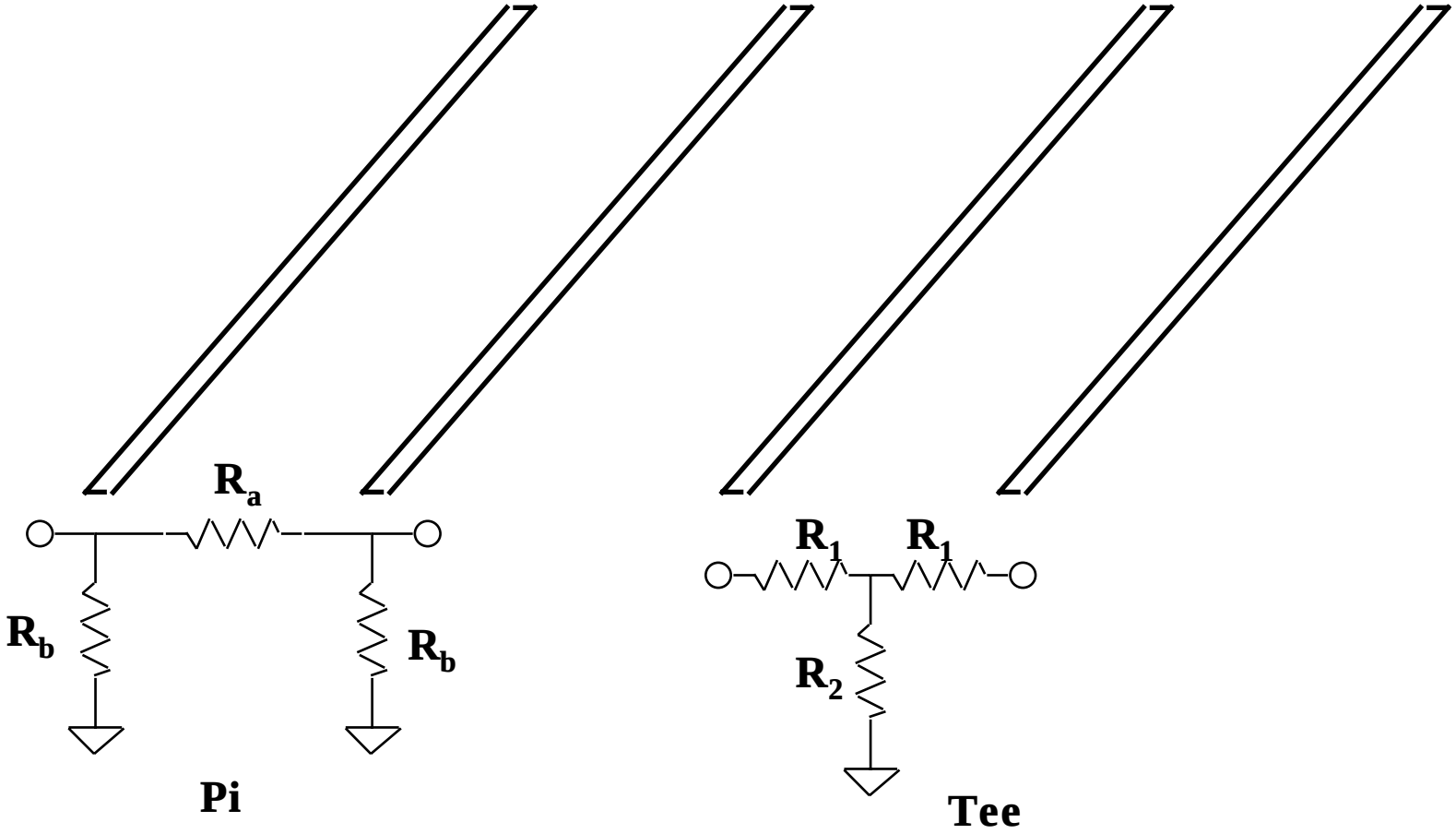
- Non-Symmetric Coupled Lines - "Unbalanced*



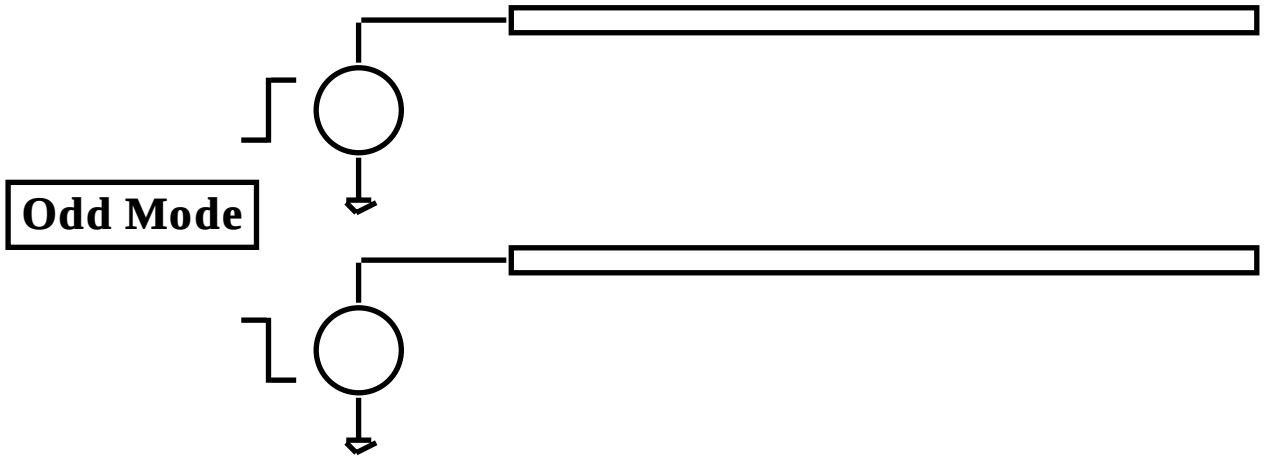
Odd and Even Modes

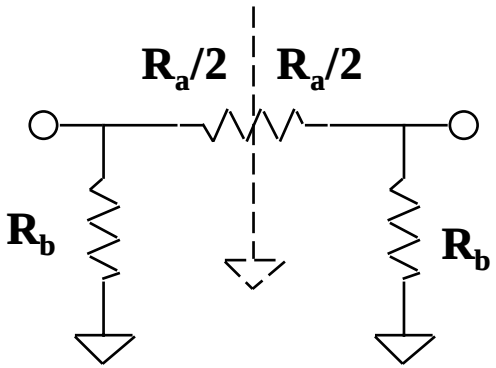


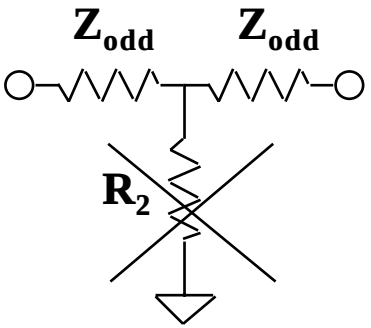
Model for Symmetric Coupled Lines



Characterizing Symmetric Coupled Lines - Odd Mode

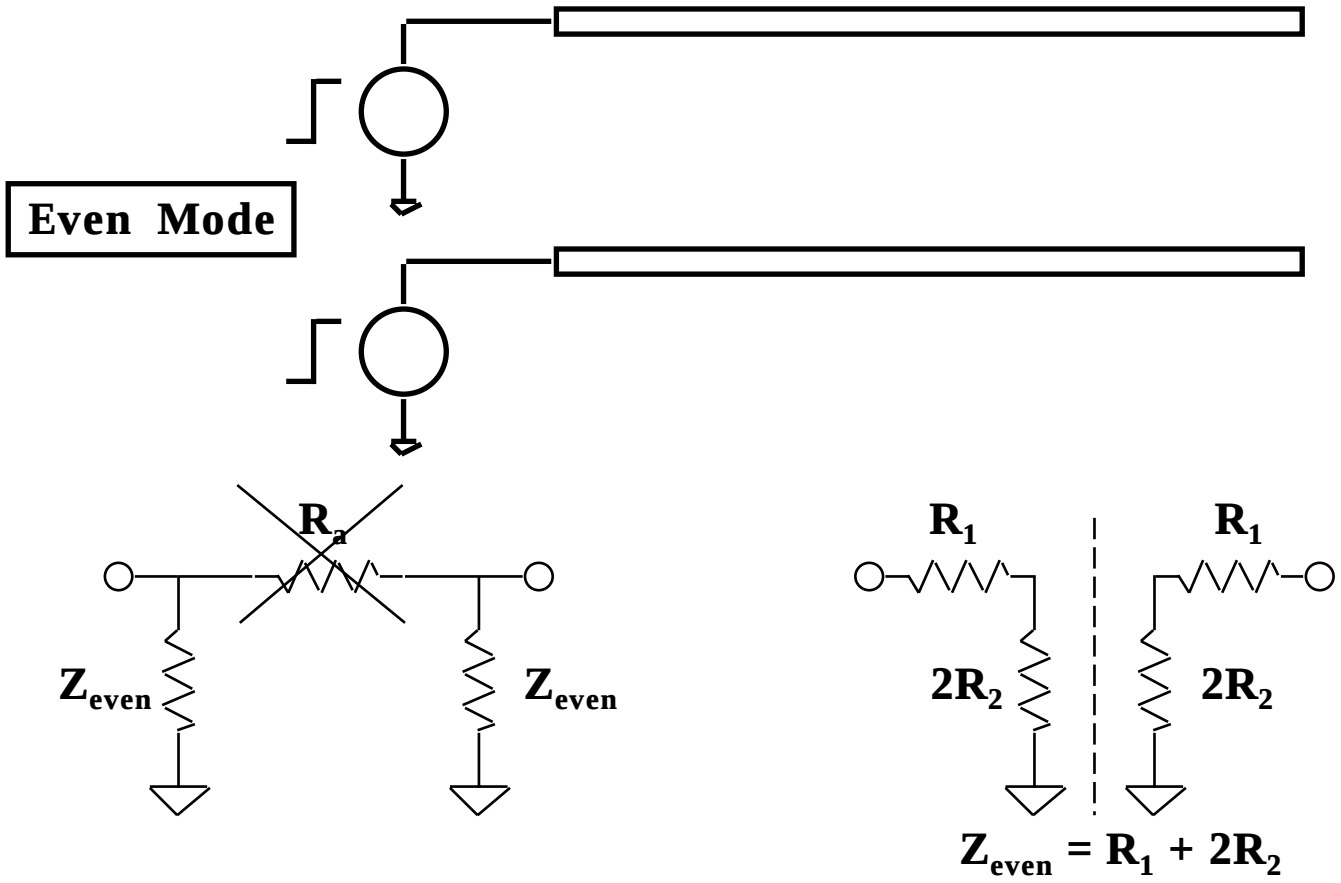






$$Z_{odd} = (R_a/2) \,||\, R_b$$

Characterizing Symmetric Coupled Lines - Even Mode

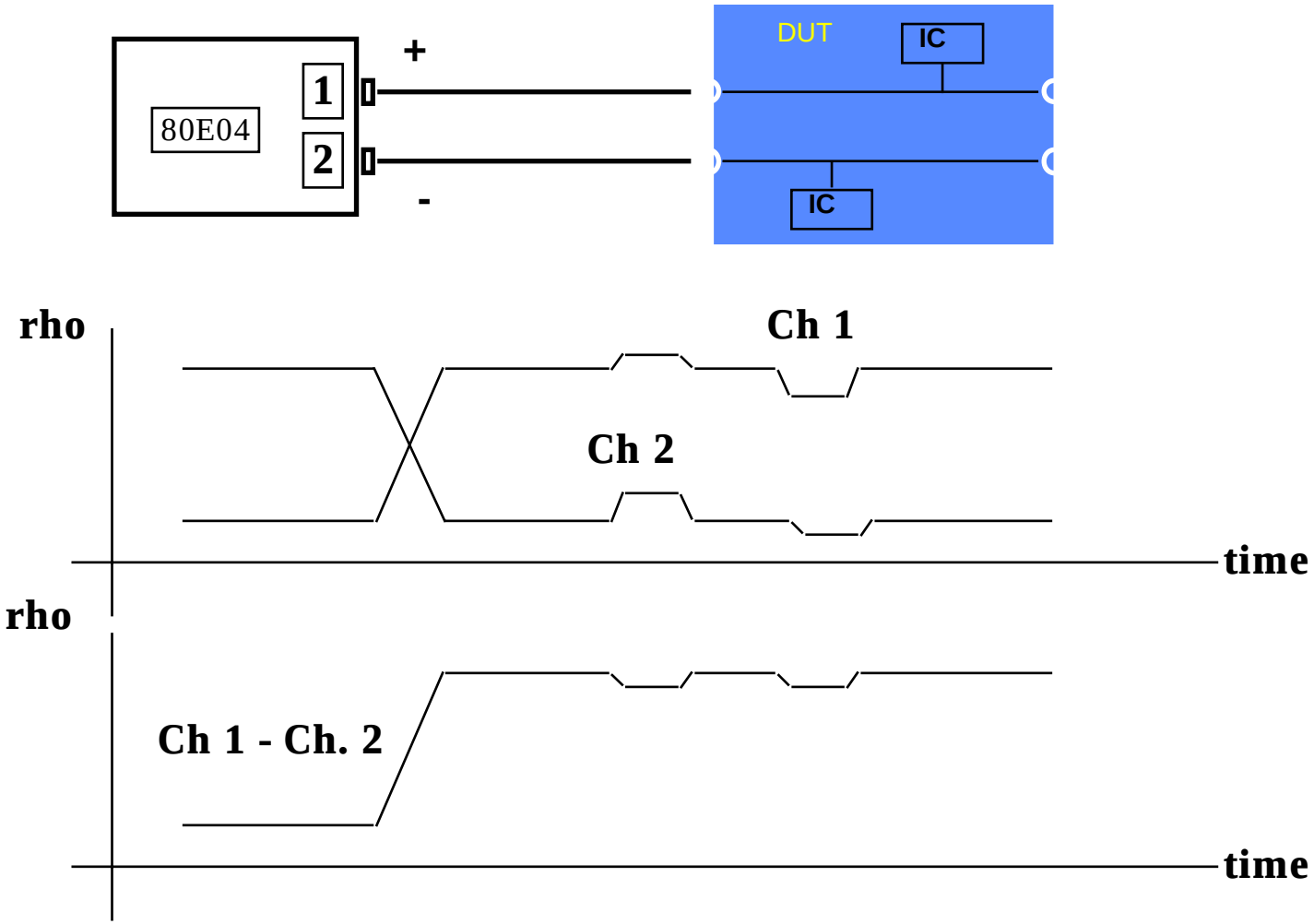


TDR Measurements – Differential TDR Measurement

With the signal integrity issues many designs have gone to differential transmission lines to achieve:

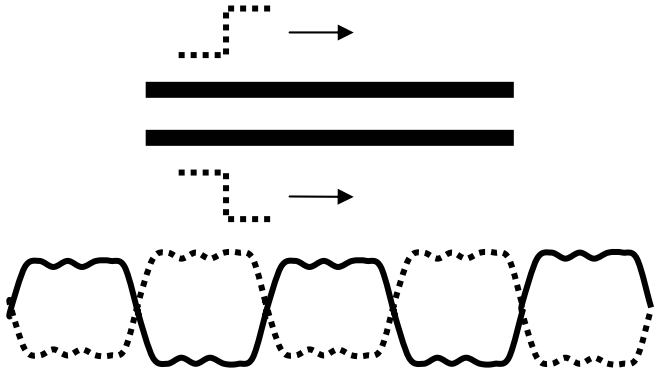
- Higher noise immunity due to common mode rejection
- Less radiated noise due to canceling fields
- More precise timing characteristics
- Less crosstalk due to noise immunity and less radiated energy
- Less power supply noise due to current transients

Almost-Differential Systems



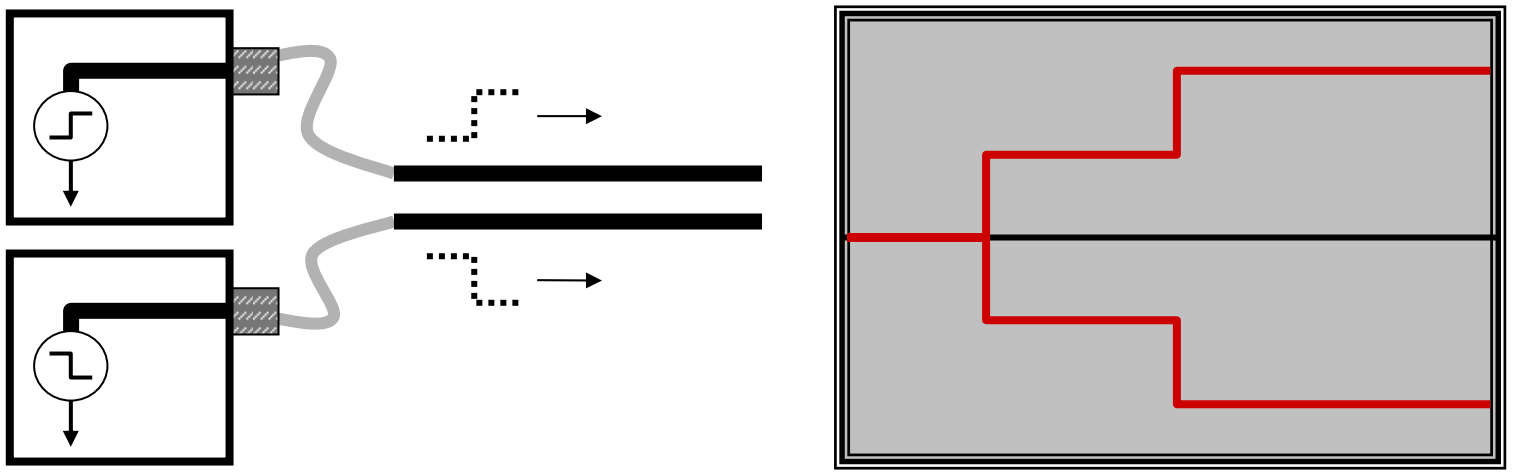
TDR Measurements – Differential Clock Coupling

- Attempting to measure the two halves of the differential pair separately can produce misleading results
- Two traces in close proximity tend to read a lower impedance than their characteristic impedance as a pair
- Proper characterization of the differential impedance of the transmission line to maintain voltage and timing margins



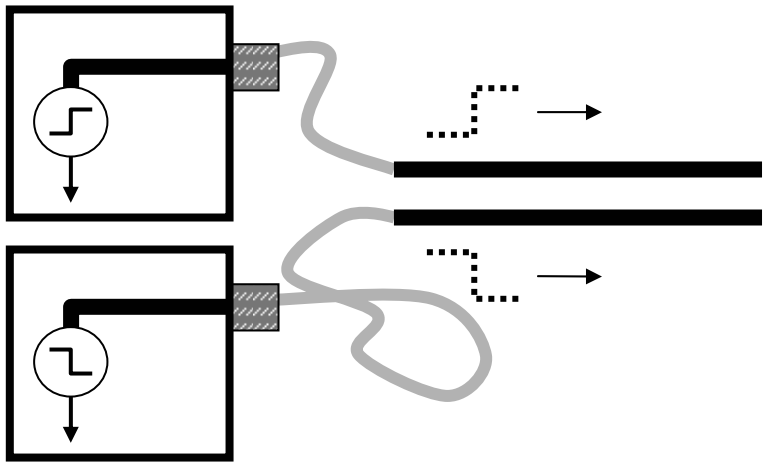
TDR Measurements – Differential TDR Measurement

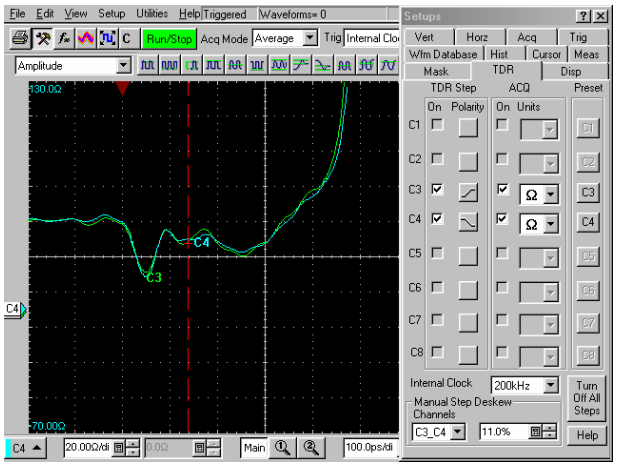
- A differential TDR measurement is performed much like a single-ended TDR measurement
- Use two TDR sampling head channels with the step generators set to opposite polarities



TDR Measurements – Differential TDR Step Timing Skew

- Another important consideration when making differential TDR measurement is the alignment of the TDR step pulses
- The positive and negative going TDR steps must be adjusted so there is not any time skew between them at the transmission line launch point





Agenda

- TDR resolution and accuracy
- Differential transmission line
- How to make test coupon
- Other TDR/TDT measurement

Test Coupons

- TDR Test Line Added to Every Circuit Board Panel
- Serves as Referee for Acceptance of Impedance Requirements for all lines on Circuit Board
- Must be representative of Lines

Use of Test Coupons

- Use test coupons when:
  - Cannot access end of actual lines for measurement
  - Don't want to perform 100% test
  - Verifiable evidence needed
- Test coupon should be representative of
  - Board material
  - Board layering and construction
  - Metallization process
  - Circuit environment

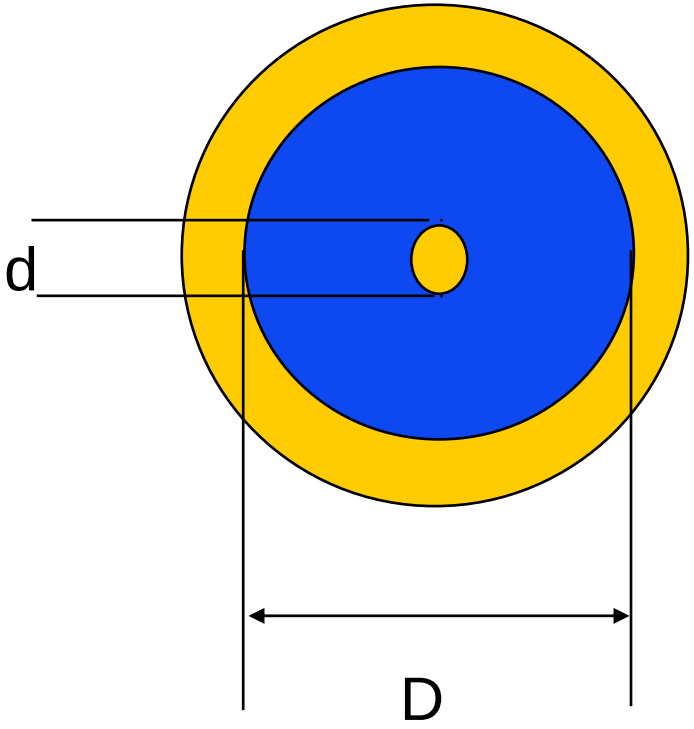
Test Coupon Rules

- Use representative line width, copper weight, dielectric thickness, dielectric type, and solder mask
- Have full ground under lines
- Don't Drill or Remove Board Material Nearby
- Locate Coupon in Panel where conditions of Plating, Lamination, and Etching are average.
- Stay within image area of Panel.
- If Isolated, Balance Plating Density nearby

Test Coupon Rules

- Keep clear of metal within 2.5 mm or 5 Line Widths (whichever is greater)
- Provide sufficient line length relative to TDR resolution (150 mm)
- Consider Type of Connection
  - Provide clean connection capability
  - Provide ground at launch points

Characterize Impedance(1)

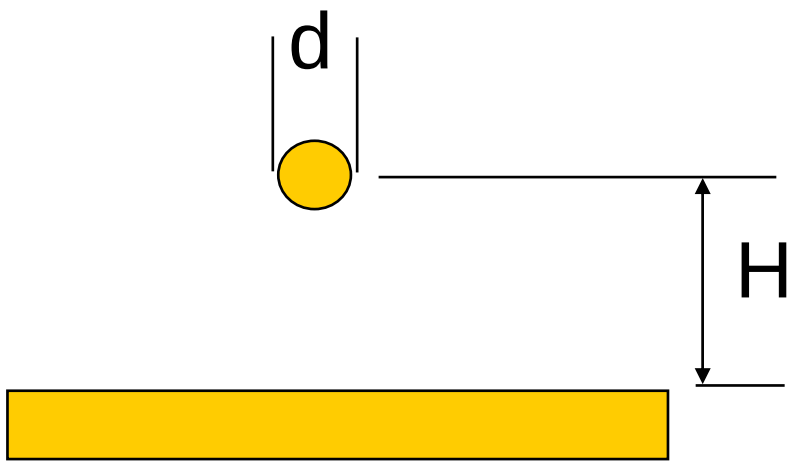


$$Zo = \frac{60}{\sqrt{\varepsilon r}} \, Ln\left[\frac{D}{d}\right]$$

$$V\sqrt{\varepsilon}$$

COAXIAL CABLE

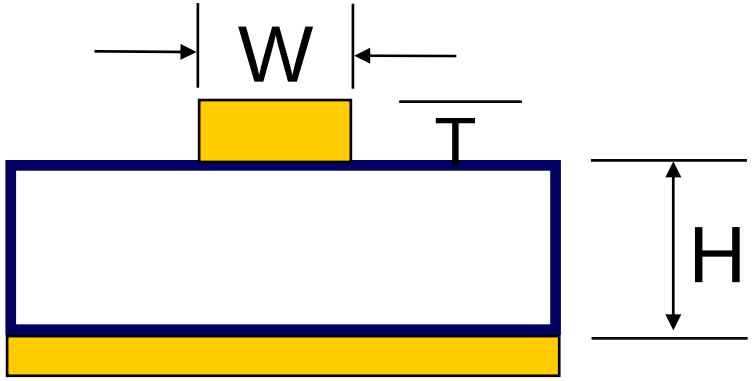
Characterize Impedance(2)



$$Zo = \frac{60}{\sqrt{\varepsilon r}} \ln\left[\frac{4H}{d}\right]$$

WIRE-OVER-GROUND

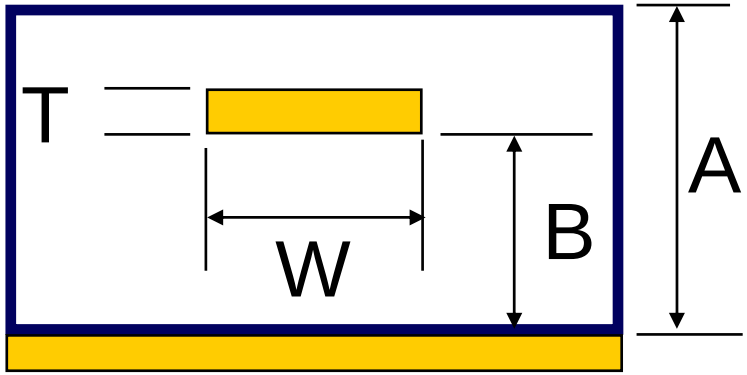
Characterize Impedance(3)



Micro-strip-line

$$Zo = \frac{87}{\sqrt{\varepsilon_r + 1.41}} \ln\left(\frac{5.98*H}{0.8W + T}\right)$$

Characterize Impedance(4)

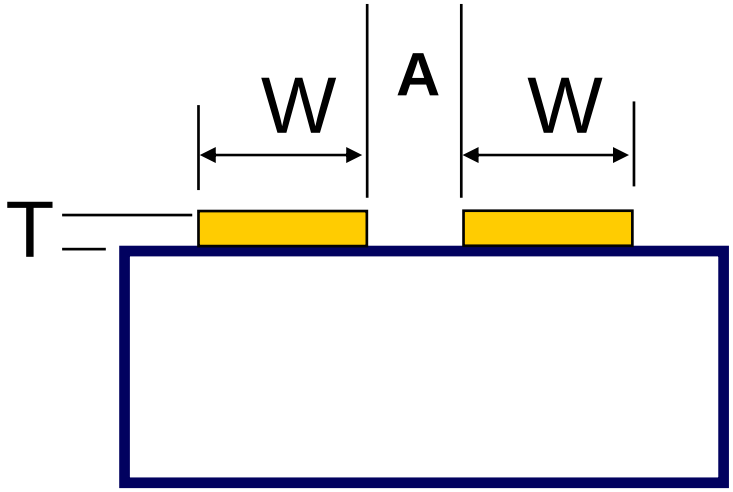


$$Zo = \frac{87}{\sqrt{\varepsilon_r + 1.41}} \ln\left(\frac{5.98*B}{0.8W + T}\right)$$

$$\varepsilon_r = \varepsilon[1 - \exp(-1.55A/B)]$$

Embedded Micro-strip or Coated micro-strip

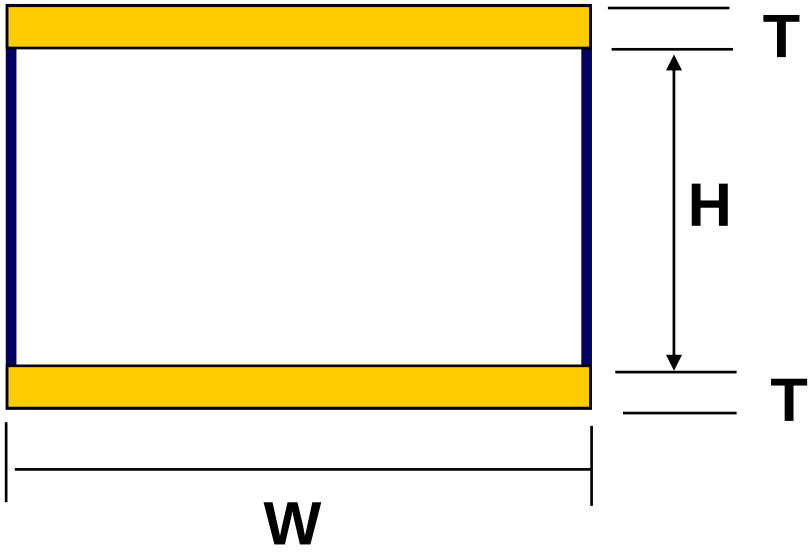
Characterize Impedance(5)



$$Zo = \frac{120}{\sqrt{\varepsilon r}} \, Ln\left[\frac{\pi A}{W+T} \right]$$

Side by side

Characterize Impedance(6)

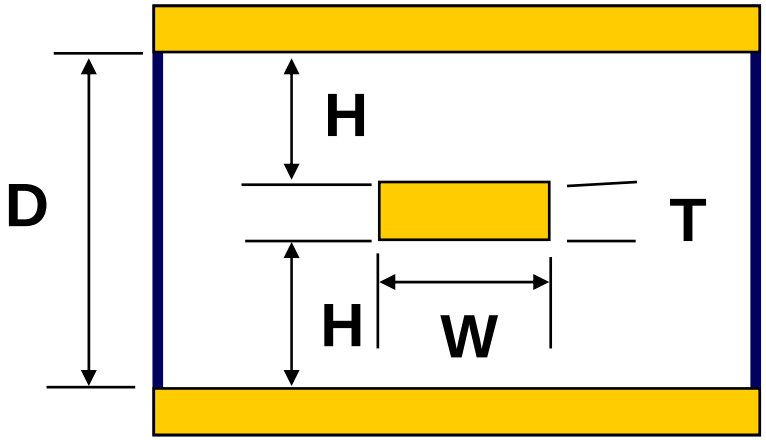


$$Zo = \frac{377}{\sqrt{\varepsilon r}} \, Ln\left[\frac{H}{W}\right]$$

W >>H and H >>T

Flat Parallel

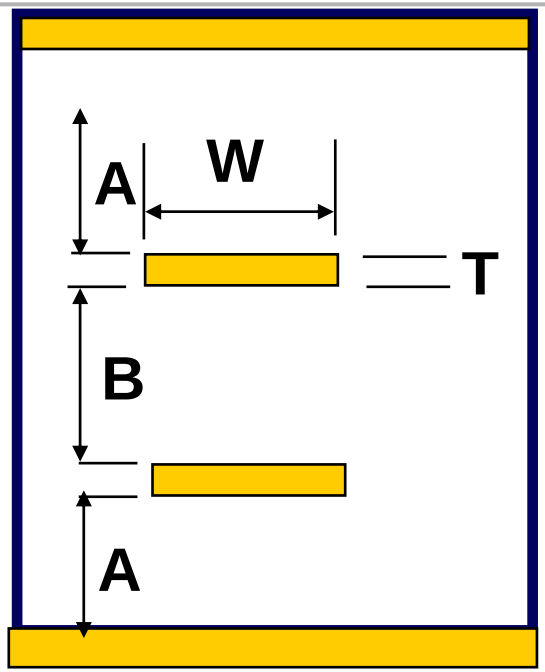
Characterize Impedance(7)



Strip-line

$$Zo = \frac{60}{\sqrt{\varepsilon r}} \, Ln\left[\frac{4D}{0.67\,\pi\,(0.8W+T)}\right]$$

Characterize Impedance(8)



Dual-strip-line or
Asymmetric strip-line

$$Zo = \frac{80}{\sqrt{\varepsilon r}} \, Ln\left[\frac{1.9(2A+T)}{(0.8W+T)} \right] x \left[1- \frac{A}{4(A+B+T)} \right]$$

Agenda

- TDR resolution and accuracy
- Differential transmission line
- How to make test coupon
- Other TDR/TDT measurement

DUT TDR / TDT Measurements

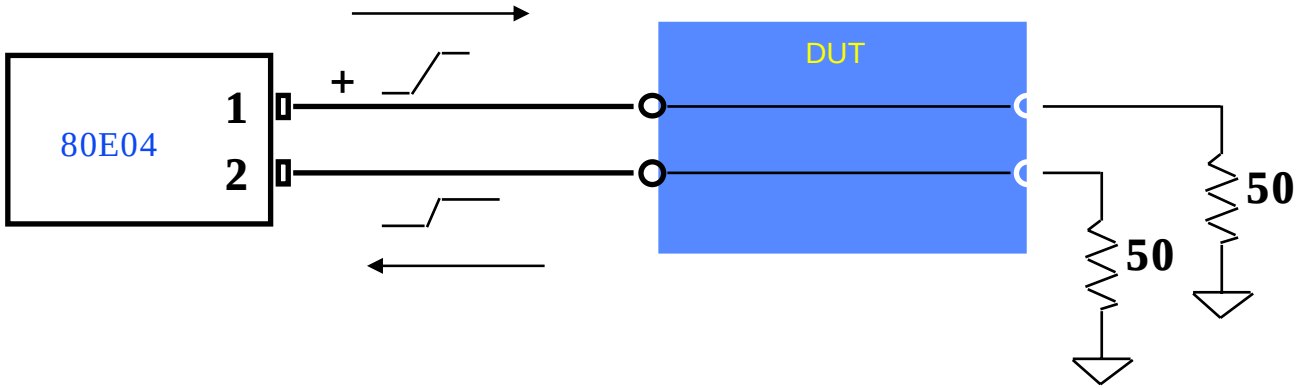
- Cross-Talk
- Moding
- Transmission Line Losses
- Transmission Line Dispersion

Crosstalk

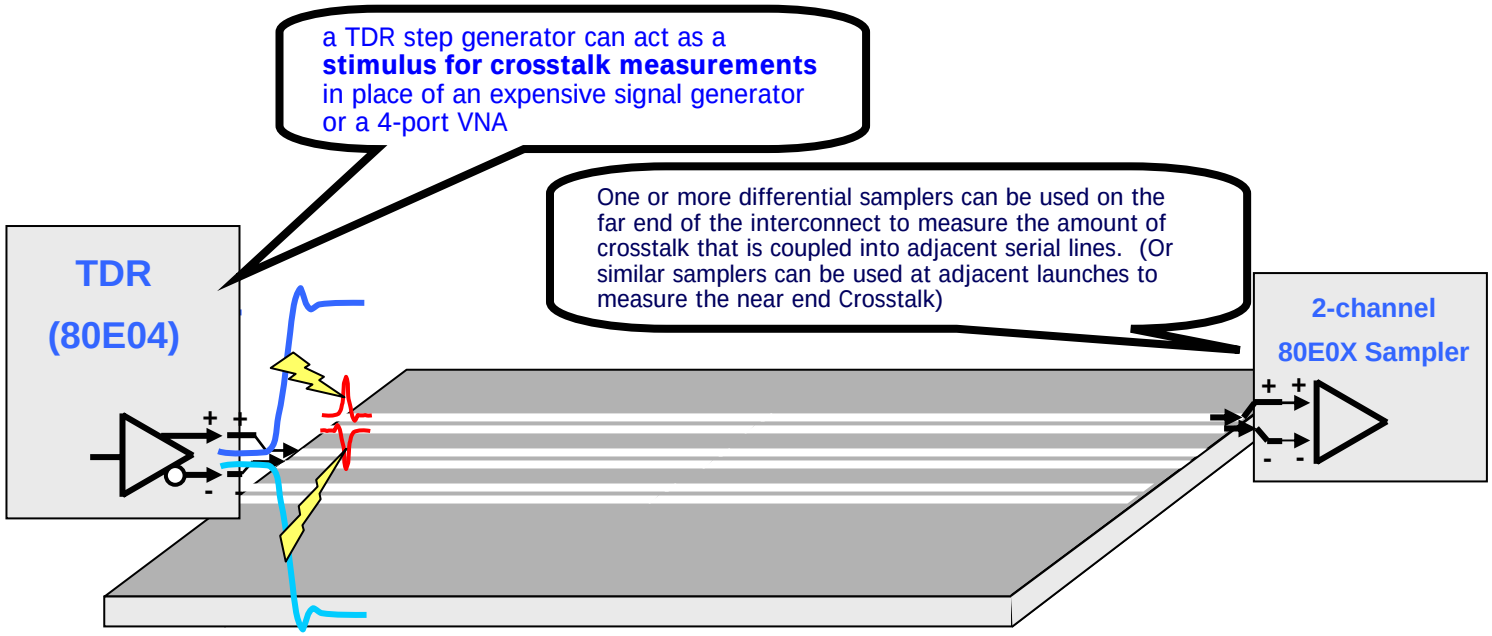
- The Coupling of Energy from One Line to Another
- The Three Elements Contributing to Crosstalk:
  - Port Terminations
  - Stimulus
  - Moding on Transmission System
- Generalities:
  - Proportional to the Line Length
  - Proportional to Rise Time of Driving Signal
  - Can be Positive or Negative
    (Inductive or Capacitive Coupling)
  - Both Forward (Near-end) and Backward (Far-end)
  - Non-Characteristic Port Terminations Make it Worse

Crosstalk Measurement Techniques

- Set up TDR on Aggressor Line
- Observe Victim Lines with TDT
- Take Care to Terminate All Other Lines
- Use Filter to Simulate Actual System Speeds

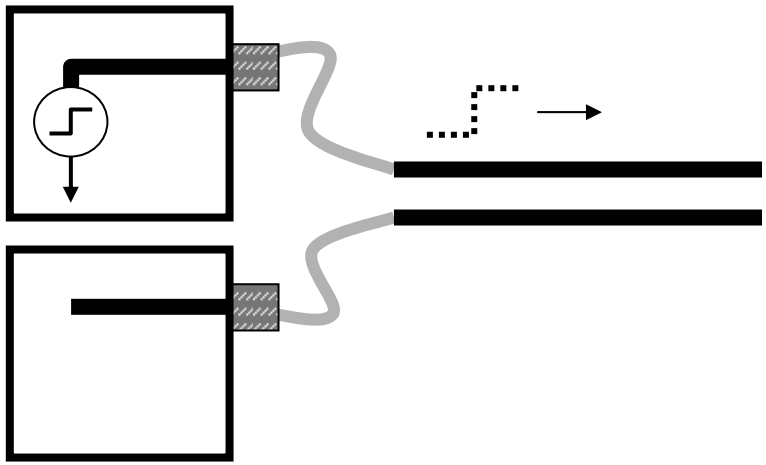


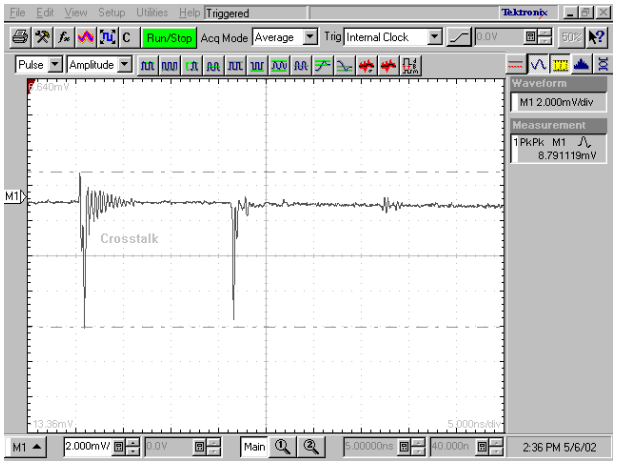
Serial Data Crosstalk: TDR/TDT is a Tool to Characterize This Difficult Problem



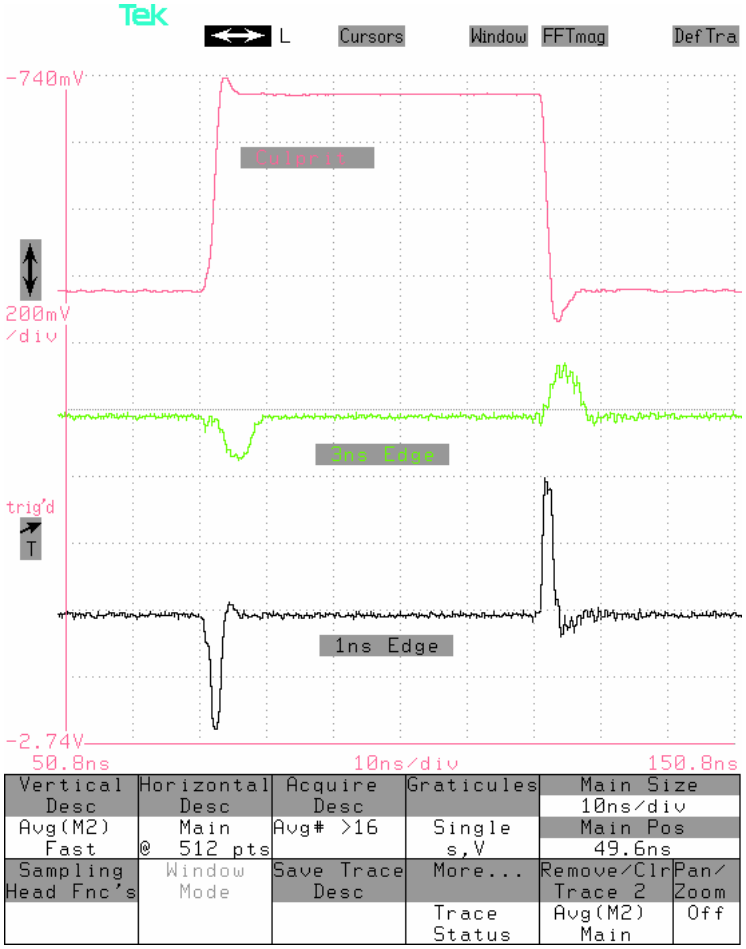
More TDR Measurements – TDT Transmission Line Coupling and Crosstalk

- Mutual coupling and crosstalk between signal lines can be characterized with TDT measurements
- Apply the TDR step on one signal line and measure the signal strength on the other





Crosstalk


Tek
L
Cursors
Window
FFTmag
Def Tra
-740mV
Culprit
200mV
/div
3ns Edge
trig'd
T
1ns Edge
-2.74V
50.8ns
10ns/div
150.8ns
Vertical Desc
Horizontal Desc
Acquire Desc
Graticules
Main Size
10ns/div
Avg(M2)
Fast
Main
@ 512 pts
Avg# >16
Single
s,V
Main Pos
49.6ns
Sampling
Head Fnc's
Window
Mode
Save Trace
Desc
More...
Remove/Clr
Trace 2
Pan/
Zoom
Trace
Status
Avg(M2)
Main
Off

Crosstalk Cures

- Smaller Loop Areas for Inputs and Outputs
- Slower Edge Speeds
- Series Resistance at Driver
- Reduce Capacitive Loading
- Use More Grounds (Z_{even} smaller)
- Randomize Periodic Shielding Geometry
- Reduce Common Run Lengths, or Route Signals at Right Angles over Common Ground Planes
- Isolate Synchronous Busses
- Use Differential Circuit Design

Moding

- n - Multiple Lines Have n - Distinct Propagation Modes
- Each Mode Orthogonal
  - Coupled line even mode is (1,1)
  - Coupled line odd mode is (1,-1)
- Each Mode May Have Unique Propagation Velocity
  - Crosstalk May Invoke Several Modes
  - Unique Mode Velocities May "Spike" Responses at Ports Due to Arrival of Moded Signal Components at Different Times

Minimizing Moding Ills

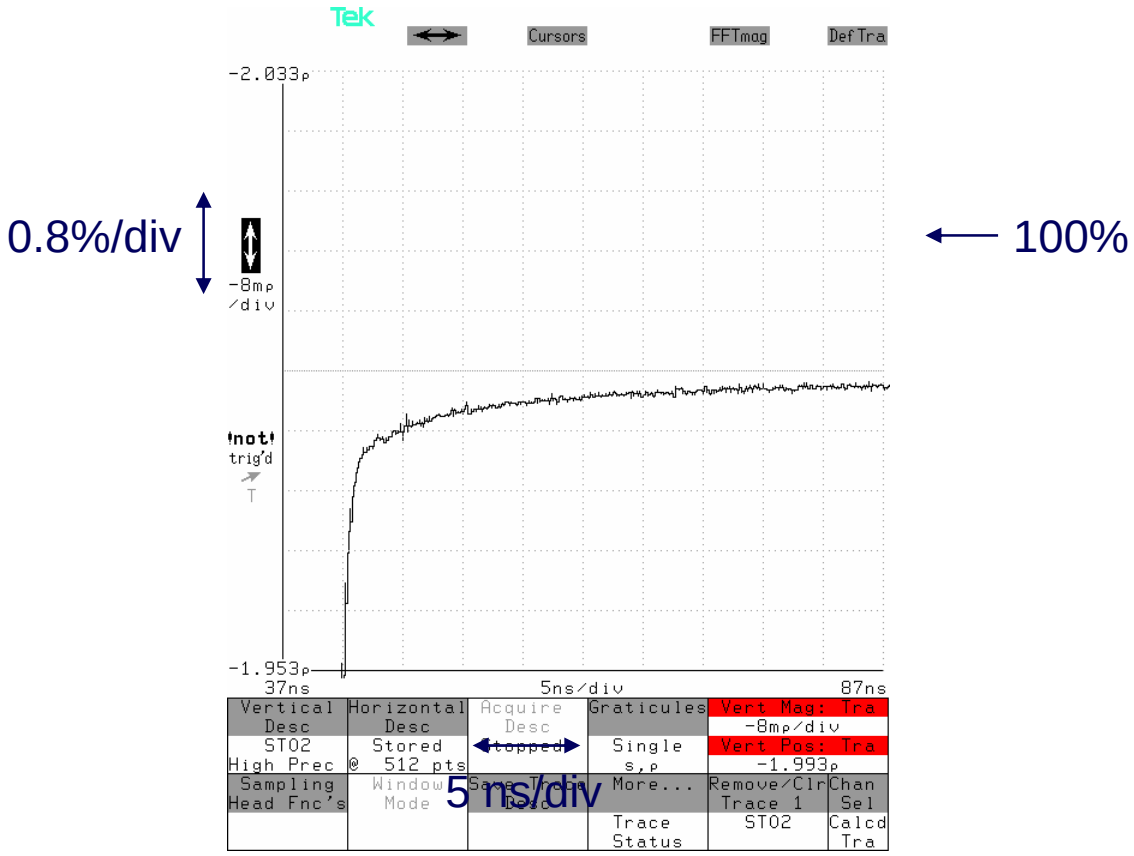
- Employ Full-Mode Terminations - see Differential Transmission Lines
- Keep Mode Velocities Equal by Keeping Dielectric Environment Equal, or Use Buried Runs (Homogeneous)

Transmission Line Losses

- Affects TDR and TDT Measurement
- Loss Mechanisms
  - DC resistive losses
  - Skin effect losses
  - Dielectric losses
  - Coupled losses (crosstalk loss)
- Generally, Skin Effect Losses Dominate at Microwave Frequencies

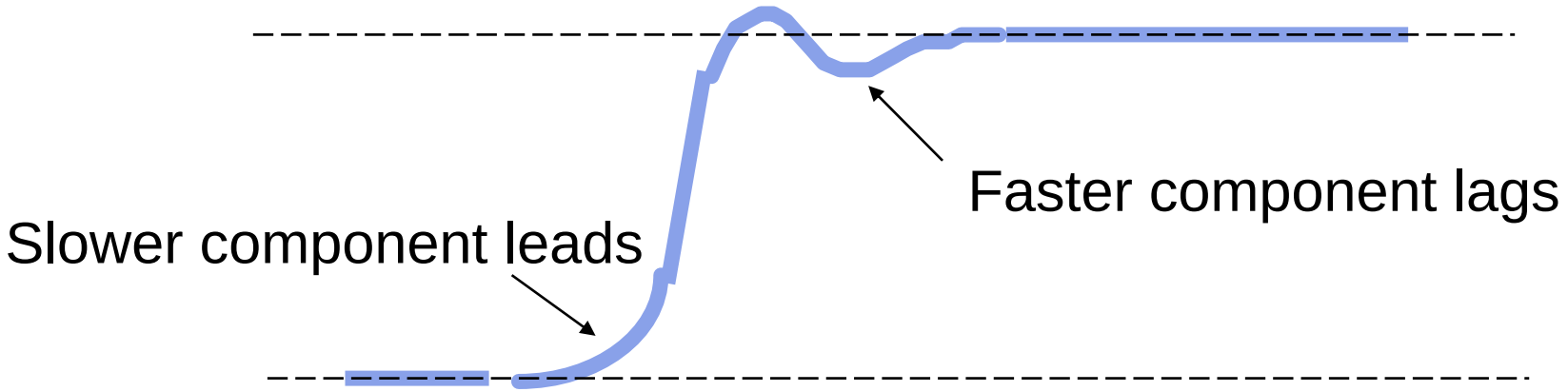
Cable Loss

TDT response of 1 meter RG-58



Transmission Line Dispersion

- Propagation Velocity Changes With Frequency
- Generally Faster Components in Signal Propagate at Slower Velocity
  - Foot or Baseline of Signal has Slow Corner
  - Topline of Signal has Ringing



TDR Alternatives

- Simulation
  - Tools such as Electro provide simulation of impedances for Z-symmetric geometries
  - Real world issues with variations in geometry, dielectric constant, loss tangent, etc. must be included
  - Quick and easy for initial design
  - Once built, use TDR to verify and debug impedances

TDR Alternatives

- Vector Network Analyzer
  - Frequency domain measurement tool
  - Separates and measures incident and reflected energy to device under test
  - S-parameter domain
  - Correlation to TDR waveforms

$$s_{11} = fft\left[\frac{\partial}{\partial t}(TDR\_reflected\_waveform)\right]$$

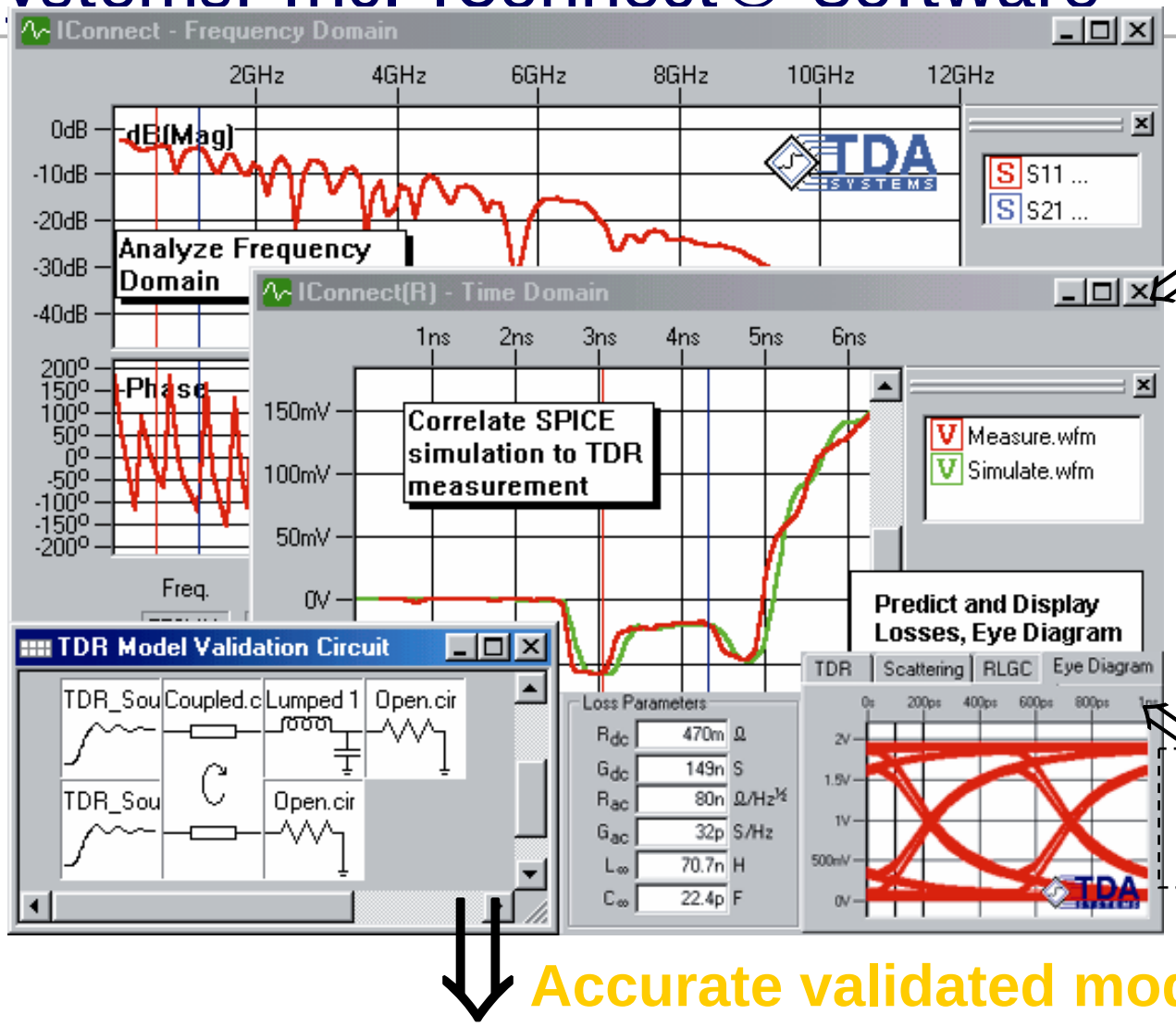
23TDA Systems, Inc. IConnect® Software

- Measure board impedance and propagation delay
  - Analyze failures, resolve smaller discontinuities
- Predict eye diagram degradation using lossy line model and eye-diagram display
- Model crosstalk and jitter in a differential line
- Model reflections and ringing in a trace on a PCB, including connectors, sockets, packages
- Validate models from field solver using IConnect integrated interface to SPICE simulators
- Analyze losses and resonances using S-parameter computation
- Obtain package or connector parasitics

TDA Systems, Inc. IConnect® Software

TDR ⇒

TDS8000



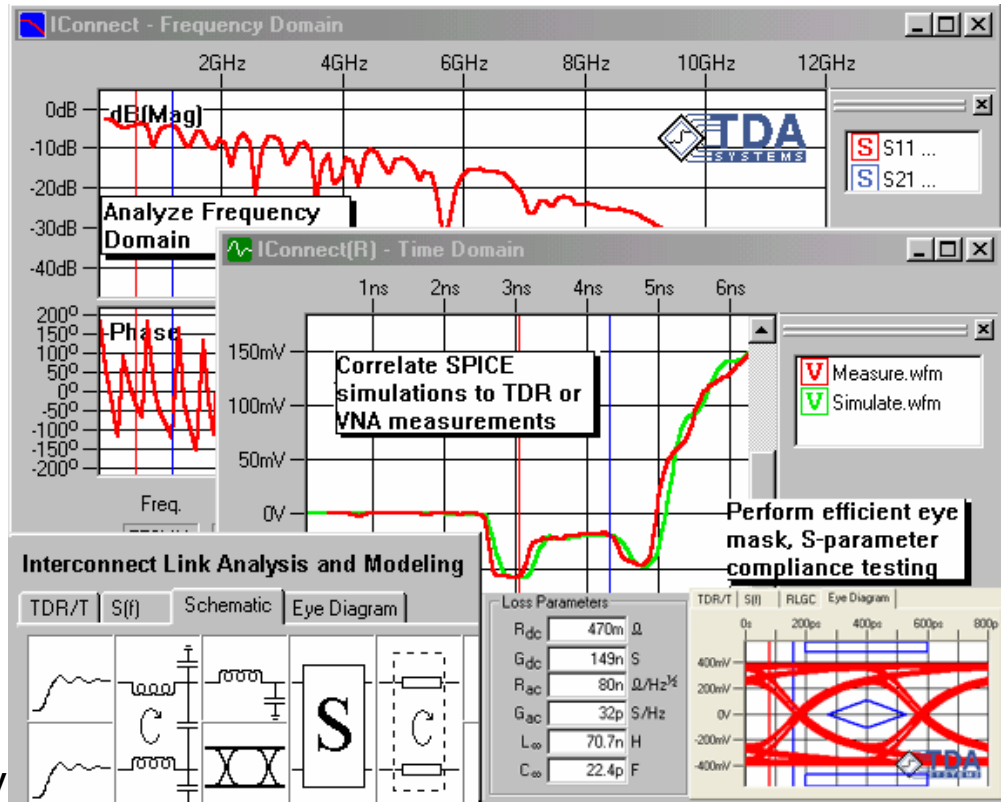
SPICE / IBIS Simulation (HSpice, PSpice BSpice)

Field Solver Analysis

Accurate validated models

What is IConnect®?

- IConnect TDR and VNA software for gigabit digital interconnects:
  - Quick signal integrity SPICE modeling and analysis
  - Easy and accurate S-parameter and eye diagram measurements
    - Electrical compliance testing
  - More accurate impedance measurements
  - Efficient fault isolation and failure analysis
- MeasureXtractor™
  - Automatically convert TDR/T or S-parameter data into exact frequency dependent models
  - Easily ensure SPICE / IBIS simulation accuracy



- *Efficient, easy-to-use and cost-effective!*
- *Works with TDS/CSA8200 TDR scope*

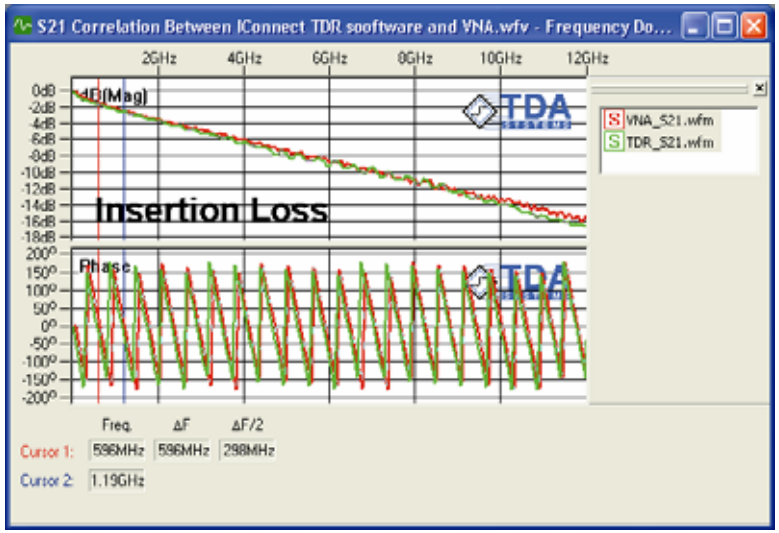
EDN innovation HONORING EXCELLENCE IN ELECTRONICS 2003 FINALIST

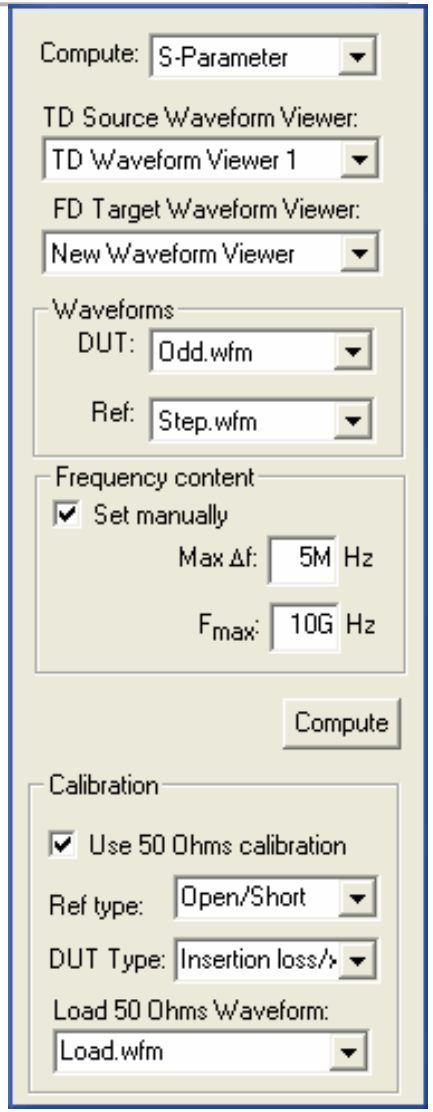
Tektronix®

What is IConnect® S-parameters?

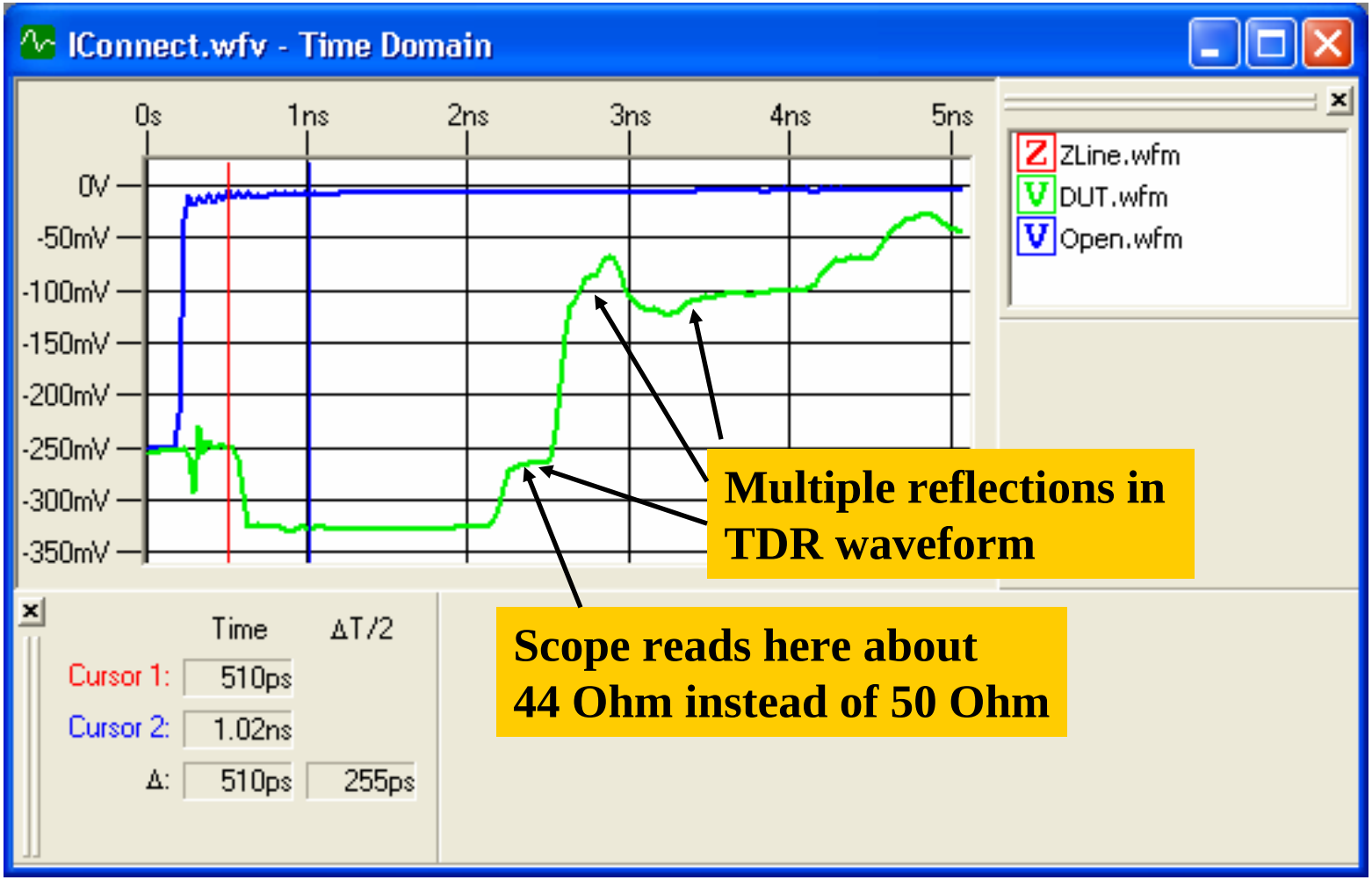
The easiest way to perform S-parameter measurements for digital interconnects

- Differential, mixed mode, single ended
- Compliance testing for PCI-Xpress, Serial ATA, Infiniband, Gigabit Ethernet and other standards
- Easily de-embed fixture effects
- Basic calibration capability

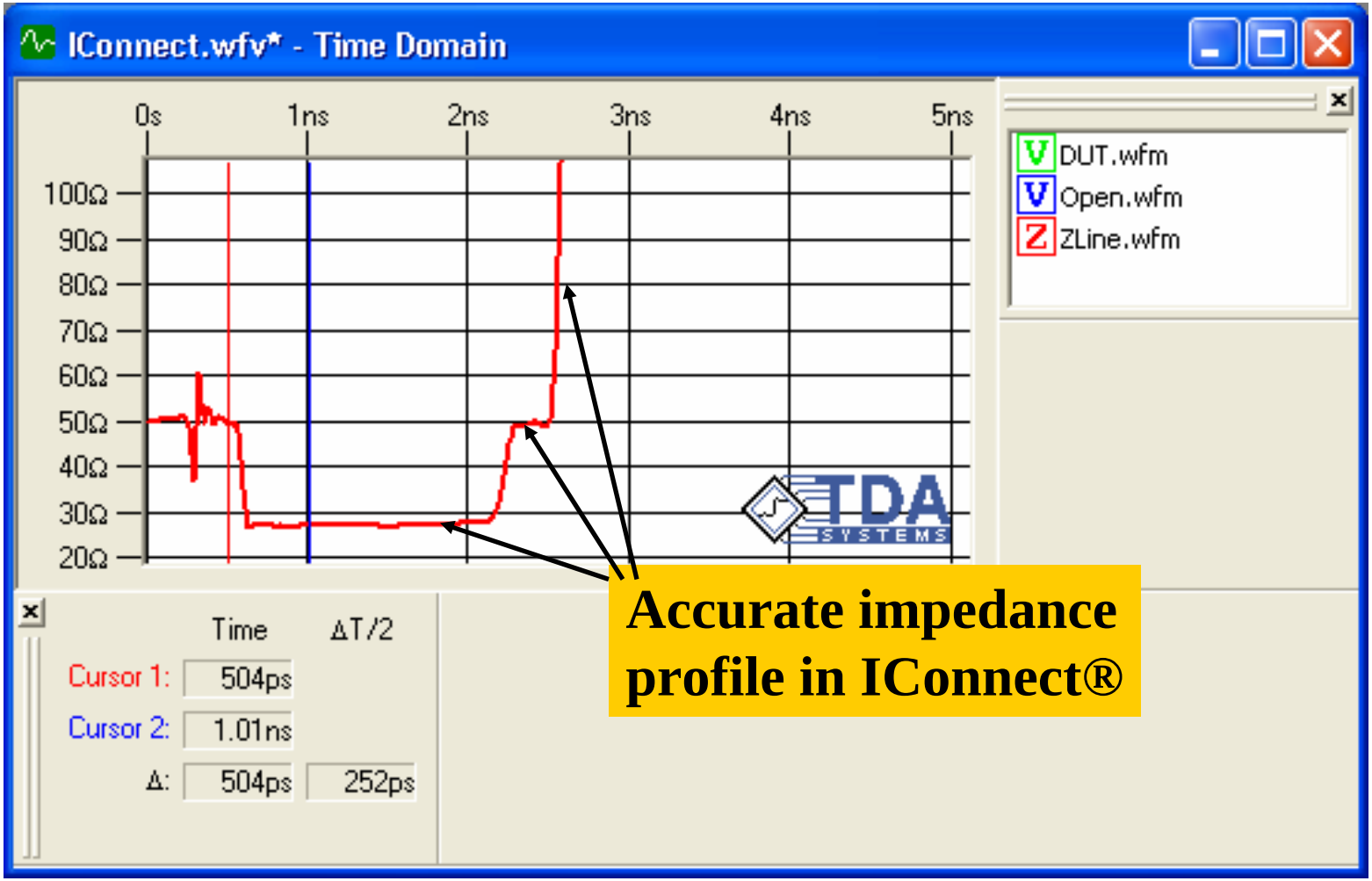




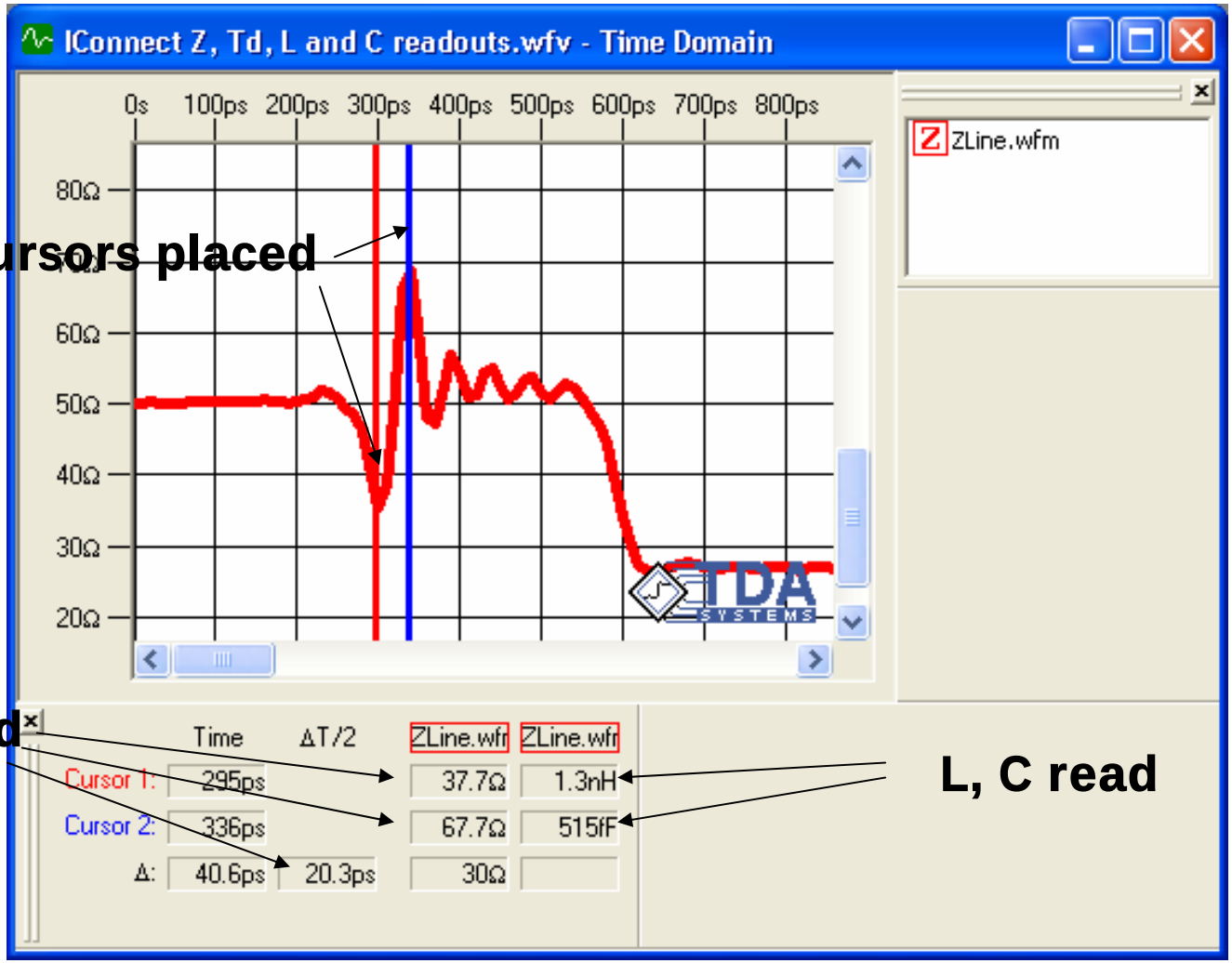
Board Trace IConnect® Z-line



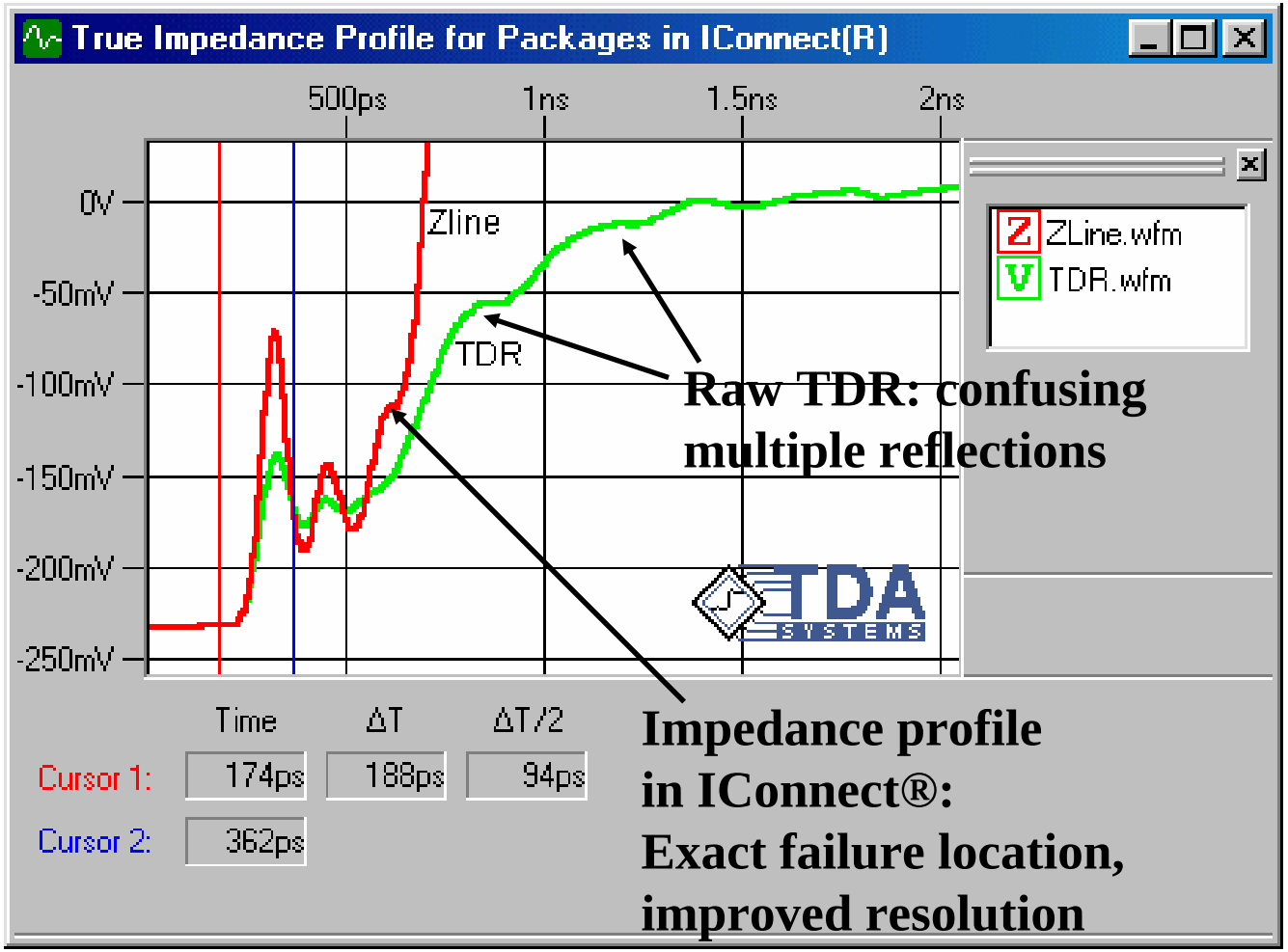
Board Trace IConnect® Z-line



Impedance, Inductance and Capacitance Readouts



Package Trace Failure Analysis

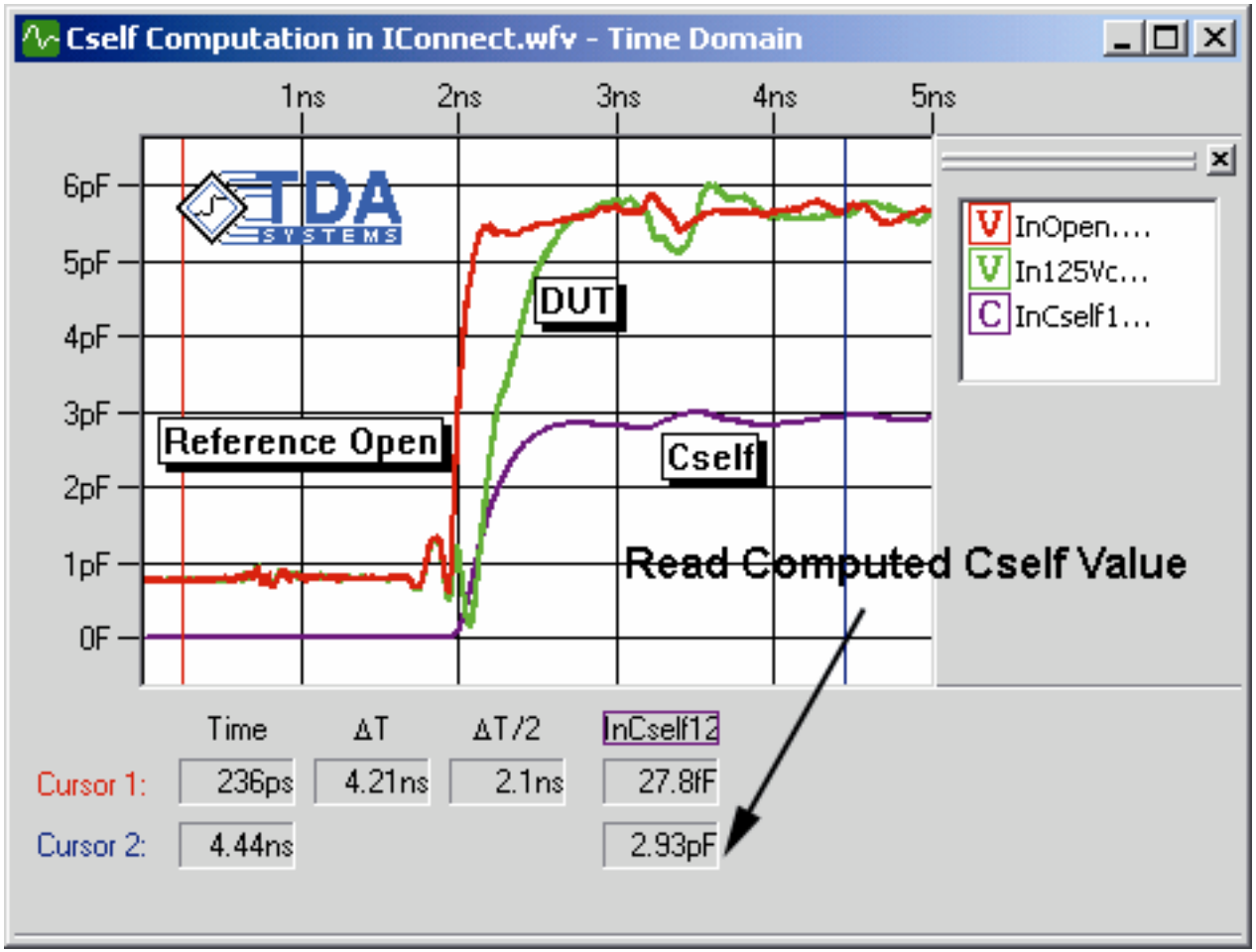


Z-line Applications and Benefits

- What does Z-line do?
  - Corrects for multiple reflections inside the DUT, which produce impedance inaccuracies
- Benefits:
  - Avoid accuracy and disputes with vendors/customers through improved accuracy and repeatability for PCB impedance measurements
    - Both in manufacturing and in PCB technology development
  - Locate package, board and connector failures faster through improved resolution
  - Get quick access to direct Z, td, L and C readouts from the corrected impedance profile

Input Die Capacitance Measurement

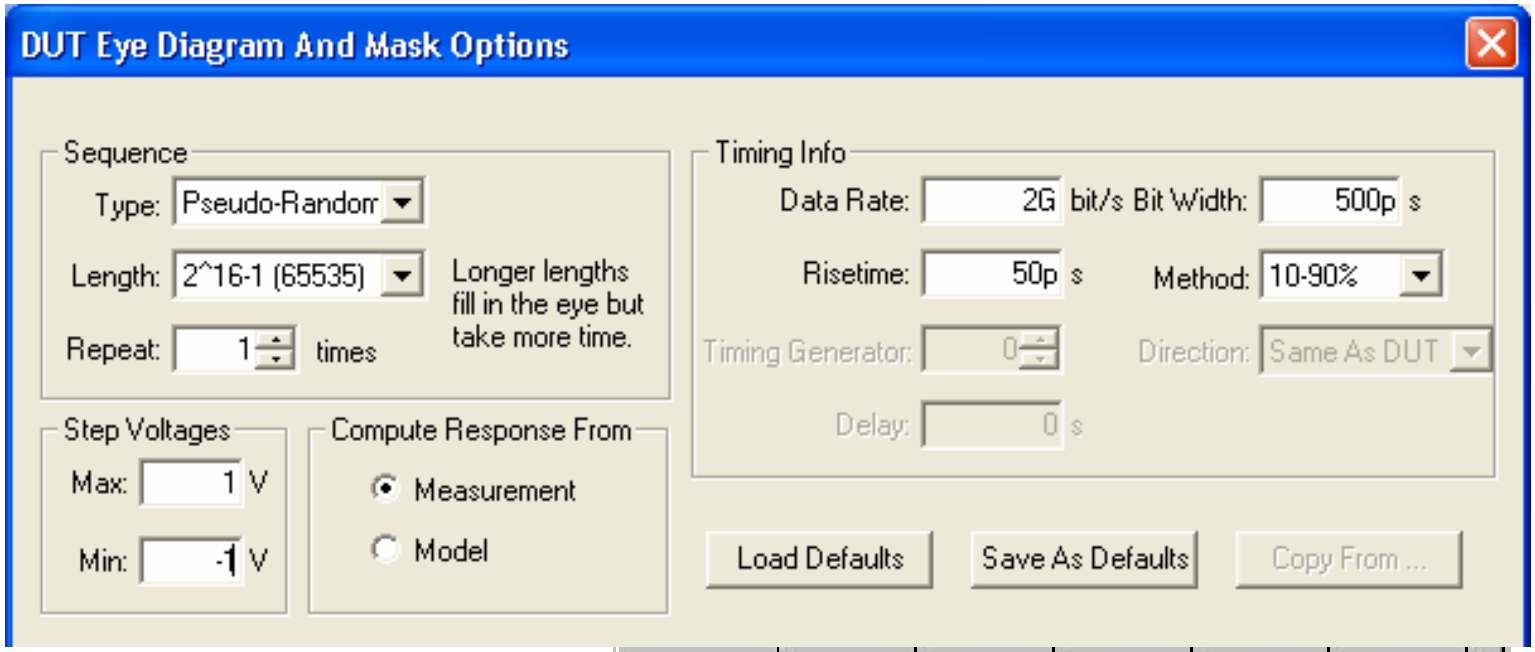
- Measure an empty fixture
- Measure fixture with DUT inside
- IConnect computes Cself based on the difference
- The same process applies to package or socket capacitance



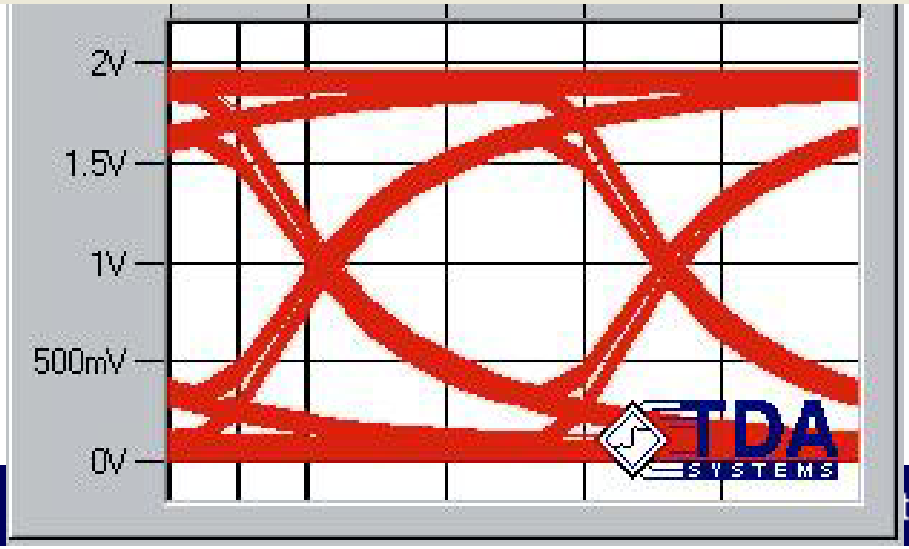
Cself Applications and Benefits

- What does Cself/mutual, Lself/mutual computation do?
  - Computes the appropriate values using JEDEC-established industry standard (JEDEC publication JEP-123) for short interconnects
- Benefits
  - Efficient and quick measurement of input die and package capacitance
    - A standard method in the semiconductor industry
    - Measurements of the Cdie in powered-up condition possible
      Appnote: “Measurement of Input ... Die Capacitance ... Using TDR”
  - Method is also efficiently applied to...
    - Small-size package, connector and socket modeling
    - Measuring inductance of a via on the board

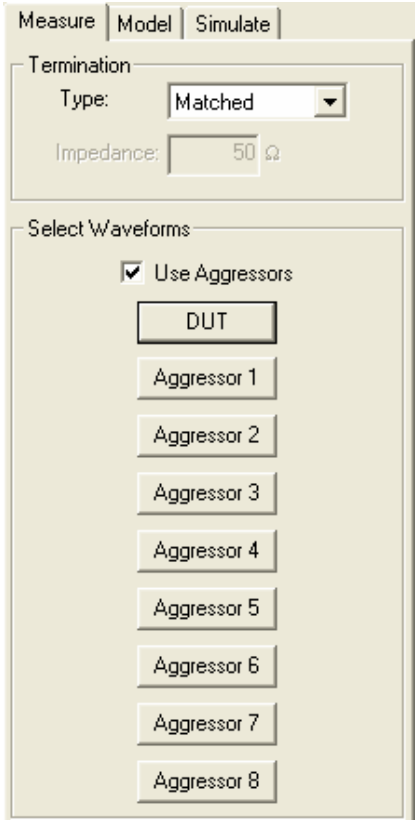
Eye Diagram In IConnect

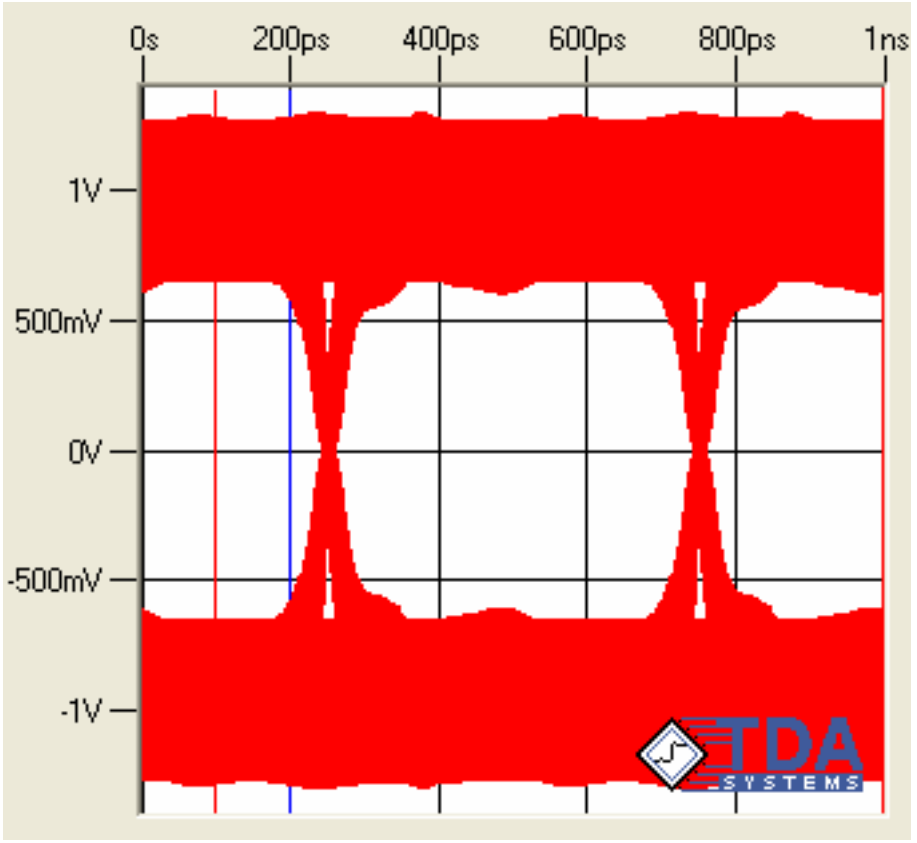


- TDT easily gives the eye diagram degradation
  - Deterministic jitter only
  - Eye degradation due to system losses, ISI, reflections



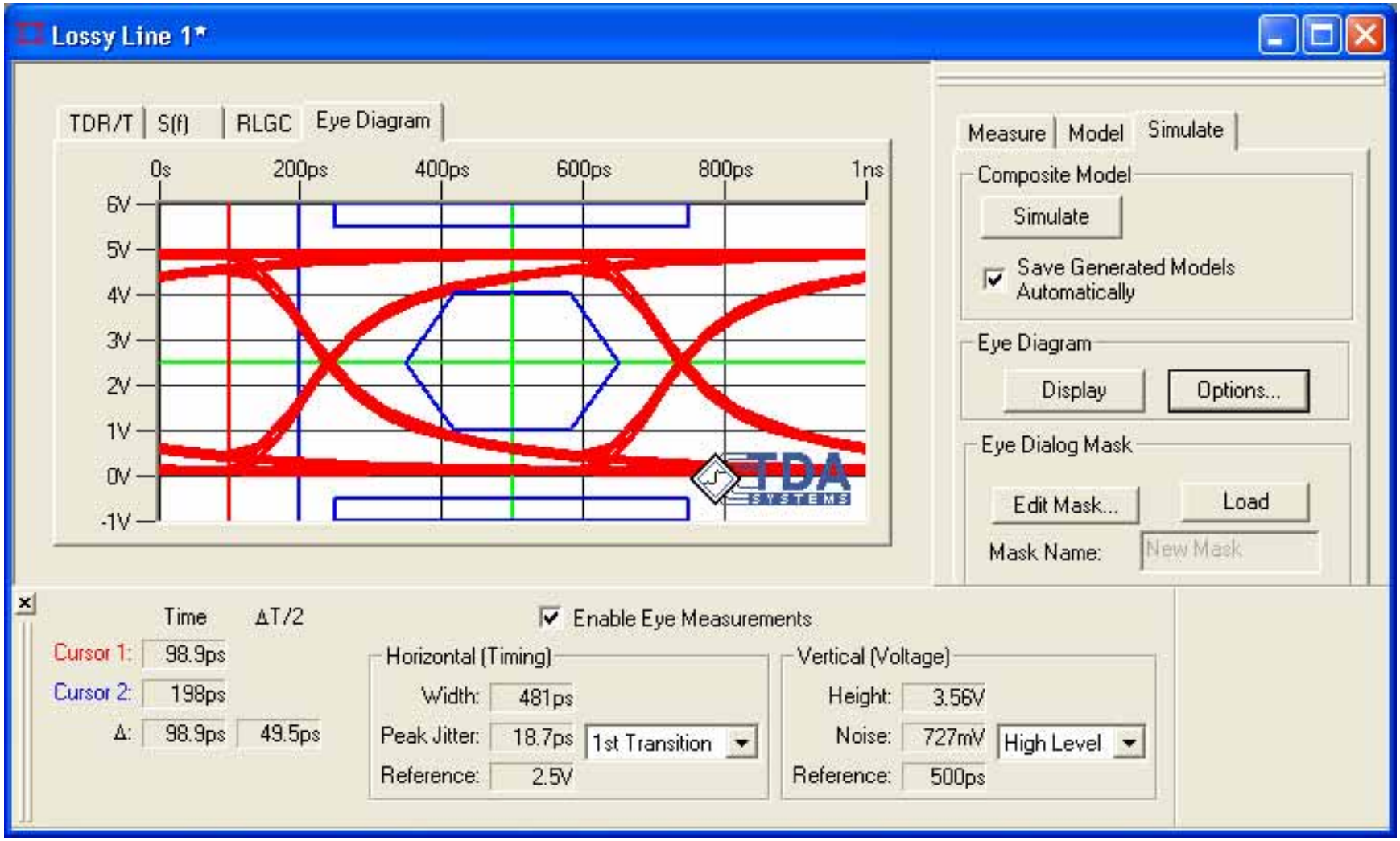
Crosstalk Effects



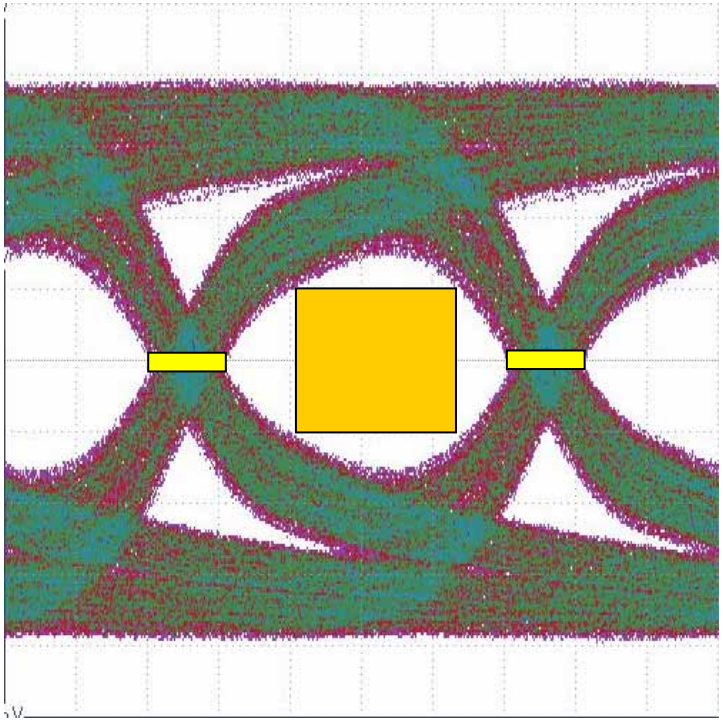


- Up to 8 aggressors can be defined (think center pin and 8 pins around)
- Aggressor signals can propagate in the same or opposite direction as the victim, and can have completely independent timing (datarate etc.)

Eye Mask and Jitter Measurements

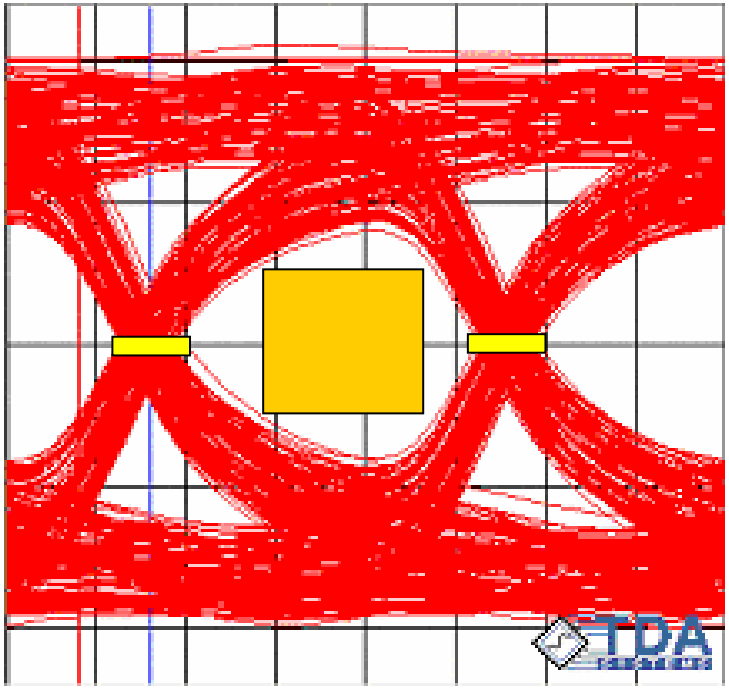


Correlation



2^10-1 pattern generator measurement

Data courtesy FCI Electronics



2^10-1 IConnect eye from TDT measurement

IConnect Eye Applications and Benefits

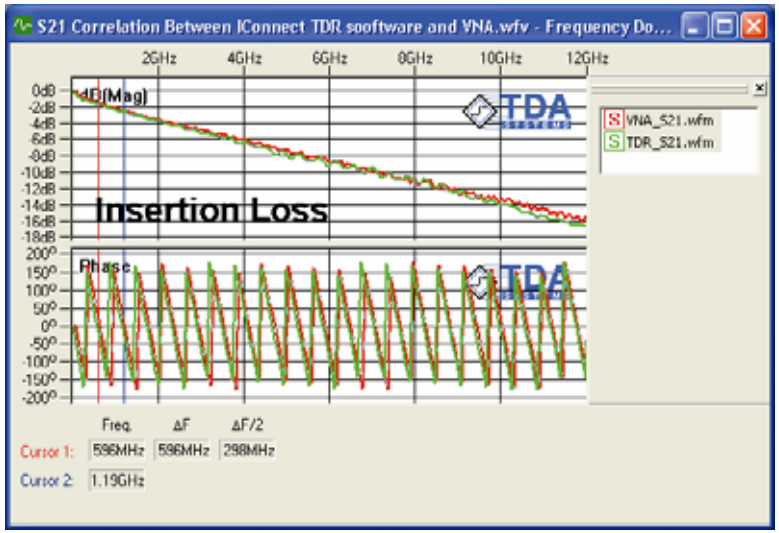
- What does IConnect eye diagram do it do?
  - Generates an eye for passive interconnect link – includes crosstalk!
  - Place standard mask, perform peak-to-peak jitter and eye opening measurements
- Benefits:
  - Efficient compliance testing for cable assemblies: (SATA, PCI Xpress, Infiniband, Gigabit Ethernet) - save time and money!
    - No pattern generator (PG) required (at 10 Gbit/sec PG can cost >>$100k vs. <$20k for IConnect!)
    - Save time: an eye is generated 100x faster than with PG!
    - Leverage your TDR oscilloscope investment and save test space
  - Quick isolation of system level problem – rapidly determine whether system performance is poor due to transmitter or to interconnect link
  - Quick evaluation of maximum performance for a legacy backplane

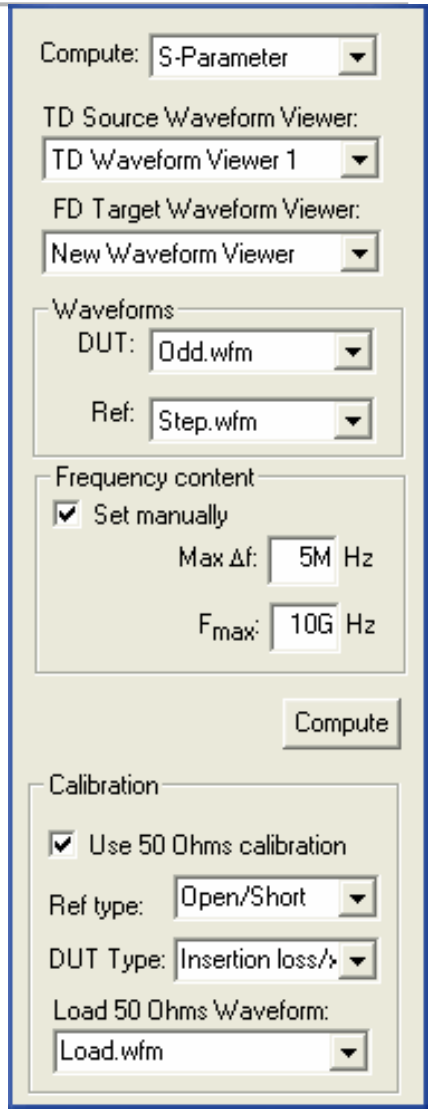
New!

IConnect® S-parameters

The easiest way to perform S-parameter measurements for digital interconnects

- Differential, mixed mode, single ended
- Compliance testing for PCI-Xpress, Serial ATA, Infiniband, Gigabit Ethernet and other standards
- Easily de-embed fixture effects
- Basic calibration capability





IConnect S-parameter Uniqueness

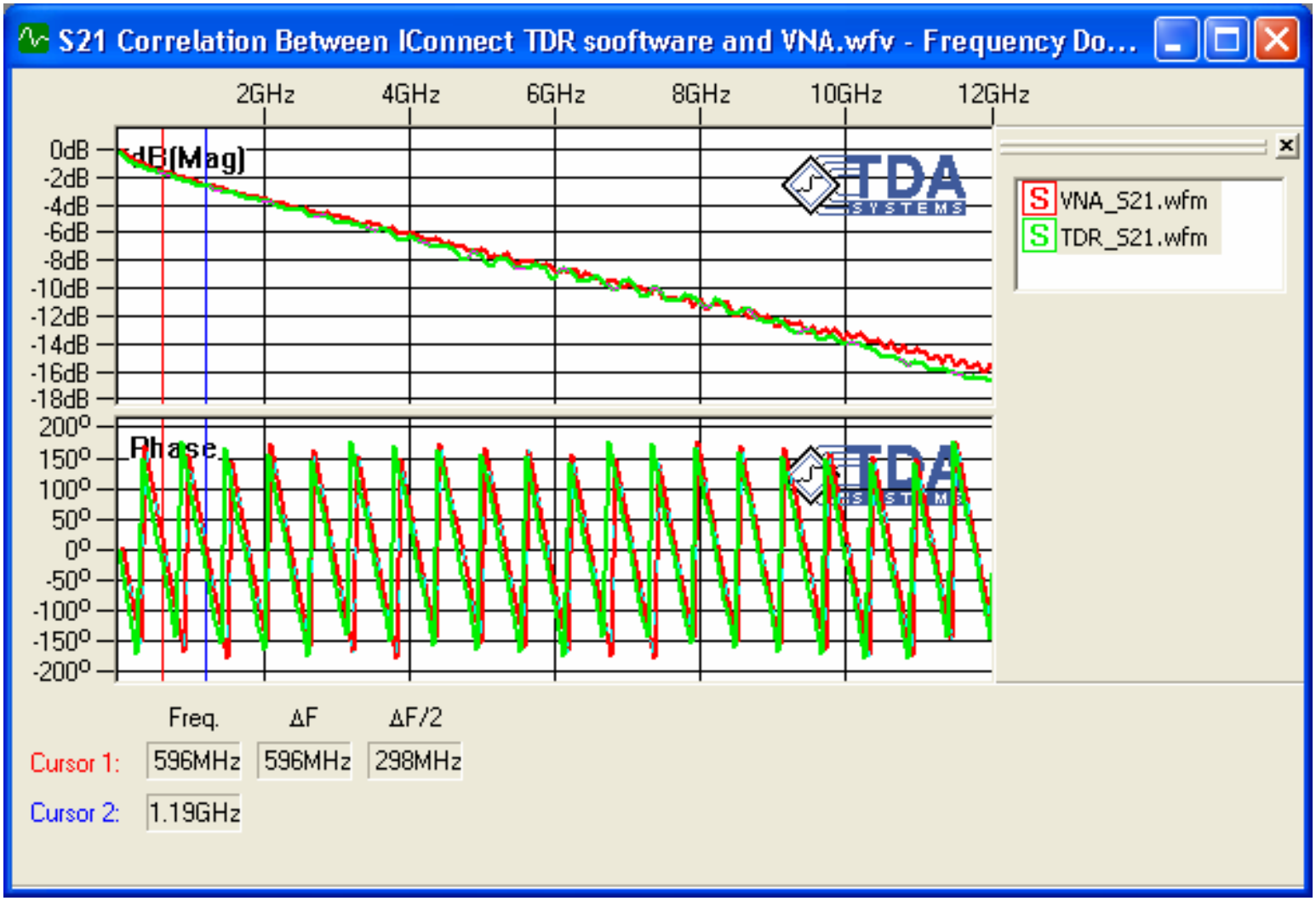
- How do you measure differential return loss of a DUT when it is soldered on the board? – with IConnect using short reference!
  - Short the two pins of the DUT package with an Xacto knife – and you have a short reference to compute S-parameters
  - **You can not do this otherwise!**
- How do you de-embed the measurement fixture for electrical compliance testing? – with IConnect!
  - Simply use the existing through calibration structure on the board, or even an open reference with DUT disconnected, and you are done!
- In any application where you precision cal kits at the DUT reference plane are unavailable, IConnect will solve the problem
- Nothing is faster and easier to use than IConnect S-parameters for a quick single S-parameter measurement of an interconnect

Choose Your Instrument: VNA Cost is 2X

	TDR instrument	VNA instrument
t_r < 80ps f < 9Ghz Datarate[1] < 6 Gbit/s	20 Ghz TDS8200 with 80E04 TDR	9 Ghz differential system
80ps<t_r<35ps 9Ghz<f<20Ghz Datarate[1] < 12.5 Gbit/sec	20 Ghz TDS8200 with 80E04 TDR; add-on calibration desired	20 Ghz differential system
15ps<t_r<35ps 20Ghz<f<50Ghz Datarate[1] < 30 Gbit/sec	TDS8200 with 80E04 with PPL 4022 and 80E06 70 Ghz module	50 Ghz differential system
9ps<t_r<15ps 20Ghz<f<50Ghz Datarate[1] < 40 Gbit/sec	TDS8200 with 80E04 with PPL 4022 and 80E06 70 Ghz module	50 Ghz differential system (9ps t_{rise} can't be achieved)

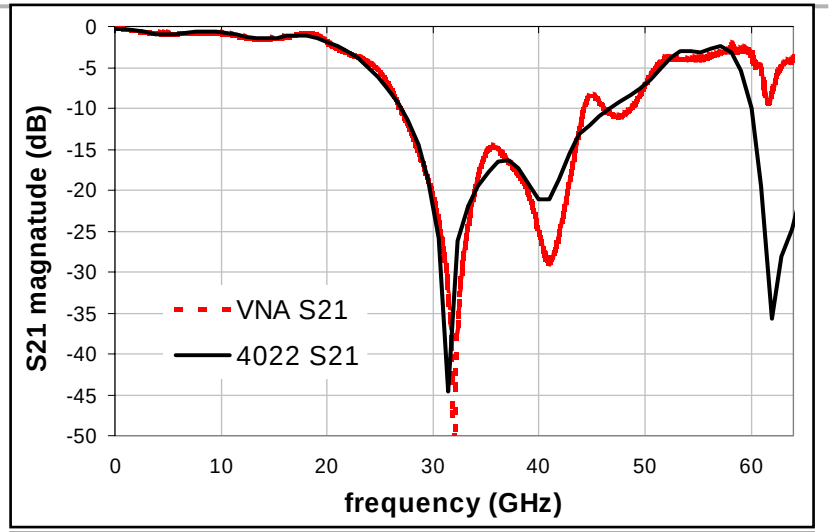
1 - Analysis to approximately 3d clock harmonic

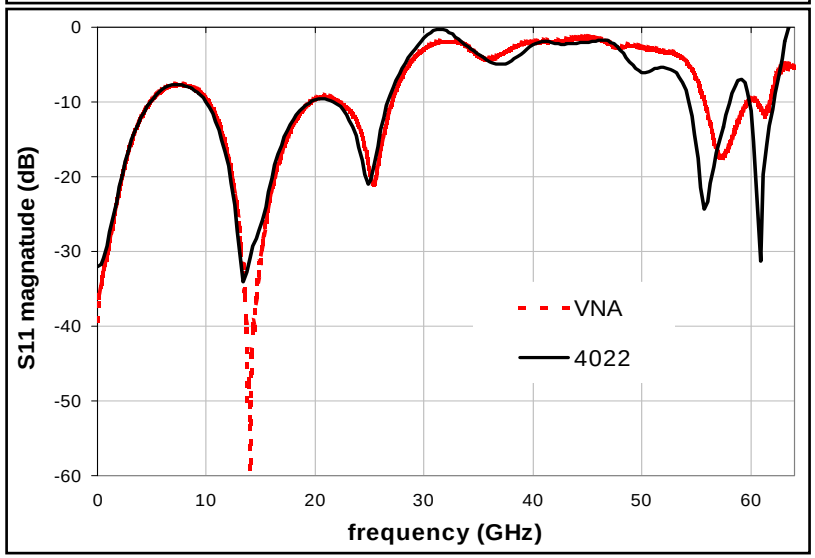
Correlation with Network Analyzer



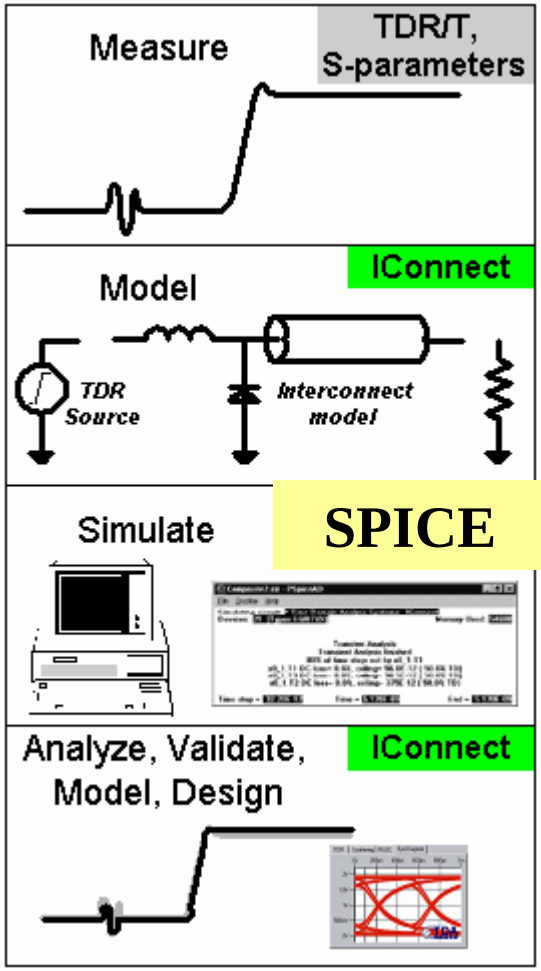
Correlation with Network Analyzer: 65 Ghz

- The TD-VNA bandwidth is directly related to TDR/T rise time
- These data were measured using the PSPL Model 4022 and a 70 GHz sampler
- S-parameters correlate to 65 GHz
- Courtesy: Kipp Schoen, Picosecond Pulse Labs



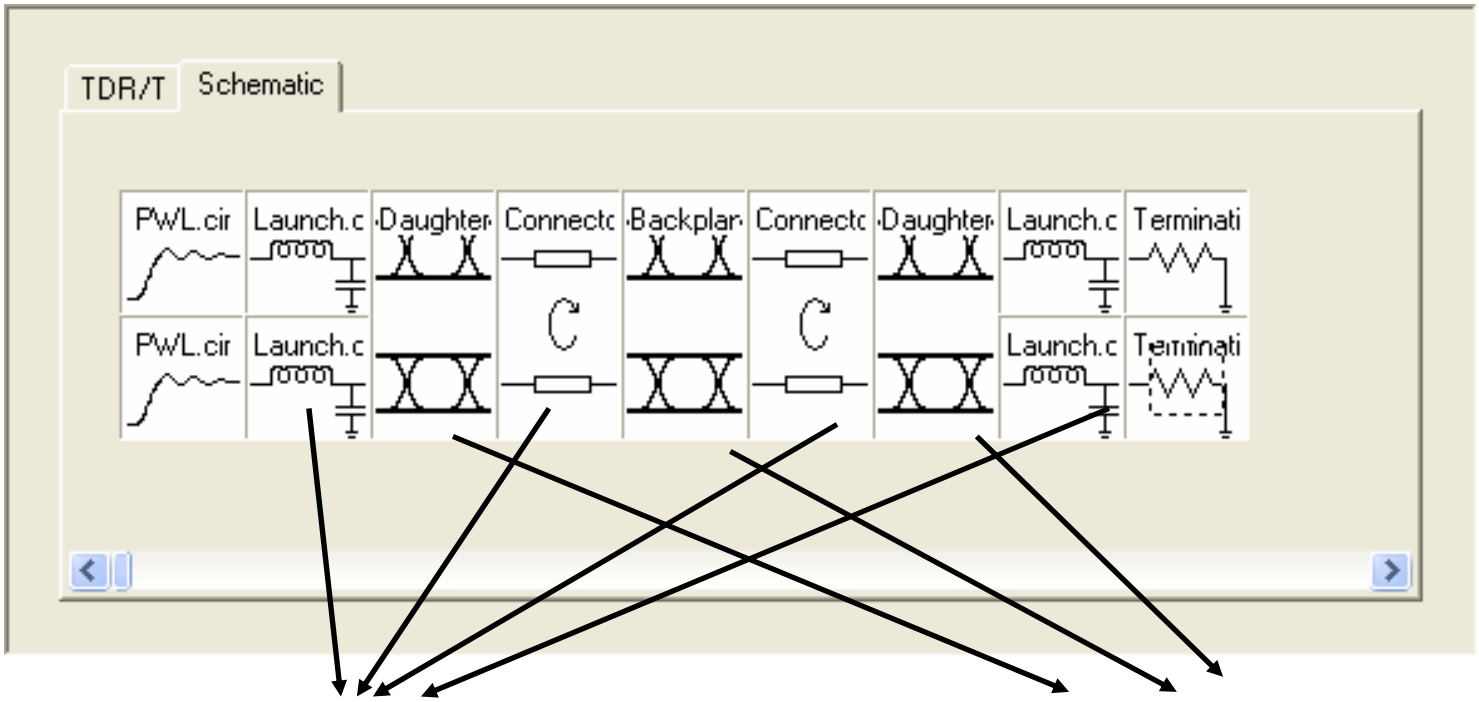


Measurement Based Approach



- **TDR/T or VNA Measurements**
- **Extracted interconnect, instrument source models**
- **Direct link to simulators**
- **Automatic comparison of simulation and measurement in IConnect waveform viewer**

Methodology: Gbit Ethernet Example



Launch, high-speed connector: Z-line modeling

Backplane and daughter cards: lossy line modeling

Any piece can be modeled in MeasureXtractor™

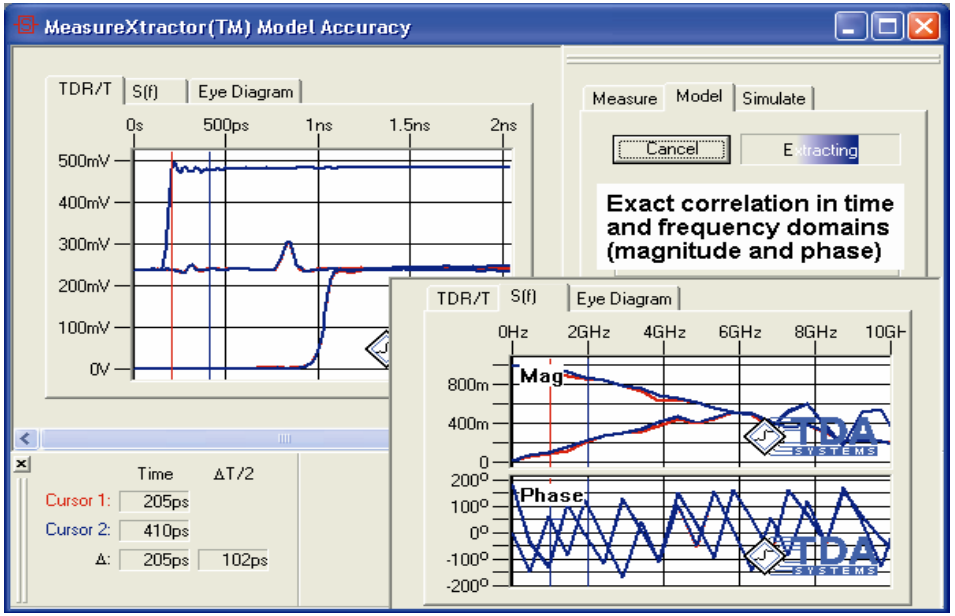
Lumped pieces can be modeled with JEDEC technique

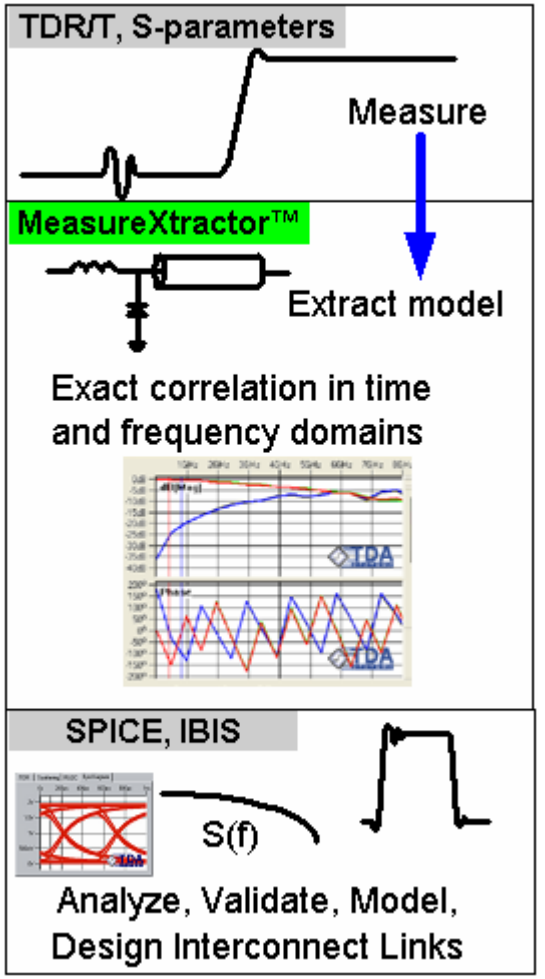
EDN innovation HONORING EXCELLENCE IN ELECTRONICS 2003 FINALIST

MeasureXtractor™

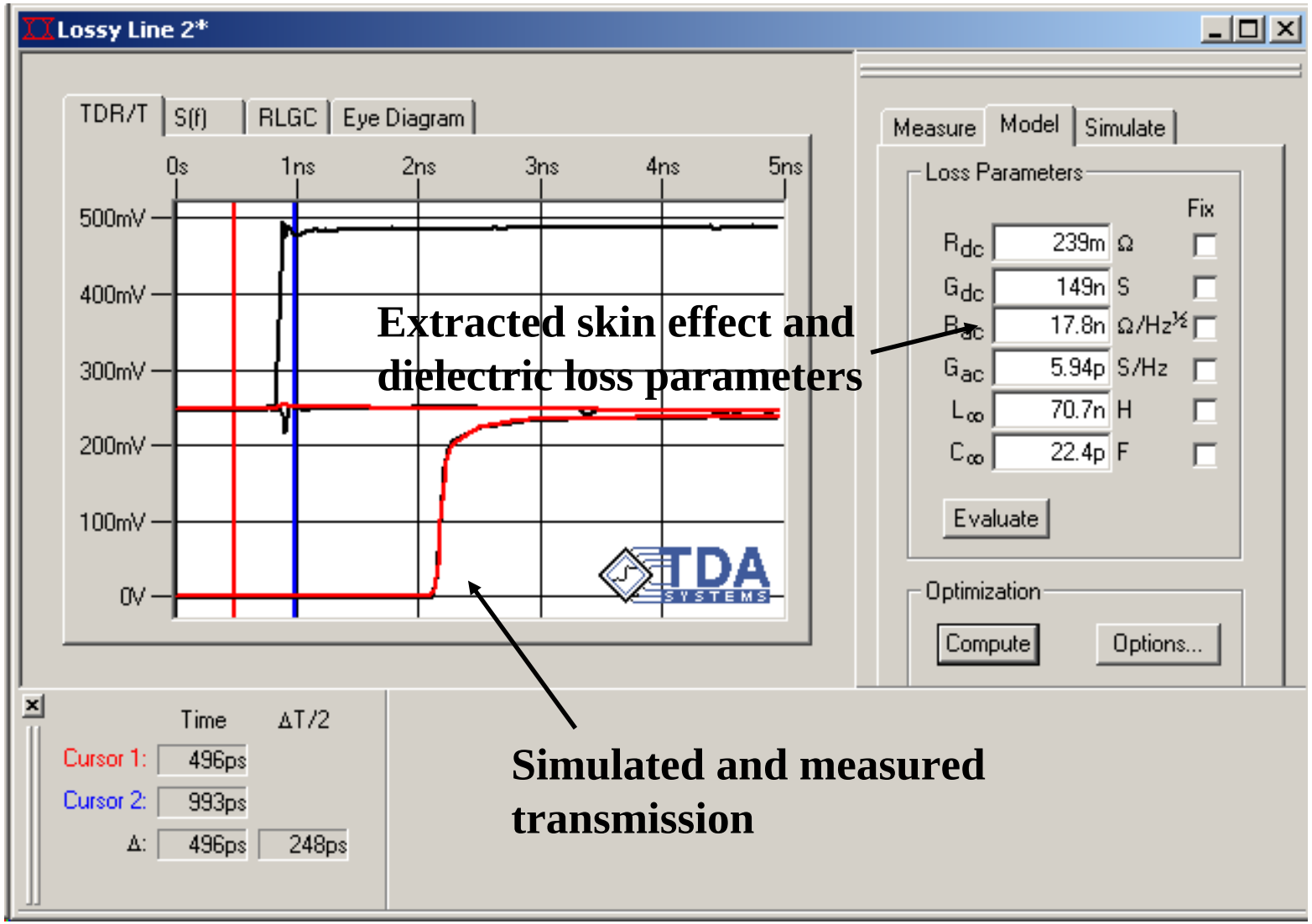
The fastest path from VNA or TDR measurements to simulations

- Exact SPICE / IBIS models
- Automatic model generation
- Measurement based
- Frequency dependent
- PASSIVITY, STABILITY, CAUSALITY ensured

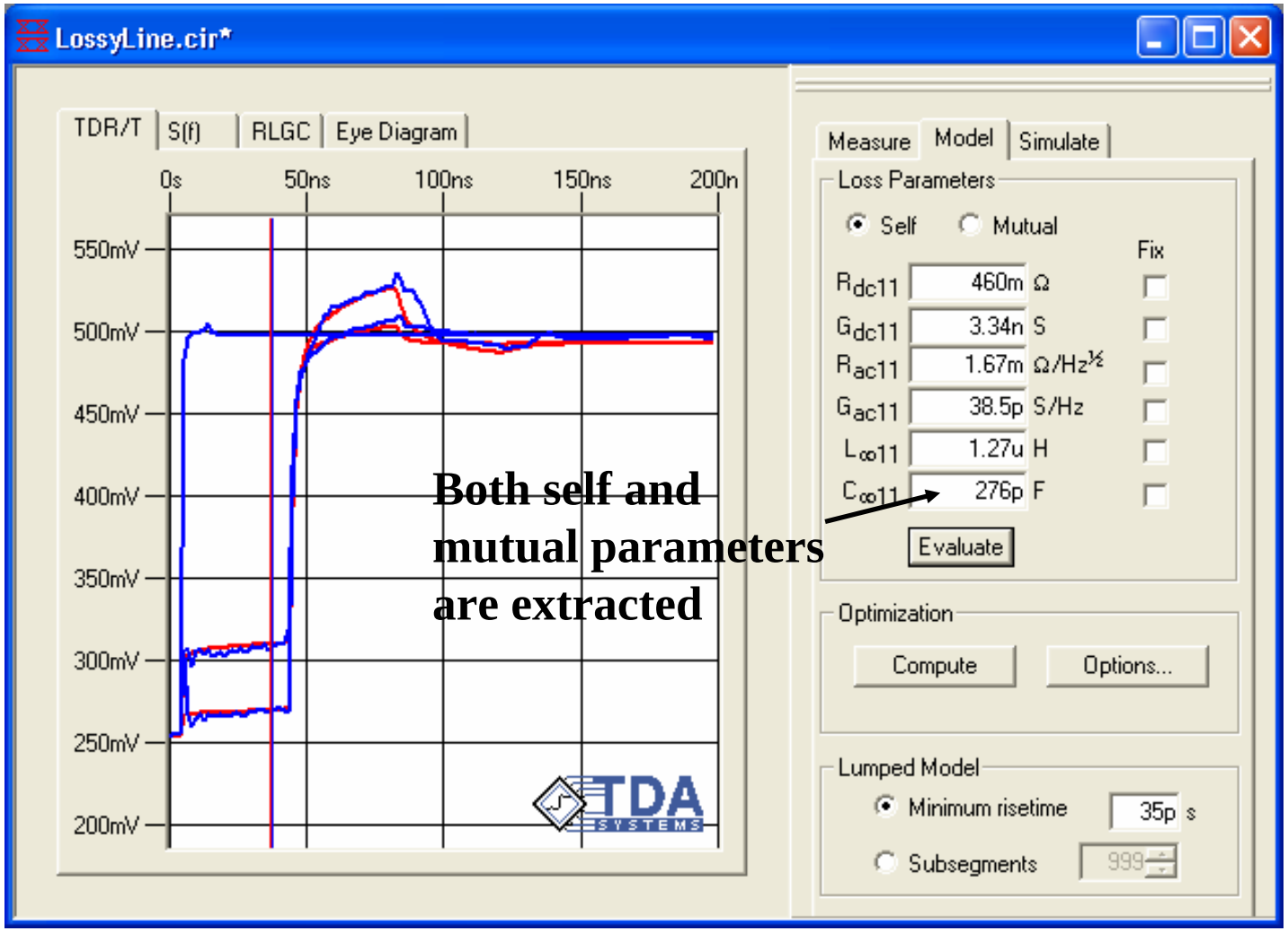




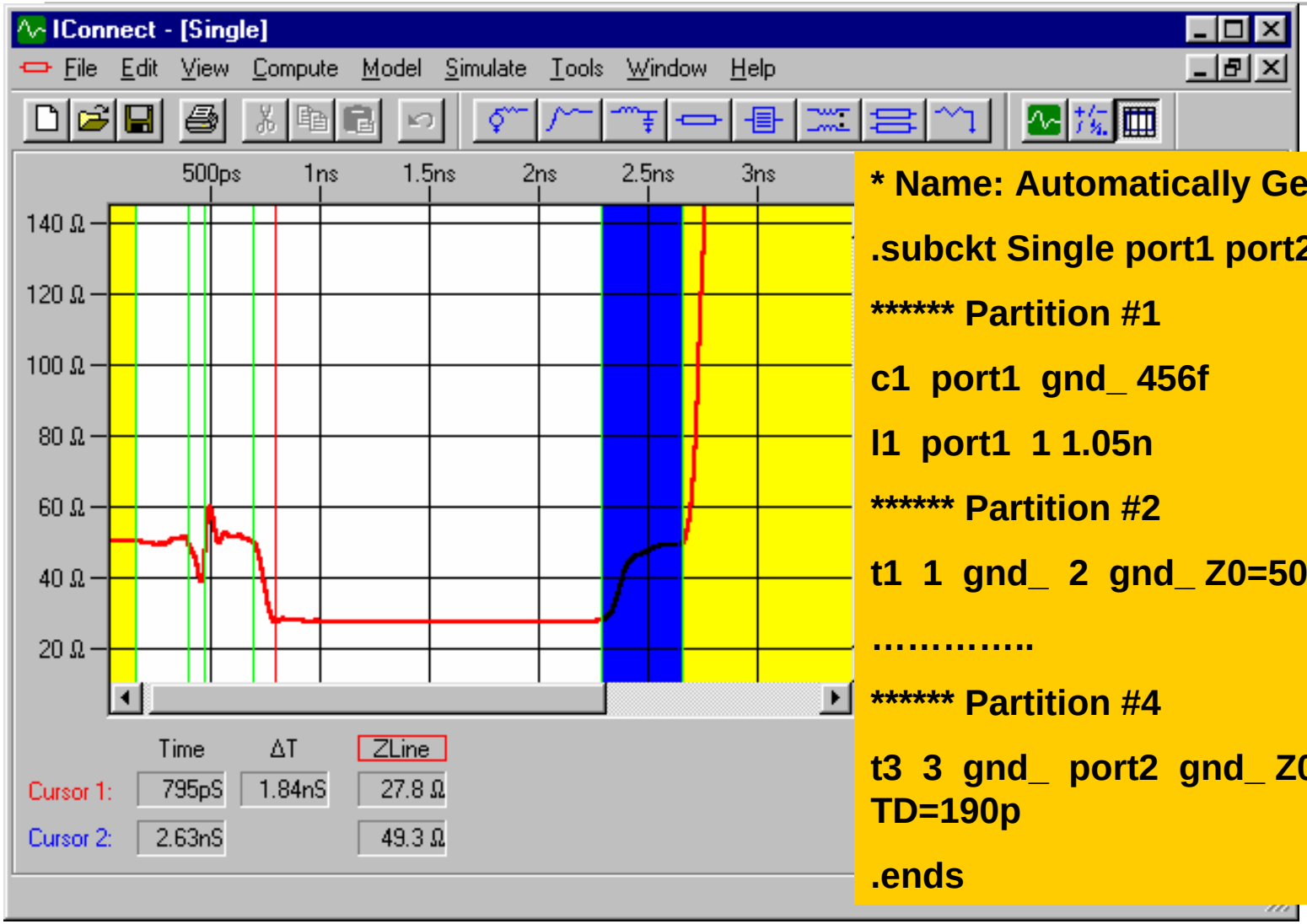
Loss Extraction Results (Transmission)



Loss Extraction Results (Reflection, Coupled)



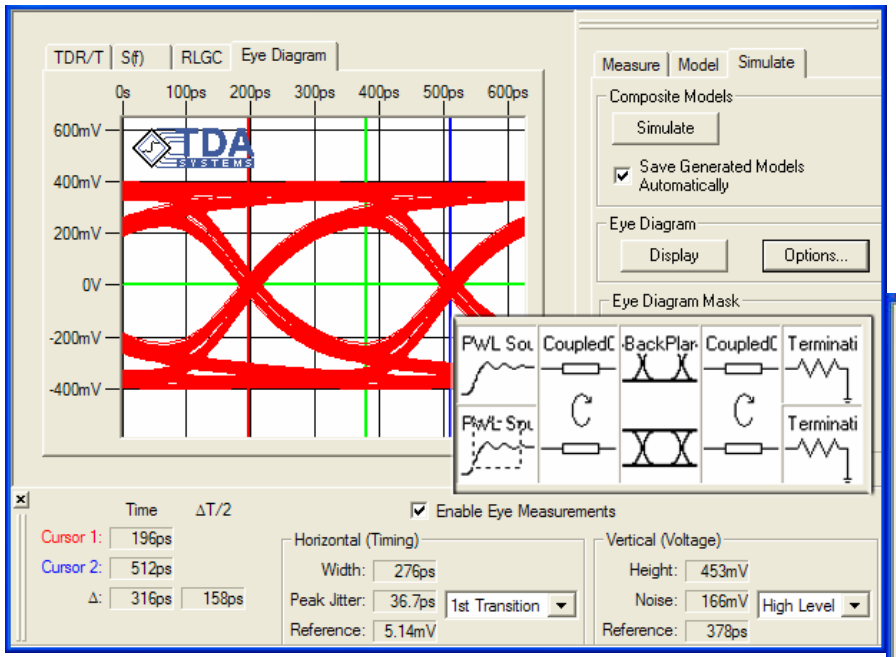
Z-line Modeling in IConnect TDR Software



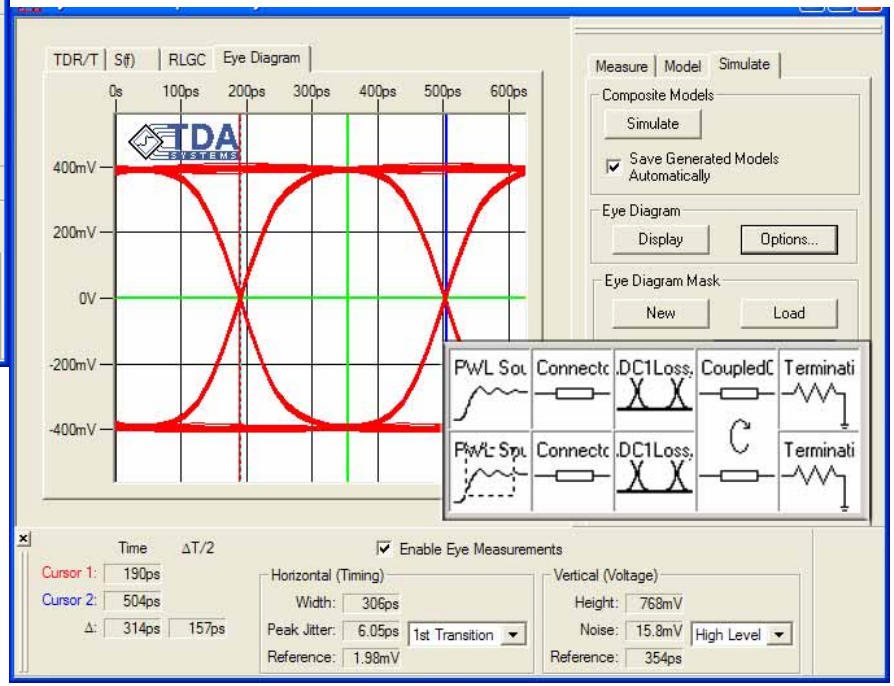

```
* Name: Automatically Generated
.subckt Single port1 port2 gnd_
****** Partition #1
c1  port1  gnd_ 456f
l1  port1  1 1.05n
****** Partition #2
t1  1  gnd_  2  gnd_ Z0=50.8 TD=125p
……..
****** Partition #4
t3  3  gnd_  port2  gnd_ Z0=48.2
TD=190p
.ends
```

Results: Selective Jitter De-embedding

Backplane Only Simulated Eye



Daughtercard Only Simulated Eye



Thanks for attend TDR seminar

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