FIRST-PASS SYSTEM SUCCESS

APPLICATION WORKSHOPS FOR HIGH-PERFORMANCE ELECTRONIC DESIGN

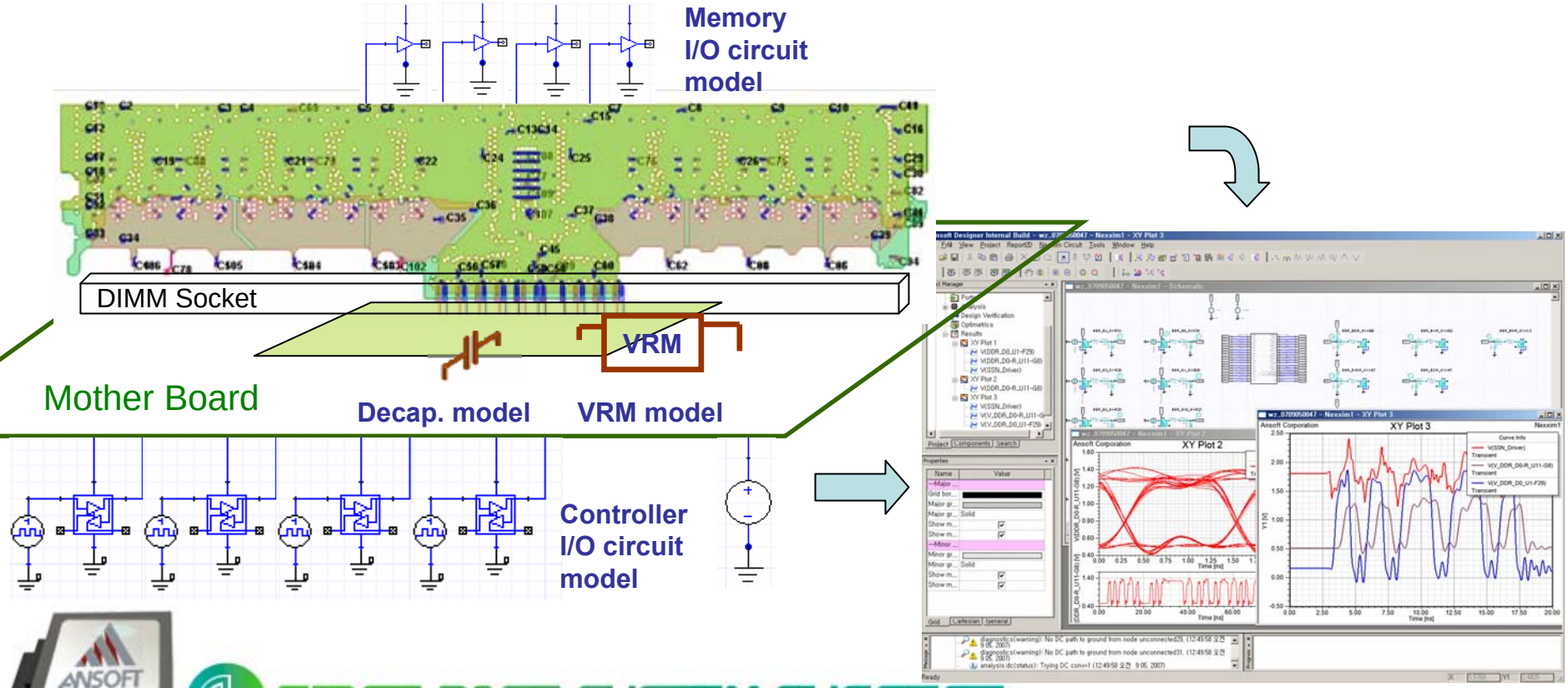
"EM-Circuit Co-Design Solution for High-speed Memory Applications"

Presenter:

Ansoft Corporation

EM-based Circuit Co-design Enables First-Pass Memory System Success

- Nexxim ® : Co-Design Environment with IC chip, PCB module, Socket/Connector and System Board



Outline

- High Speed Memory System
  - First-Pass Memory System Success
  - Design Issues
- High Speed Memory System Analysis
  - SSN/Eye Analysis Example
  - Impedance Analysis Example (DDR3 RDIMM)
- Introducing: Memory system virtual test wizard
  - SSN/ Eye Diagram Analysis
- Summary

First-Pass Memory System Success

Achieve First-Pass high-speed memory system success with full channel simulation

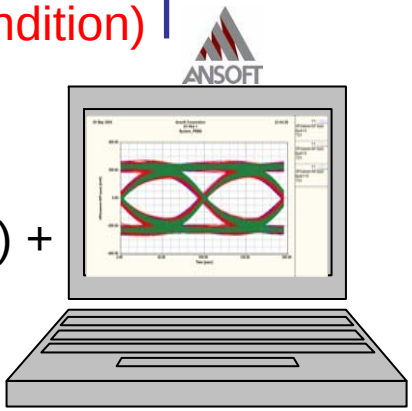
System Design
-Performance
-Topologies
-Feasibility
-DFM
-Spice simulation

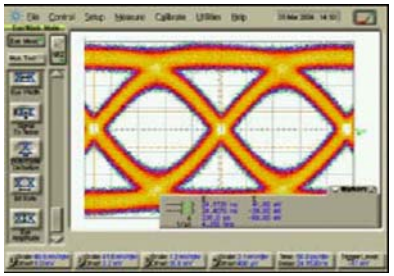
Manufacture
Test& Meas.

First Pass

Tuning & Optimization
(in worst cast condition)

EM based model (Connector/PCB) +
Circuit : Full Channel simulation



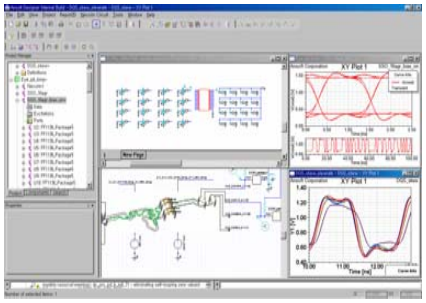


SSN, Jitter, Skew
TDR
Decap. tuning
Cavity resonance
EMI

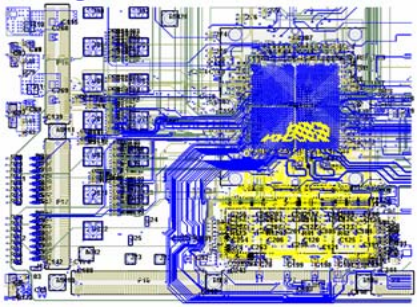
FIRST-PASS SYSTEM SUCCESS
APPLICATION WORKSHOPS FOR HIGH-PERFORMANCE ELECTRONIC DESIGN

Design Suite for High-speed Memory Applications

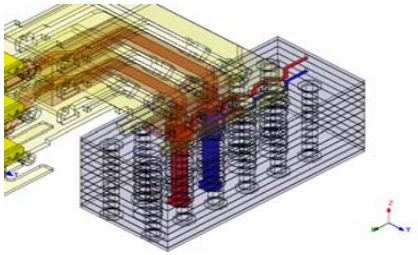
- Nexxim® : Design environment for memory systems
  - Frequency and time domain circuit analysis
  - Co-simulation and dynamic link
  - Optimization and Tuning



- SIwave™ : PCB and Package EM analysis and modeling
  - S-parameter extraction for bus lines
  - Export SPICE sub-circuit
    (HSPICE or Full-wave s-element model)

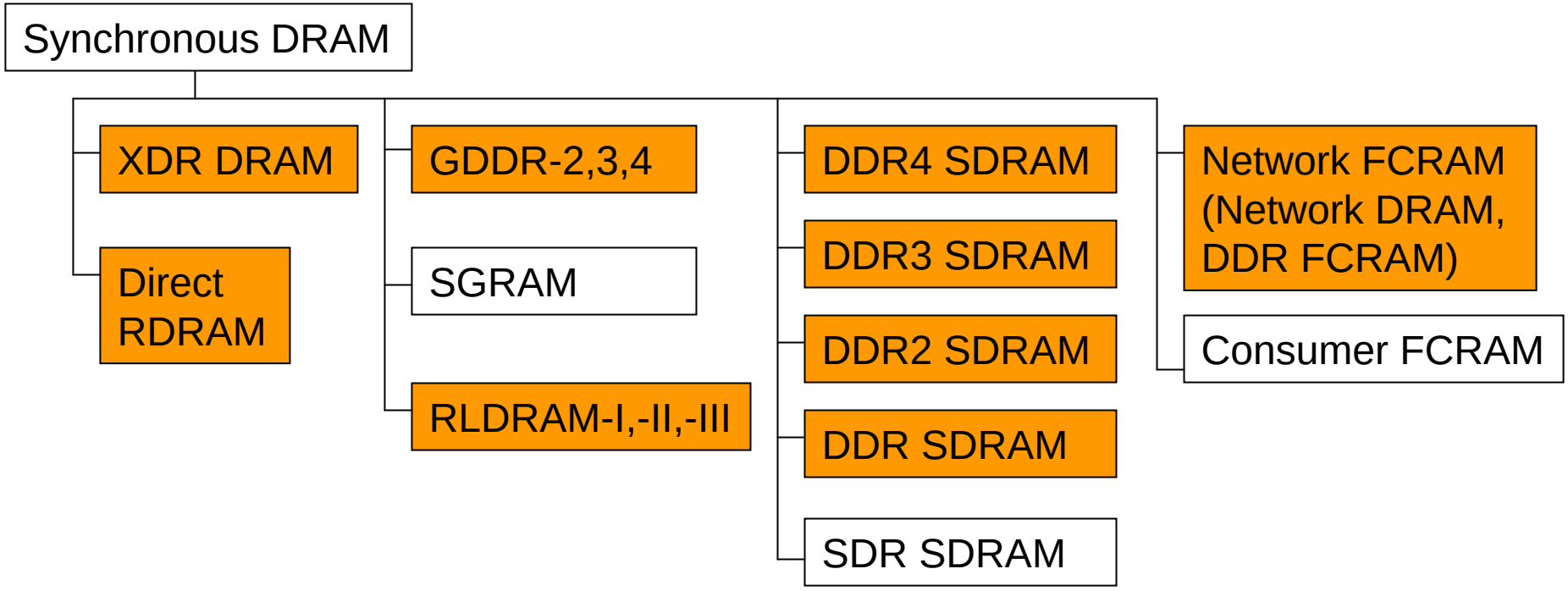


- HFSS™ : Connector and Socket EM analysis and modeling



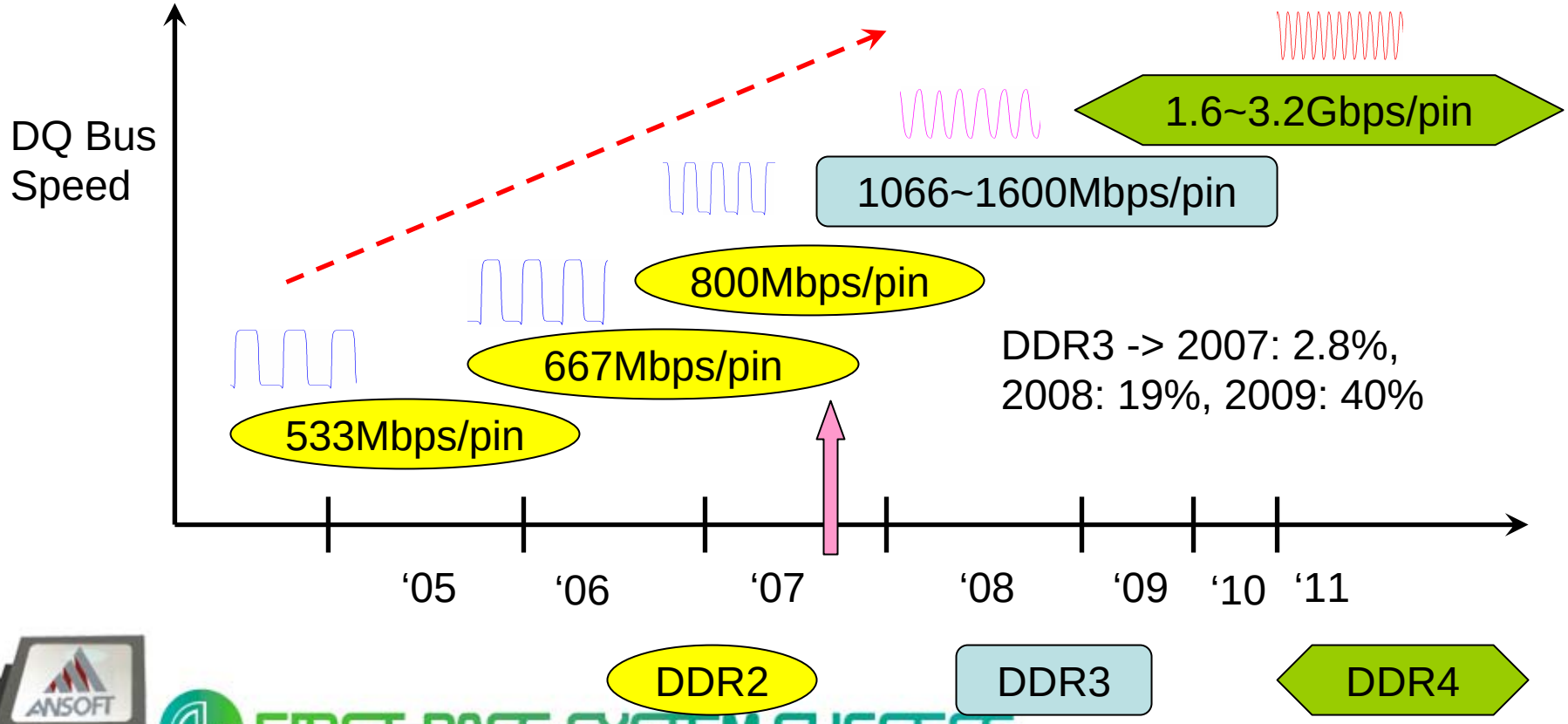
High-speed Memory system

- Introduction : What is High-speed Memory ?



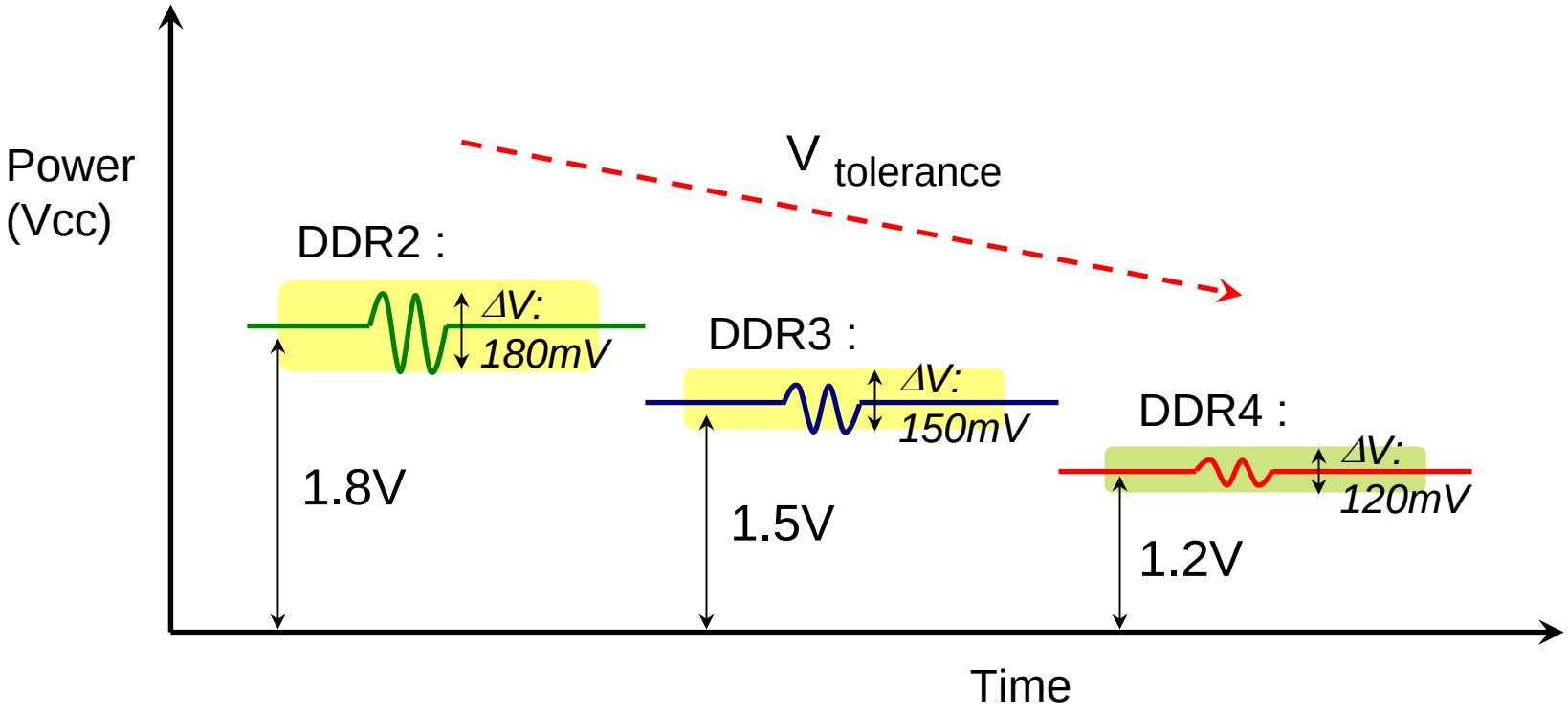
Design Issues: Speed

– Fundamental frequency increase => more SI/PI issues
(Mismatch, ISI, Cross-talk, EMI)

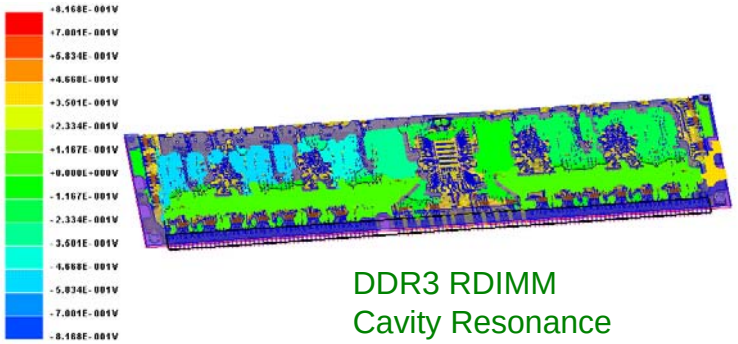


Design Issues: Power

Supply power decrease => more PI issues (Power Noise)



Design Issues at each part



DDR3 RDIMM
Cavity Resonance

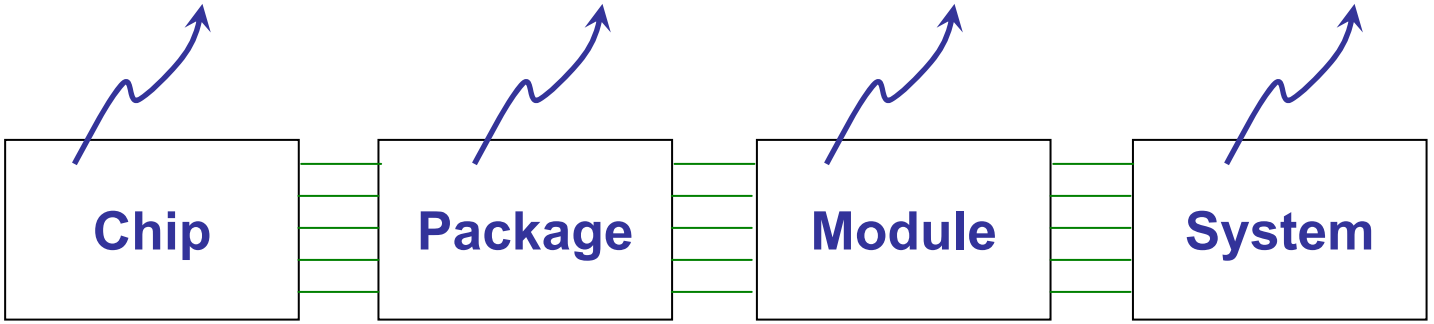
Jitter
Skew
On-chip PDN

Lumped model ?

-> S-para. Based model (freq. depend. Factor)

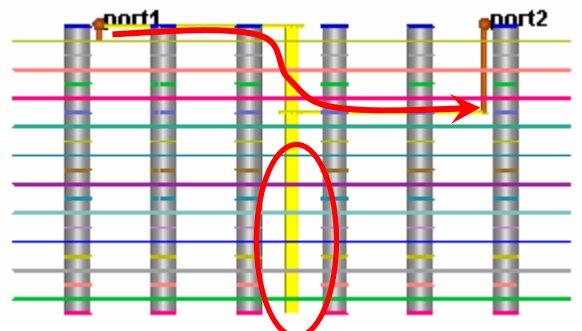
Cavity resonance
Decap. tuning

EMI

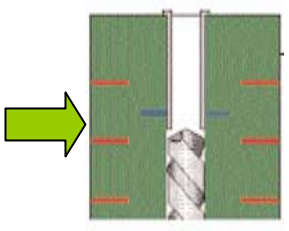


High-speed Memory system

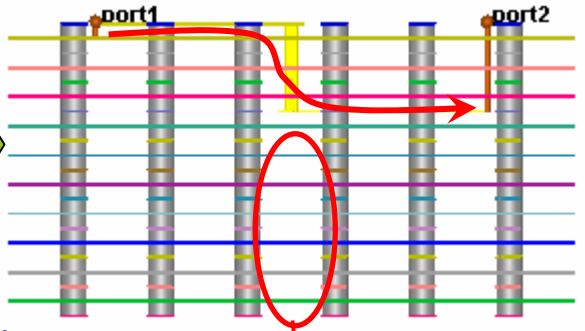
Design Issues : Board level - Via Stub effect

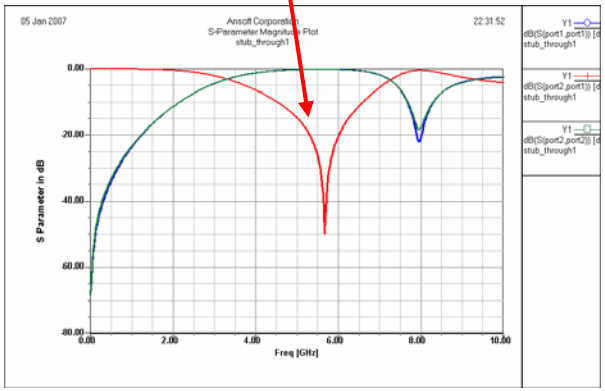


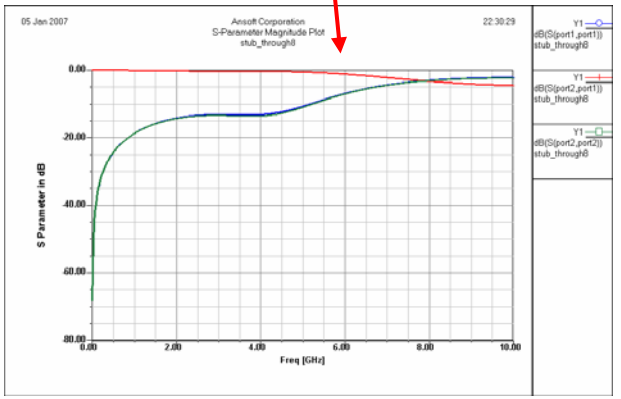
Via Stub Effect



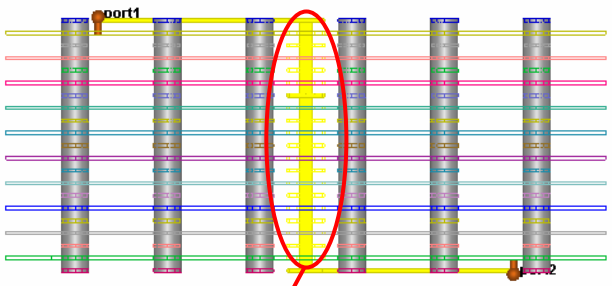
Back Drilling :
remove the unused portion of PTH



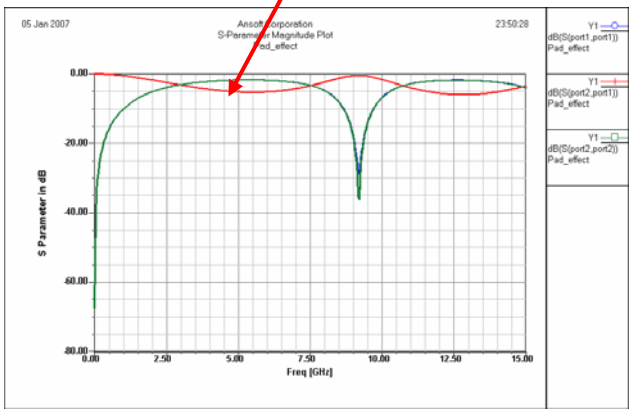




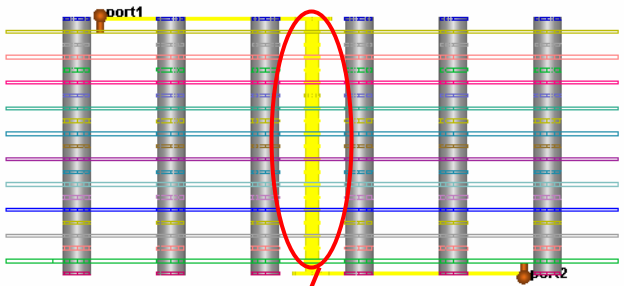
Design Issues : Board level - Via Pad size effect

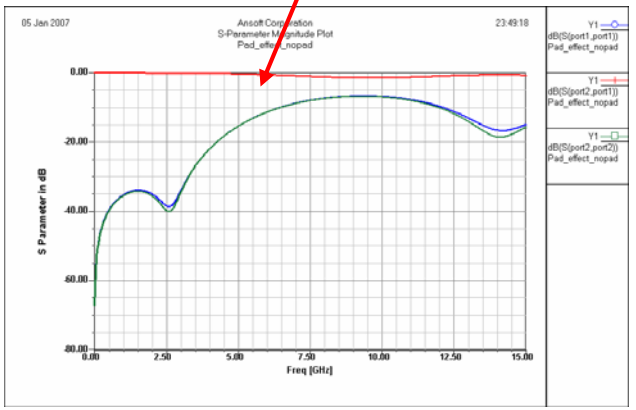


Pad Size Effect : **Capacitive**



Pad-stripping

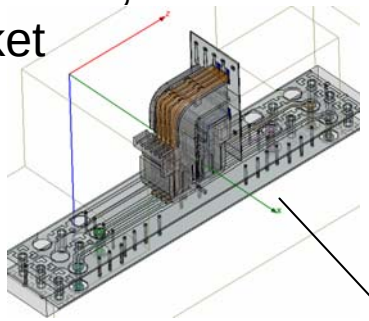




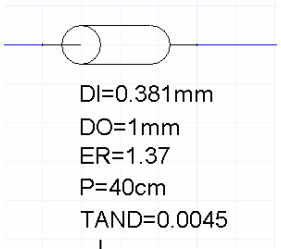
Design Issues : 3D Interconnection

– 3D interconnects are critical for high-speed design

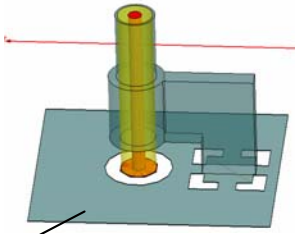
Connector, Socket

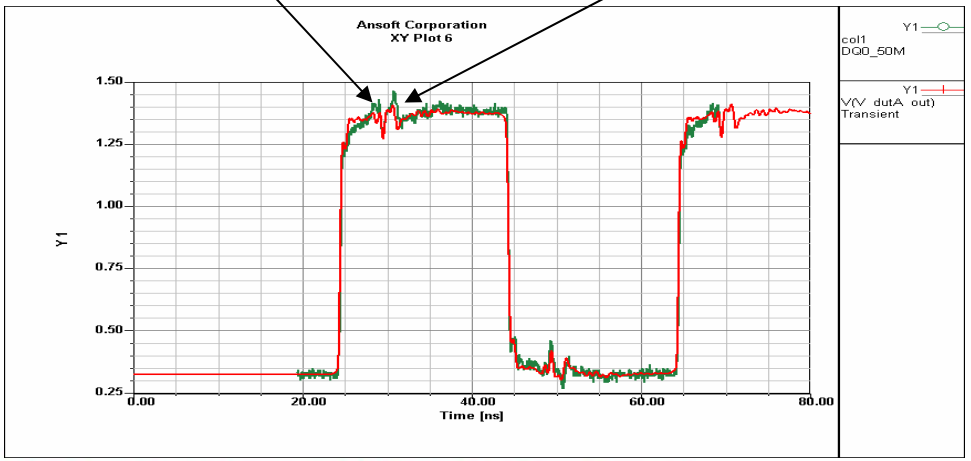


Cable



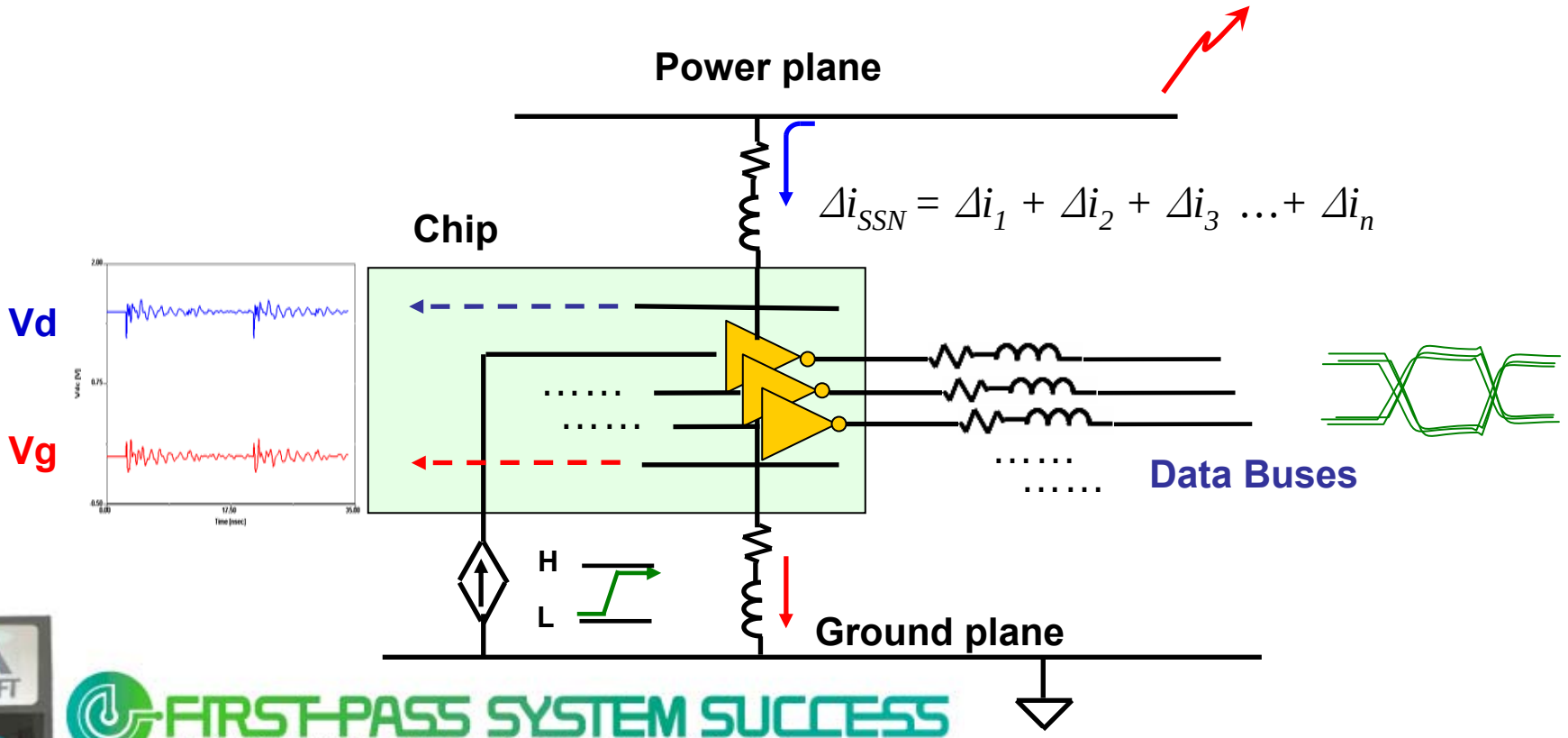
Cable Launch



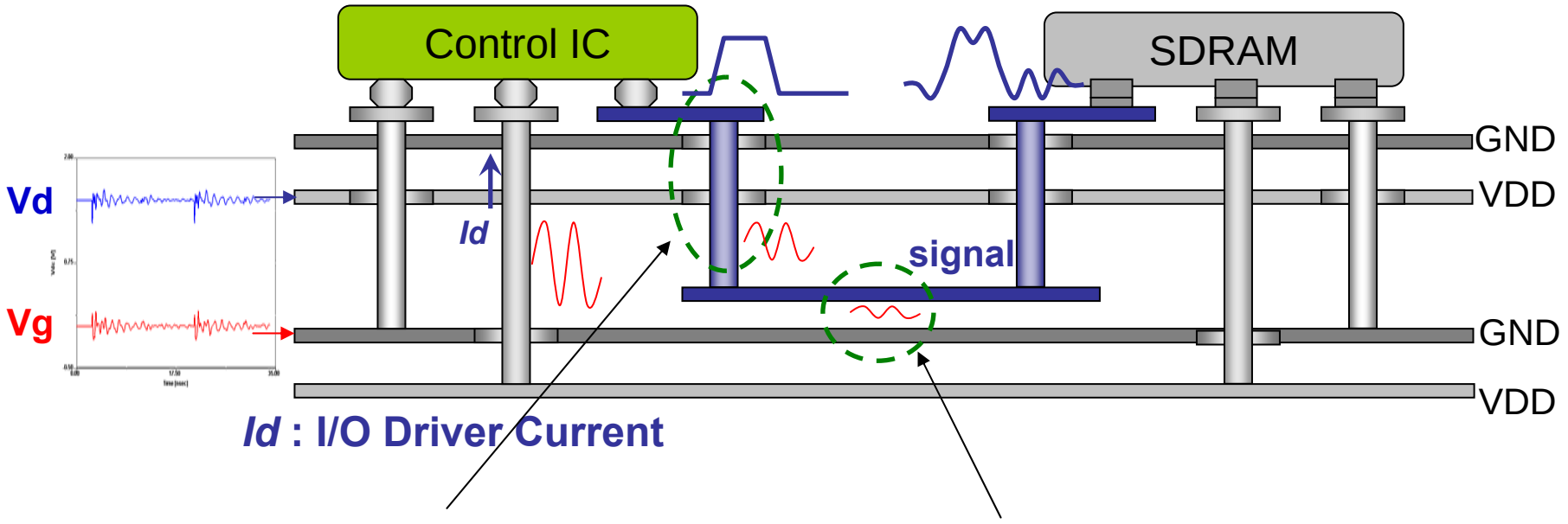


Design Issues: Wide data buses SSN/SSO

- Power/Ground SSN will cause:
  - Logic failure, Timing delay/skew, Coupling to signal line, EMI
- How to analyze the complex Power/Ground plane ?



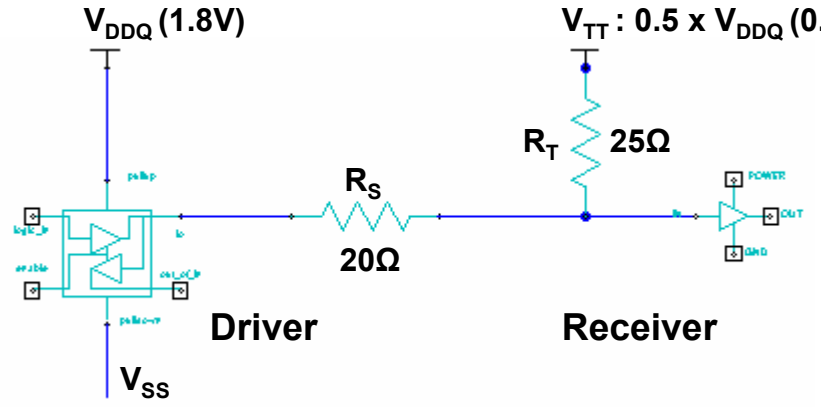
Design Issues: SSN coupling to signal line



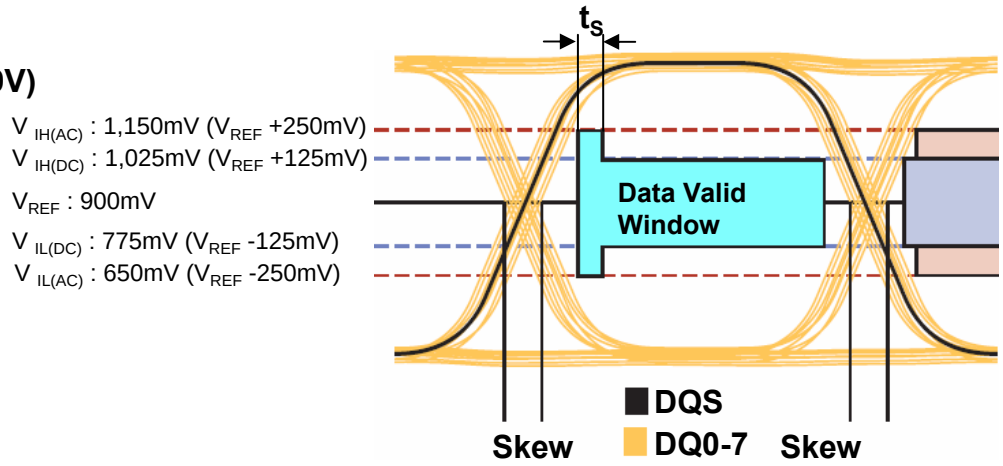
Design Issues: Termination scheme

– SSTL18: Stub-Series Terminated Logic for 1.8 Volts
(DDR2, JEDEC interface standard)

- SSTL18 specifies 13.4mA into a 25 Ω load
- t_S is the minimum time interval within which a valid signal must meet $V_{IH(AC)}$ or $V_{IL(AC)}$



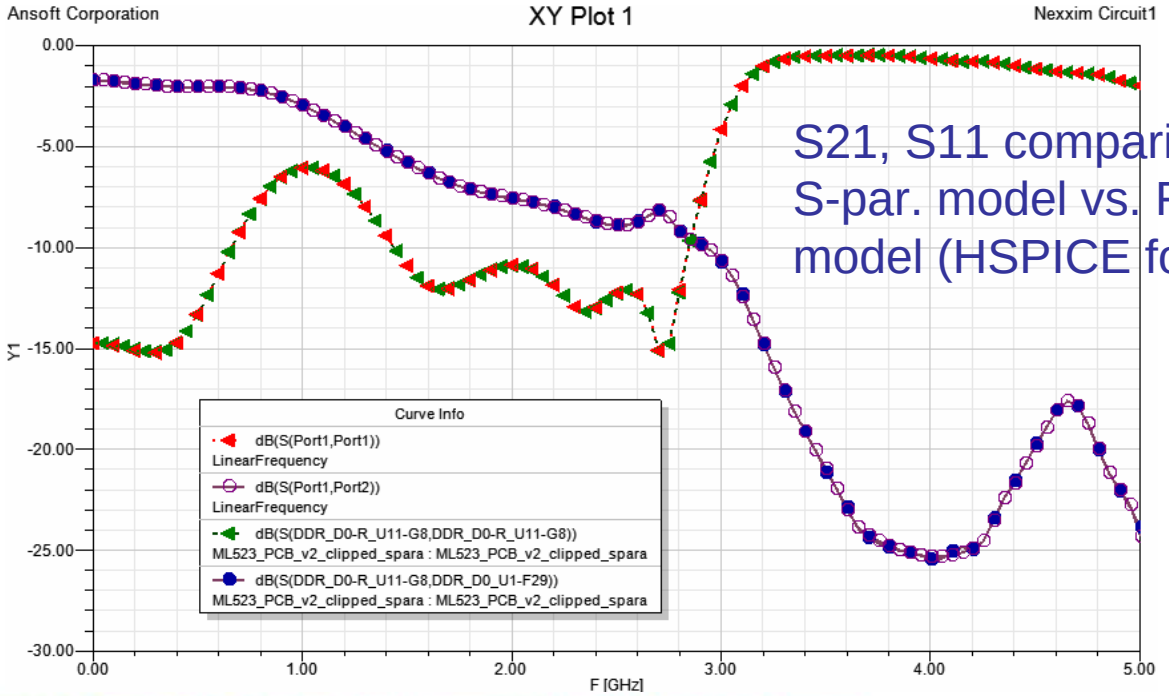
Typical driver environment for SSTL18



DDR2 SSTL18 dc and ac Input Logic Levels

FWS model for bus channel

- FWS model : SPICE model ensures wide band accuracy (Full Wave)
- S-parameter model vs. HSPICE format model from SIwave FWS export

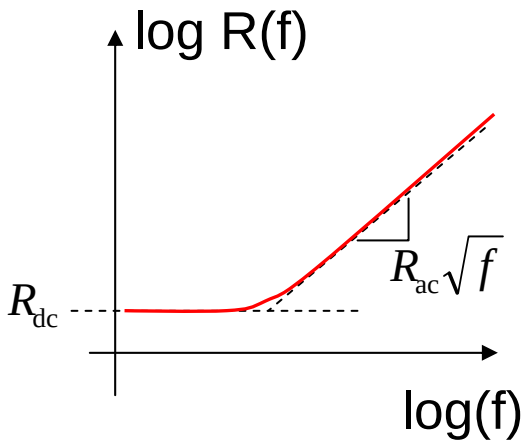


S21, S11 comparison : S-par. model vs. FWS model (HSPICE format)

Frequency dependent parameter

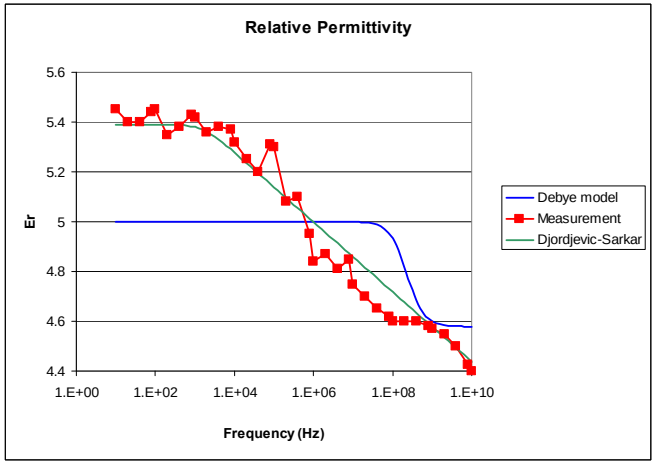
Have to consider :

- Conductor loss
  - Skin Effect
- Dielectric constant and loss
  - Djordjević-Sarkar model



$$\varepsilon(\omega) = \varepsilon'(\omega) + j\varepsilon''(\omega)$$

$$= \varepsilon_\infty + \frac{\Delta\varepsilon}{\ln(\omega_B/\omega_A)} \ln\left(\frac{\omega_B + j\omega}{\omega_A + j\omega}\right) + \frac{\sigma}{j\omega\varepsilon_0}$$



Frequency dependent models are default in Slwave

High-speed Memory system Analysis Example

SSN/Eye Analysis Example

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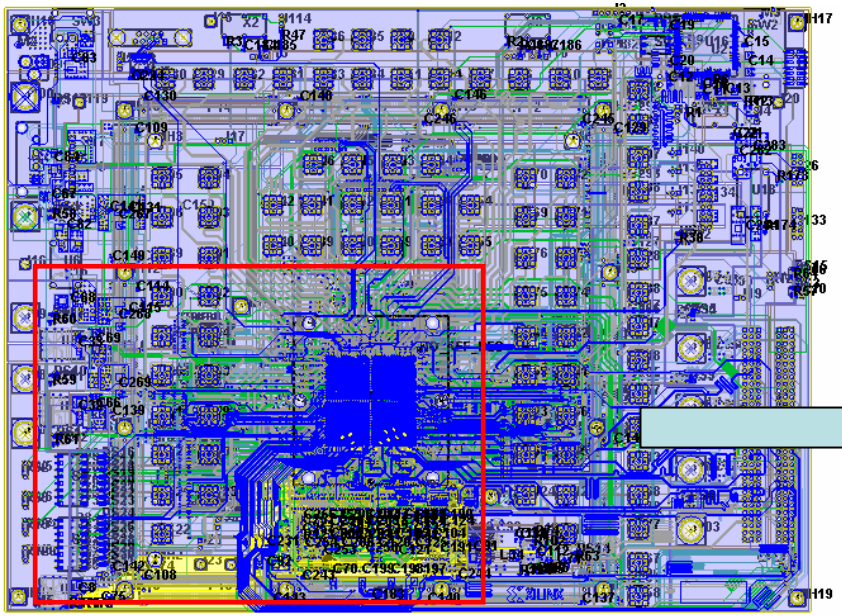
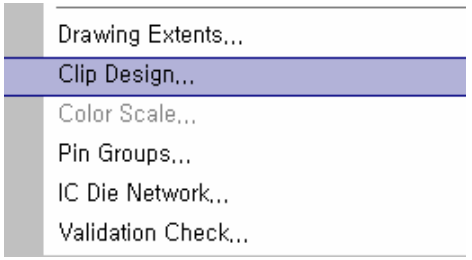
SSN/Eye Analysis Example

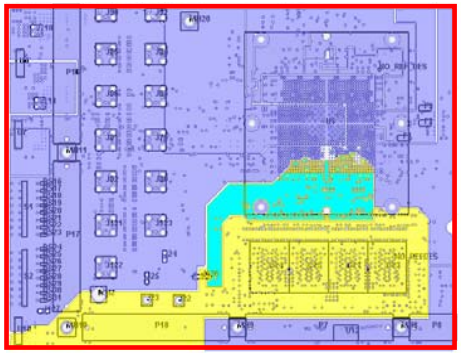
- Xilinx Virtex5 ML523 Board [1]
- Micron DDR2 Memory [2]



Xilinx Virtex5 ML523 Board



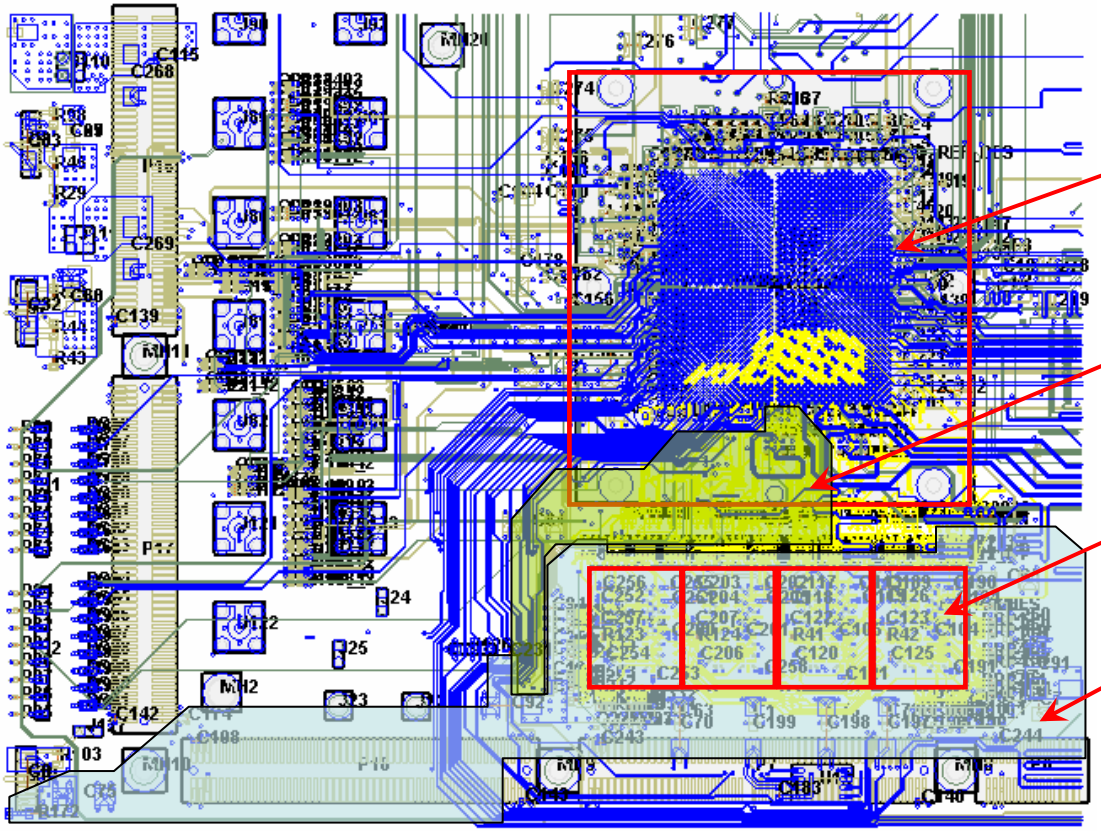
Clip Design in SIwave



Region for SSN/Eye Analysis

DDR2 Nets & Power

- DDR2 signal nets and Power nets on clipped design



FPGA:
Xilinx Vertex-5

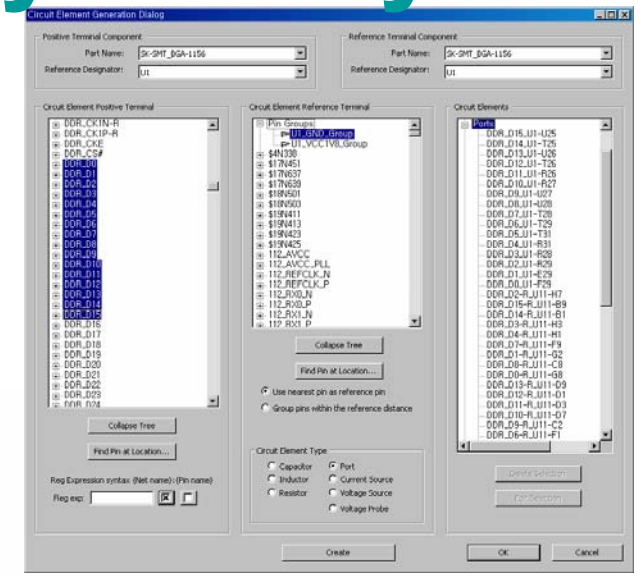
Control I/O Power:
Vcc (1.8V)

DDR2 Memory:
Micron MT47H16M16BG-3:B

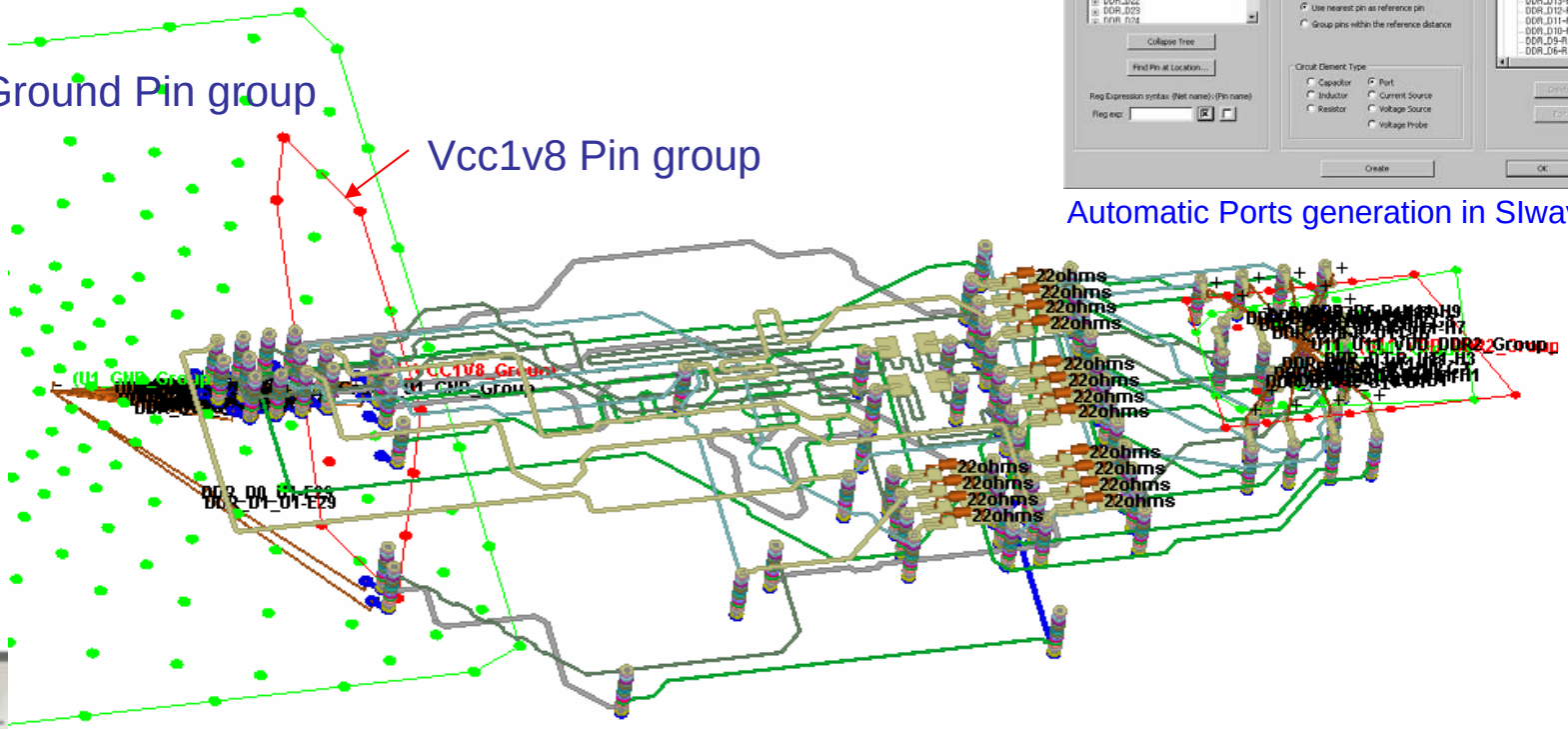
Memory I/O Power:
VDD DDR2 (1.8V)

Ports setup for SSN/Eye Analysis

- 36Ports setup for SSN/Eye Analysis
  - Ports for Data line : DQ0-15
  - VRM Ports : Vcc1v8 net, Vdd_DDR2 net
  - Power Ports : Vcc1v8 net, Vdd_DDR2 net

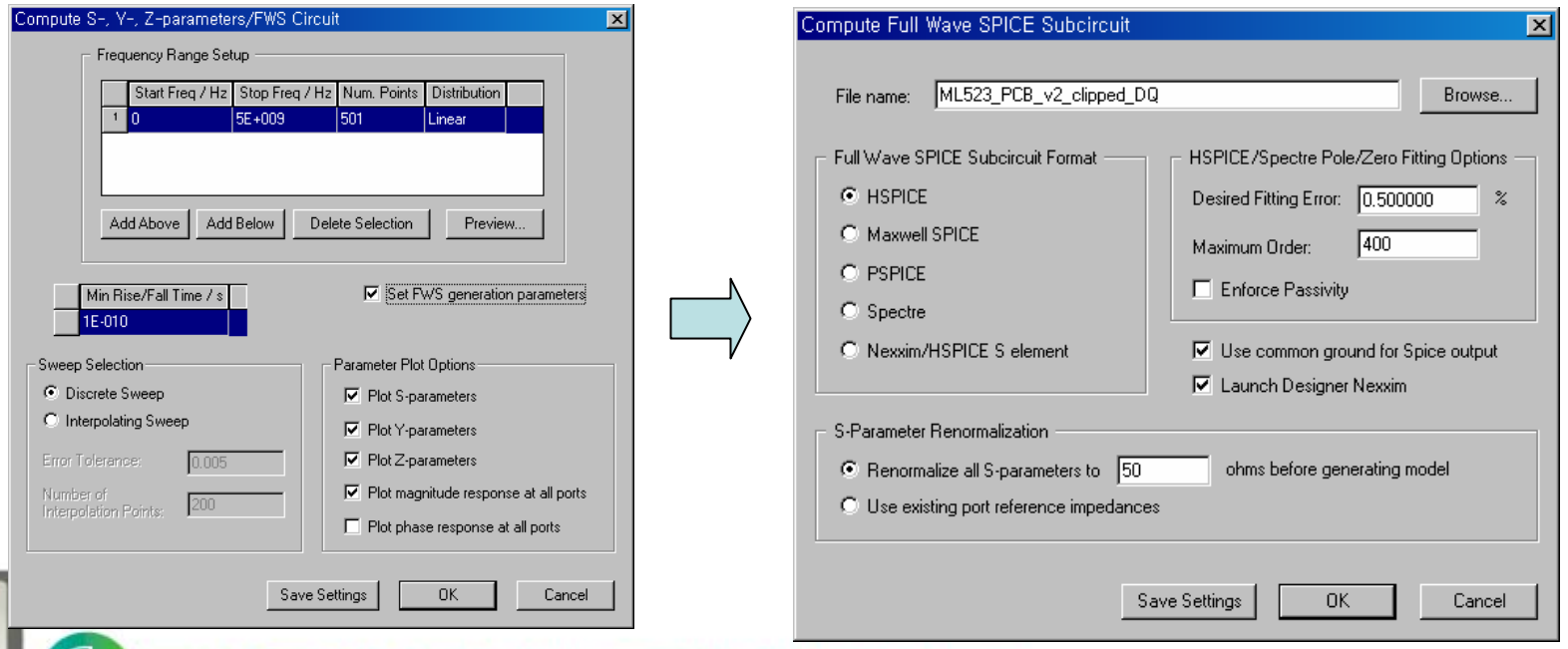


Automatic Ports generation in SIwave



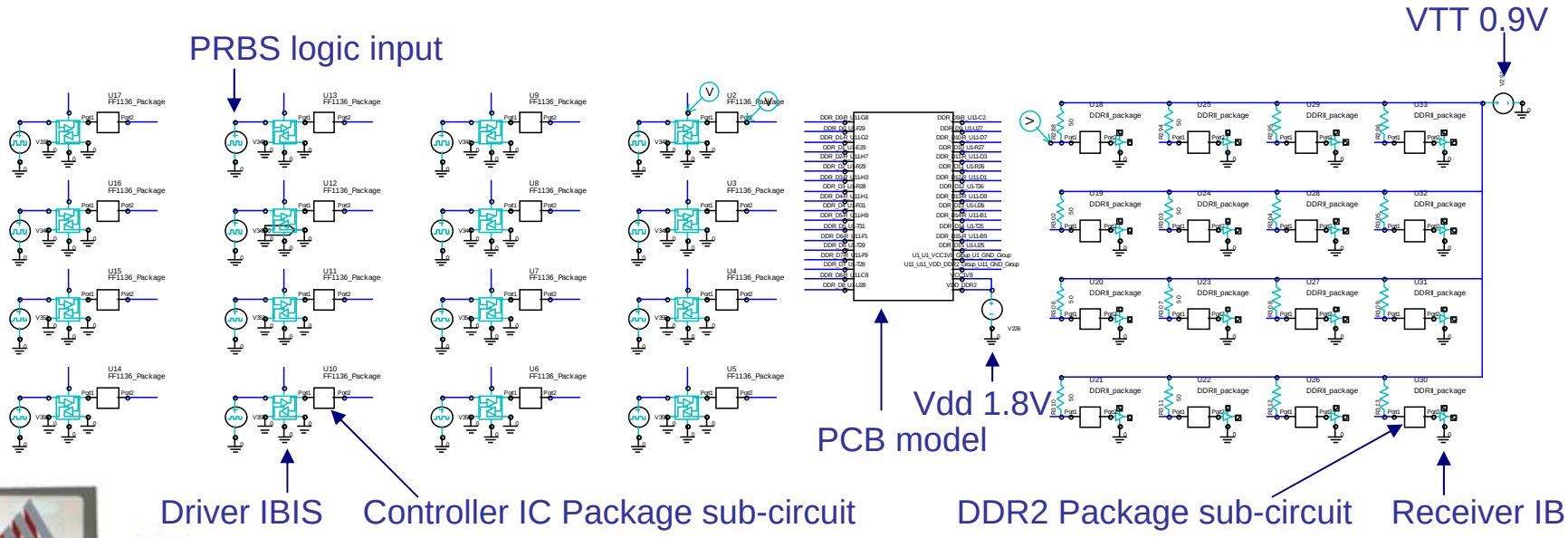
SIwave FWS Export

- S-Y-Z-parameter setup
  - Discrete 0~5GHz, 501 point sweep for transient analysis
- Full Wave SPICE Sub-circuit setup
  - HSPICE format



Nexxim Schematic for SSN/Eye Analysis

- SSN/Eye Analysis Schematic
  - PCB model : HSPICE format model from SIwave FWS export
  - Driver/Receiver : SSTL18_II , IBIS I/O buffer model
  - Package sub-circuit
  - PRBS logic and DC source for VTT termination

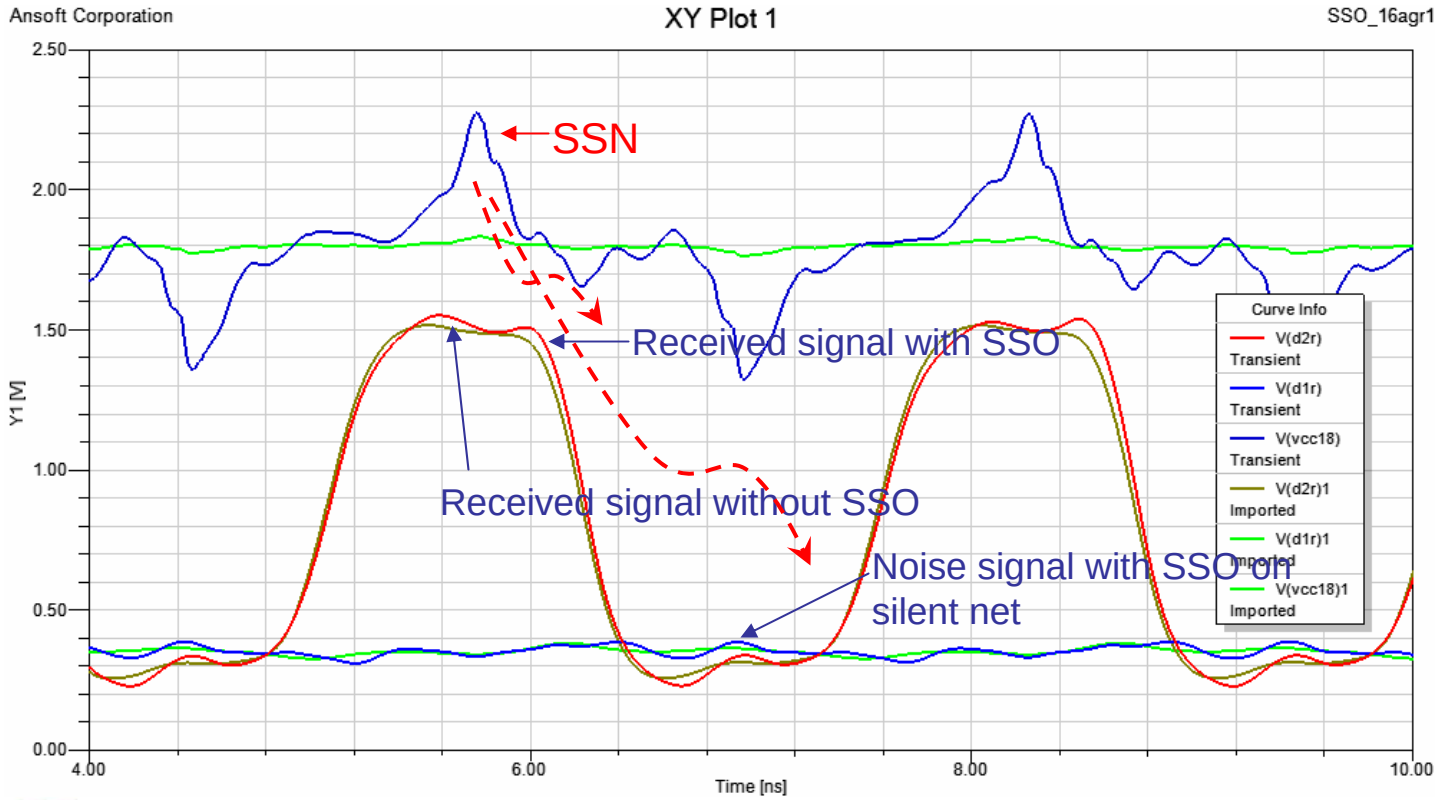


SSN results and Jitter noise by SSN

- Vdd tolerance SPEC : ± 100mV

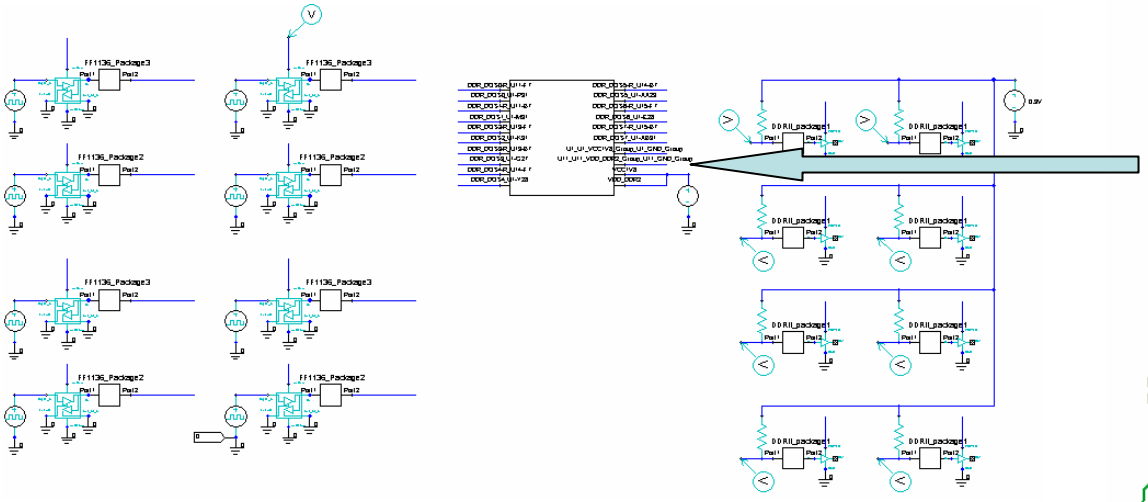
SSN coupling to signal

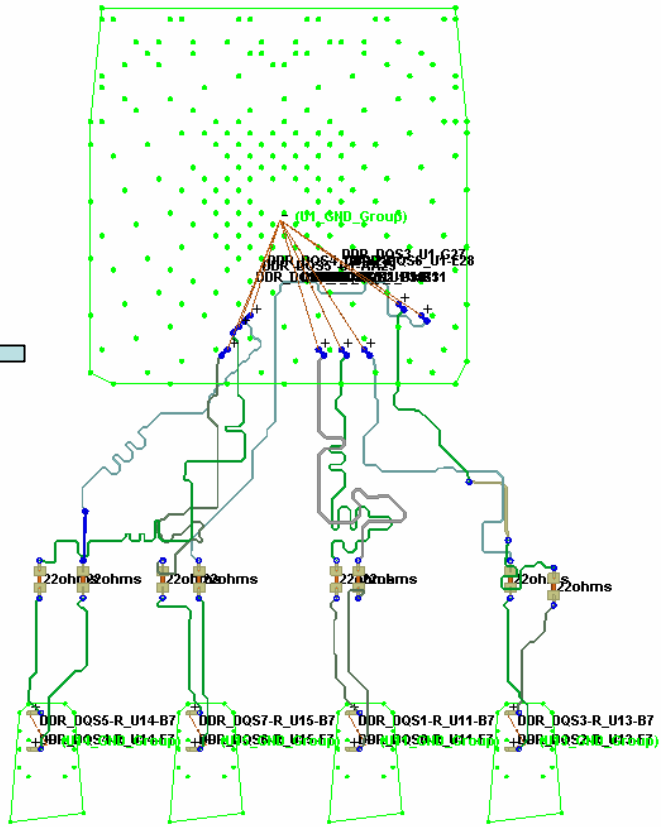
- Switching noise coupling to signal



DQS Lines Skew Analysis

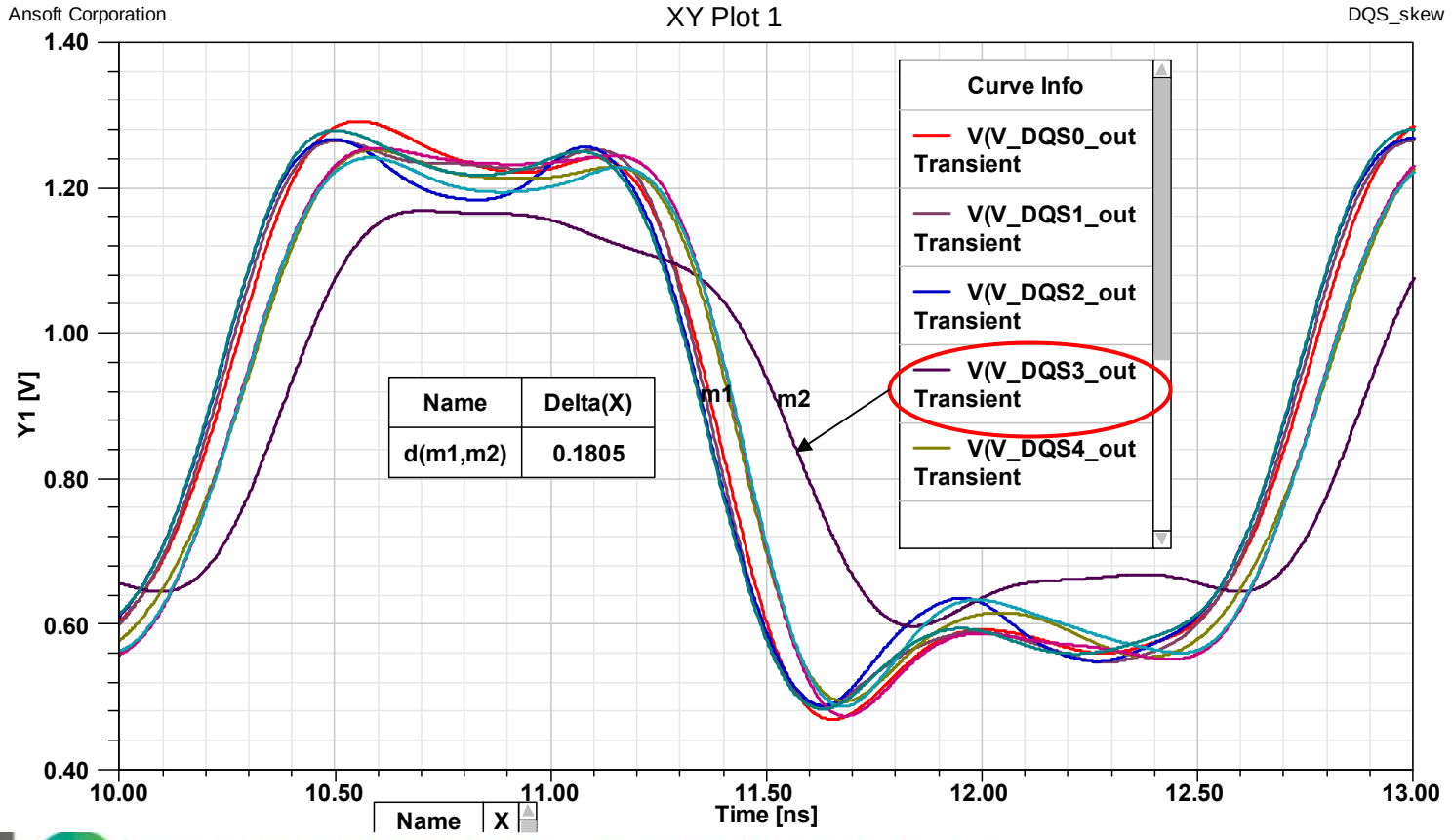
- DQ,DQS include meander lines for delay and skew
- Schematic for DQS lines skew analysis





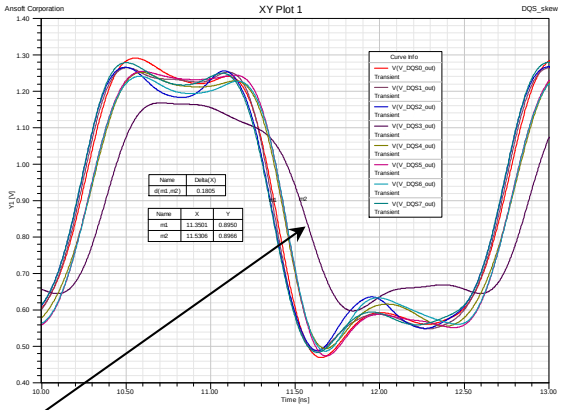
DQS Lines Skew Analysis Results

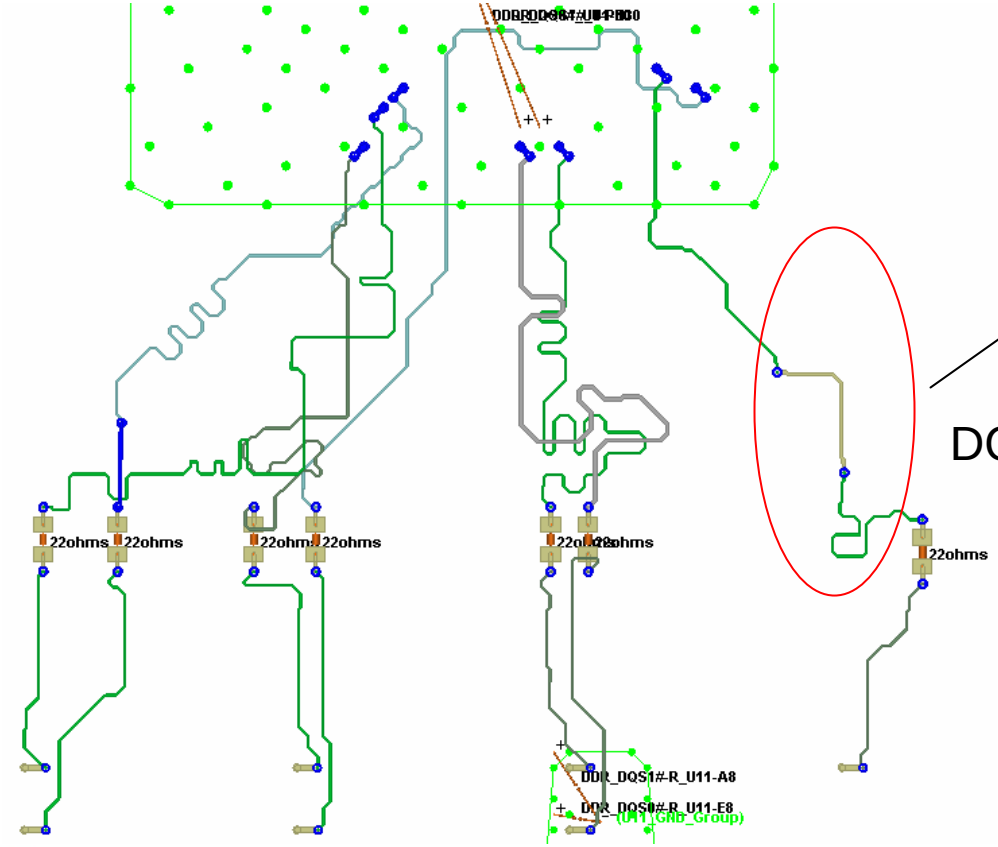
- Skew Analysis results for DQS0-7
  - DQS3 line show larger skew than others



Skew Analysis Results

Why DQS3 line show large skew than others ?

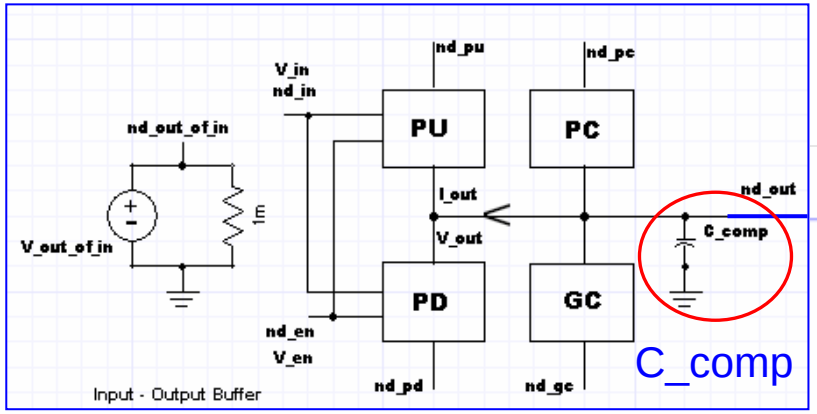




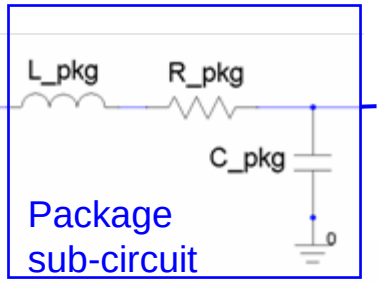
DQS3 net has 2 more vias

DQS, DQ Line Timing and Slew Rate Analysis

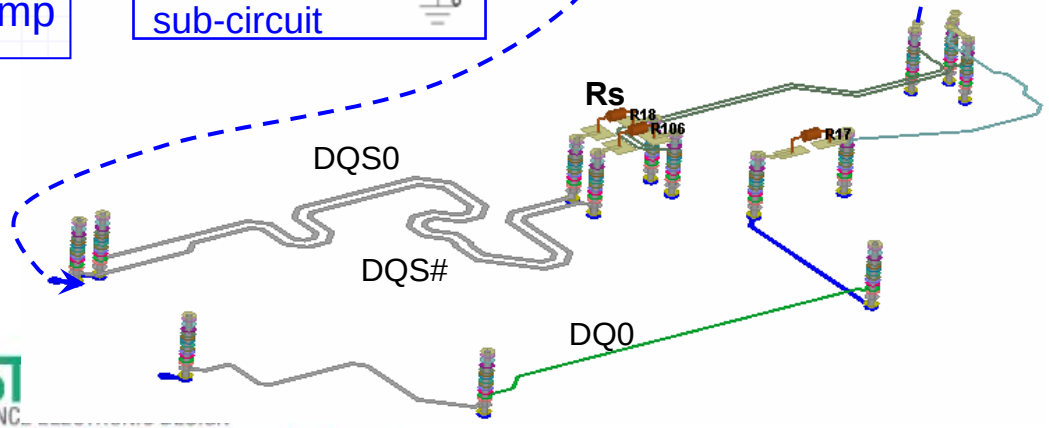
- DQS, DQ point-to-point connection:
  - Controller IC Package – Via – Line – Via – Rs – Via – Line – Via – SDRAM Package
  - Driver and Receiver buffer model , C_comp, L_pkg, R_pkg, C_pkg



Nexxim IBIS buffer model :
Controller IC Input/Output

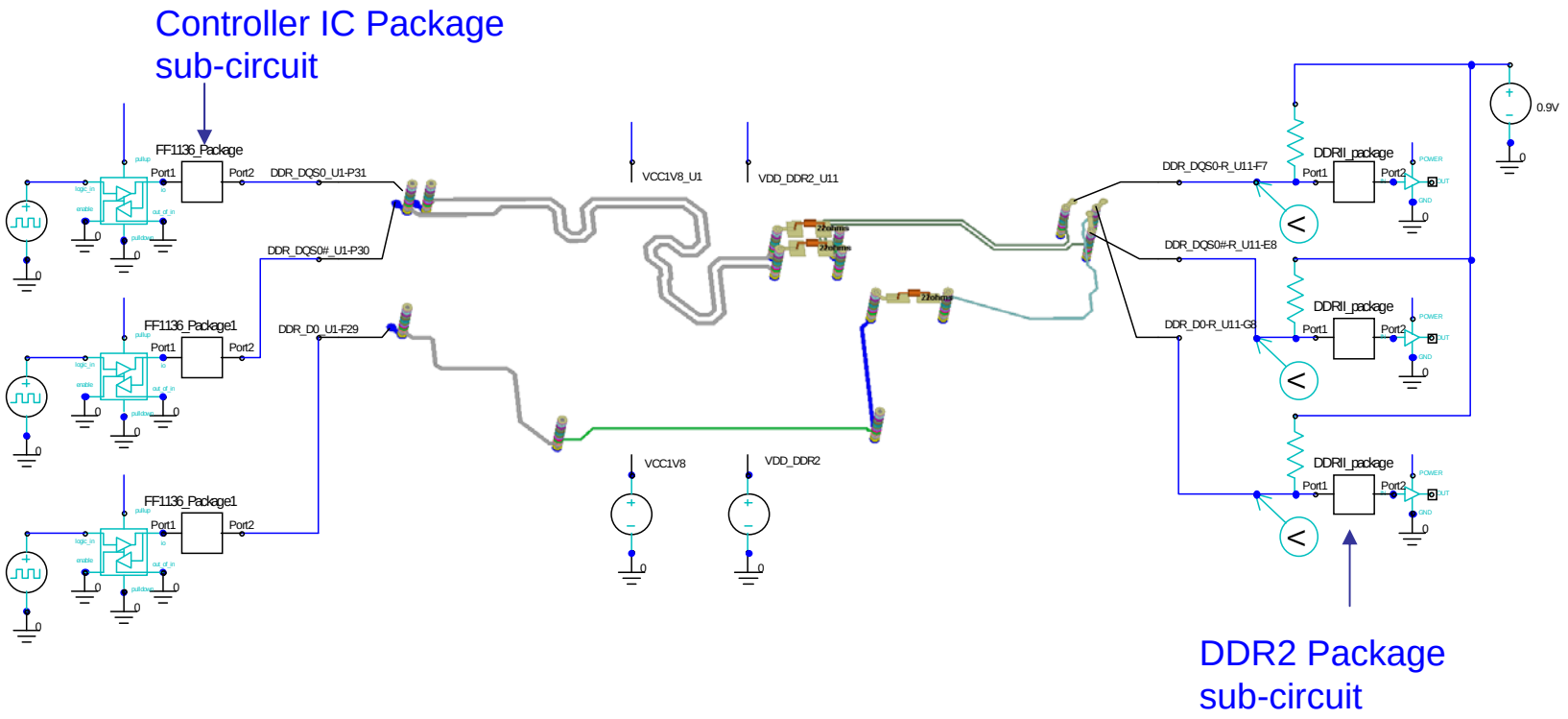


DDR2 PKG and buffer model



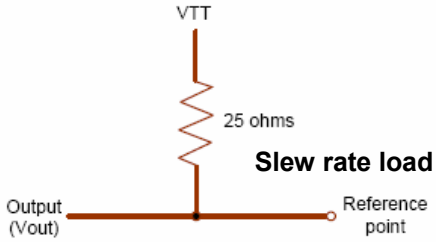
DQS, DQ Line Timing and Slew Rate Analysis

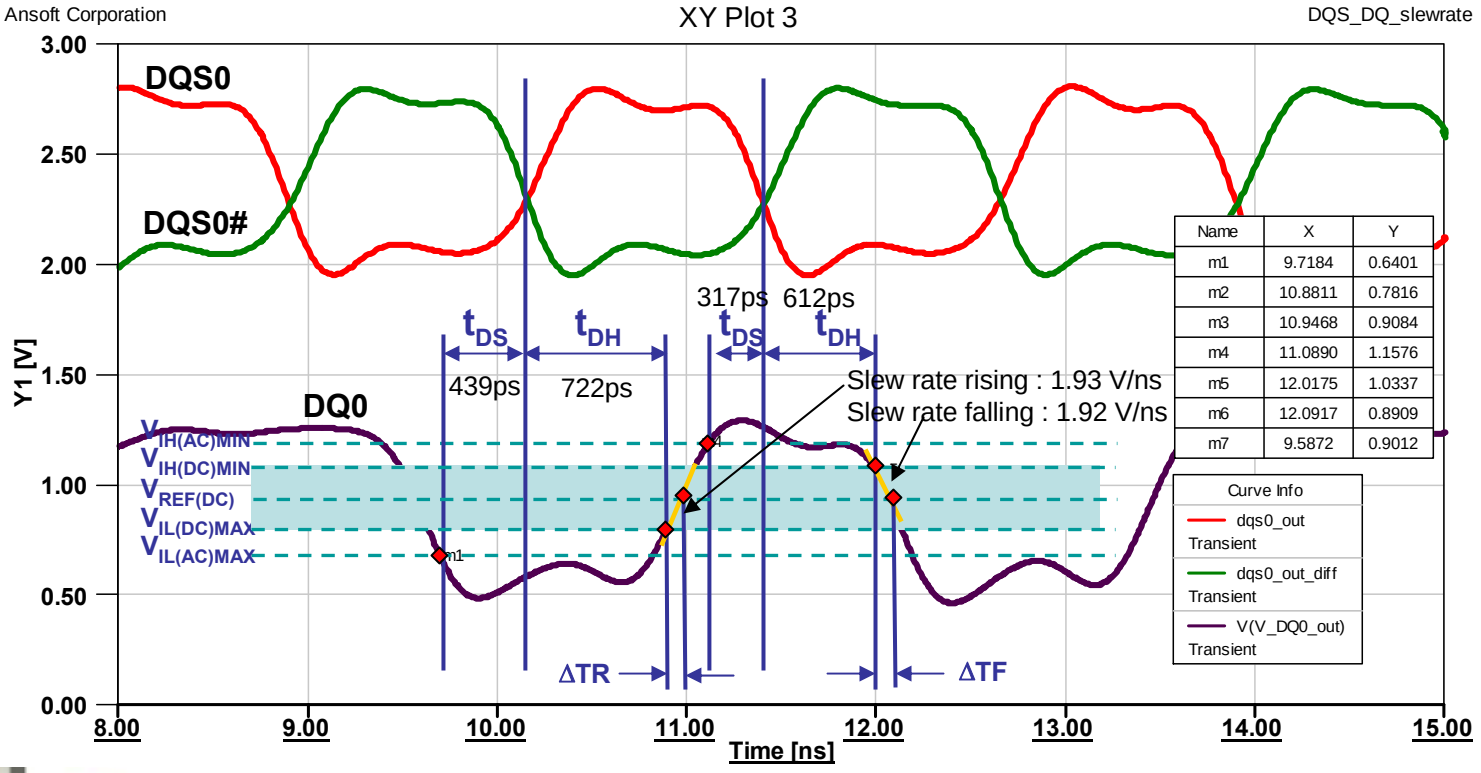
- Nexxim Schematic for DQS, DQ lines timing and slew rate analysis



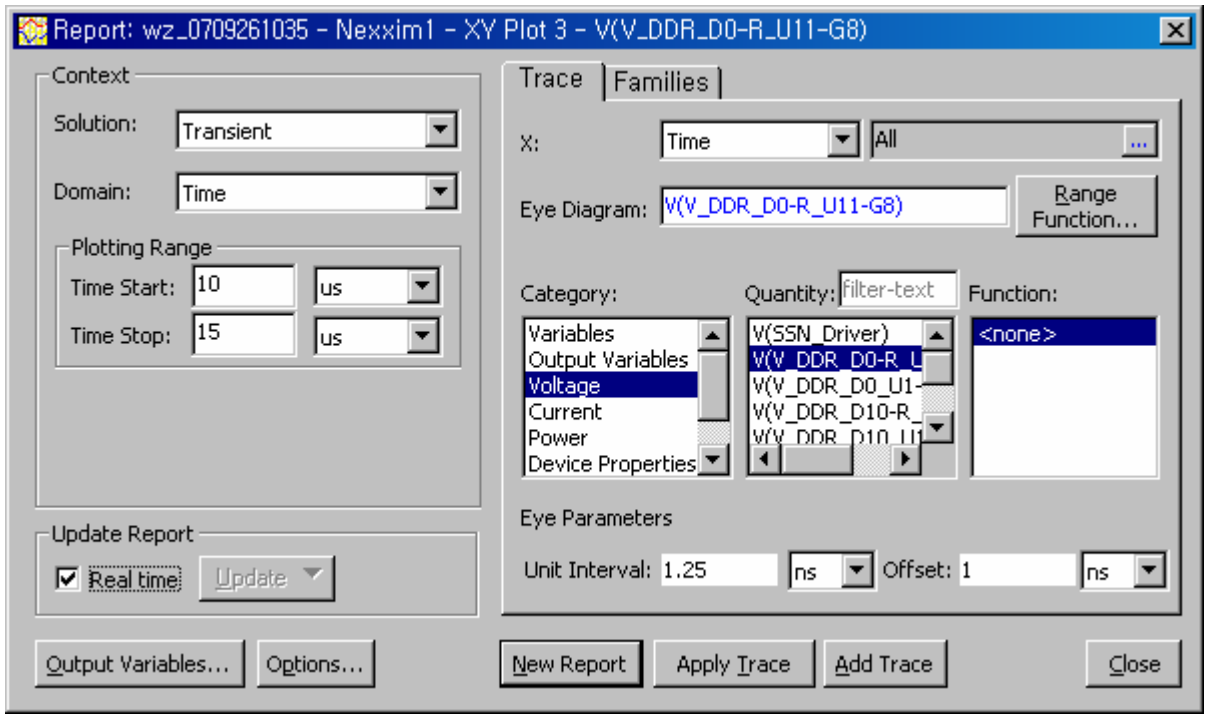
Timing and Slew Rate Analysis

- t_{DS} : Data setup time , t_{DH} : Data hold time
- Slew rate rising signal = $[V_{REF(DC)} - V_{IL(DC)MAX}] / \Delta TR$
- Slew rate falling signal = $[V_{IH(DC)MIN} - V_{REF(DC)}] / \Delta TF$
- Slew rate load : 25ohm between Vout and VTT



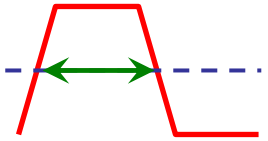


Nexxim Eye Diagram Plot

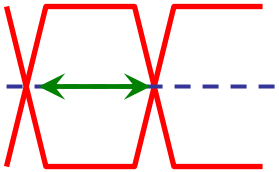


Transient Result

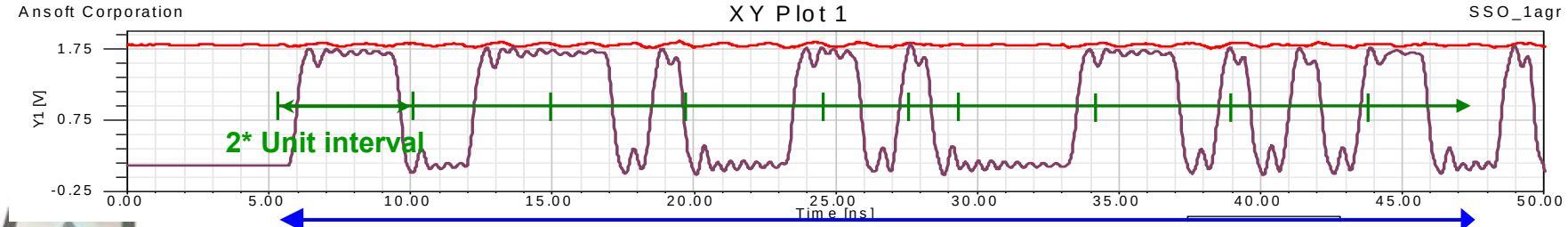
Unit Interval
= 0.5Tr + PW + 0.5Tf



Cut and Fold
(2 unit interval)

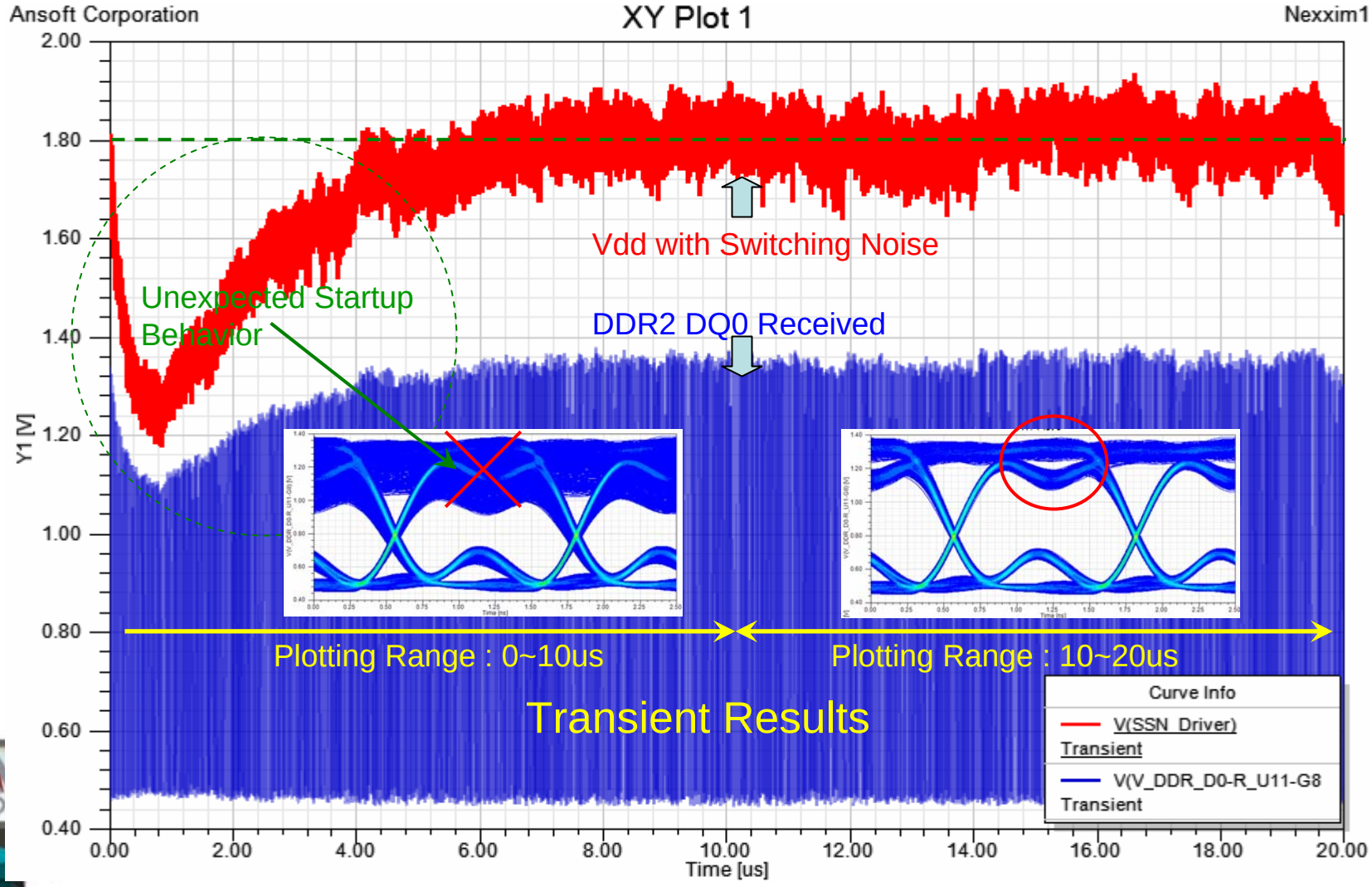


Eye Diagram



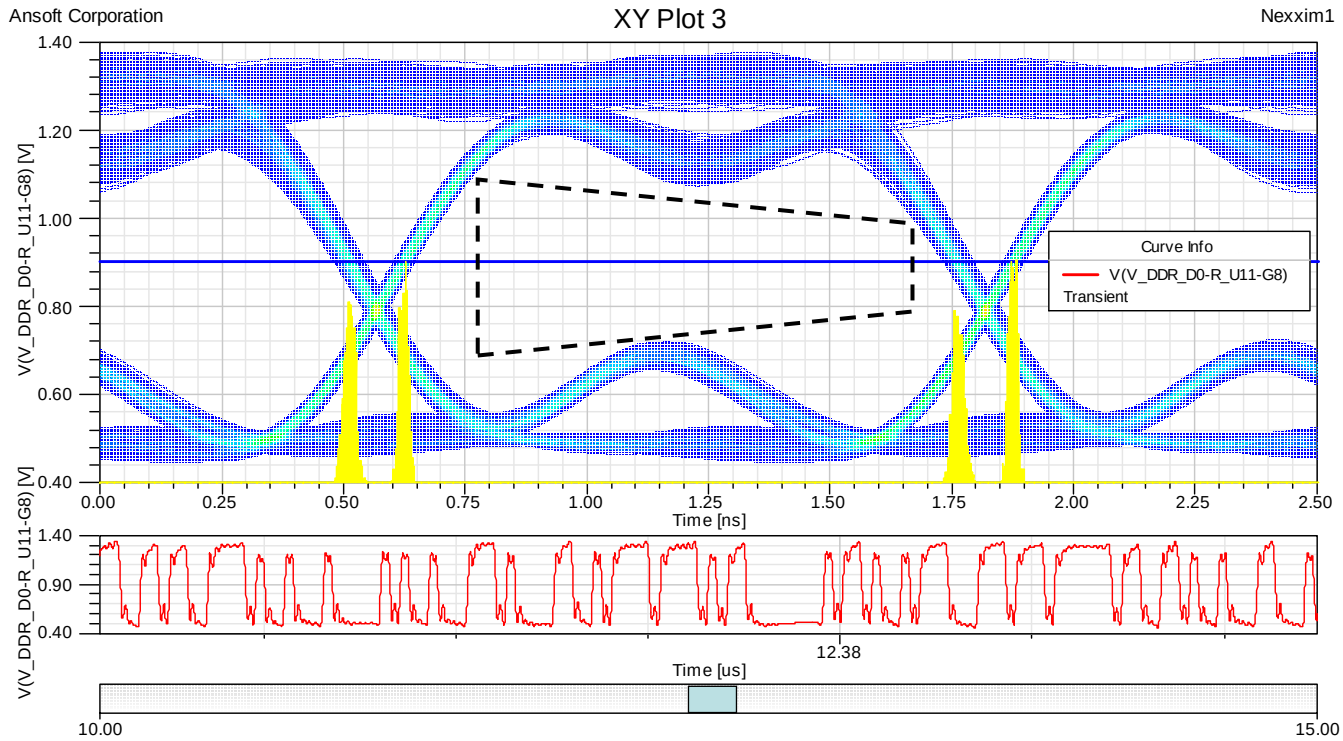
Plotting Range

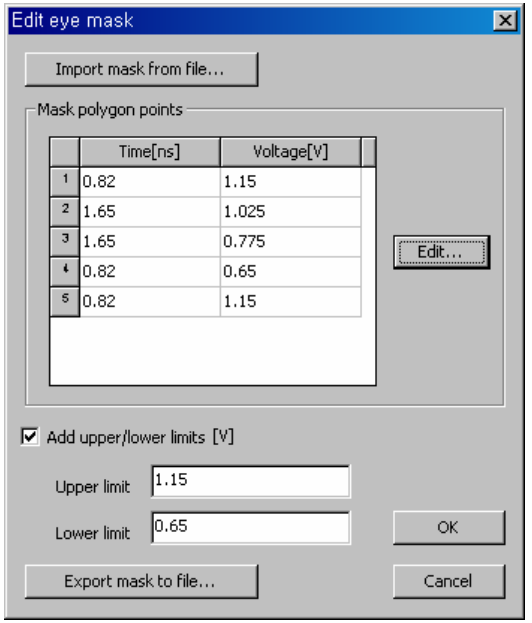
- Eye Plotting Range of Transient Results

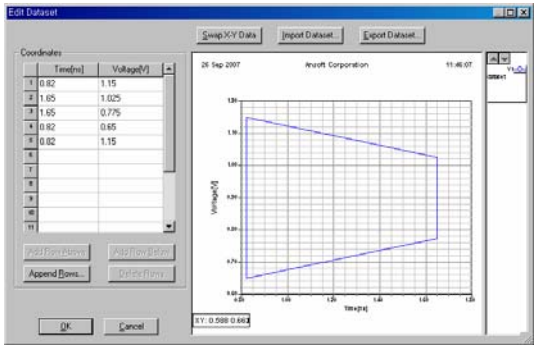


Add Eye Mask

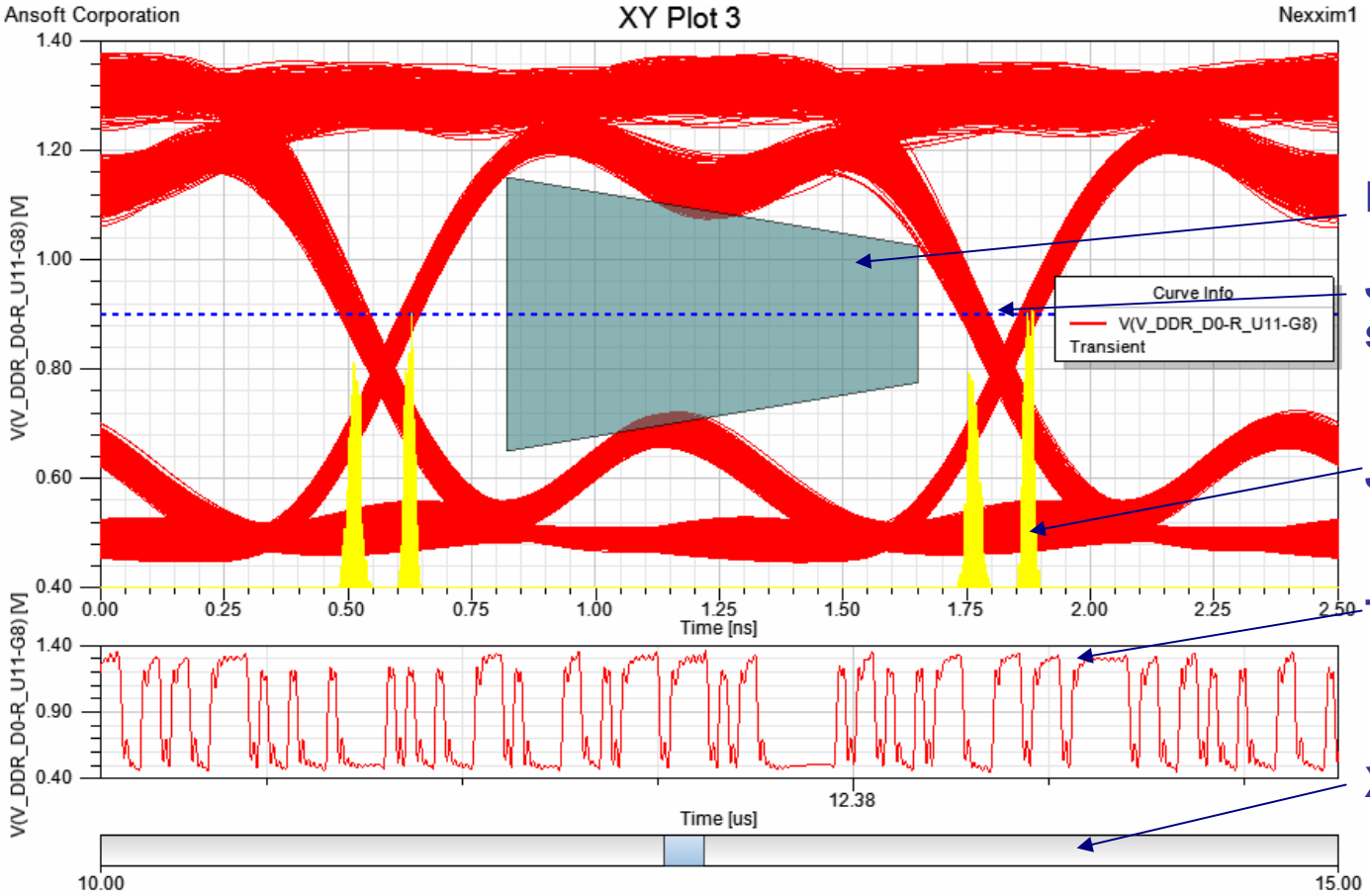
- Eye Mask
  - Edit Eye Mask
  - Export/ Import Mask file







Nexxim Eye Diagram Plot



DDR2 Data Valid window

Jitter Histogram sampling across Y-value

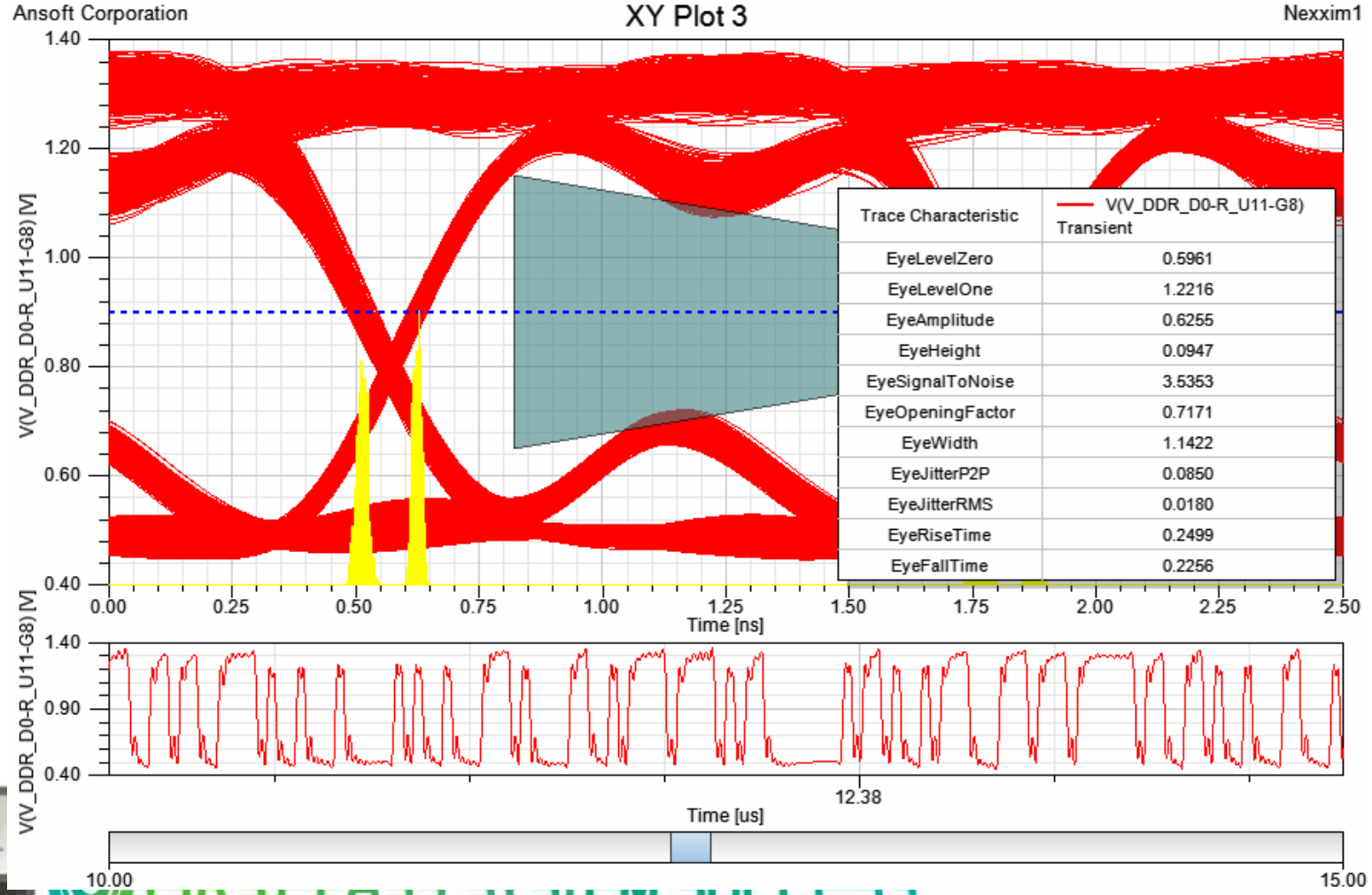
Jitter Histogram

Transient Results

X scroll bar

Add Eye Measurements

- All Eye measurements can be displayed



High-speed Memory system Analysis Example

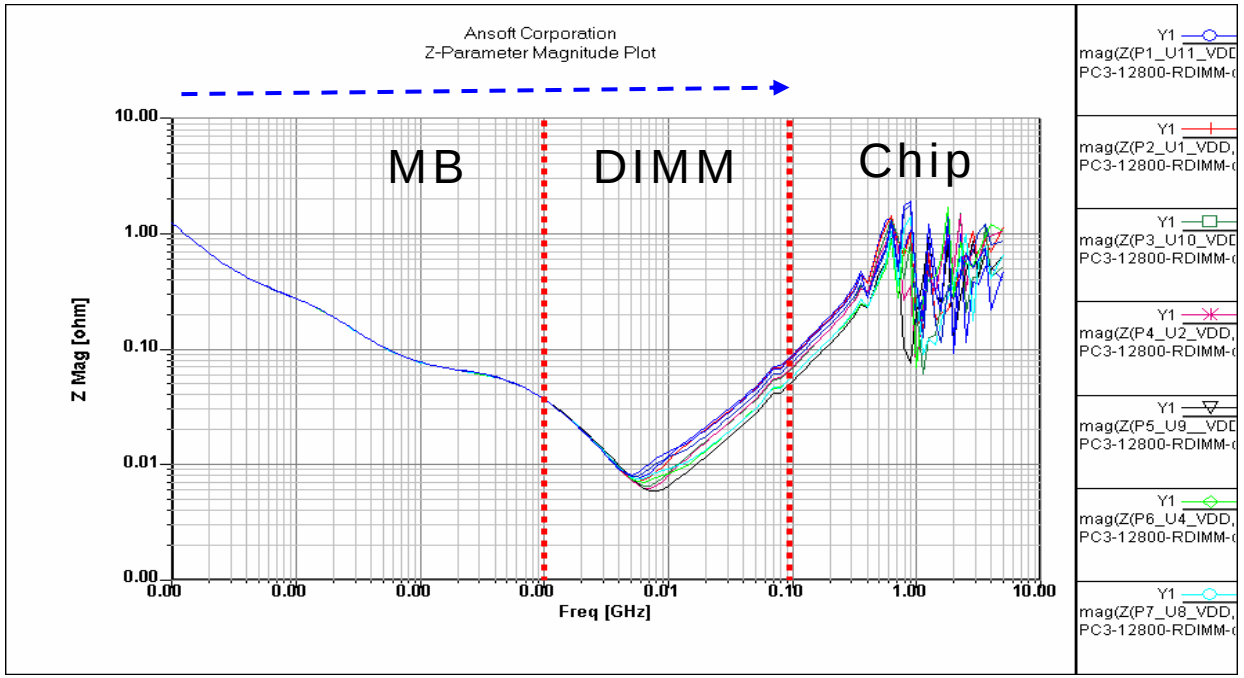
Impedance Analysis Example
(DDR3 RDIMM)

DDR3 Memory Module PDN

- Power Distribution Network Design for DDR3 memory module
  - Should be considered with Main board PDN impedance
  - Should meet the Vdd noise SPEC : ± 75mV (Vdd=1.5V)
  - Vdd noise is transferred to Vref
  - Need Freq. domain optimization (de-cap. Tuning) with P/G Impedance Plot

DIMM Decoupling Capacitor

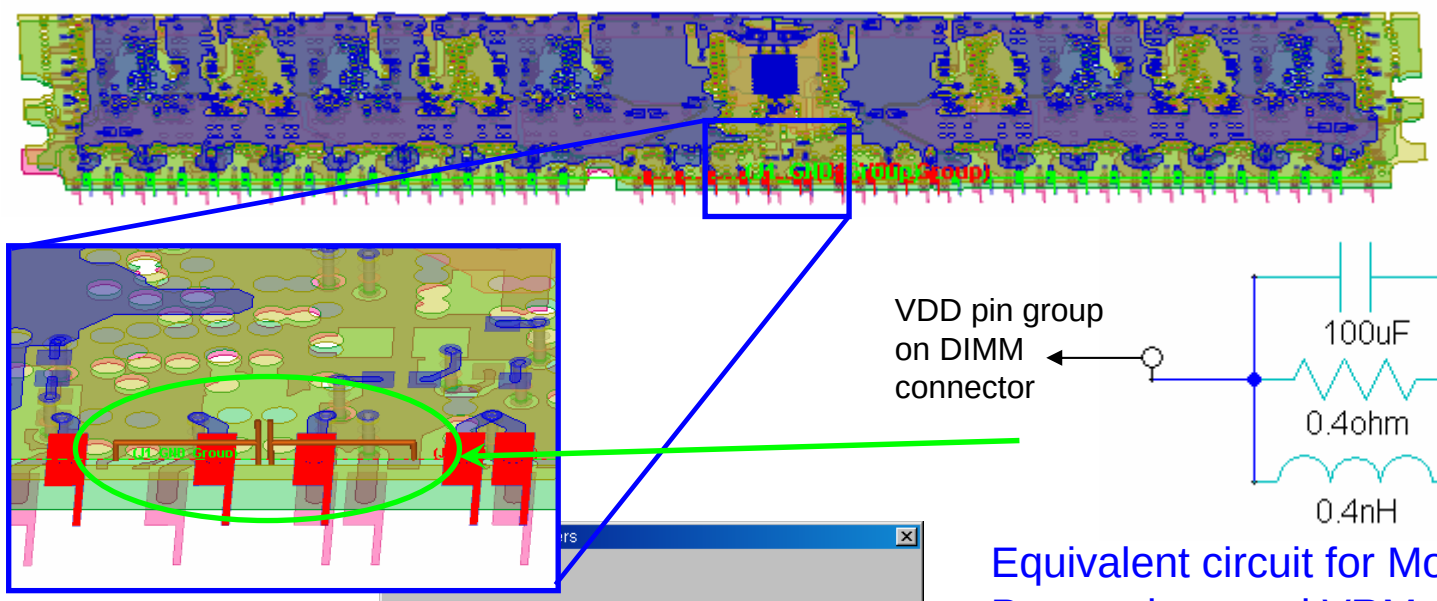
- DIMM decoupling capacitor :
  - Affect at range of ~150MHz



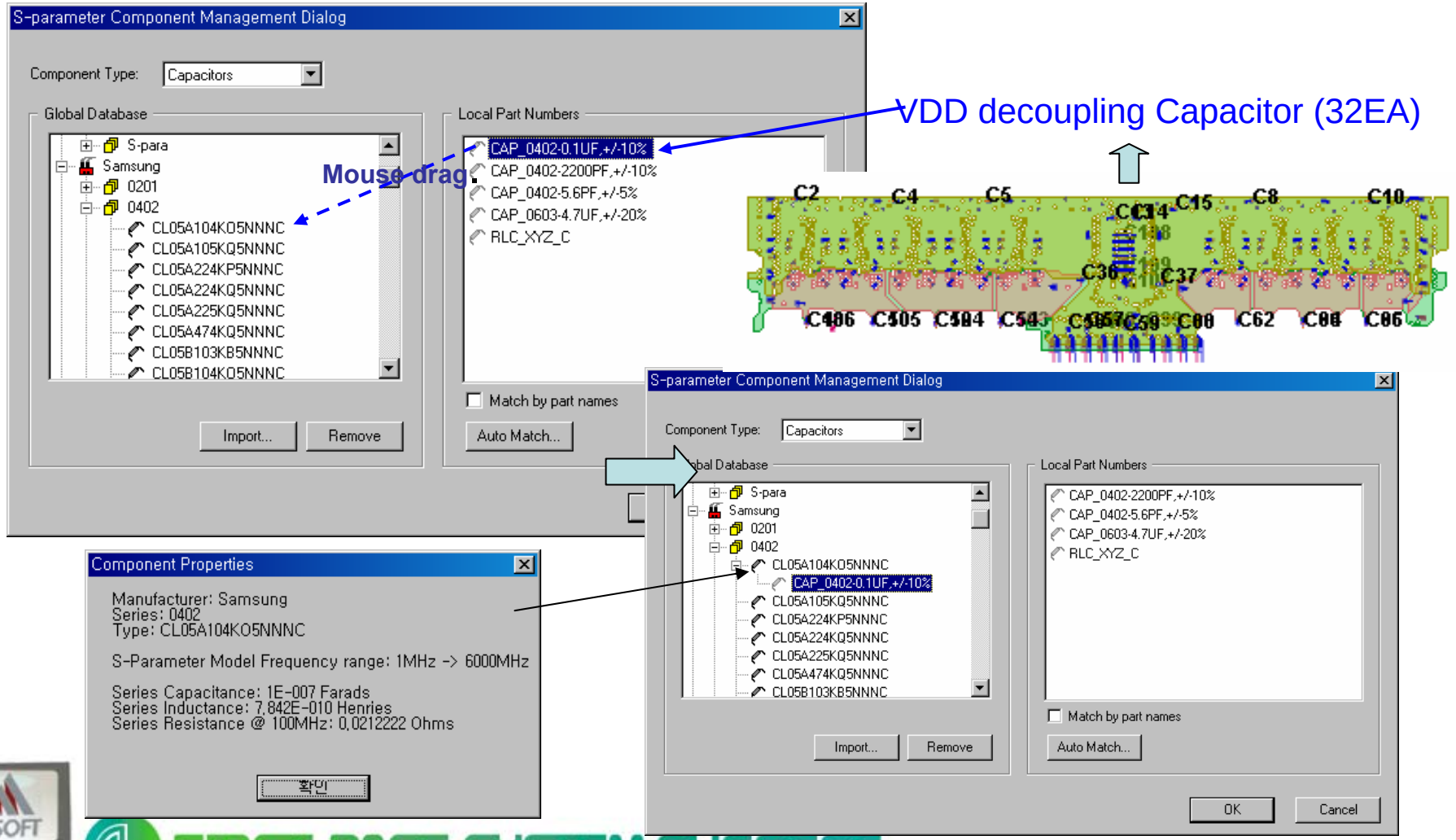
Impedance profile for DDR_VDD nets

DDR3 RDIMM PDN Analysis

- Mother board PDN can be modeled by equivalent Capacitor which has series R/L

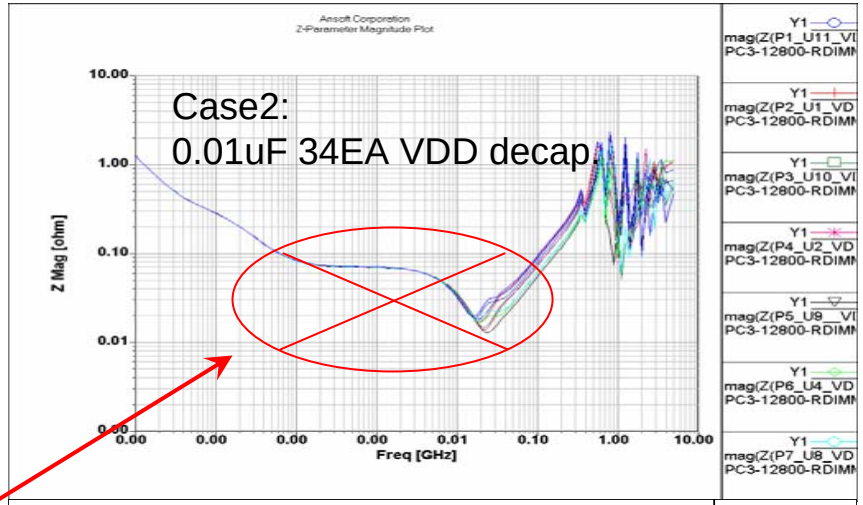


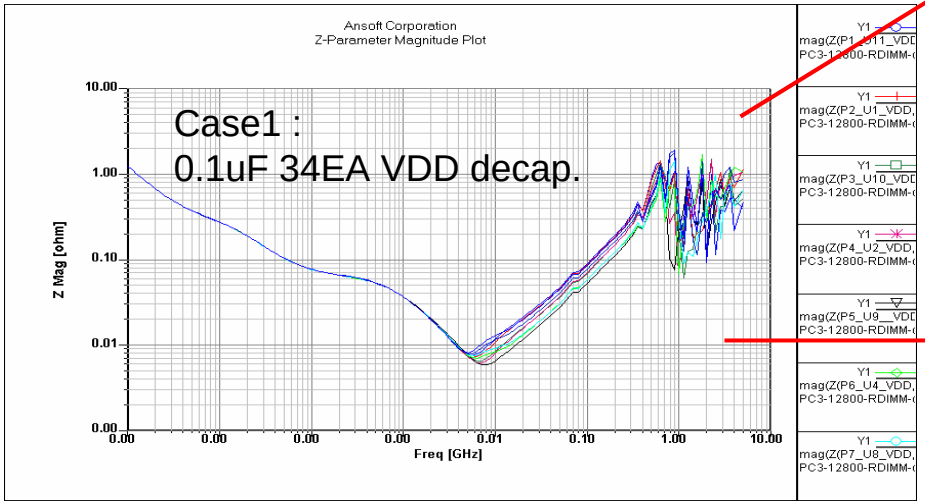
What If ? De-Cap. Change

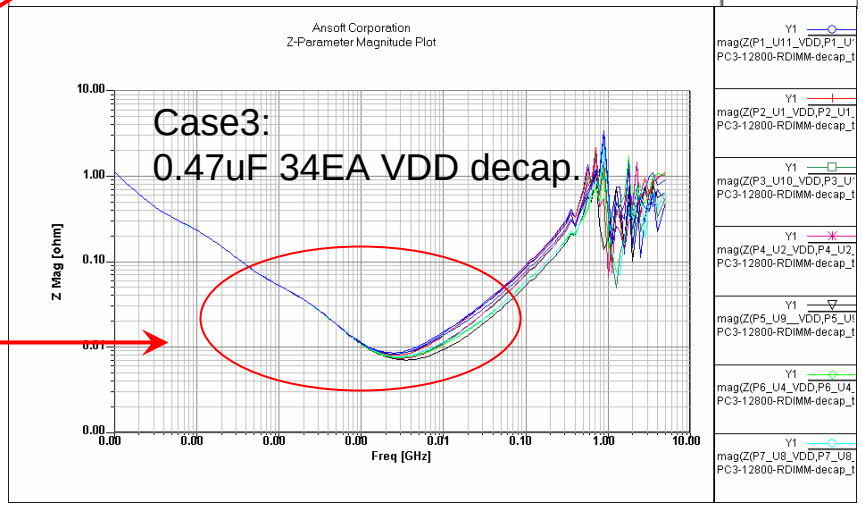


What If ? De-Cap. Change

- De-Cap. Tuning
  - Case1 : 0.01uF (34EA, VDD De-cap.)
  - Case2 : 0.1uF (34EA, VDD De-cap.)
  - Case3 : 0.47uF (34EA, VDD De-cap.)







Introducing: Memory System Virtual Test Wizard

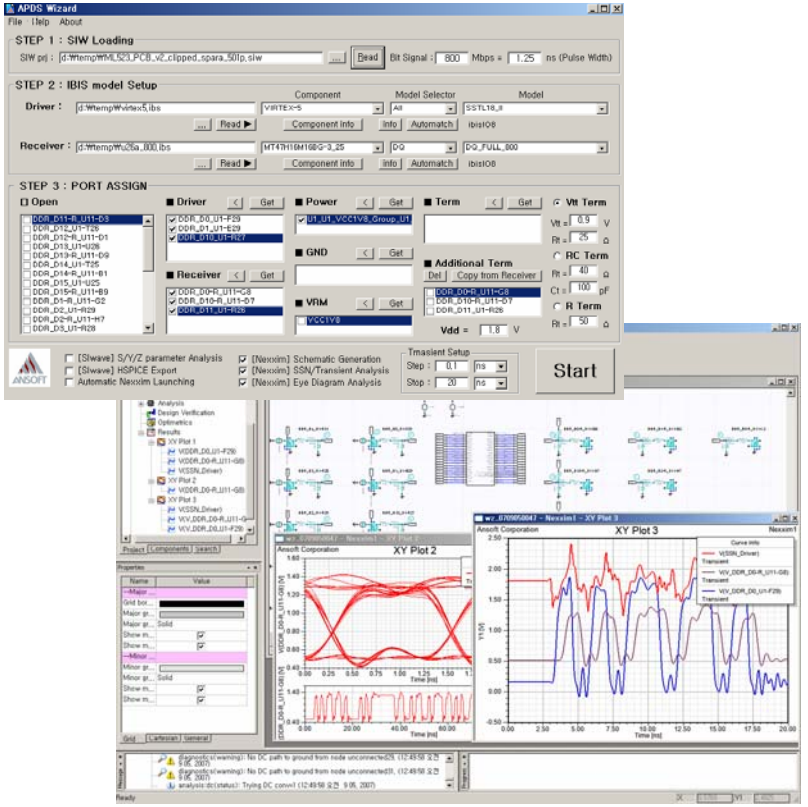
(Ansoft PCB Design Suite Wizard)

FIRST-PASS SYSTEM SUCCESS

APPLICATION WORKSHOPS FOR HIGH-PERFORMANCE ELECTRONIC DESIGN

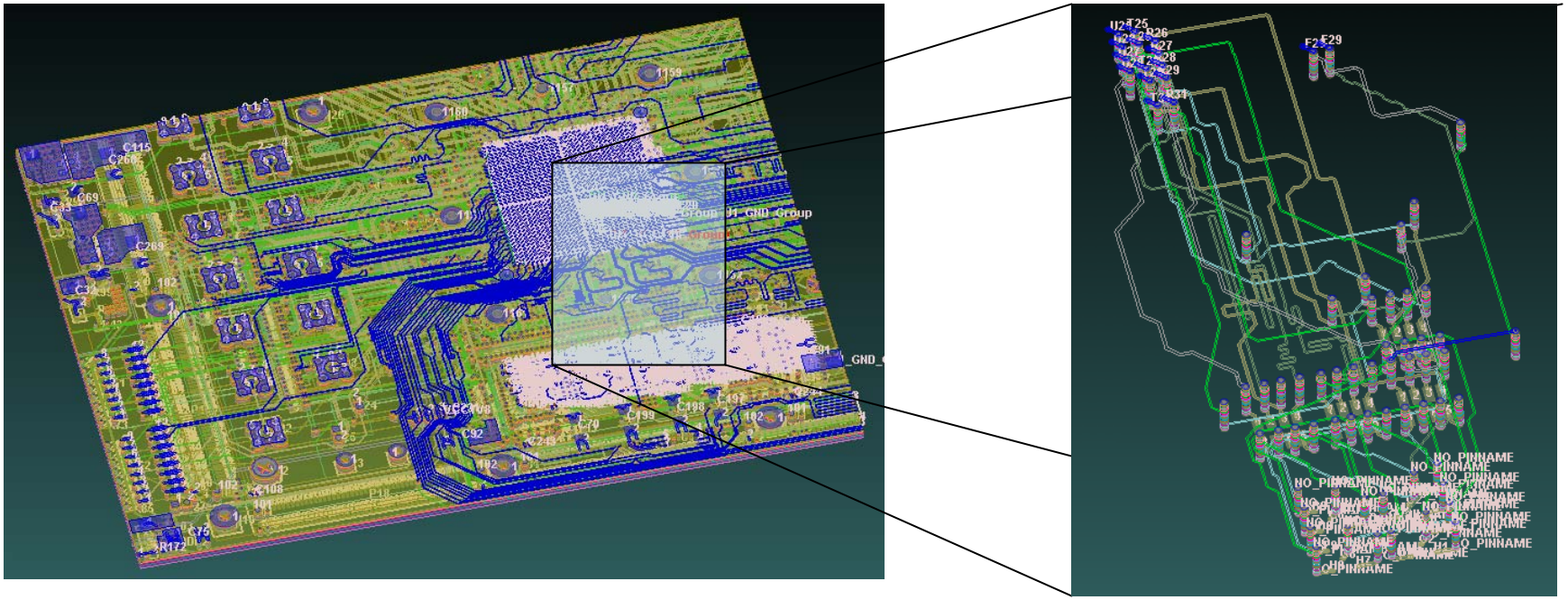
APDS Wizard Demo

SSN & Eye-Diagram
for High Speed Memory Data Bus



Simulation Target

Memory Controller

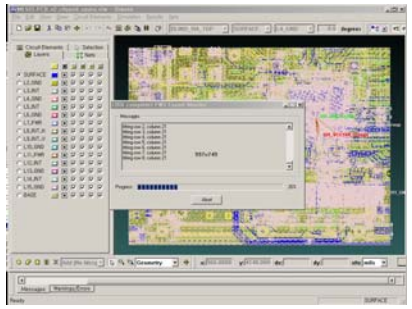


DDR2 Memory

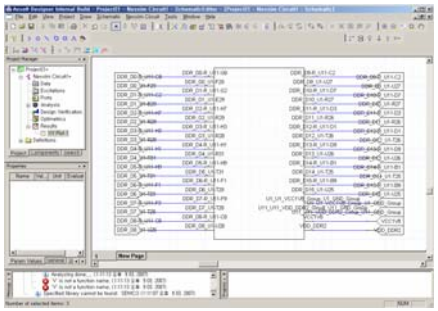
Checking data Lines: Controller IC-to-DDR2 Memory

→ it's a critical path for High-Speed Memory

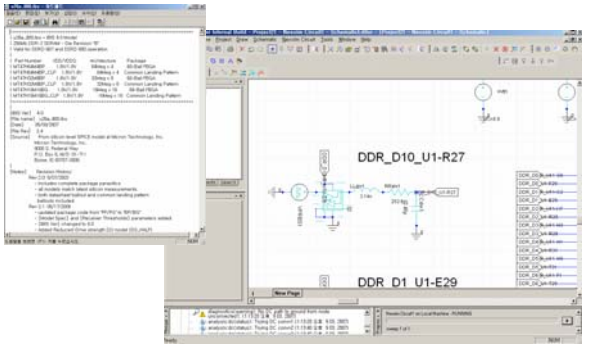
Previously …



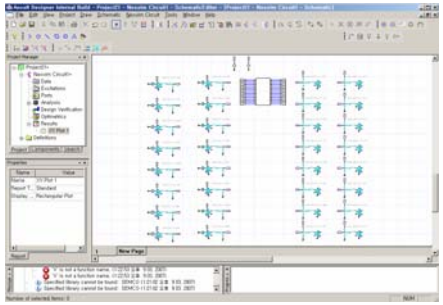
1. PCB S/Y/Z parameter Simulation
SPICE Model Extraction



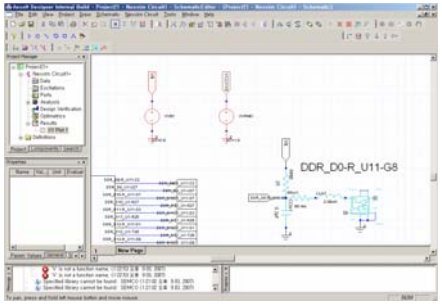
2. Import SPICE model
Assign port name at each pin



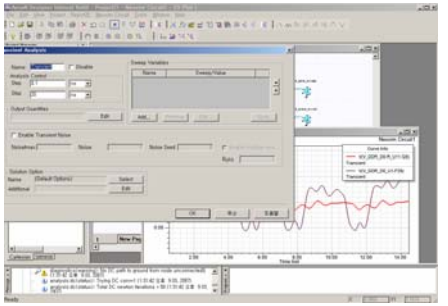
3. Apply package models..
Check up IBIS files..
Set up IBIS buffer models..



4. Copy & paste & modify…
repetition, repetition …



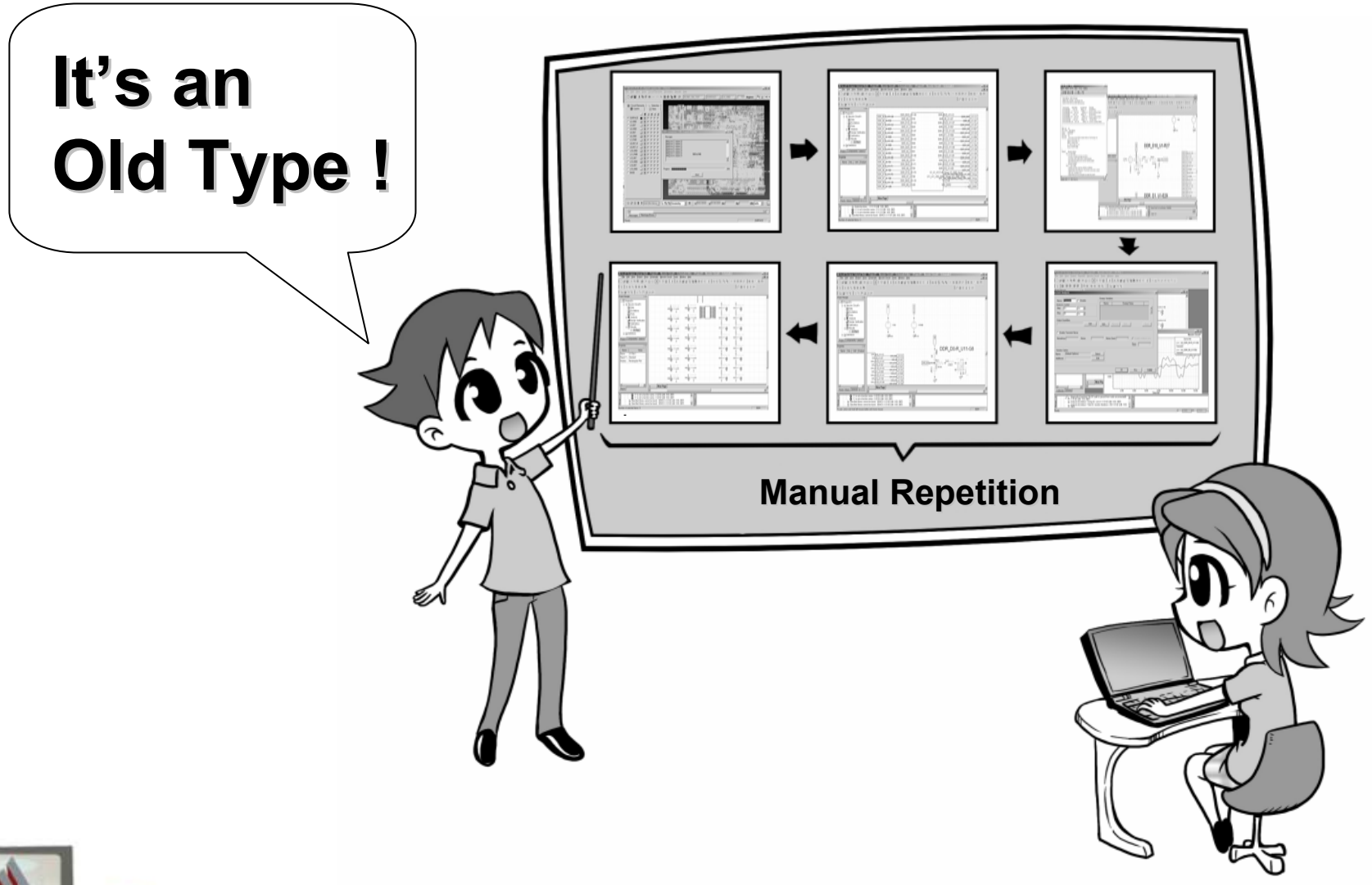
5. Assign Vdd & GND…
Attach voltage probe…
Routing…



6. Setup simulation….
Analyzing….
make Report….

Previously, these steps were completed manually.

And..



Now!

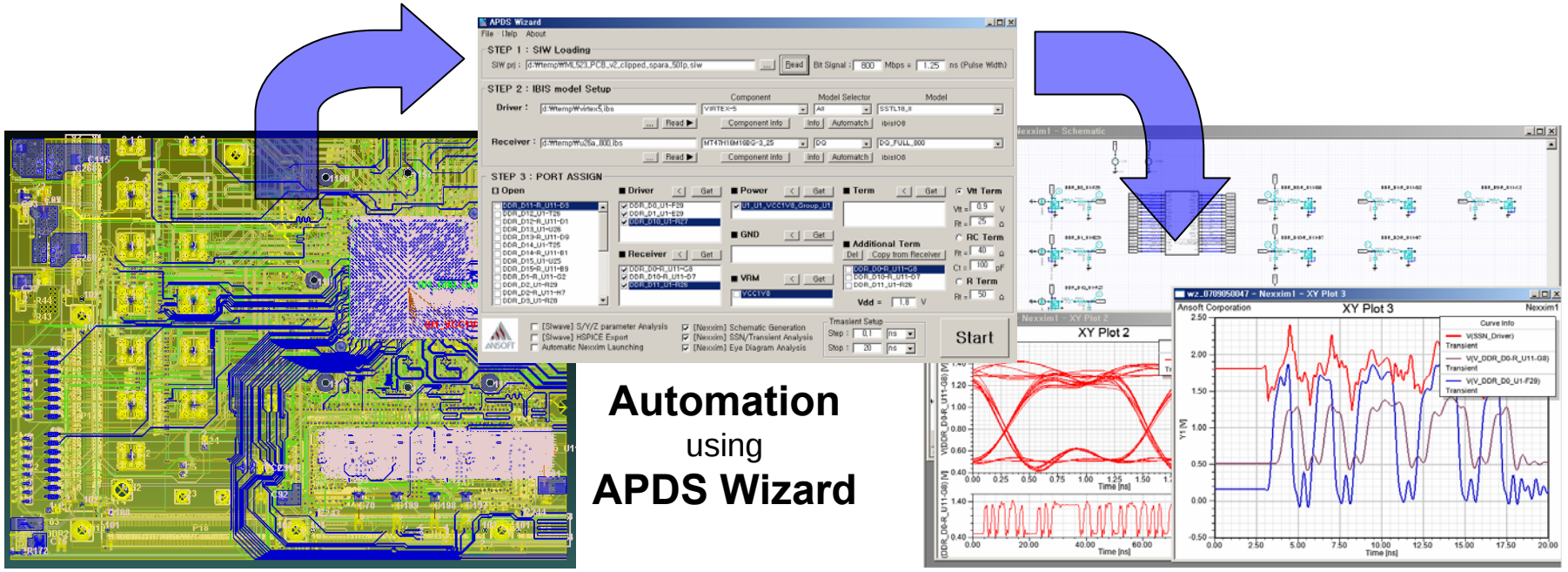
“ What you have to check up ”

PCB Layout

JUMP UP !

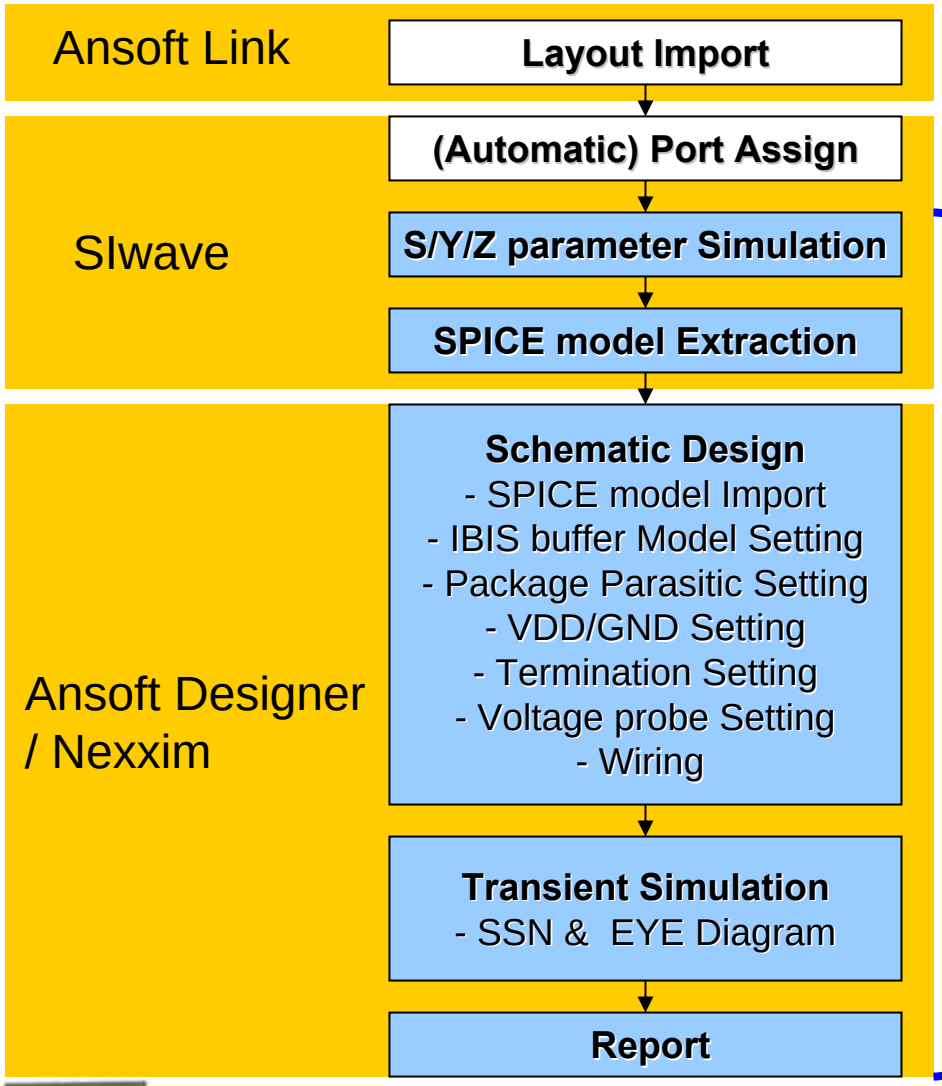
“ What you want ”

Simulation Result



Automation
using
APDS Wizard

Automation Process



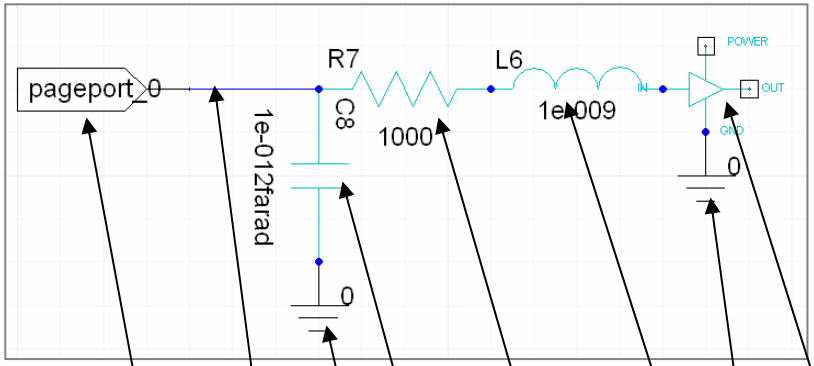
Save Time,

Eliminate Steps!

Automation!

Using VBscript & Visual Basic

What is VB Script?



- All Design Processes can be reproduced and modified by Visual Basic Script

IBIS Model

```
Array("NAME:ComponentProps", "Name:=", "IbisInput4", "Id:=", _
 "5", Array("NAME:CellLayerMerger", "DrawLayers:=", Array("Measures:Measures", _
 "Rats:Rats", "Errors:Errors", "Symbols:Symbols"))), Array("NAME:Attributes", "Page:=", _
 1, "X:=", -0.01016, "Y:=", 0.00508, "Angle:=", 0, "Flip:=", false)
```

Inductor

```
oEditor.CreateComponent Array("NAME:ComponentProps", "Name:=", "IND_", "Id:=", "6", Array("NAME:CellLayerMerger", "DrawLayers:=", Array( _
 "Measures:Measures", "Rats:Rats", "Errors:Errors", "Symbols:Symbols"))), Array("NAME:Attributes", "Page:=", _
 1, "X:=", -0.01778, "Y:=", 0.00508, "Angle:=", 0, "Flip:=", false)
```

Resistor

```
oEditor.CreateComponent Array("NAME:ComponentProps", "Name:=", "Res_", "Id:=", "7", Array("NAME:CellLayerMerger", "DrawLayers:=", Array( _
 "Measures:Measures", "Rats:Rats", "Errors:Errors", "Symbols:Symbols"))), Array("NAME:Attributes", "Page:=", _
 1, "X:=", -0.02794, "Y:=", 0.00508, "Angle:=", 0, "Flip:=", false)
```

Capacitor

```
oEditor.CreateComponent Array("NAME:ComponentProps", "Name:=", "Cap_", "Id:=", "8", Array("NAME:CellLayerMerger", "DrawLayers:=", Array( _
 "Measures:Measures", "Rats:Rats", "Errors:Errors", "Symbols:Symbols"))), Array("NAME:Attributes", "Page:=", _
 1, "X:=", -0.03302, "Y:=", 0, "Angle:=", 4.71238898038469, "Flip:=", false)
```

GND1

```
oEditor.CreateGround Array("NAME:GroundProps", "Id:=", 18), Array("NAME:Attributes", "Page:=", _
 1, "X:=", -0.03302, "Y:=", -0.00762, "Angle:=", 0, "Flip:=", false)
```

GND2

```
oEditor.CreateGround Array("NAME:GroundProps", "Id:=", 23), Array("NAME:Attributes", "Page:=", _
 1, "X:=", -0.01016, "Y:=", 0, "Angle:=", 0, "Flip:=", false)
```

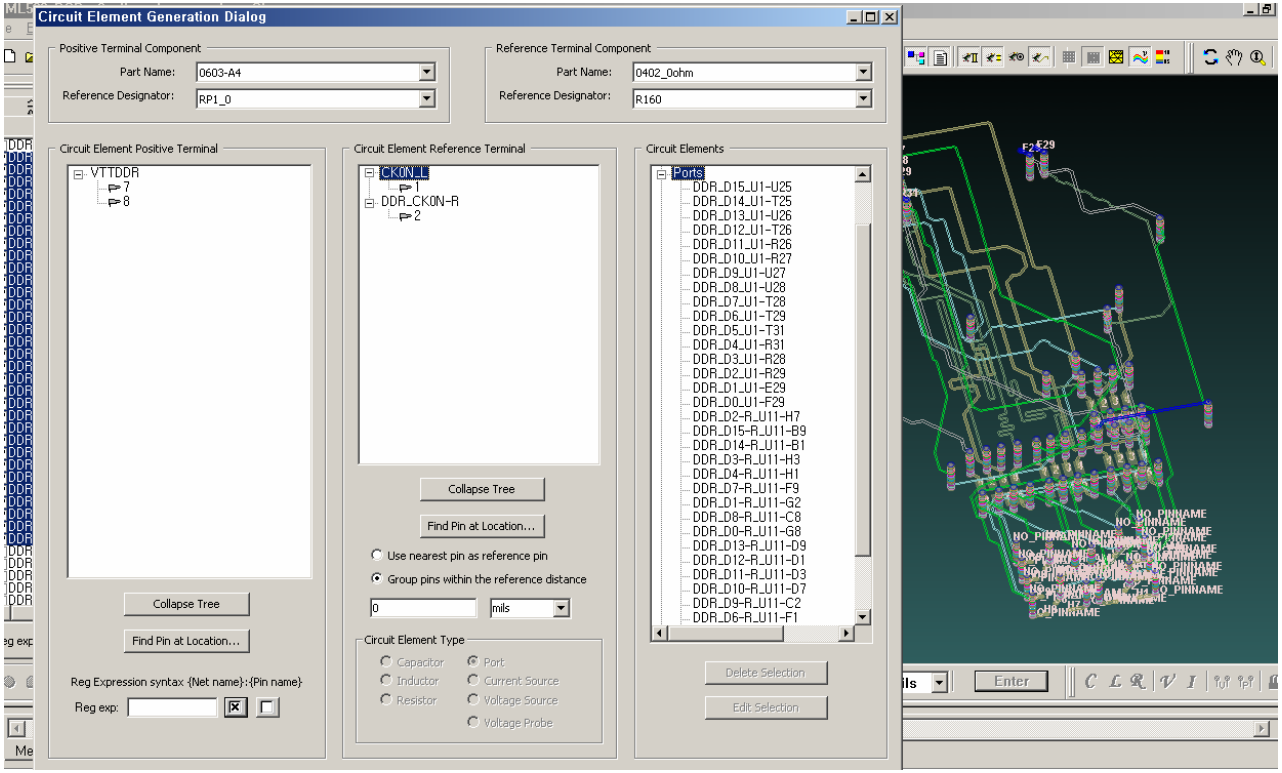
```
oEditor.CreatePagePort Array("NAME:PagePortProps", "Name:=", "pageport_0", "Id:=", _
 28), Array("NAME:Attributes", "Page:=", 1, "X:=", -0.04064, "Y:=", 0.00508, "Angle:=", 0, "Flip:=", false)
```

PagePort

```
oEditor.CreateWire Array("NAME:WireData", "Name:=", "", "Id:=", 32, "Points:=", Array( _
 "(-0.040640, 0.005080)", "(-0.033020, 0.005080)")), Array("NAME:Attributes", "Page:=", 1)
```

Wire

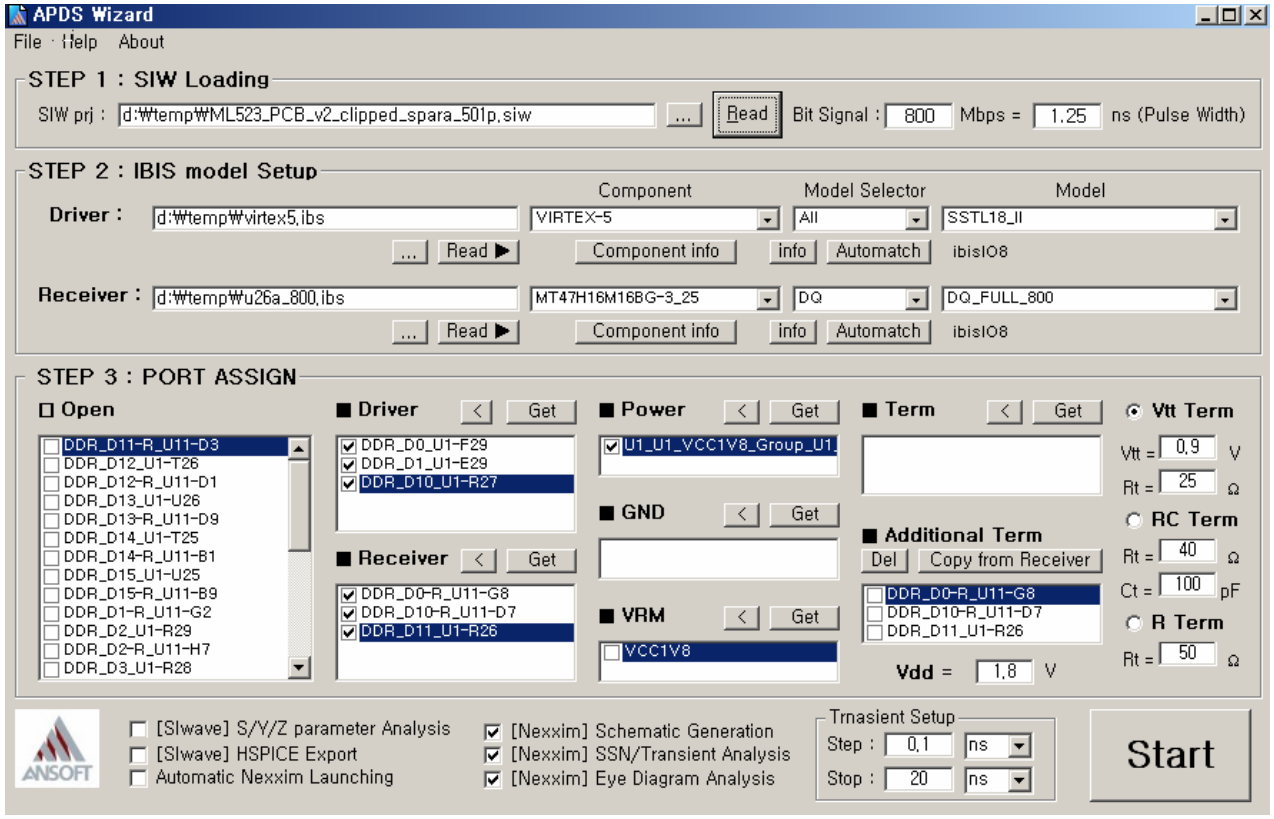
Port Assignments on PCB Line



1. **Import layout data & component information to SIwave**
2. **Just Select PCB lines to simulate.**
   → SIwave will automatically generate the ports

That's ALL that you have to do…

APDS Wizard



Slwave file Loading

↓

IBIS file Loading

↓

IBIS Component & Model Selection

↓

Port Assign

↓

Add Termination Check Probe Point

↓

Simulation Setting

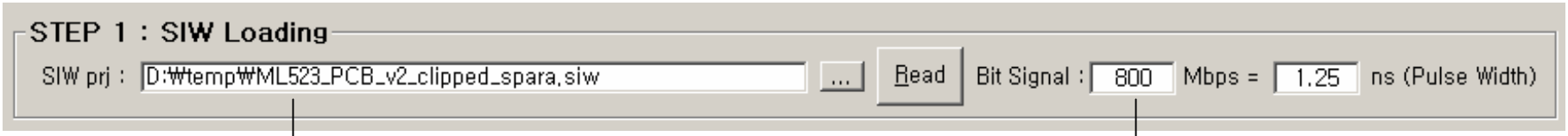
You don't need simulation skill.

Just Use.

FIRST-PASS SYSTEM SUCCESS

APPLICATION WORKSHOPS FOR HIGH-PERFORMANCE ELECTRONIC DESIGN

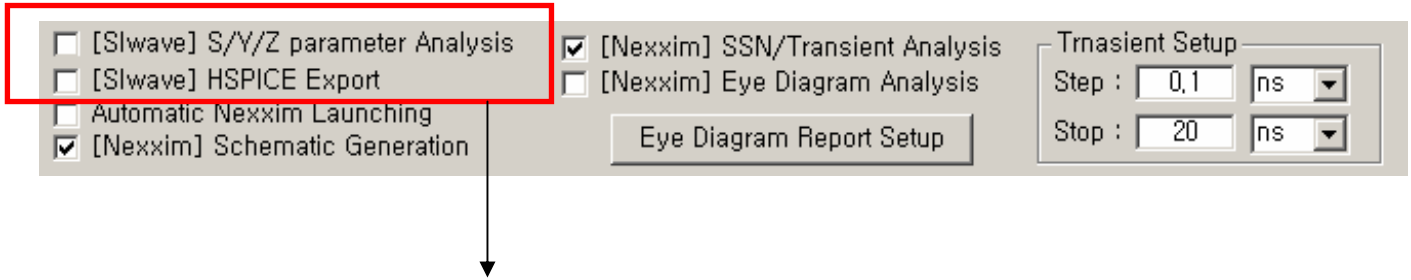
Step #1 – SIW Loading



1. Load the SIwave file with pre-assigned ports

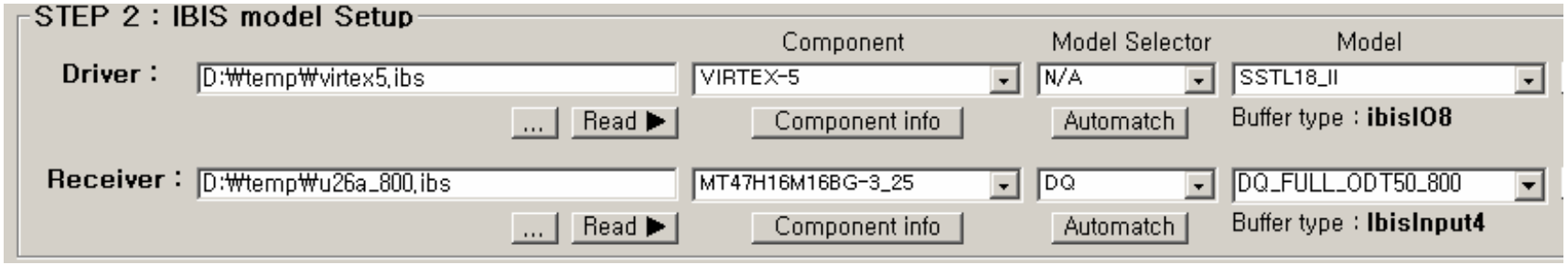
2. Input the data speed of memory

→ to decide the sweep range of S parameter simulation



3. Check this option for S parameters simulation & SPICE extraction using SIwave

Step #2 – IBIS File Analysis

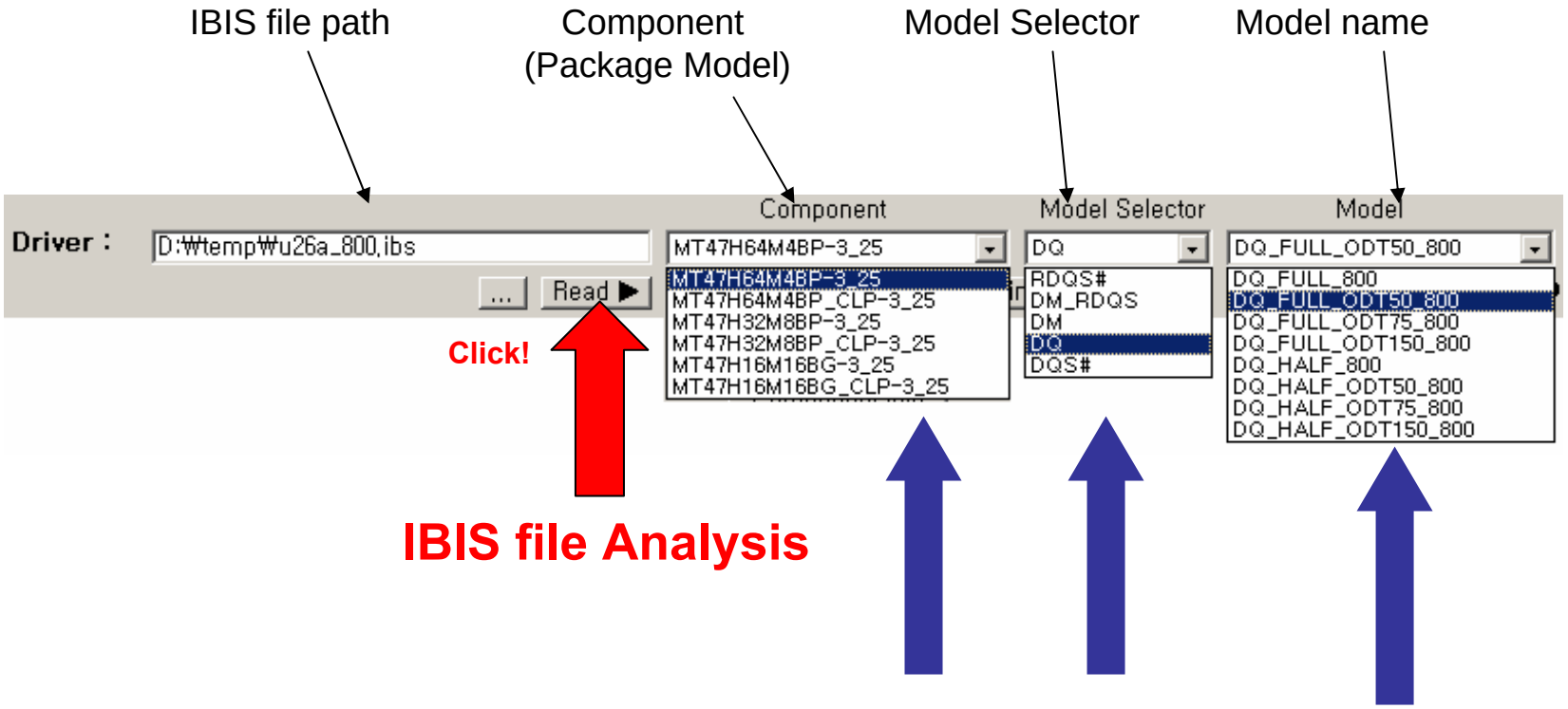


APDS wizard contains **Intelligent** **IBIS file Analysis Engine**

Major functions of IBIS file Analysis Engine

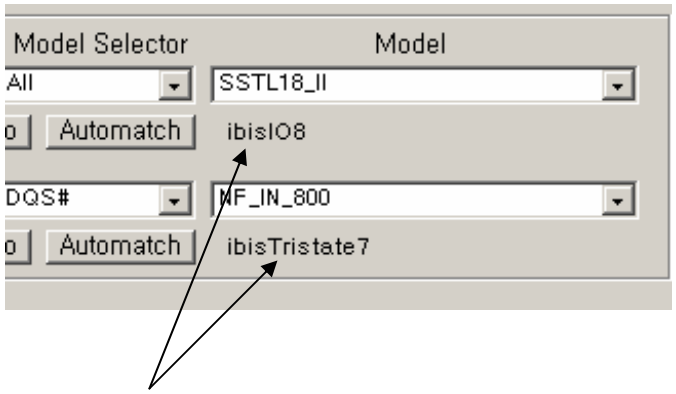
- Extract all package models (Components) at each pin.
- Extract Typical & Min & Max R/L/C parasitic for each component
- Model selector listing & auto-mapping with models
- Extract all model information such as model_type, VDD/GND clamp…
- Automatic composite IBIS buffer model name for Nexxim at each model
- Intelligent Handling for IBIS file with off-standard format (IBIS rule check engine)

Step #2 – IBIS File Analysis



Just select what you need!
Components, Model Selector, Model

Step #2 – IBIS File Analysis



Model type generation for Nexxim simulation

When a model name is selected ,
IBIS file analysis engine checks the model_type & clamp condition of that pin in the IBIS file and then composes the model type for the Nexxim simulation at the same time.

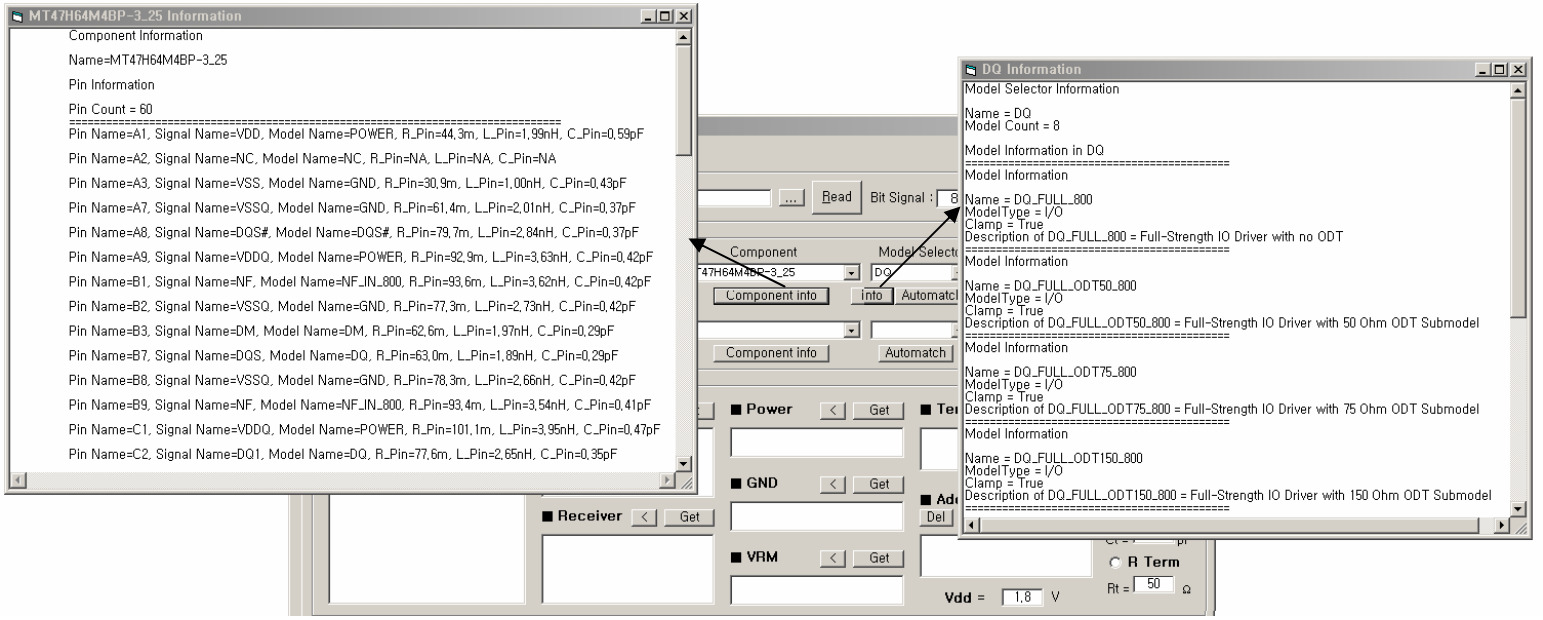
Ex) pin model : **SSTK18_II**

Model_type in IBIS file : I/O
Clamp : exist at VDD & GND node

→ Needs **I/O with Clamp** type buffer.
→ automatically generate model name "**ibisIO8**" for IBIS model of Nexxim

Step #2 – IBIS File Analysis

IBIS File Information

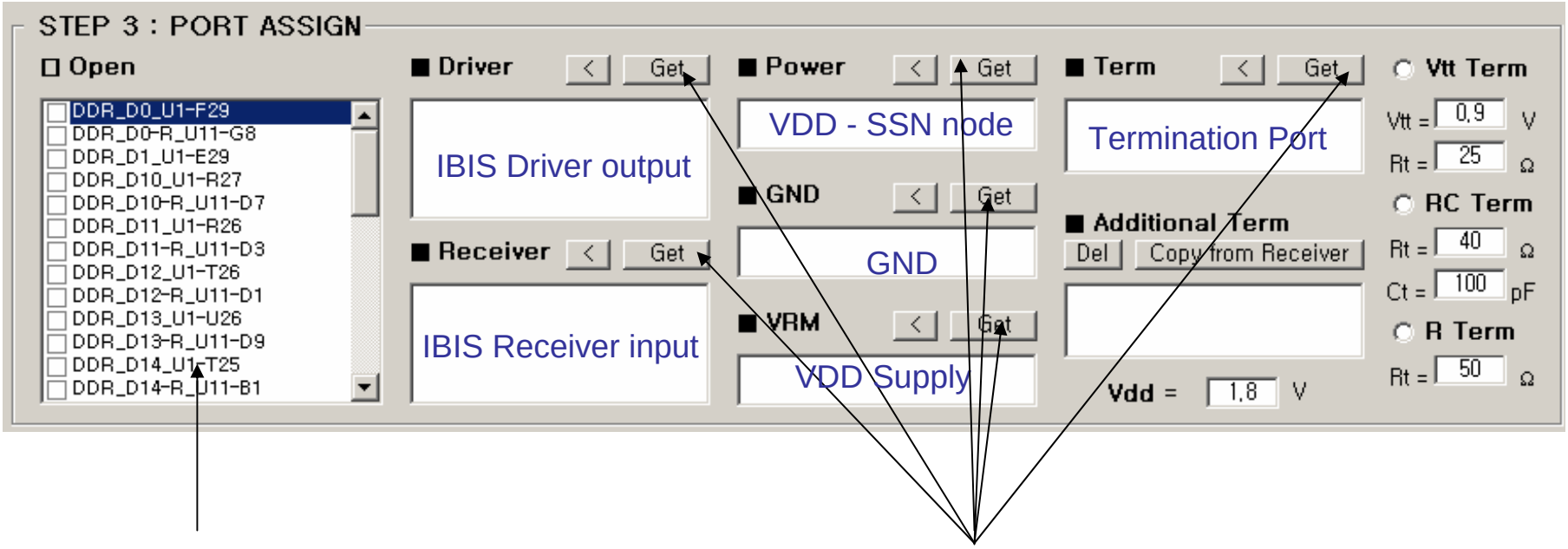


Main information of the IBIS file is presented in the APDS wizard

Component description, package models, model type, signal name of each pin …

Note: Don't open & read IBIS file with text editors such as Notepad, VI, etc. ☺

Step #3 – Port Assignments



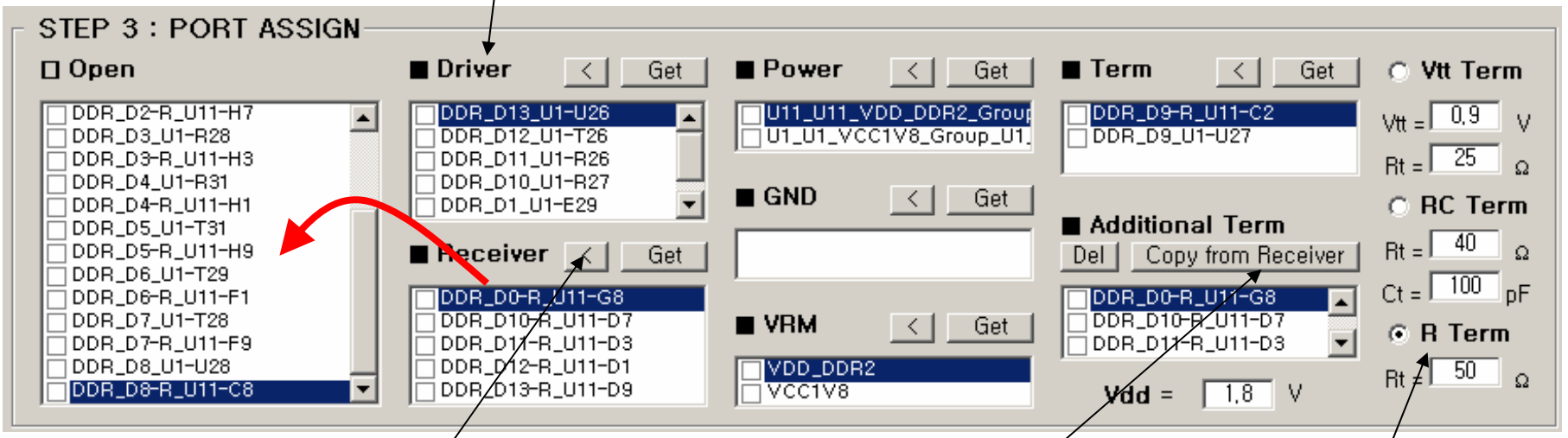
1. When you read SIwave file(*.siw) ,
   All PCB ports will load to Open Port List

2. You can move ports to any port list from open port by clicking **Get** Button

Very Simple & Easy

Step #3 – Port Assignments

All ports in each list can be checked at once by clicking the port name (toggle)

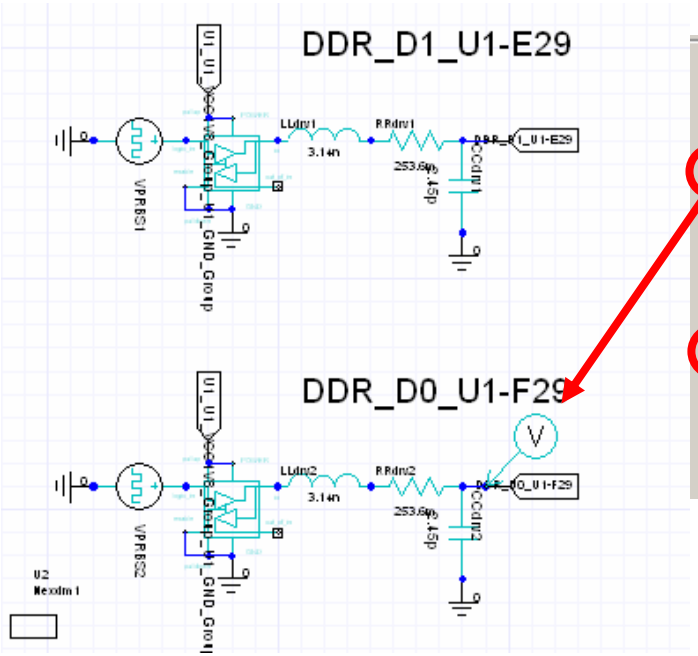


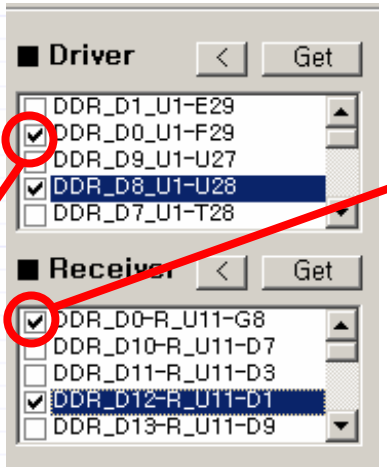
3. Return the ports to open port list by clicking " < " button

4. Select termination type

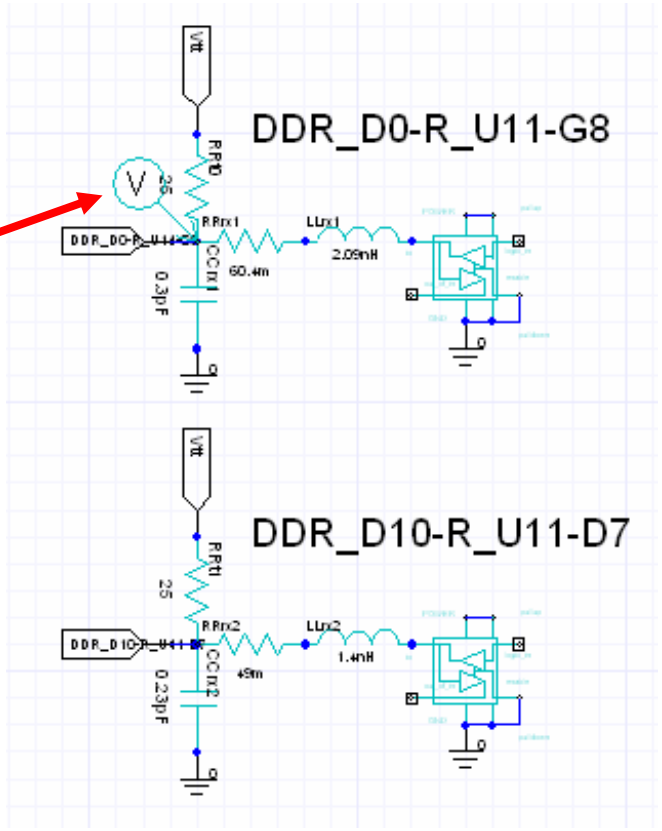
5. If it's needed, add external termination to all receiver ports by clicking the "Copy from Receiver" button once.

Step #3 – Port Assignments





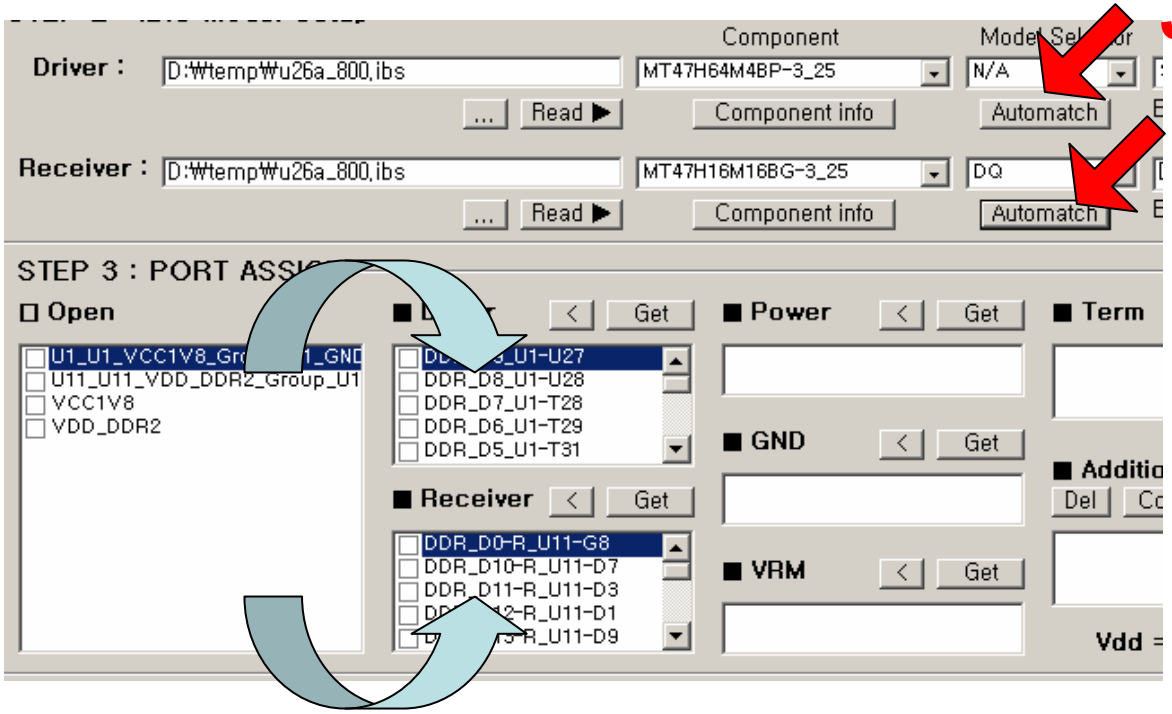
Auto Probing



Check the box adjacent to any port whose voltage is to be plotted.
A probe will appear next to all selected ports.

Step #3 – Port Assignments

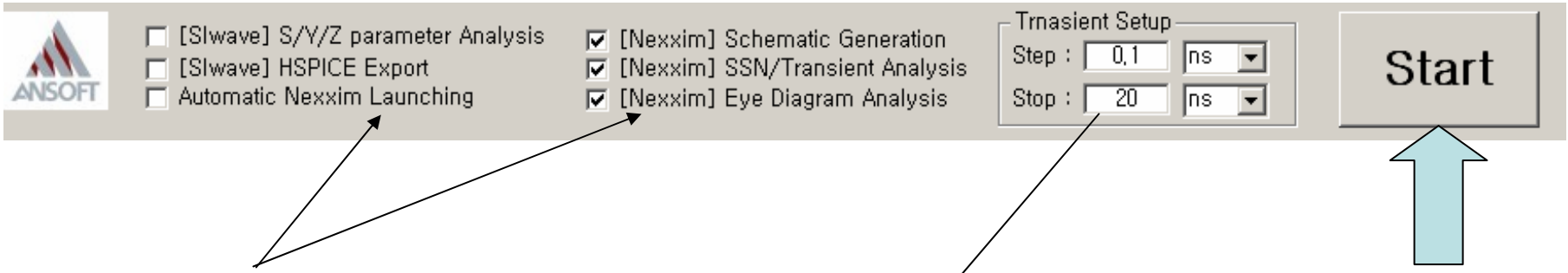
Automatch



Just 1 Click!

The Automatch option will assign all Driver & Receiver ports at once, by checking the SIwave port name and pin name in the IBIS file.

Last Step – Optional Setting

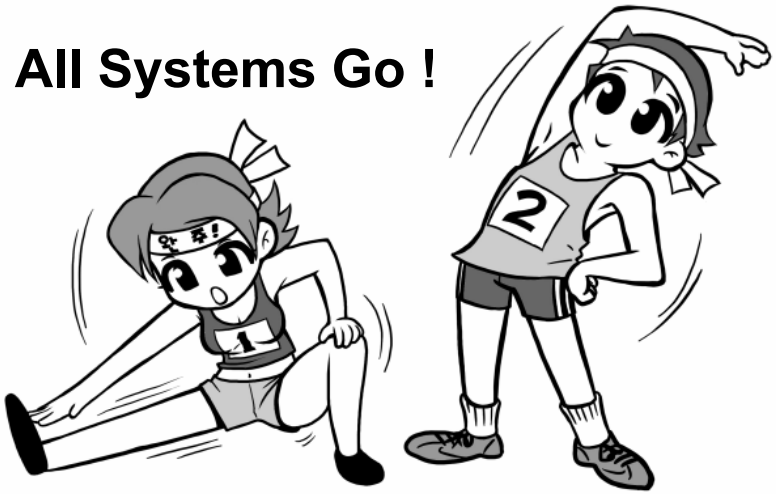


1. Select function to automate.

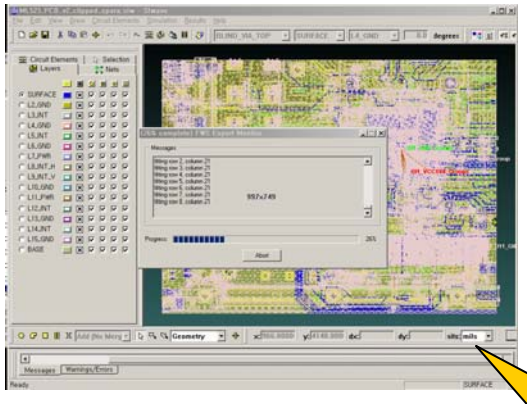
2. Setup simulation conditions.

3. Run!

All Systems Go !



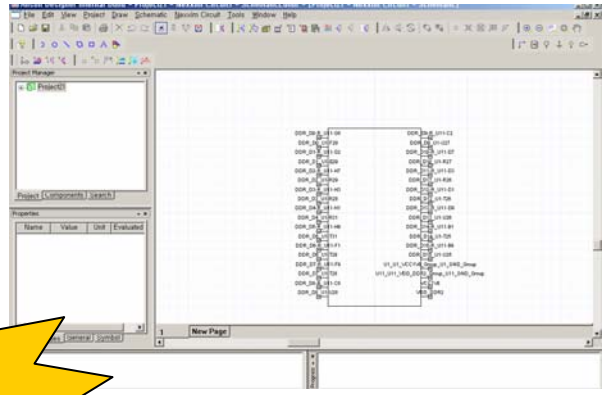
Wizard Start!

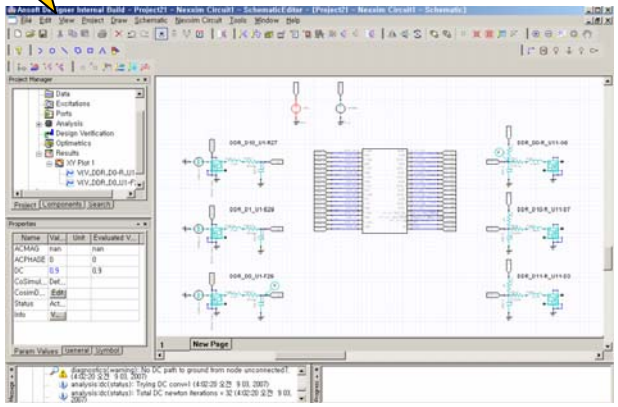


- PCB Line S/Y/Z Simulation
  SPICE model Extraction

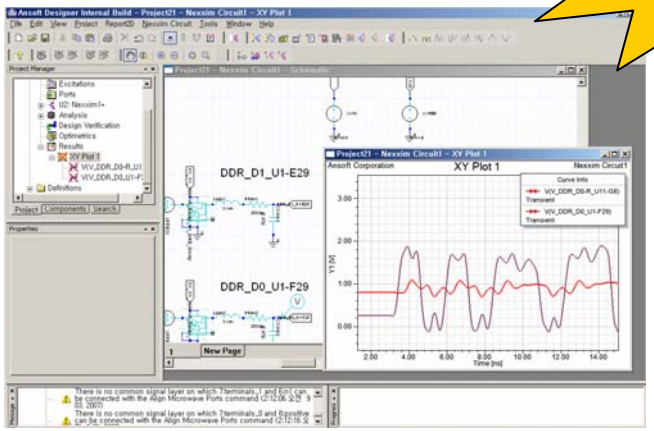
AUTOMATIC !

2. SPICE Model Import



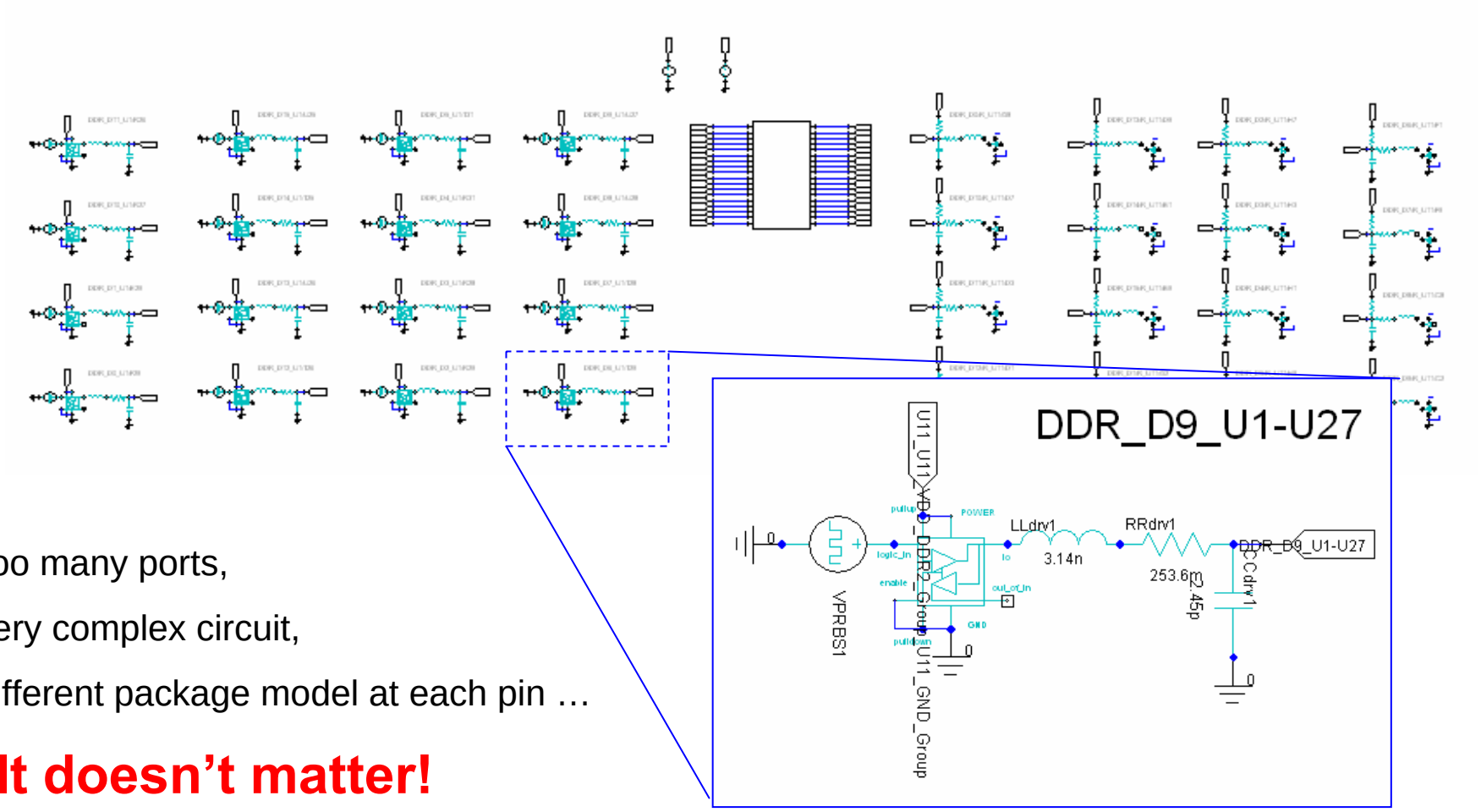


3. Schematic Generation



4. Transient Simulation & Report

Automatic Schematic Generation



Too many ports,

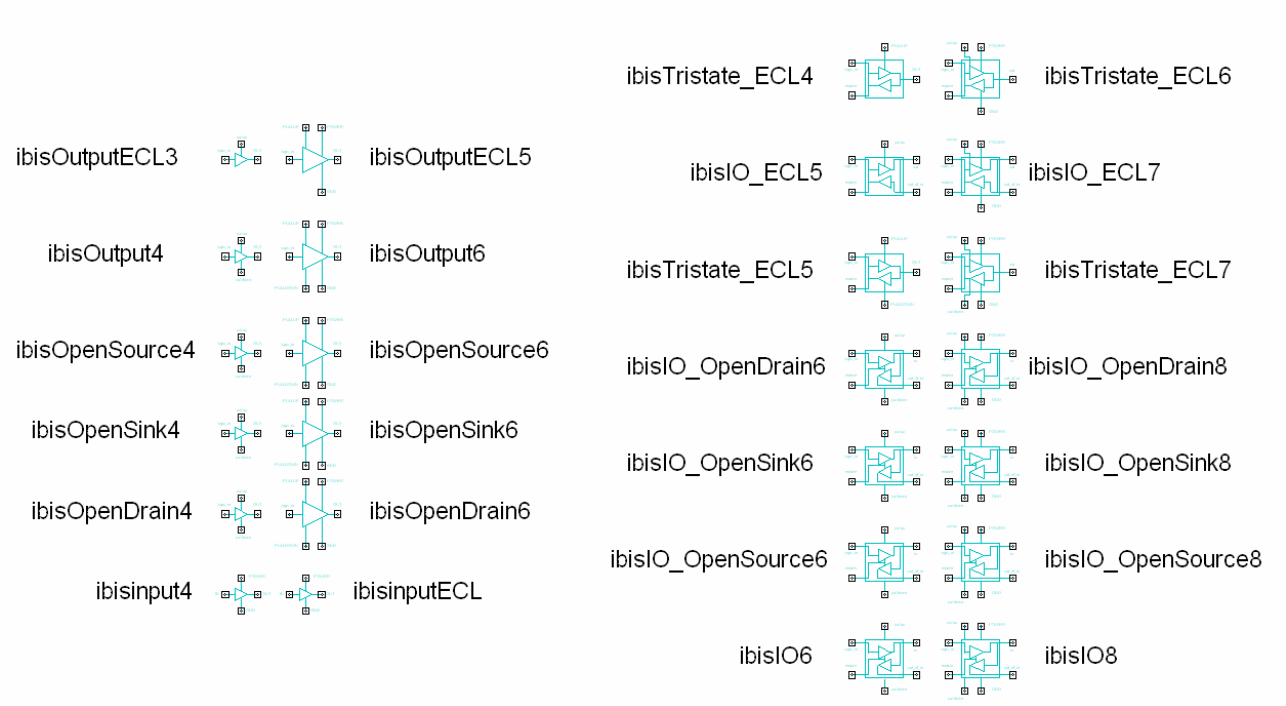
Very complex circuit,

Different package model at each pin …

It doesn't matter!

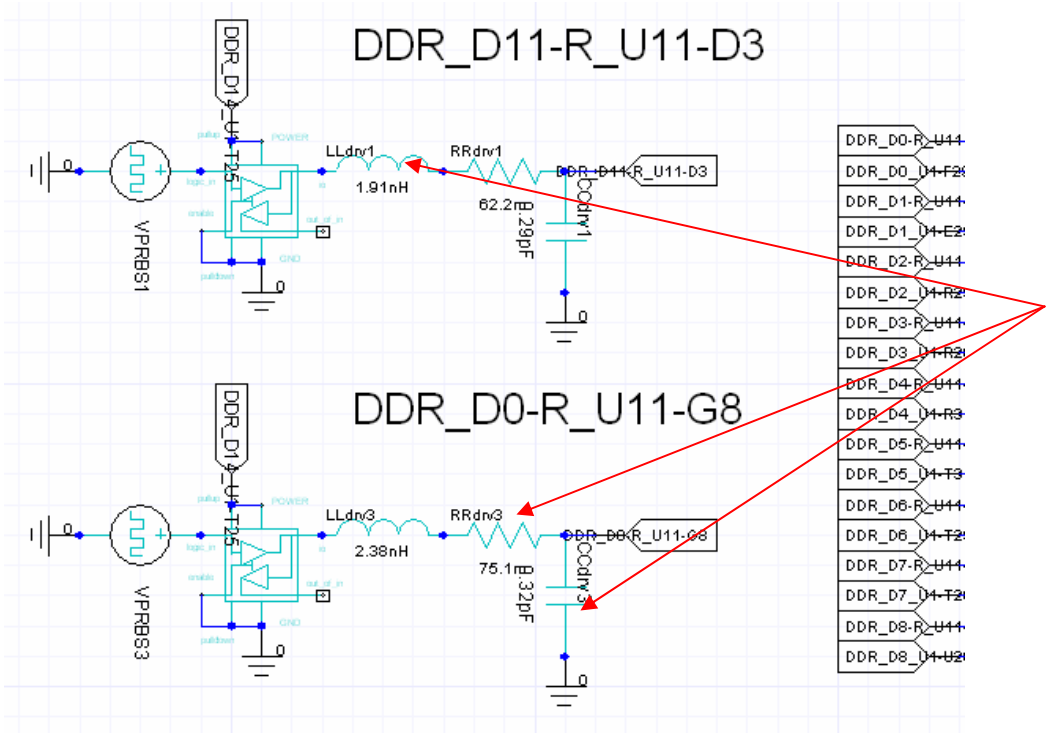
Simply watch the animation of the schematic being generated ☺

IBIS models in NEXXIM



APDS Wizard can generate a schematic
for any IBIS model type in NEXXIM
using the **Adaptive Schematic Generation Engine.**

R/L/C Package models



It's very important at high speeds to apply accurate package models.

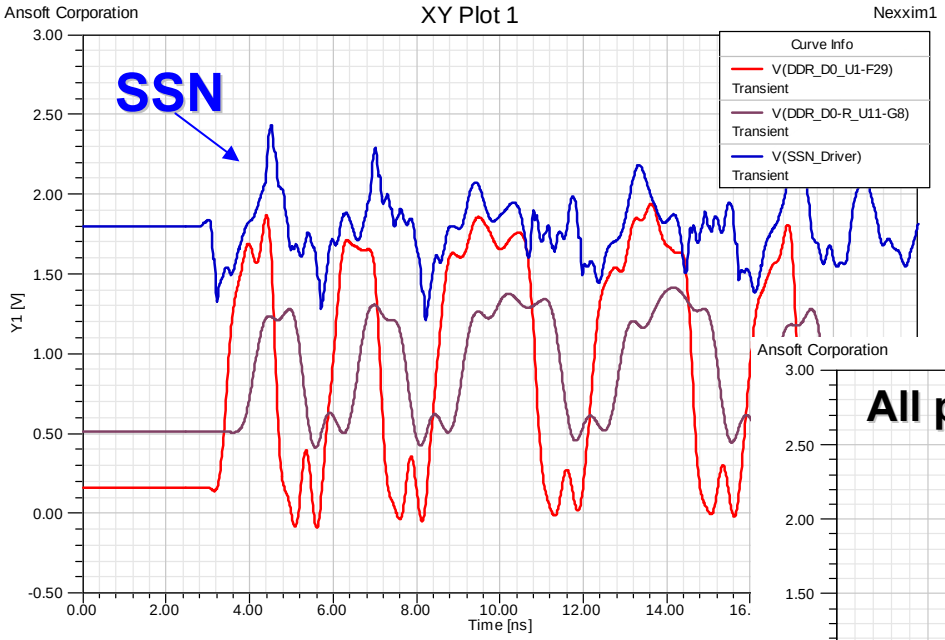
However,

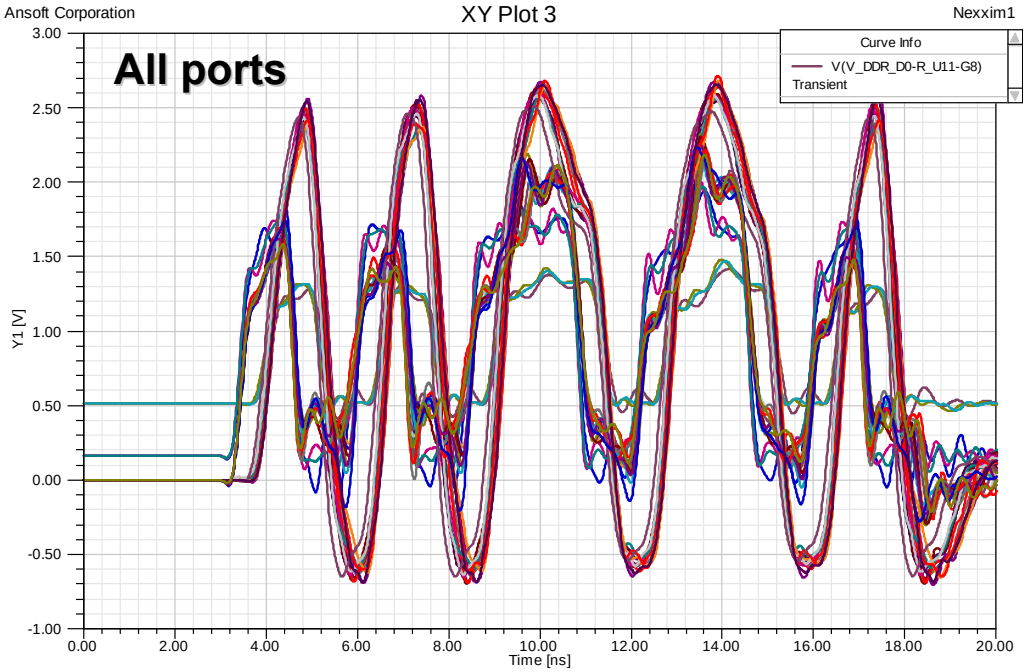
individually assigning different R/L/C parasitics to each pin/port is time consuming & prone to error.

Now, the APDS Wizard allows R/L/C parasitics to be applied rapidly and accurately.

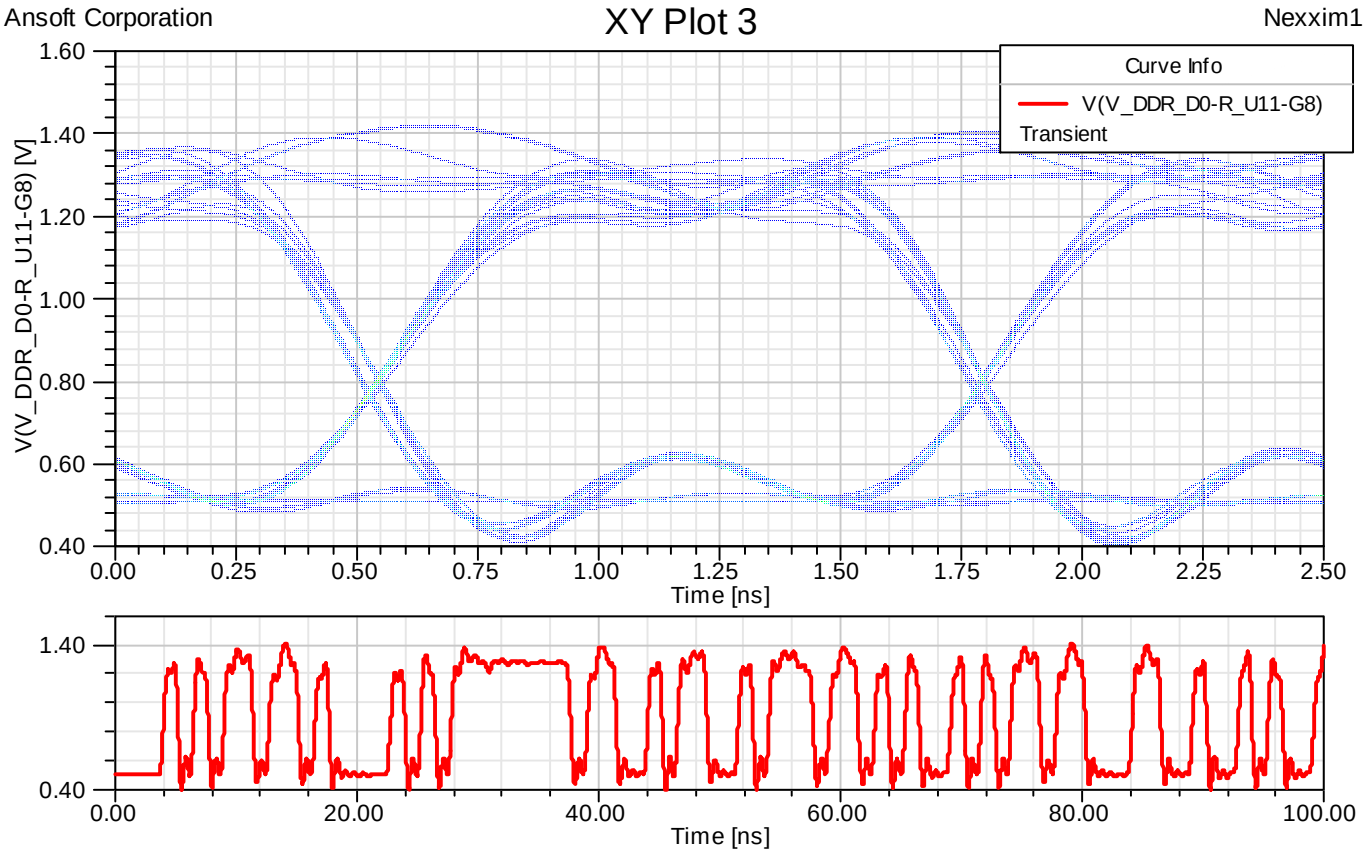
Note: If the IBIS file doesn't have exact parasitic information for each pin, the APDS Wizard will extract typical parasitic values from the IBIS file and will automatically apply these to all R/L/C components.

Simulation Result - SSN





Eye-Diagram

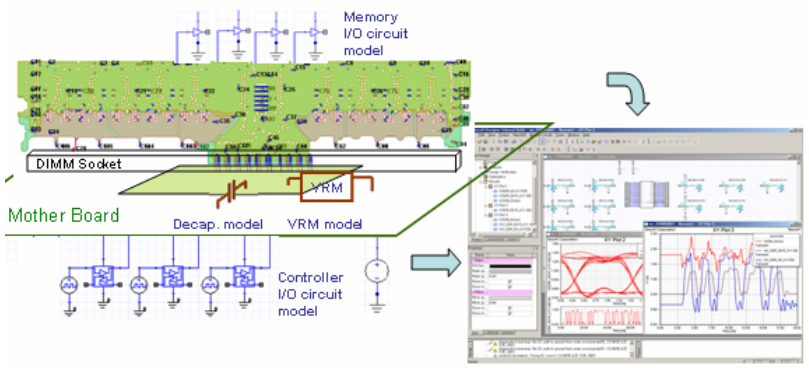


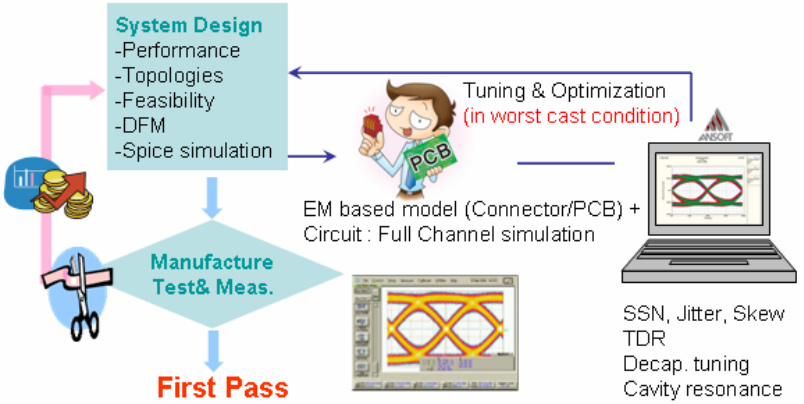
Automatic Simulation & Eye-Diagram Report

Summary

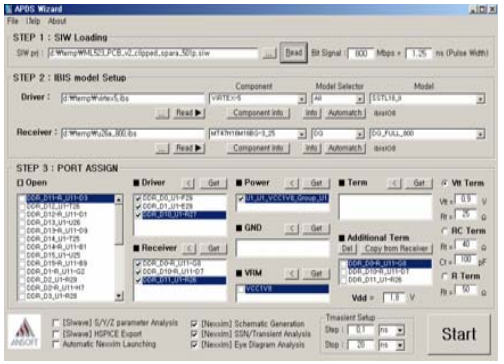
- EM-based circuit co-design

- Through examples, it was shown how simulation technology may be used to address several current, high-speed memory design challenges and, ultimately, to identify optimal first-pass designs. Specifically, we focused on:
  Signal noise analysis : Jitter, Eye-Diagram : Power noise : SSN





- The Ansoft PCB Design Suite Wizard for Eye/SSN analysis was introduced.



References

[1] UG225 (v1.1) August 6, 2007, ML52x user guide, www.xilinx.com

[2] Micron *DDR2 SDRAM* data sheet, http://download.micron.com/pdf/datasheets/dram/ddr2/256MbDDR2.pdf

[3] Hynix *DDR2 SDRAM* data sheet, http://www.hynix.co.kr/datasheet/pdf/dram/HY5PS124(8_16)21C(L)FP(Rev0.6).pdf

[4] Tom Granberg, “Handbook of Digital Techniques for High-speed Design”, Prentice Hall, pp. 156-160 and Part 3.