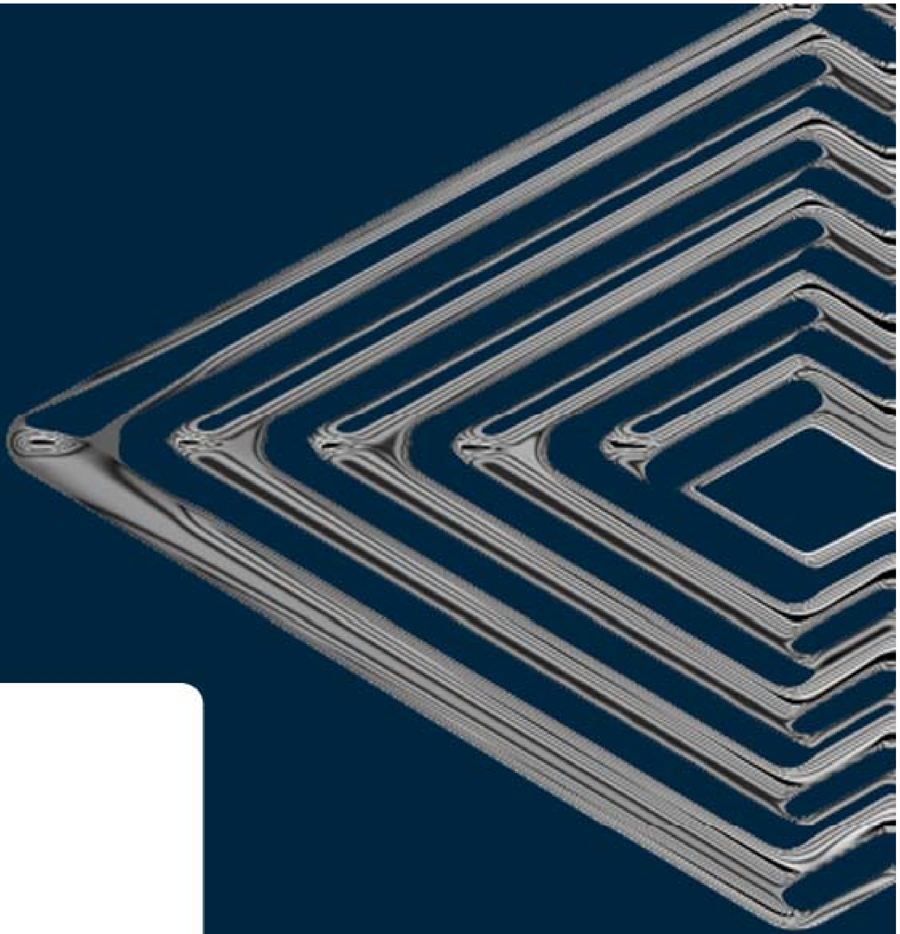


Accurate and Efficient SSN Modeling

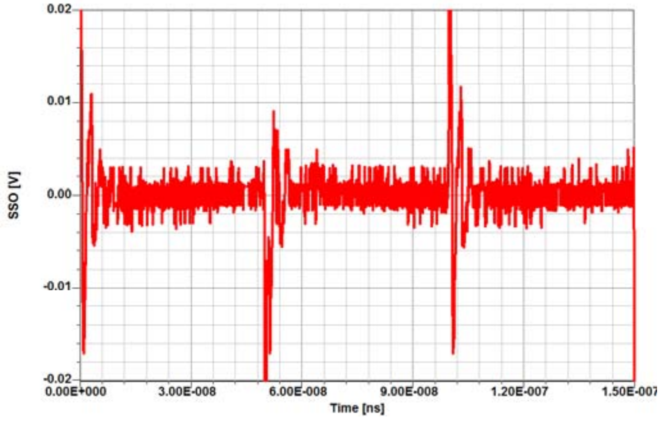
Chris Herrick

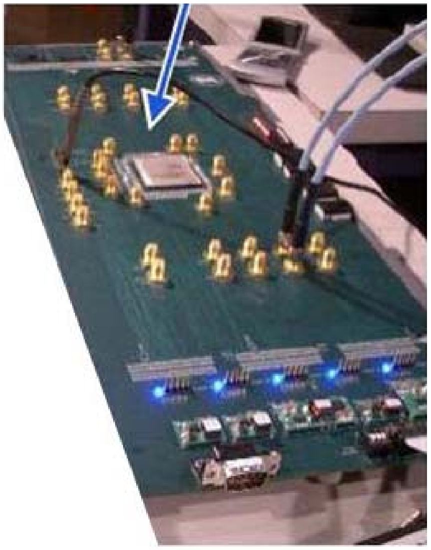
Agenda

- What is SSN?
- Model Types
- Modeling techniques
- Simulation Tips and Tricks
- Incorporating the latest Ansoft features
- Conclusions

What is SSN?

- Simultaneous Switching Noise is the deleterious effect of simultaneous switching outputs (SSO).
- Also referred to as Ground Bounce or Power Bounce
- Exacerbated by poor return path and high loop inductance
- Measured by fixing victim High or Low and monitoring output

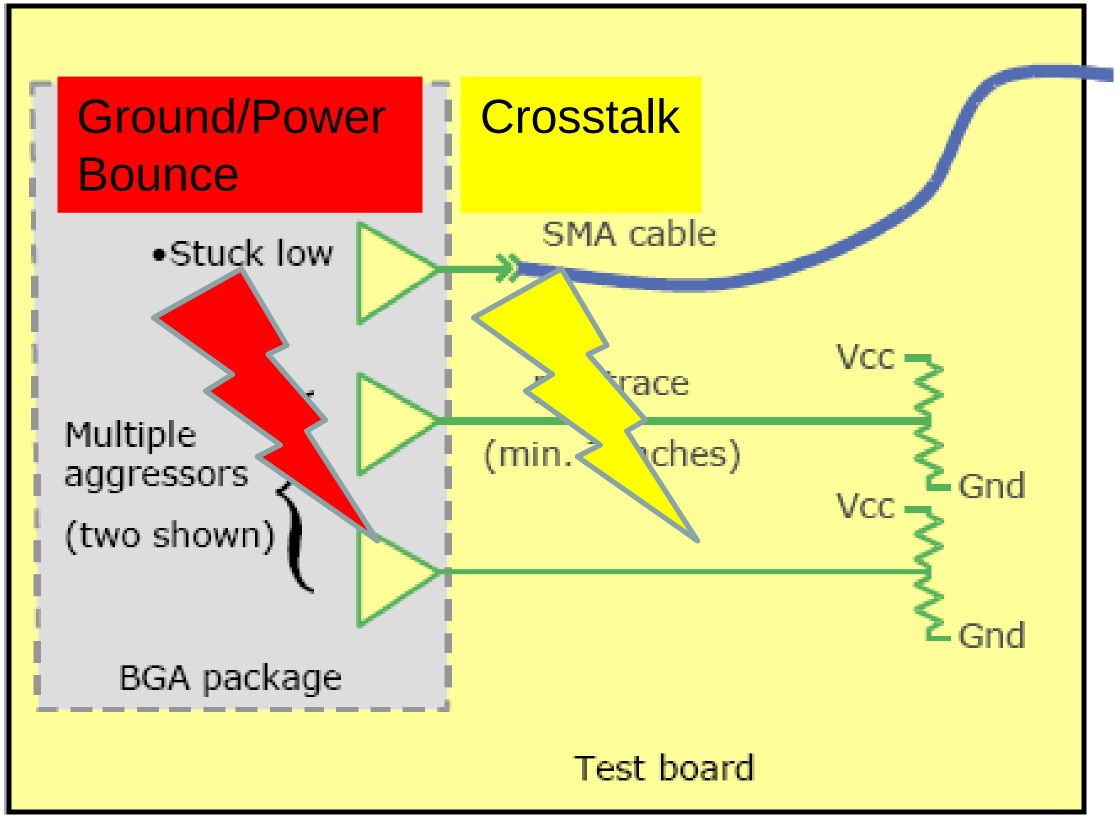




Why is SSN important?

- SSN Analysis gives more complete picture of both Signal Integrity and Power Integrity
- Ignoring the effects of SSO can result in a failed system design
- Increased challenges as speeds increase, voltages decrease and current increases
- Helps uncover problematic crosstalk
- Helps evaluate true PDN performance

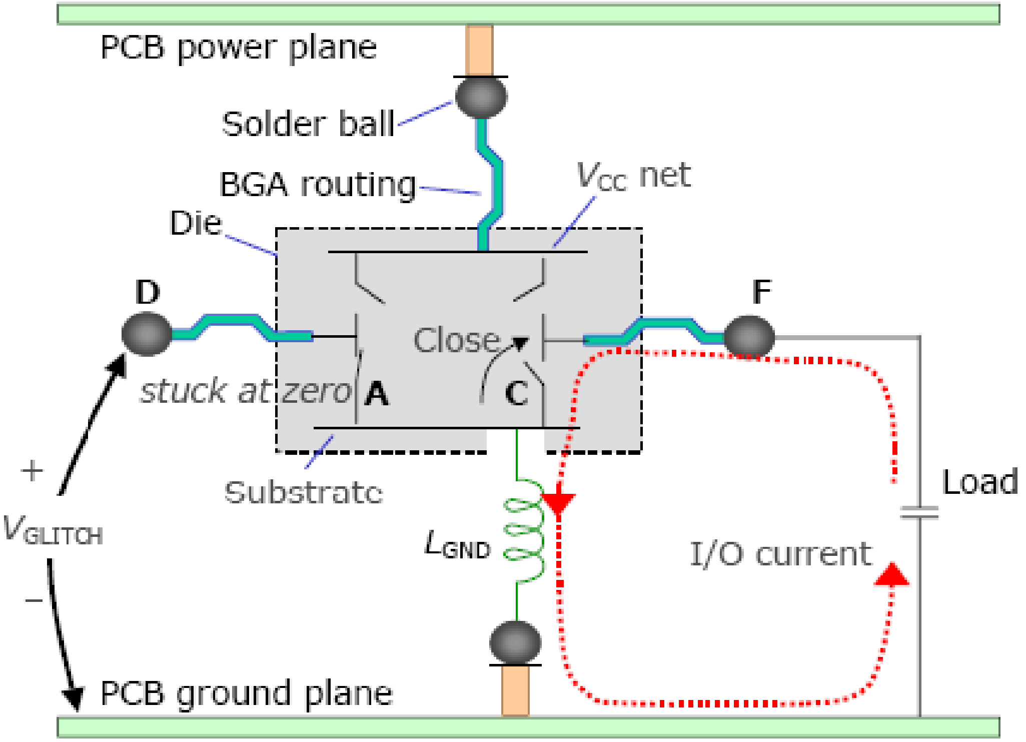
Typical Setup



- Setup
  - Victim is held “high” or “low”
  - Many I/O’s driven at the same time
  - Worst case Data Patterns transmitted
  - Noise monitored on victim from PCB location

Ref: BGA Crosstalk by Howard Johnson, March 1, 2005

SSN From Ground Bounce



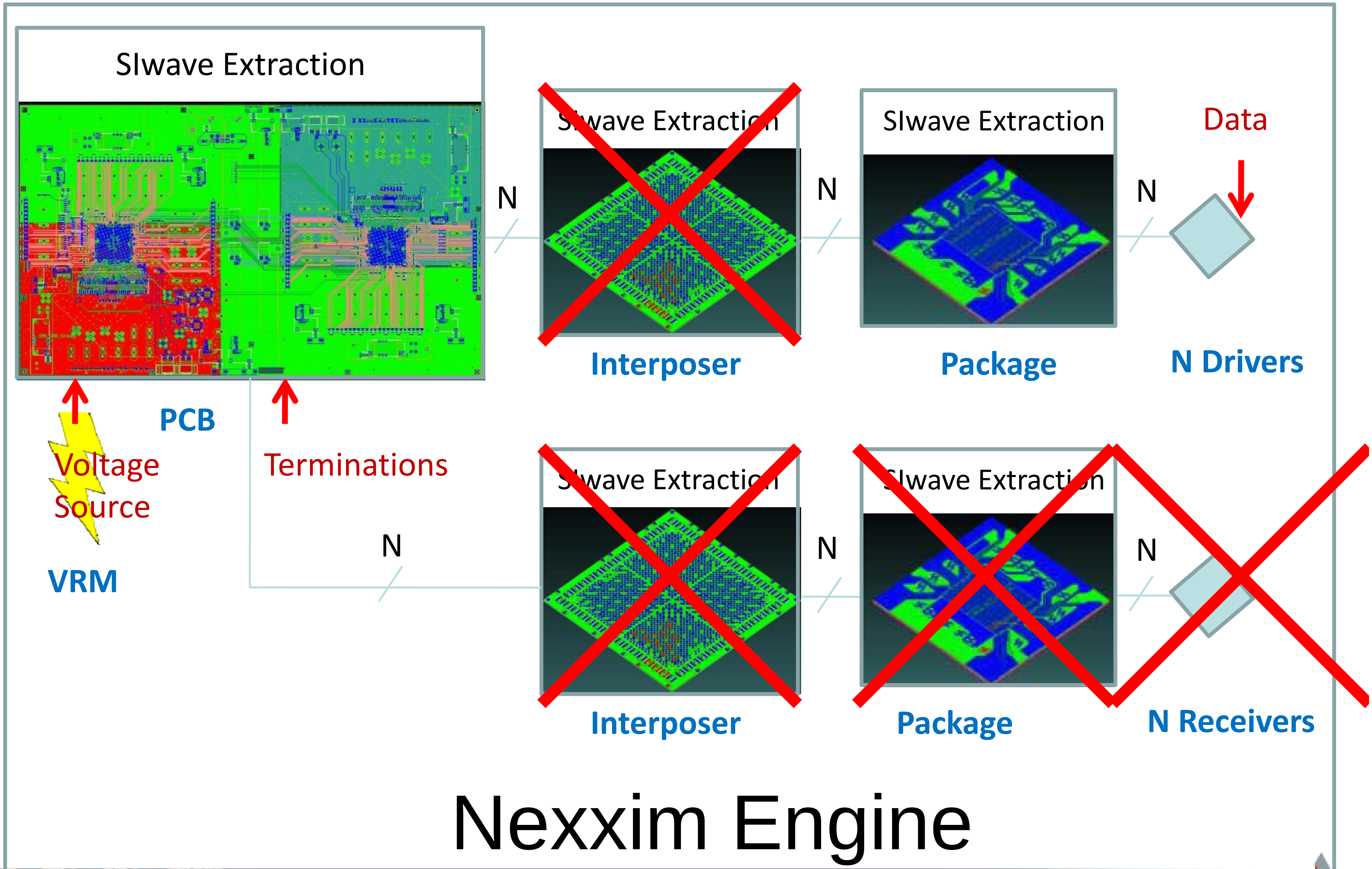
- BGA between PCB power and ground planes
- At time zero switches C closed and F transitions Low -> huge I/O current transient
- V_{glitch} = L_{gnd} di/dt
- Victim D is held low will transmit voltage V_{glitch}

Ref: BGA Crosstalk by Howard Johnson, March 1, 2005

Model Types

- Need to include all relevant effects of system; Both SI and PI
- Need models for: ICs, Packages, PCBs and VRMs
- Models may be extracted or gathered from vendors
- Each model should be independently verified for accuracy

Designer Environment



SIwave Extraction

PCB

Voltage Source

VRM

Terminations

N

SIwave Extraction

Interposer

N

SIwave Extraction

Package

N

Data

N Drivers

N

SIwave Extraction

Interposer

N

SIwave Extraction

Package

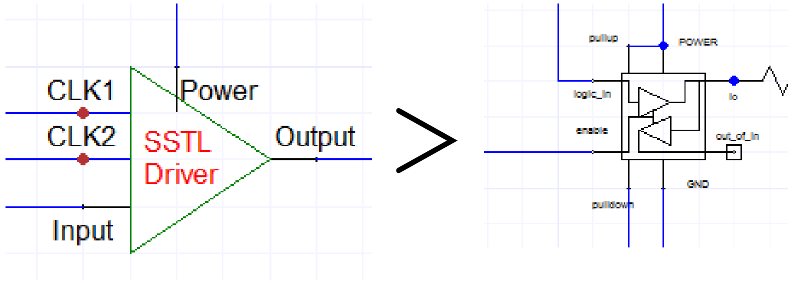
N

N Receivers

Nexxim Engine

Driver Models

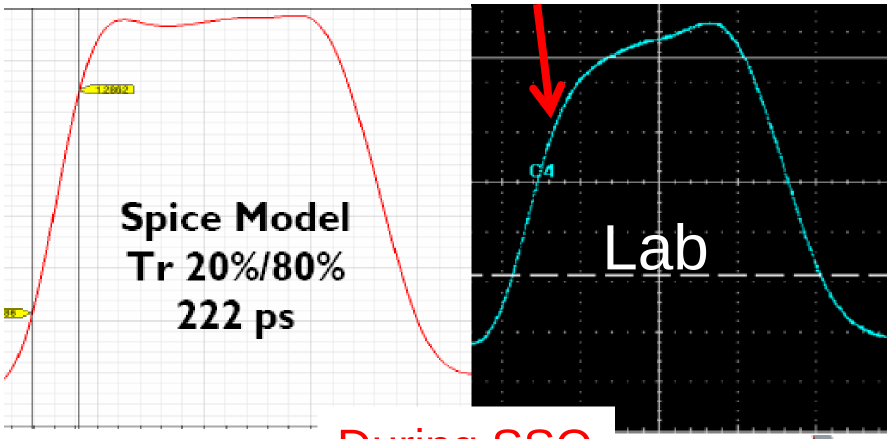
- Need to accurately model Signals and Power
- Obtain transistor level models if at all possible
- IBIS tends to be pessimistic because current scales linearly with increased drivers
- Verify waveforms for single driver AND during SSO



Spice

IBIS

Rail Collapse



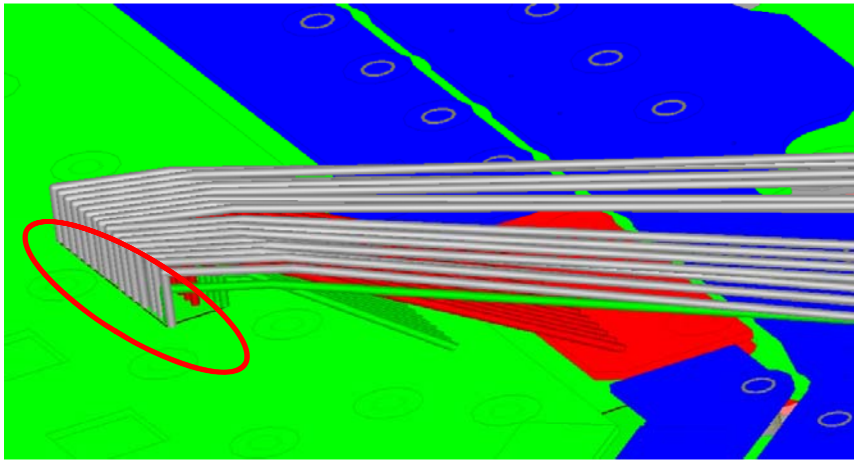
Spice Model
Tr 20%/80%
222 ps

Lab

During SSO

Package Model

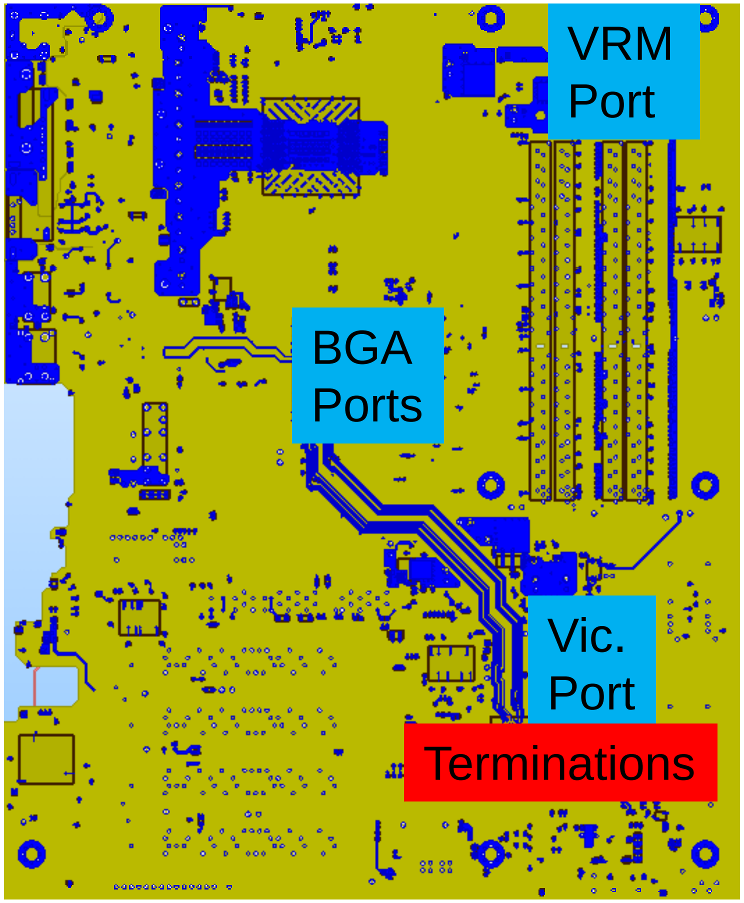
- Obtain layout and extract if possible
- Add Solderballs, Solderbumps, Bondwires to model



- Group Power/Ground pins on die side
- Extract Bank of signals

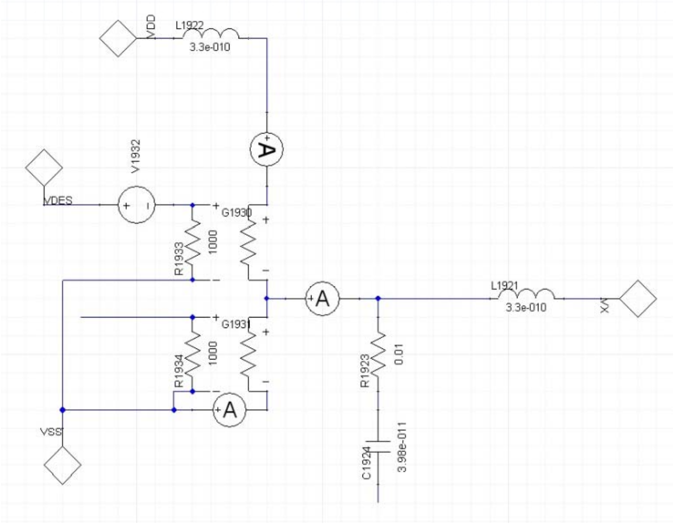
PCB Model

- Extract individual Signal Power/Ground Pins at Package if feasible
- Place port at VRM
- Place port on victim far end
- Terminate far end of line with resistors



VRM Model

- Almost always modeled as an ideal voltage source
- Could also use non-ideal circuit model
- Important for DC-DC switching power supplies

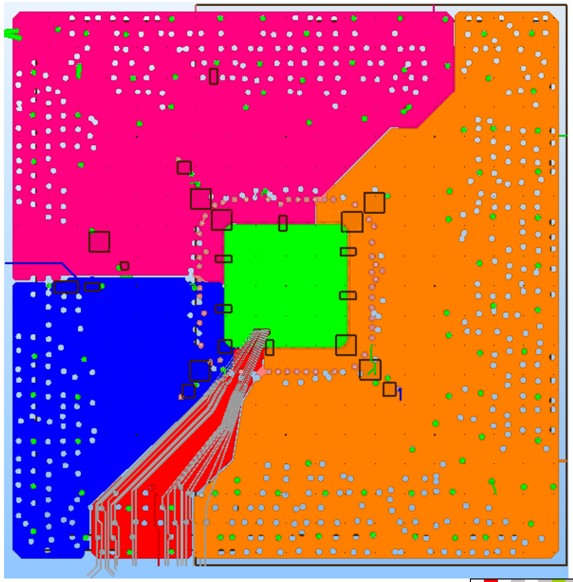


Modeling Techniques

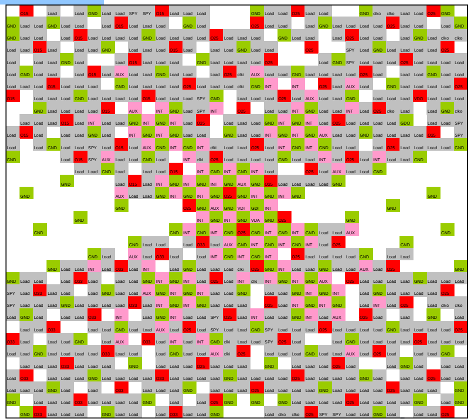
- Kitchen Sink - Simulate Everything!
  - Generally not practical
- Nearest Neighbors
  - Only simulate what's relevant
- Signal grouping
  - Combine many pins into one and scale driver
- Current Mirror
  - Mirror a single driver multiple times

Nearest Neighbors

1. Identify Victim and nearest neighbors based on proximity
2. Extract largest segment you can afford with available hardware
3. Attached Driver models to each signal pin



High Speed Packages generally have banks-easy to segment



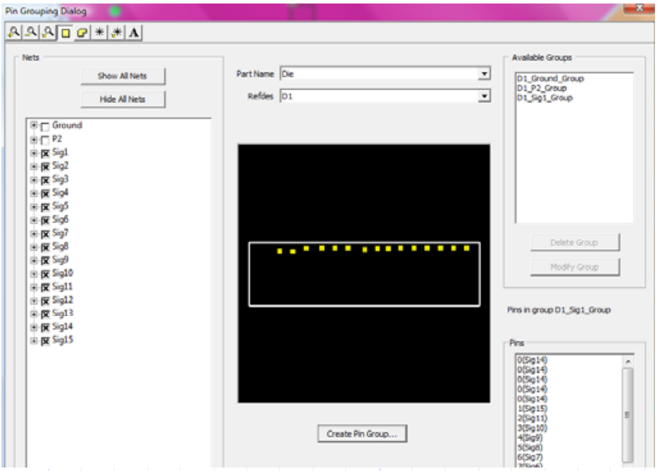
Well placed PWR/GND balls limit return path loop area

Nearest Neighbor Tradeoffs

- Most accurate and flexible method
- Simulates Skew/Delay between lines
- Allows different data patterns
- Long transient simulation
- Potential for convergence trouble

Signal Grouping

1. Apply pin grouping to signals at Die side
2. Attach single port for Aggressor group
3. Extract PCB ports as before
4. Create subcircuit for driver model
5. Multiply subcircuit M times and connect to aggressor port



Part Name: Die

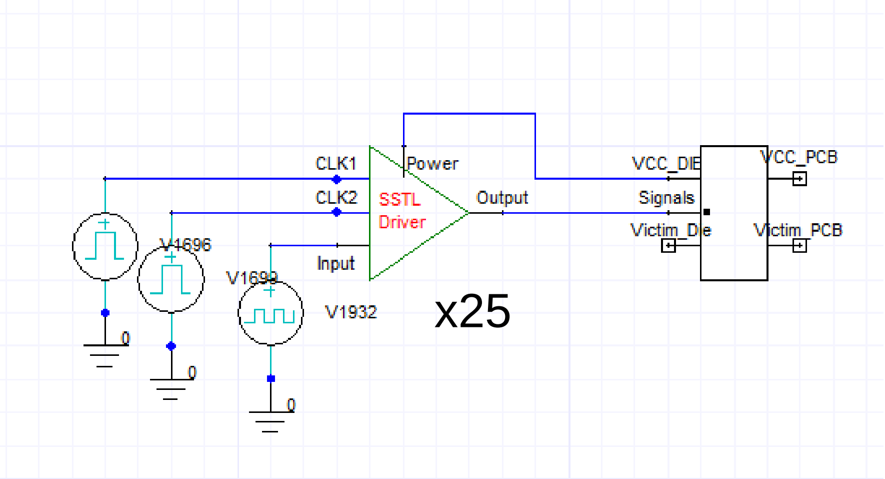
Refdes: D1

Nets:
- □ Ground
- □ P2
- ☒ Sig1
- ☒ Sig2
- ☒ Sig3
- ☒ Sig4
- ☒ Sig5
- ☒ Sig6
- ☒ Sig7
- ☒ Sig8
- ☒ Sig9
- ☒ Sig10
- ☒ Sig11
- ☒ Sig12
- ☒ Sig13
- ☒ Sig14
- ☒ Sig15

Available Groups:
- D1_Ground_Group
- D1_P2_Group
- D1_Sig1_Group

Pins in group D1_Sig1_Group

Pins:
- 0(Sig14)
- 0(Sig14)
- 0(Sig14)
- 0(Sig14)
- 0(Sig14)
- 1(Sig15)
- 2(Sig11)
- 3(Sig10)
- 4(Sig9)
- 5(Sig8)
- 6(Sig7)



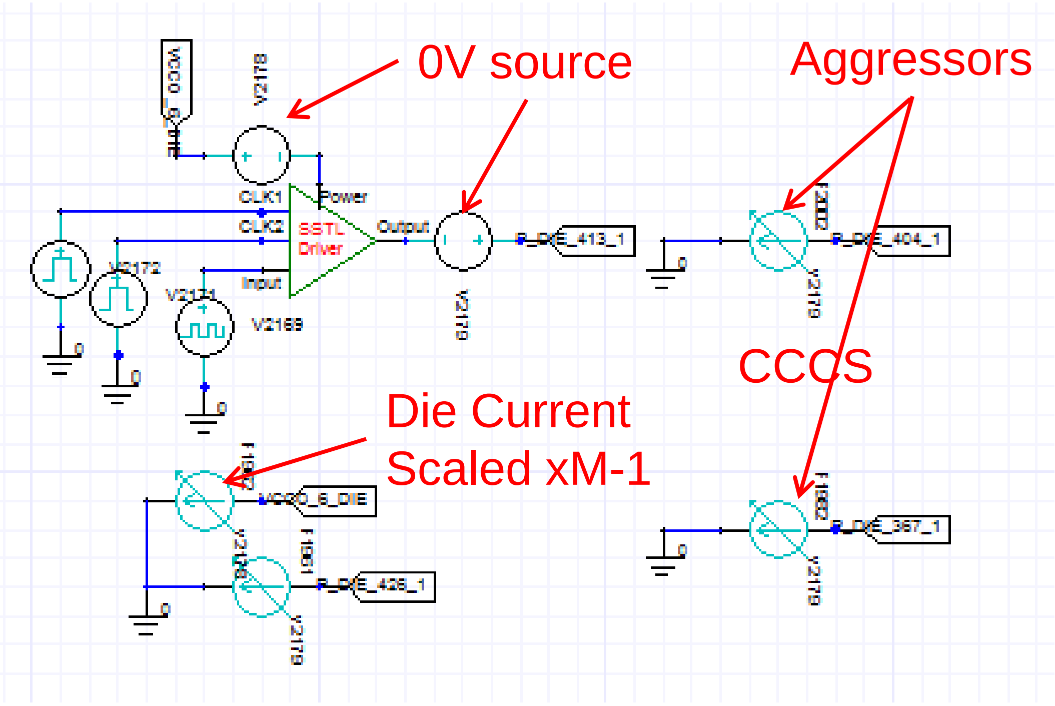
X1 CK1 CK2 Input Output Power driver M=25

Signal Grouping Tradeoffs

- Much quicker analysis
- Greatly reduces port count
- Eliminates convergence issues with multiple drivers
- Not simulating XTLK induced skew
- Same data pattern used on all aggressors
- Assumes all lines are similar in impedance and delay
- Lose information on individual lines
- One bad signal line will affect net results

Current Mirroring

1. Use same extracted model as “Nearest Neighbors”
2. Place driver on one aggressor
3. Monitor current at signal and die connections using series 0v Voltage sources
4. Attach CCCS to all other signal lines mirroring same current as driver
5. Attach CCCS to die scaling current x M-1 drivers


0V source

Aggressors

CCCS

Die Current Scaled xM-1

Ref: Digital Signal Integrity, Young

Current Mirroring Tradeoffs

- Much quicker analysis
- Eliminates convergence issues with multiple drivers
- Still can inspect individual s-parameters
- Not simulating XTLK induced skew
- Same data pattern used on all aggressors
- Assumes all lines are similar in impedance and delay

Simulation Tips and Tricks

- Convolution versus state-space
- Frequency sweep setup
- Mixed port impedances
- Achieving Convergence

S-parameter Handling

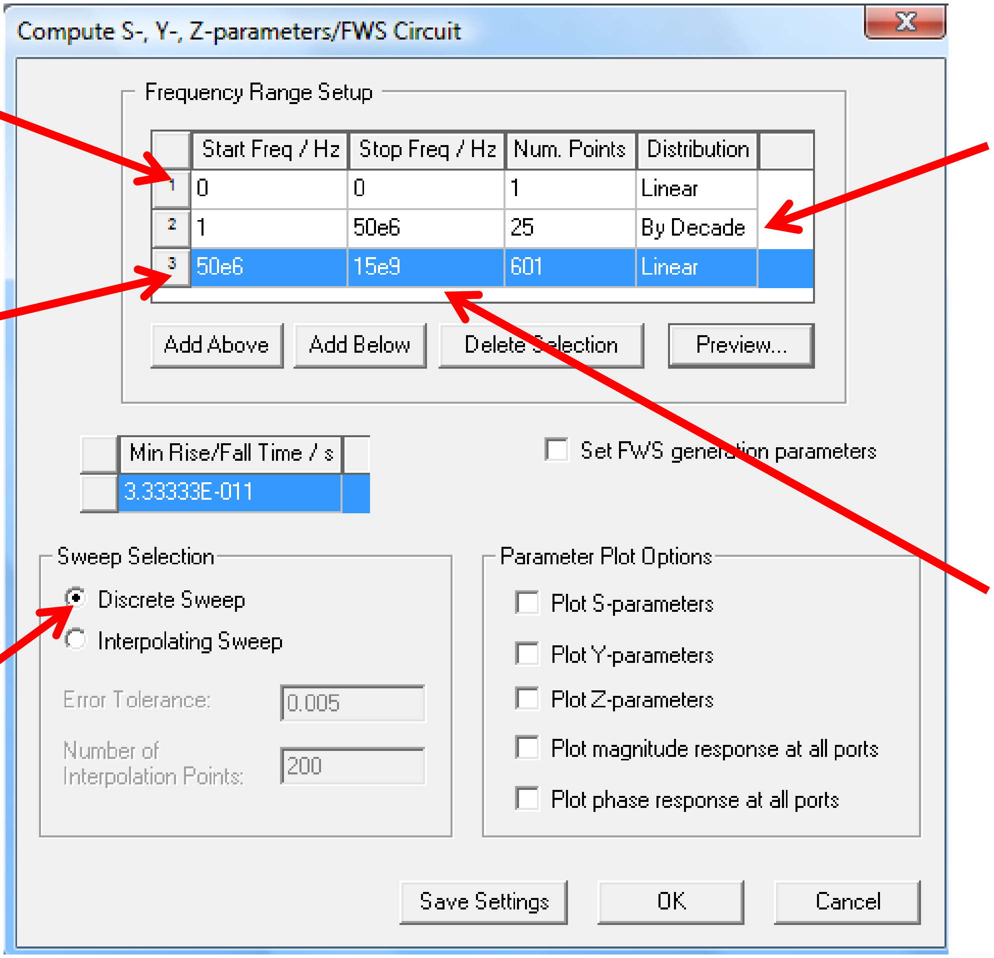
State-Space (Default)

- Much faster for long transients
- Passivity enforcement
- Causality enforcement
- Up front cost building model
- Does not extrapolate
- May not achieve fit on noisy data
- Cannot model long delays, ~22 λ

Convolution

- More options for convergence
- Can handle long delays
- Data filtering options
- Extrapolates well
- Sim time increases quadratically with tran time
- Requires linearly spaced data

Sweep Setup



Compute S-, Y-, Z-parameters/FWS Circuit

Frequency Range Setup

	Start Freq / Hz	Stop Freq / Hz	Num. Points	Distribution
1	0	0	1	Linear
2	1	50e6	25	By Decade
3	50e6	15e9	601	Linear

Min Rise/Fall Time / s: 3.33333E-011

□ Set FWS generation parameters

Sweep Selection

● Discrete Sweep

○ Interpolating Sweep

Error Tolerance: 0.005

Number of Interpolation Points: 200

Parameter Plot Options

□ Plot S-parameters

□ Plot Y-parameters

□ Plot Z-parameters

□ Plot magnitude response at all ports

□ Plot phase response at all ports

DC point required

Coarser sweep used at Higher frequencies

Discrete Sweep ensures causality and passivity enforcement

Log sweep helps capture low frequencies important to PDN

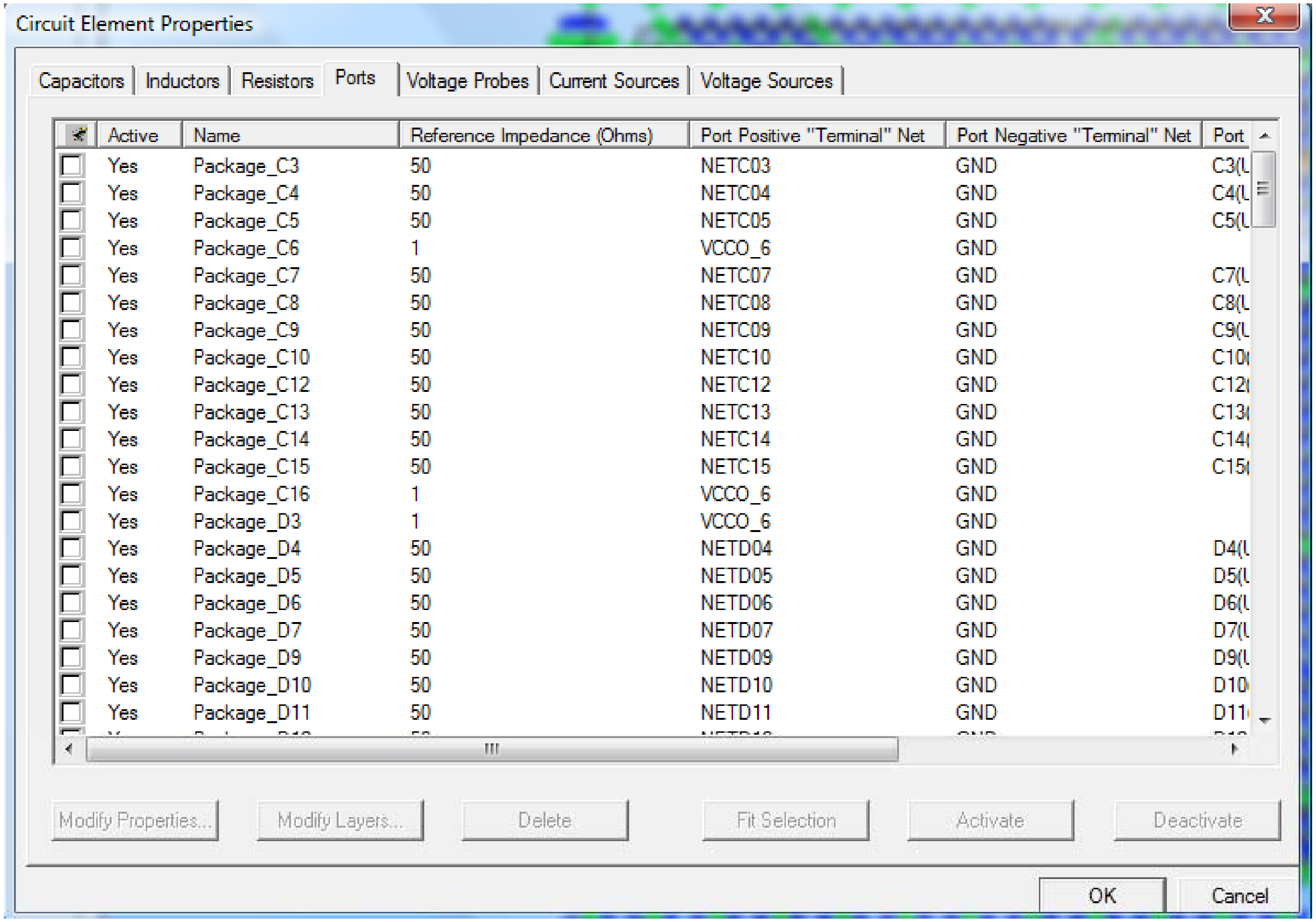
Set max even higher than knee frequency: State space doesn’t extrapolate!

Port Impedances

Choose port impedances that are relatively close to structure impedance

Use 1 or .1 ohms for power, 50 ohms for signal lines

This helps model accuracy and avoids 0dB values in touchstone file

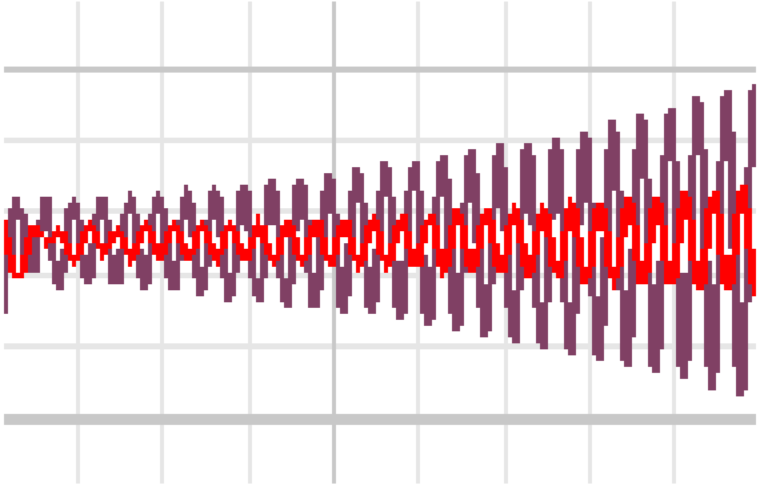


☑	Active	Name	Reference Impedance (Ohms)	Port Positive "Terminal" Net	Port Negative "Terminal" Net	Port
□	Yes	Package_C3	50	NETC03	GND	C3(U
□	Yes	Package_C4	50	NETC04	GND	C4(U
□	Yes	Package_C5	50	NETC05	GND	C5(U
□	Yes	Package_C6	1	VCCO_6	GND	
□	Yes	Package_C7	50	NETC07	GND	C7(U
□	Yes	Package_C8	50	NETC08	GND	C8(U
□	Yes	Package_C9	50	NETC09	GND	C9(U
□	Yes	Package_C10	50	NETC10	GND	C10(
□	Yes	Package_C12	50	NETC12	GND	C12(
□	Yes	Package_C13	50	NETC13	GND	C13(
□	Yes	Package_C14	50	NETC14	GND	C14(
□	Yes	Package_C15	50	NETC15	GND	C15(
□	Yes	Package_C16	1	VCCO_6	GND	
□	Yes	Package_D3	1	VCCO_6	GND	
□	Yes	Package_D4	50	NETD04	GND	D4(U
□	Yes	Package_D5	50	NETD05	GND	D5(U
□	Yes	Package_D6	50	NETD06	GND	D6(U
□	Yes	Package_D7	50	NETD07	GND	D7(U
□	Yes	Package_D9	50	NETD09	GND	D9(U
□	Yes	Package_D10	50	NETD10	GND	D10
□	Yes	Package_D11	50	NETD11	GND	D11

Designer dynamic link to SIwave will preserve port impedances

Achieving Convergence

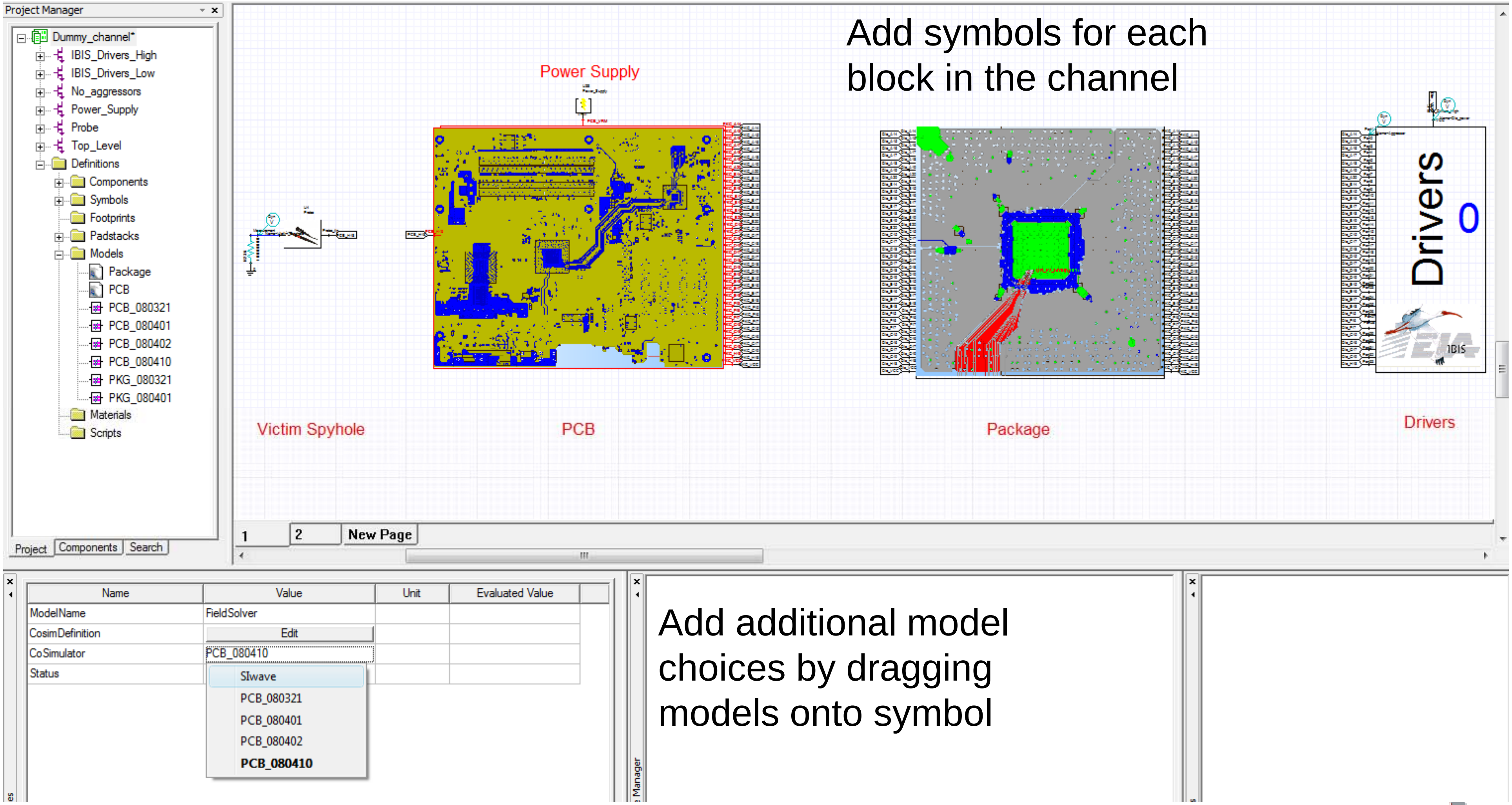
- Inspect individual models (Divide and Conquer)
  - Realistic data, passive, causal
  - Sufficient bandwidth, resolution
  - Frequency dependent materials
- Bypass/Deactivate components to find root cause
- Check state-space fit; tighten s_element.reltol
- Increase s_element.max_states
- Slow risetimes/Soften Edges
- Try generic sources, i.e. Gaussian PRBS
- Reduce .tran step
- Decrease reltol and abstol
- Try convolutions 1-3
- Reduce s-parameter port count



Schematic Setup

- Schematic setup can be tedious and error prone when working with large number of components
- Modular/hierarchical blocks can aid with design management and debugging
- Four methods for automatic setup:
  - Dynamic Linking
  - APDS
  - Designer I/O Wizard
  - SIwave SIwizard

Dynamic Links



Add symbols for each block in the channel

Add additional model choices by dragging models onto symbol

Project Manager

- Dummy_channel*
  - IBIS_Drivers_High
  - IBIS_Drivers_Low
  - No_aggressors
  - Power_Supply
  - Probe
  - Top_Level
  - Definitions
    - Components
    - Symbols
    - Footprints
    - Padstacks
    - Models
      - Package
      - PCB
      - PCB_080321
      - PCB_080401
      - PCB_080402
      - PCB_080410
      - PKG_080321
      - PKG_080401
    - Materials
    - Scripts

Name	Value	Unit	Evaluated Value
ModelName	FieldSolver		
CosimDefinition	Edit		
CoSimulator	PCB_080410		
Status			

- SIwave
- PCB_080321
- PCB_080401
- PCB_080402
- **PCB_080410**

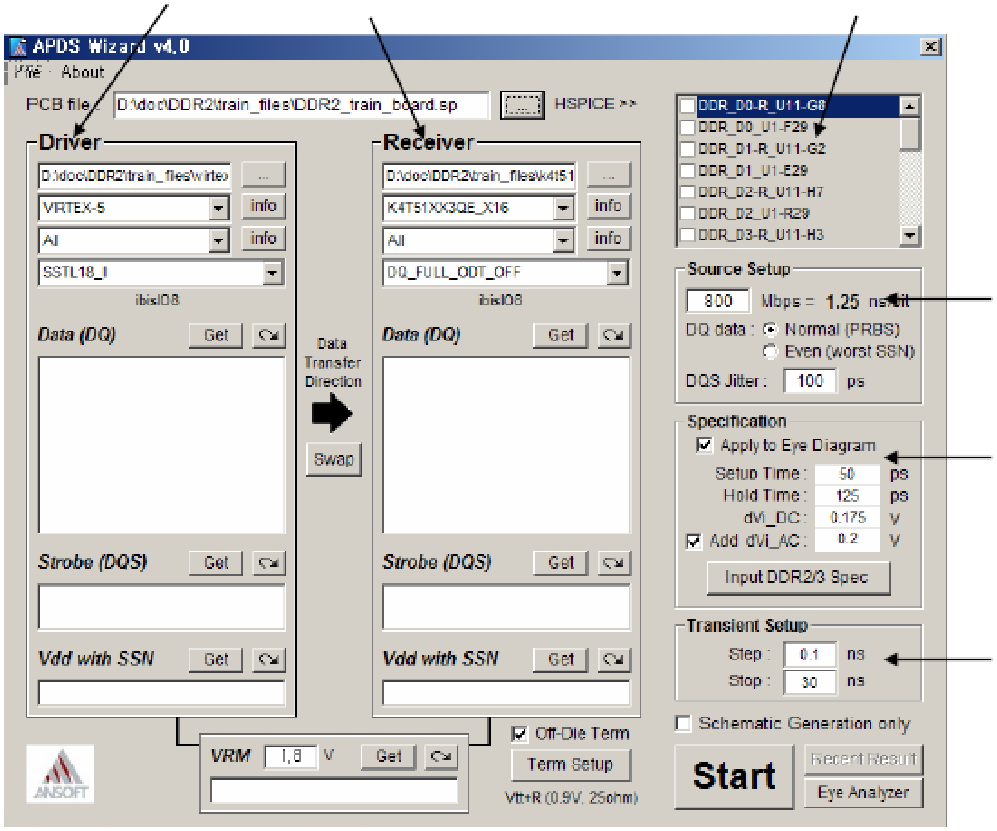
APDS

Stand-alone GUI to setup transient analysis

Specifically tailored to SSN of DDR interfaces

Separated IBIS & ports for Driver & Receiver

Open ports list to be applied to appropriate port



APDS Wizard v4.0

PCB file : D:\doc\DDR2\train_files\DDR2_train_board.sp

Driver

- D:\doc\DDR2\train_files\virtex
- VIRTEX-5
- All
- SSTL18_I
- ibisIO8

Receiver

- D:\doc\DDR2\train_files\k4t51
- K4T51XX3QE_X16
- All
- DQ_FULL_ODT_OFF
- ibisIO8

- □ DDR_D0-R_U11-G8
- □ DDR_D0_U1-F29
- □ DDR_D1-R_U11-G2
- □ DDR_D1_U1-E29
- □ DDR_D2-R_U11-H7
- □ DDR_D2_U1-R29
- □ DDR_D3-R_U11-H3

Source Setup

800 Mbps = 1.25 ns/bit

DQ data : ● Normal (PRBS) ○ Even (worst SSN)

DQS Jitter : 100 ps

Specification

☑ Apply to Eye Diagram

Setup Time : 50 ps

Hold Time : 125 ps

dVi_DC : 0.175 V

☑ Add dVi_AC : 0.2 V

Transient Setup

Step : 0.1 ns

Stop : 30 ns

□ Schematic Generation only

☑ Off-Die Term

Vtt+R (0.9V, 25ohm)

VRM 1.8 V

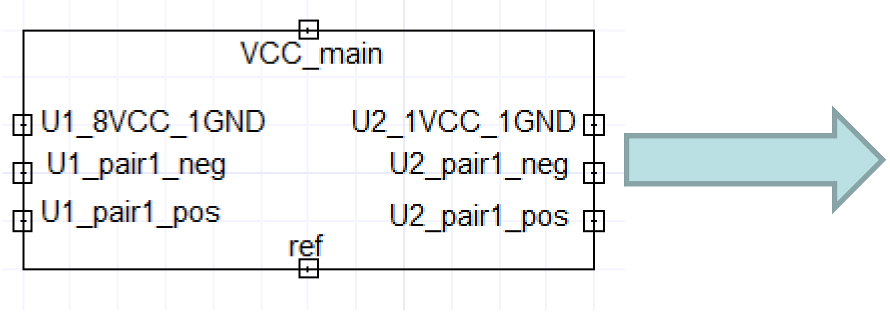
Source Setup

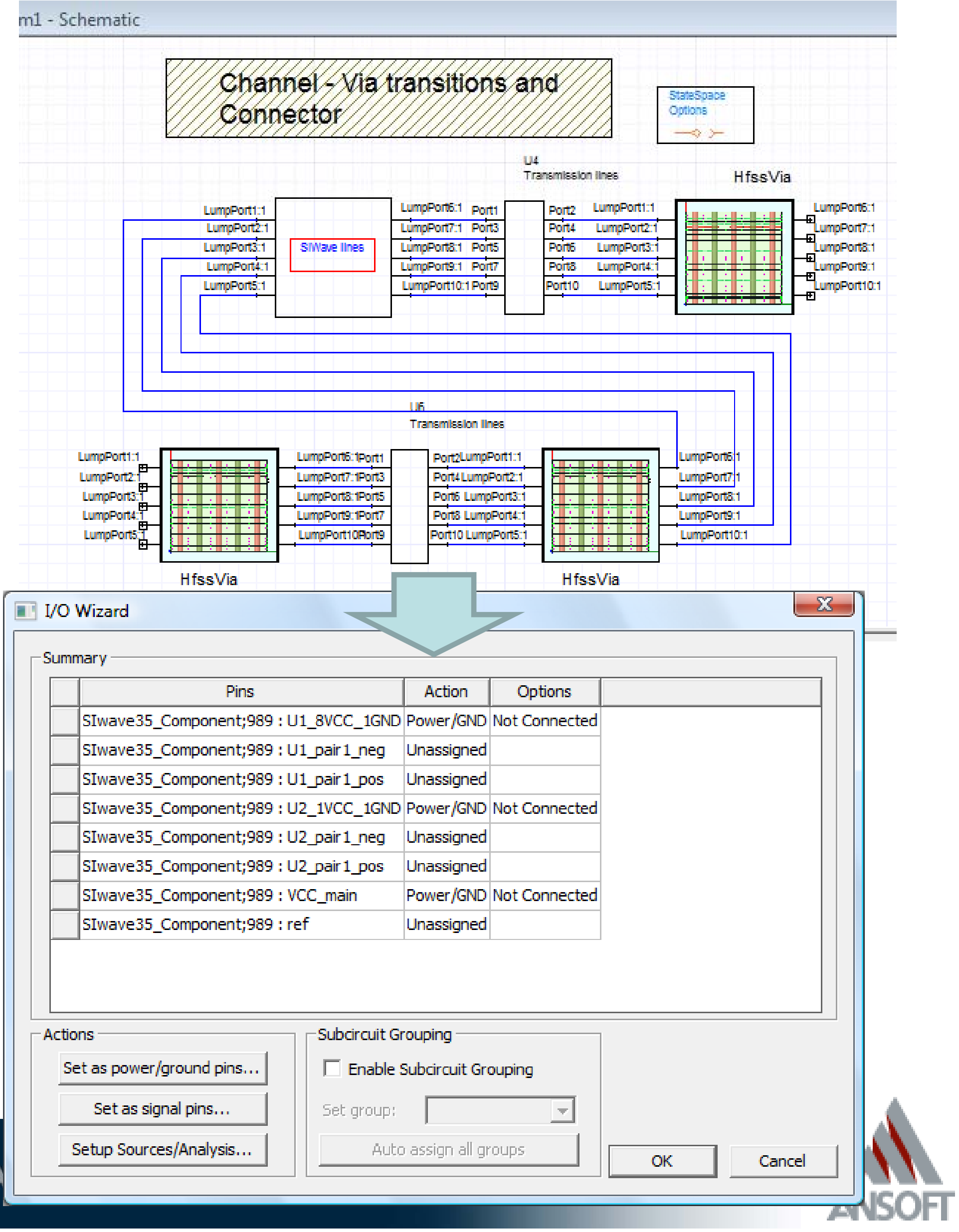
Spec Setup

Transient Setup

Designer I/O Wizard

- Launch GUI from Designer 4.1
- Rapid setup of drivers for high pin counts
- Easily link generic model types for all blocks in the channel





I/O Wizard

Summary

	Pins	Action	Options
	SIwave35_Component;989 : U1_8VCC_1GND	Power/GND	Not Connected
	SIwave35_Component;989 : U1_pair1_neg	Unassigned	
	SIwave35_Component;989 : U1_pair1_pos	Unassigned	
	SIwave35_Component;989 : U2_1VCC_1GND	Power/GND	Not Connected
	SIwave35_Component;989 : U2_pair1_neg	Unassigned	
	SIwave35_Component;989 : U2_pair1_pos	Unassigned	
	SIwave35_Component;989 : VCC_main	Power/GND	Not Connected
	SIwave35_Component;989 : ref	Unassigned	

Actions

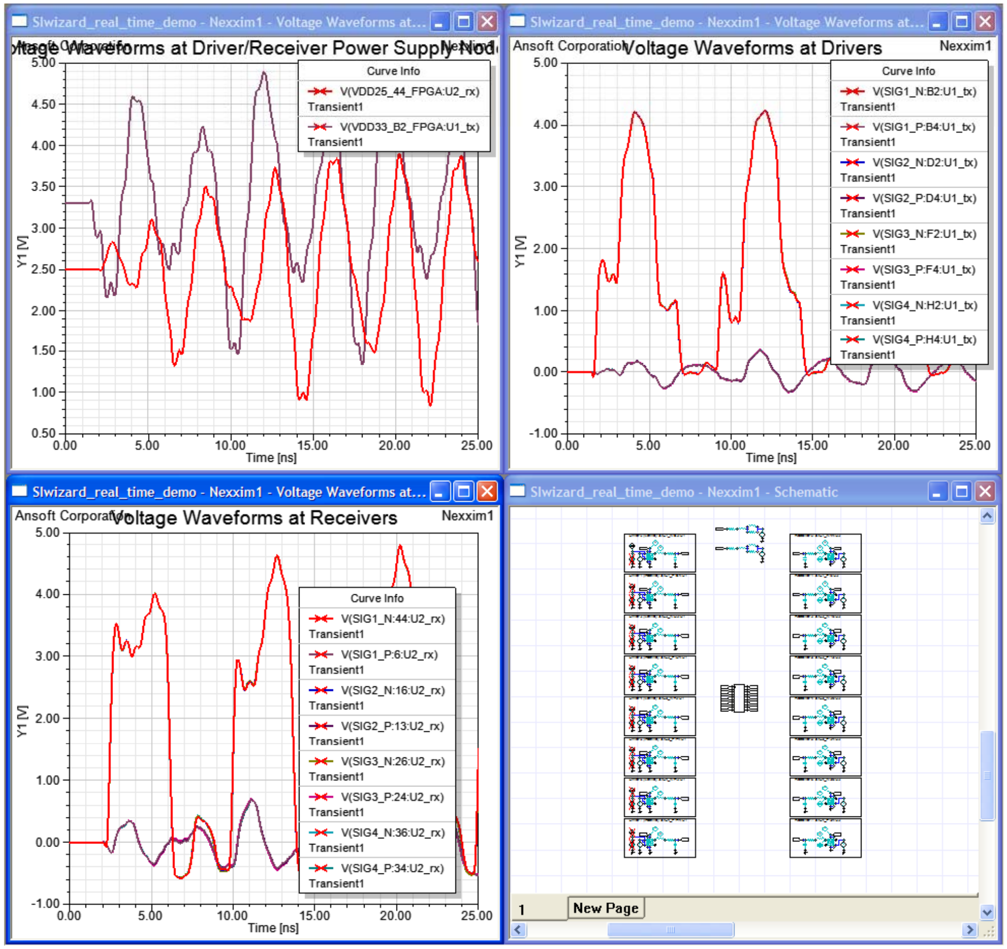
Subcircuit Grouping

☐ Enable Subcircuit Grouping

Set group:

SIwizard in v4.0 SIwave

1. Select signal nets to simulate
2. Assign IBIS TX/RX models to pins on nets
3. Identify component power/ground nets
4. (Optional) Set VRM parameters
5. Set Transient Simulation parameters


SIwizard_real_time_demo - Nexxim1 - Voltage Waveforms at...
Ansoft Corporation
Voltage Waveforms at Driver/Receiver Power Supply Nodes
Nexxim1
Curve Info
V(VDD25_44_FPGA:U2_rx) Transient1
V(VDD33_B2_FPGA:U1_tx) Transient1
Y1 [V]
Time [ns]
0.50
1.00
1.50
2.00
2.50
3.00
3.50
4.00
4.50
5.00
0.00
5.00
10.00
15.00
20.00
25.00
SIwizard_real_time_demo - Nexxim1 - Voltage Waveforms at...
Ansoft Corporation
Voltage Waveforms at Drivers
Nexxim1
Curve Info
V(SIG1_N:B2:U1_tx) Transient1
V(SIG1_P:B4:U1_tx) Transient1
V(SIG2_N:D2:U1_tx) Transient1
V(SIG2_P:D4:U1_tx) Transient1
V(SIG3_N:F2:U1_tx) Transient1
V(SIG3_P:F4:U1_tx) Transient1
V(SIG4_N:H2:U1_tx) Transient1
V(SIG4_P:H4:U1_tx) Transient1
Y1 [V]
Time [ns]
-1.00
0.00
1.00
2.00
3.00
4.00
5.00
SIwizard_real_time_demo - Nexxim1 - Voltage Waveforms at...
Ansoft Corporation
Voltage Waveforms at Receivers
Nexxim1
Curve Info
V(SIG1_N:44:U2_rx) Transient1
V(SIG1_P:6:U2_rx) Transient1
V(SIG2_N:16:U2_rx) Transient1
V(SIG2_P:13:U2_rx) Transient1
V(SIG3_N:26:U2_rx) Transient1
V(SIG3_P:24:U2_rx) Transient1
V(SIG4_N:36:U2_rx) Transient1
V(SIG4_P:34:U2_rx) Transient1
Y1 [V]
Time [ns]
SIwizard_real_time_demo - Nexxim1 - Schematic
1
New Page

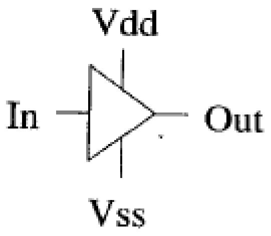
Pin info preserved from layout

Conclusions

- SSN is a powerful simulation offering insight to both Signal and Power behavior
- Accurate device models are critical
- Set realistic goals and choose the best method to obtain them
- Ansoft has the capabilities and the automation to perform accurate and efficient SSN simulations

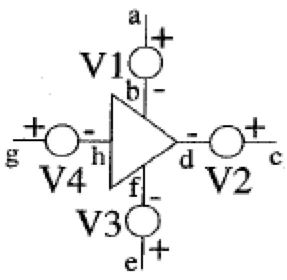
Current Mirroring

- Place drivers for a single aggressor and the victim. Mirror the current to all other aggressors using CCCS.

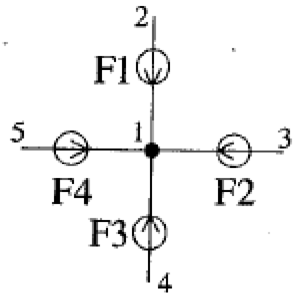


Original

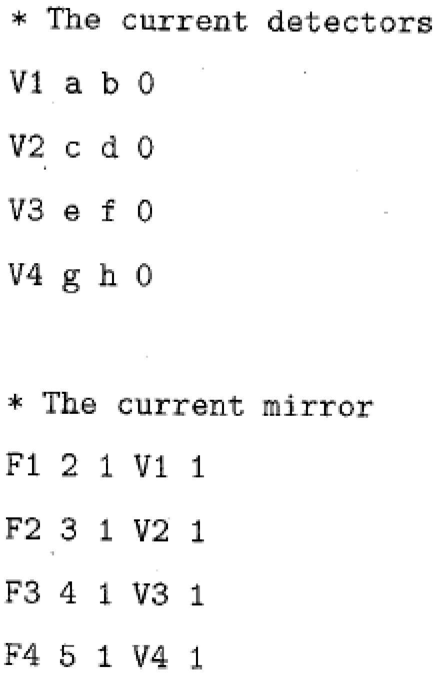
Ref: Digital Signal Integrity, Young



Original
w/ Detectors



Mirrored



```
* The current detectors

V1 a b 0

V2 c d 0

V3 e f 0

V4 g h 0


* The current mirror

F1 2 1 V1 1

F2 3 1 V2 1

F3 4 1 V3 1

F4 5 1 V4 1
```