Power Plane and Decoupling Optimization

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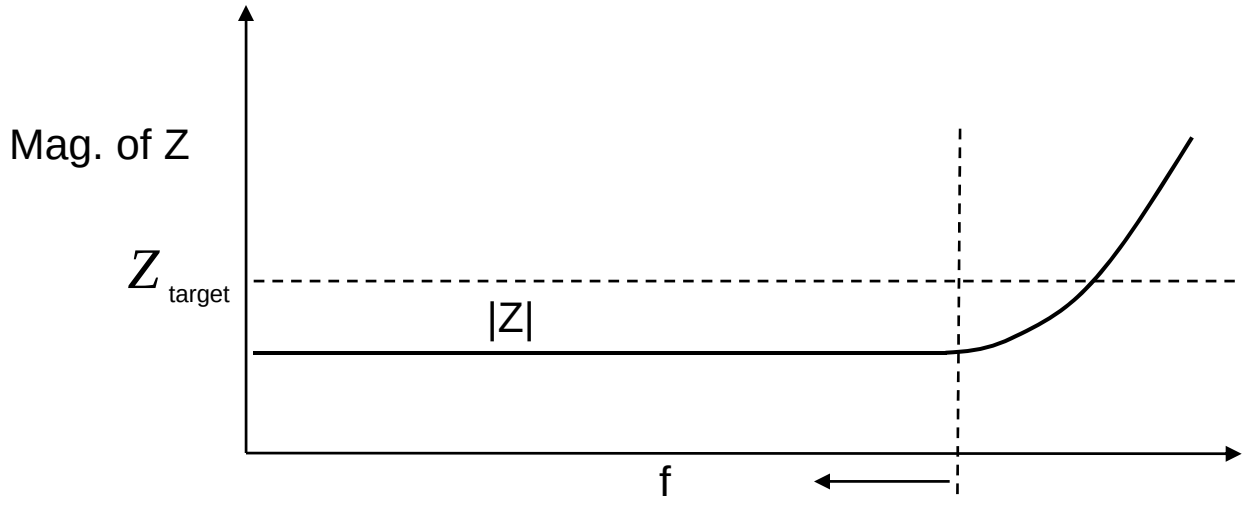
ANSOFT

Overview

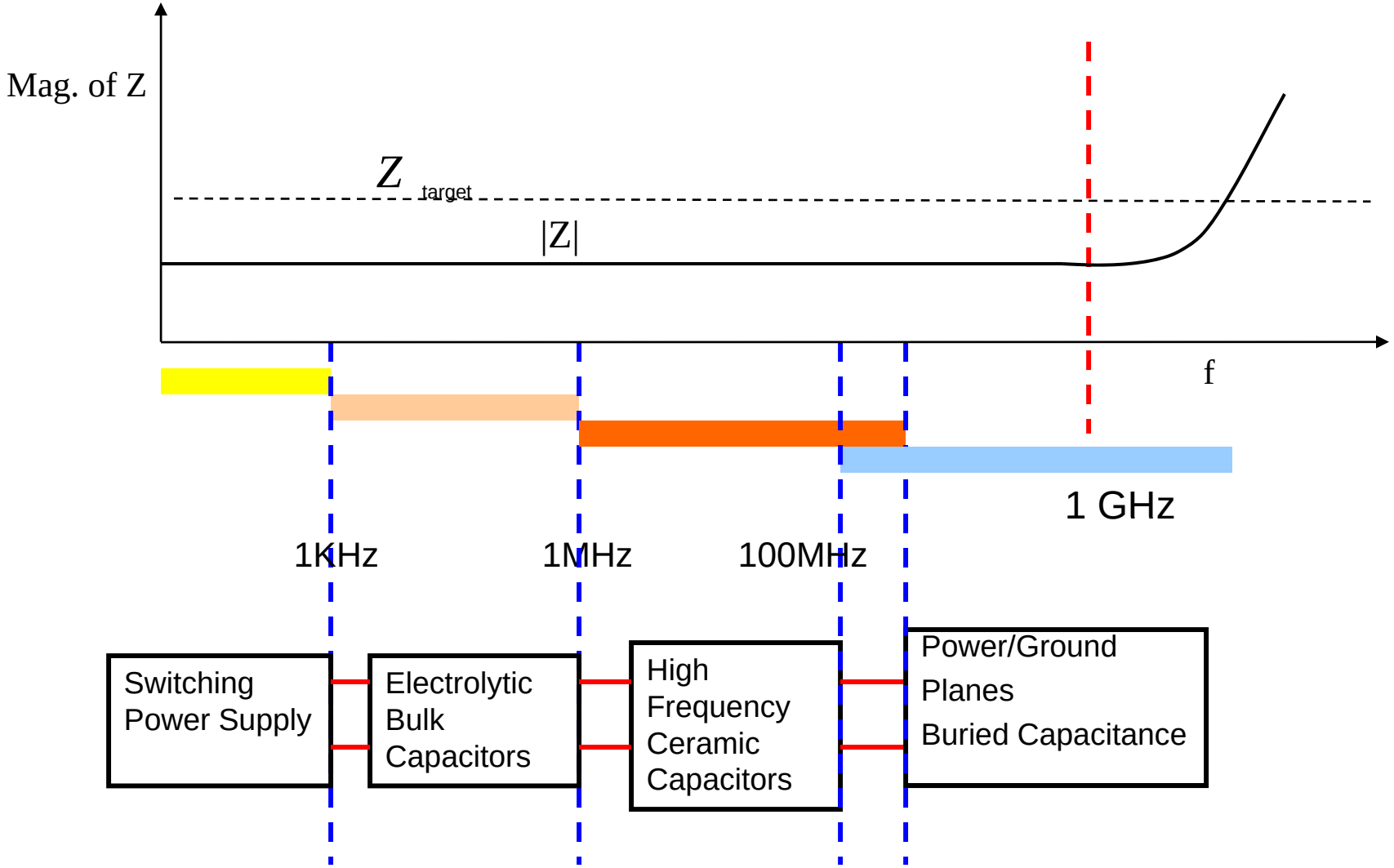
- Frequency- and time-domain power distribution system specifications
- Decoupling design example
  - Bare board
  - Added capacitors
  - Buried Capacitance
- Conclusion

Frequency Domain PDS Targets

- Excessive impedance seen by a device drawing power from a PDS will cause power voltage to fluctuate
- On a board, impedance must be below target from DC to several hundred MHz
- Working in the frequency domain allows quick estimation of power quality



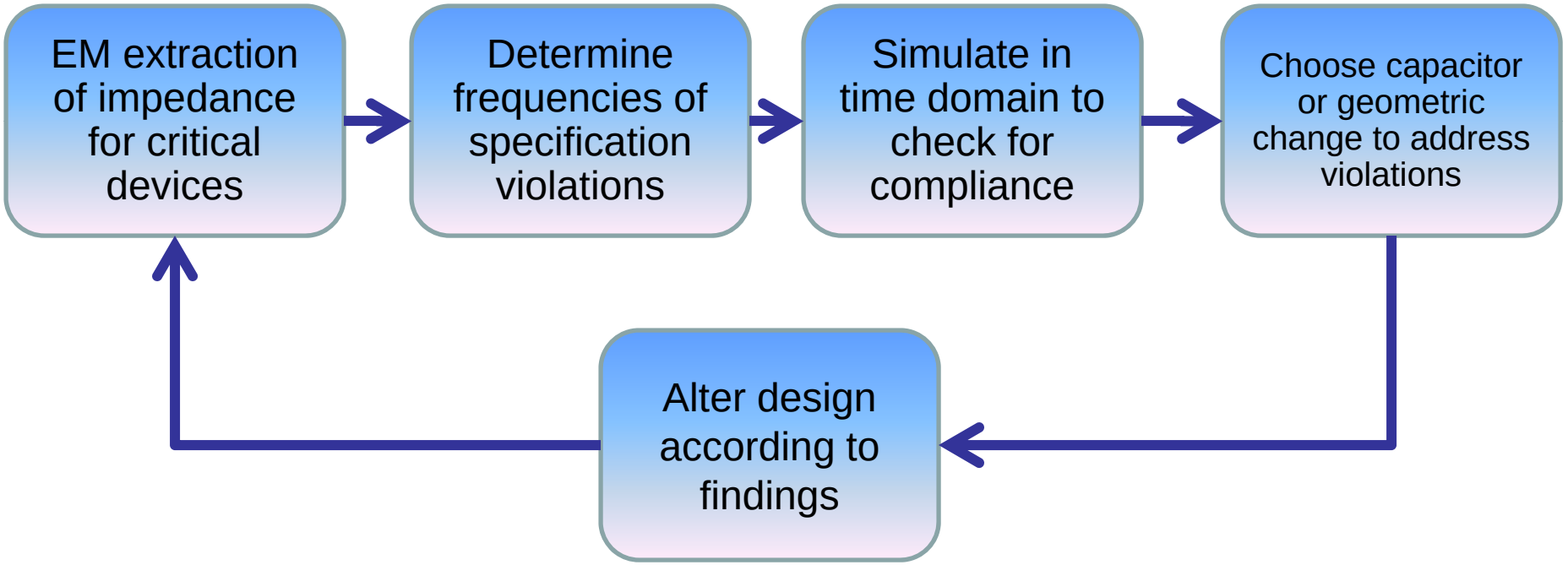
PDS Components



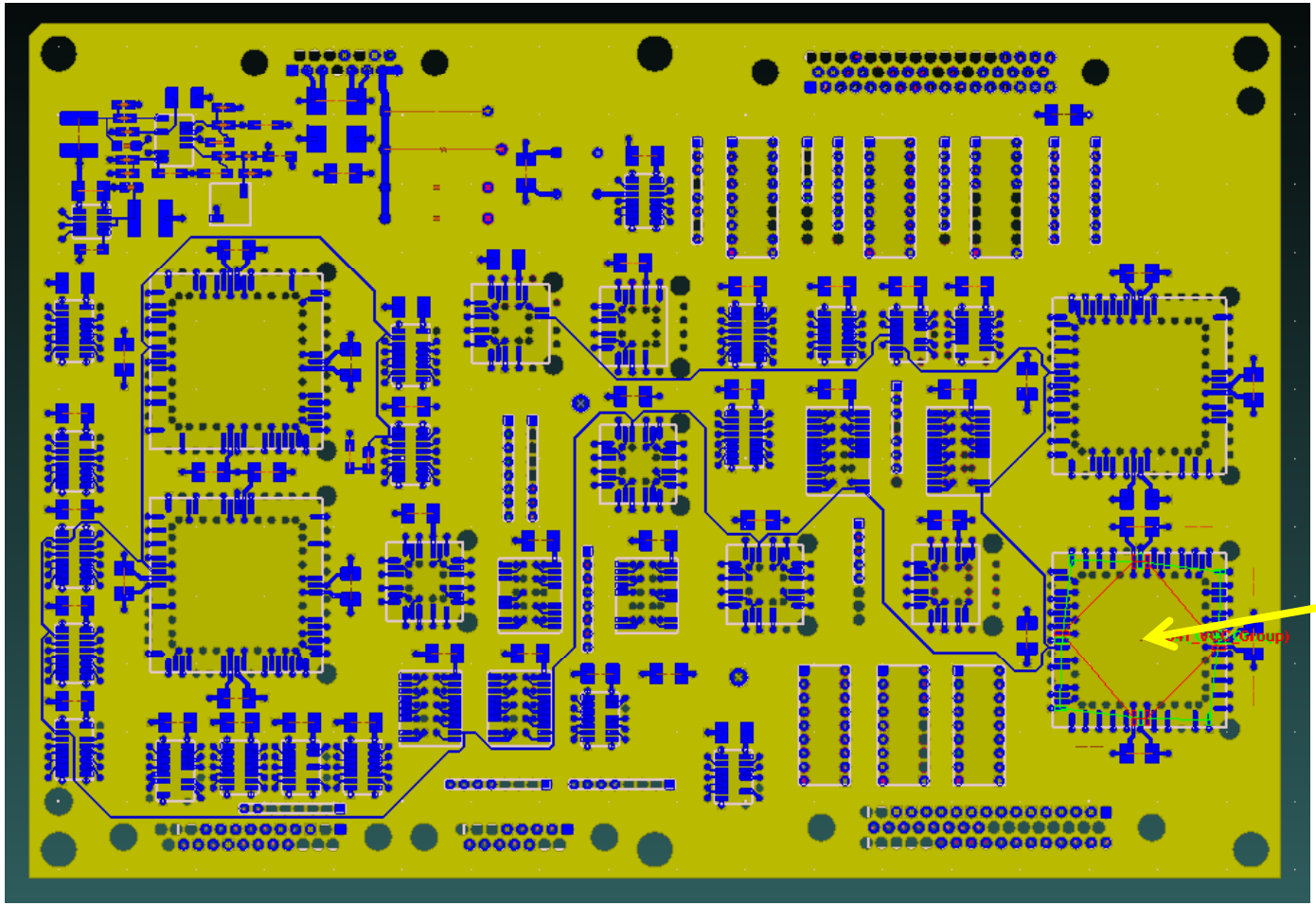
Time Domain PDS Targets

- S-parameters and impedance are calculated in the frequency domain
- Device specifications are typically given in the time domain
- Example: maximum VCC excursion 10% of nominal value
  - 1.8 V VCC has an allowable range of 1.62 V to 1.98 V

PDS Design Flow



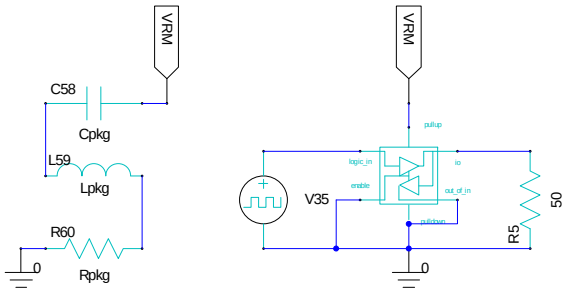
Board Imported from Layout



Measuring impedance at the six VCC pins on U41

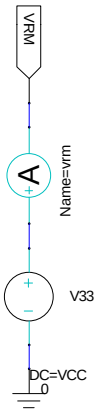
Defining the Target Impedance

Package Model



Driver

VRM



- To define the target impedance we need to consider two factors:
  - Peak current
    - Determines maximum impedance
  - Spectral power
    - Determines cutoff frequency

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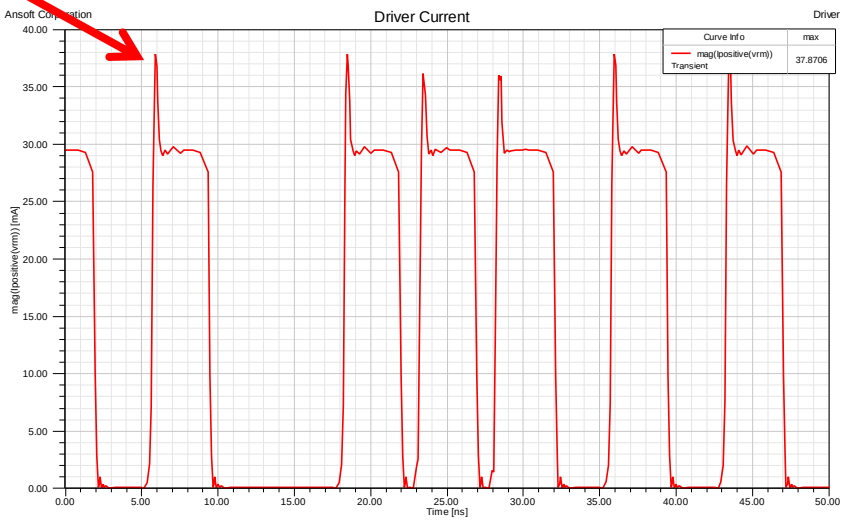
Peak Current

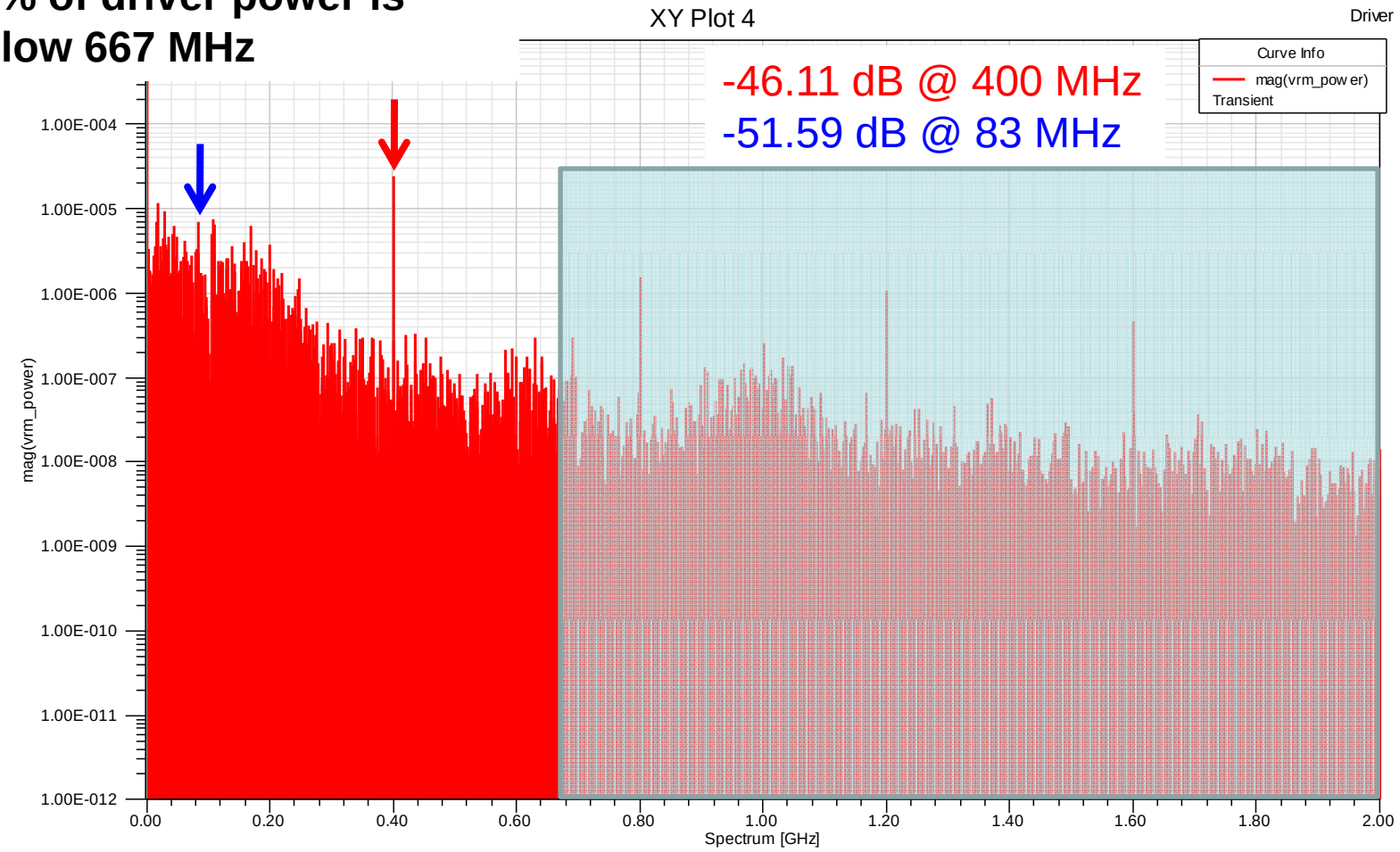
- Peak current 37.87 mA
- Six drivers and 0.18 V maximum voltage swing:

$$\frac{0.18\ \mathrm{V}}{6(37.87\ \mathrm{mA})} = 800\ \mathrm{m\Omega}$$

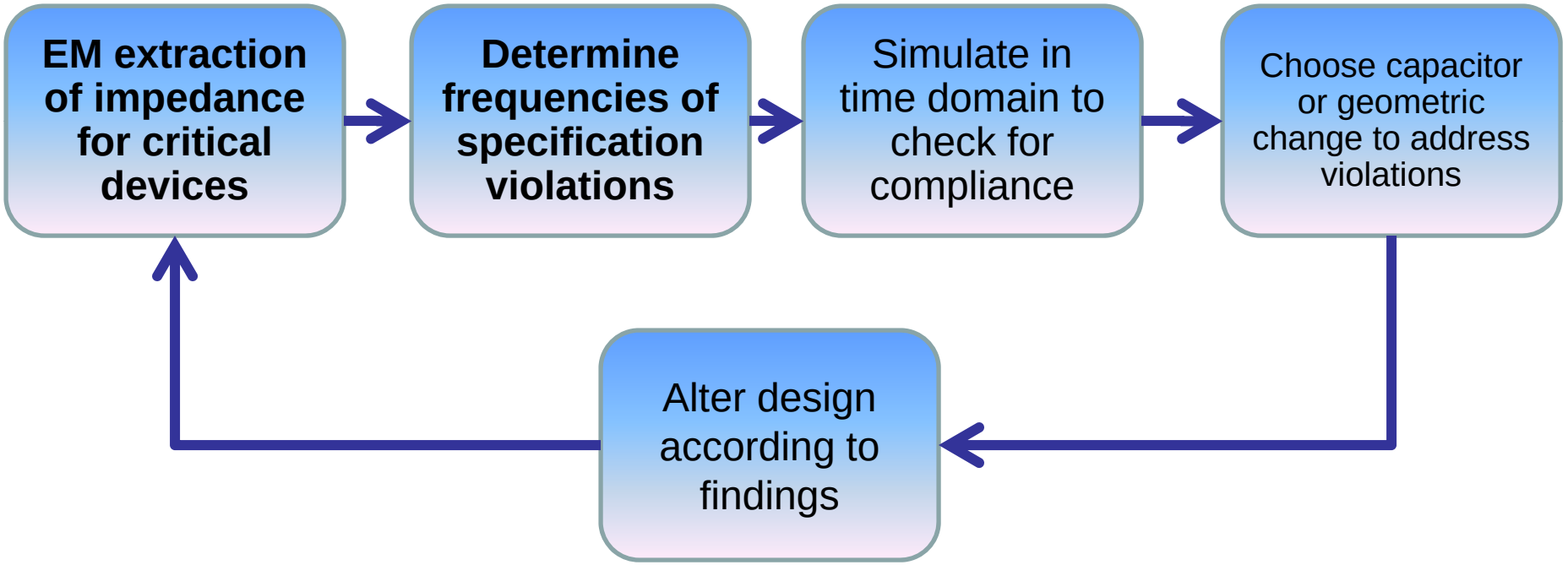


Driver Spectrum

95% of driver power is below 667 MHz

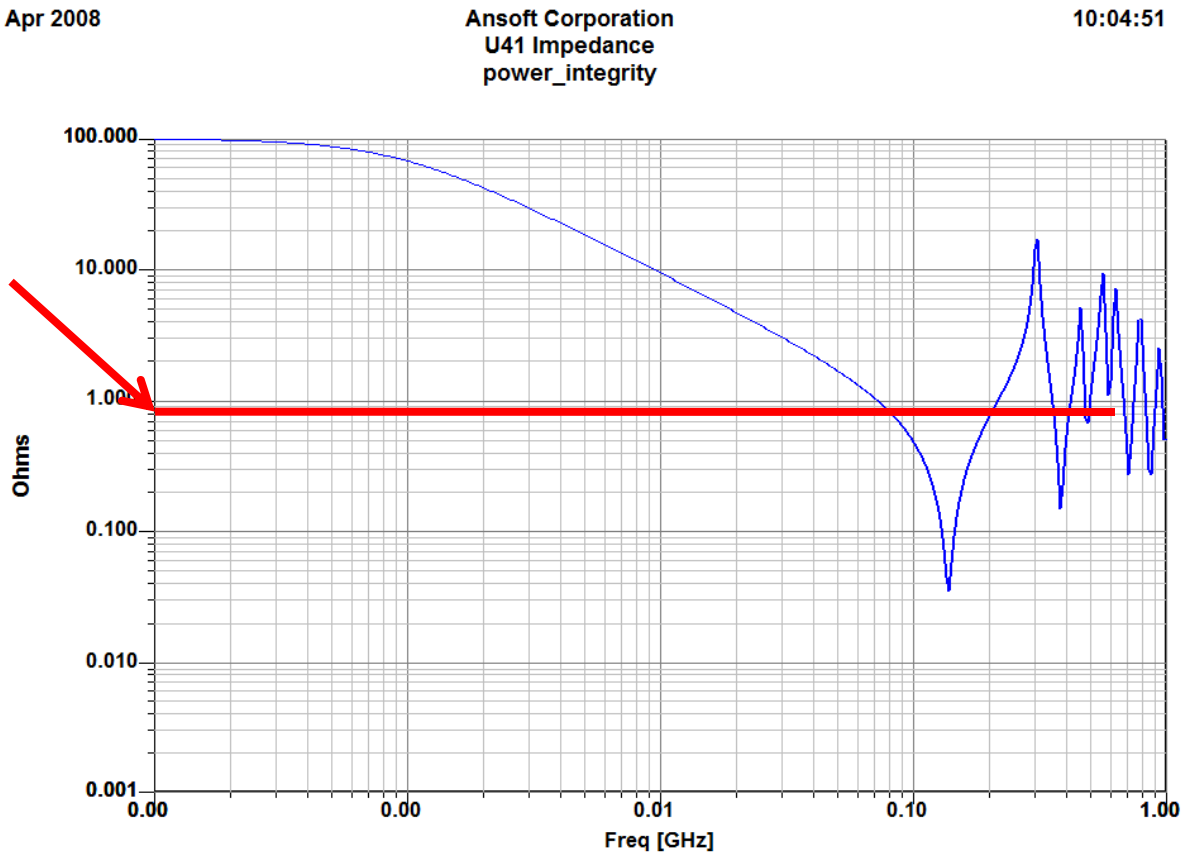


PDS Design Flow



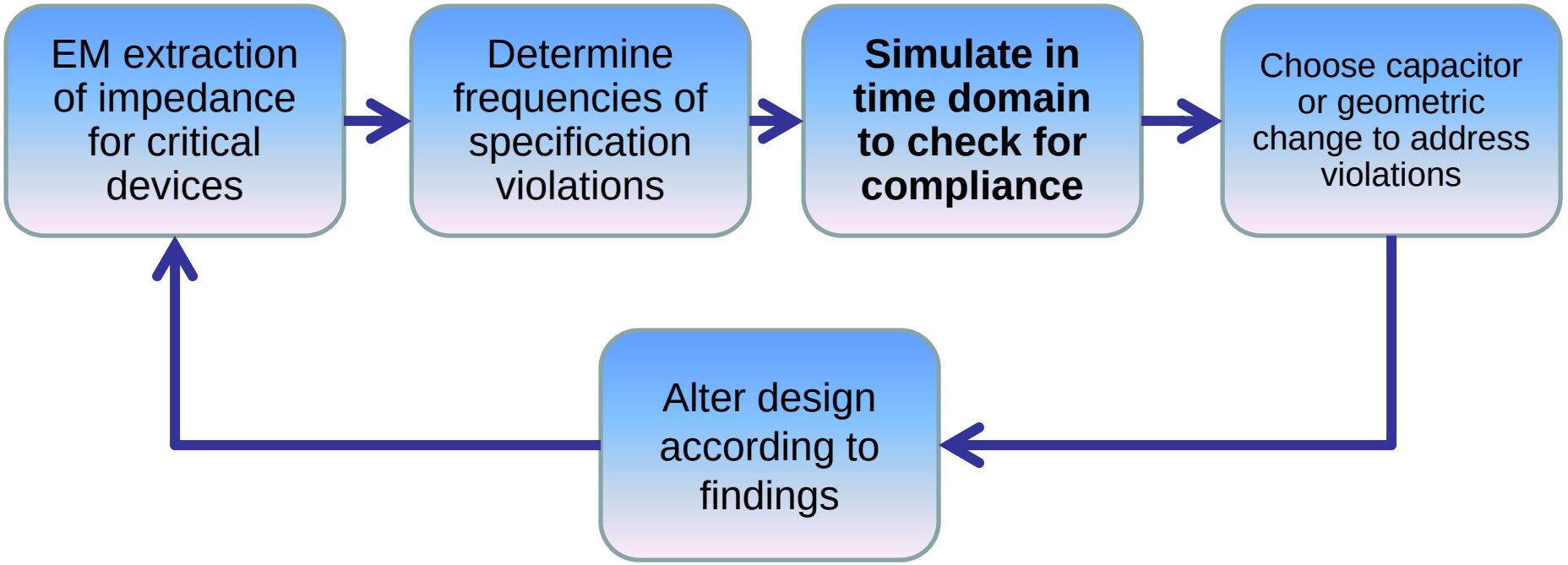
Bare Board

Target impedance 800 mOhm to 667 MHz

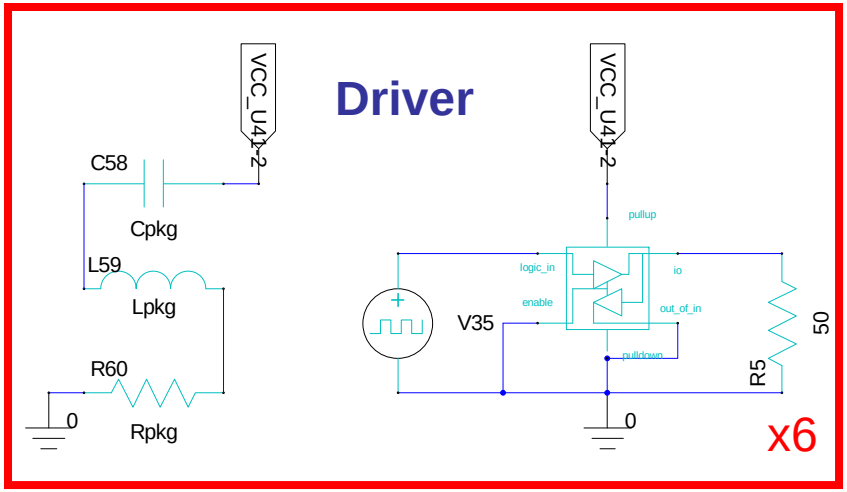


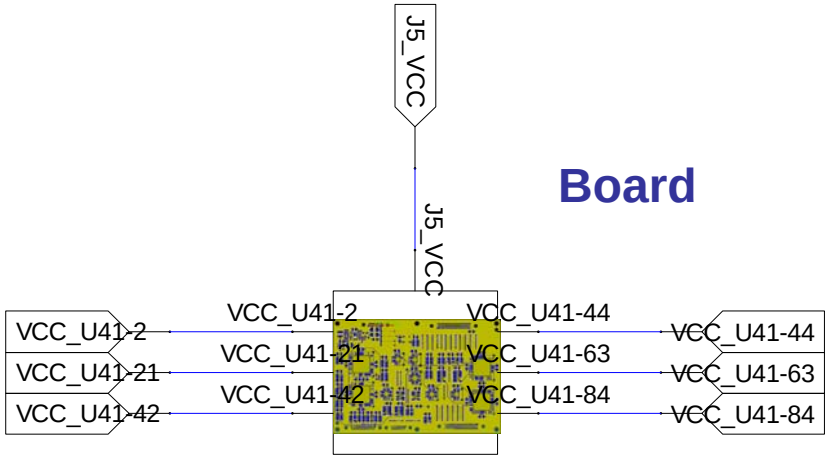
Bare Board

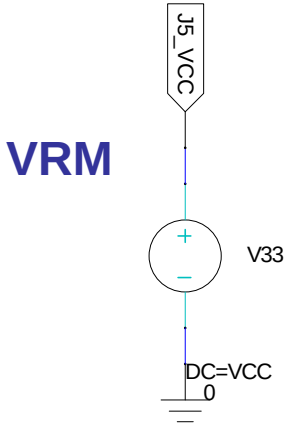
PDS Design Flow



Time Domain Schematic





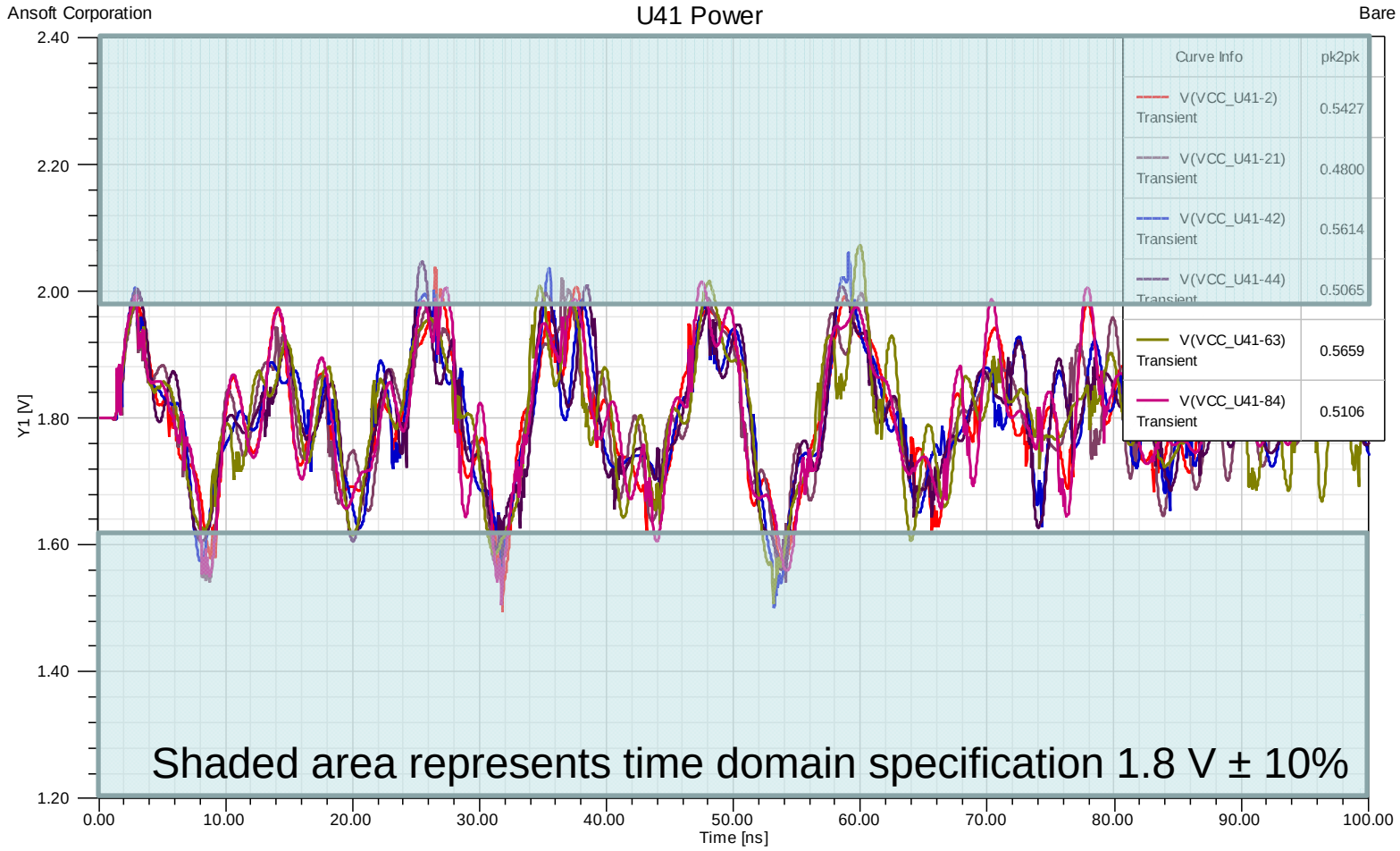


800 Mbps data rate

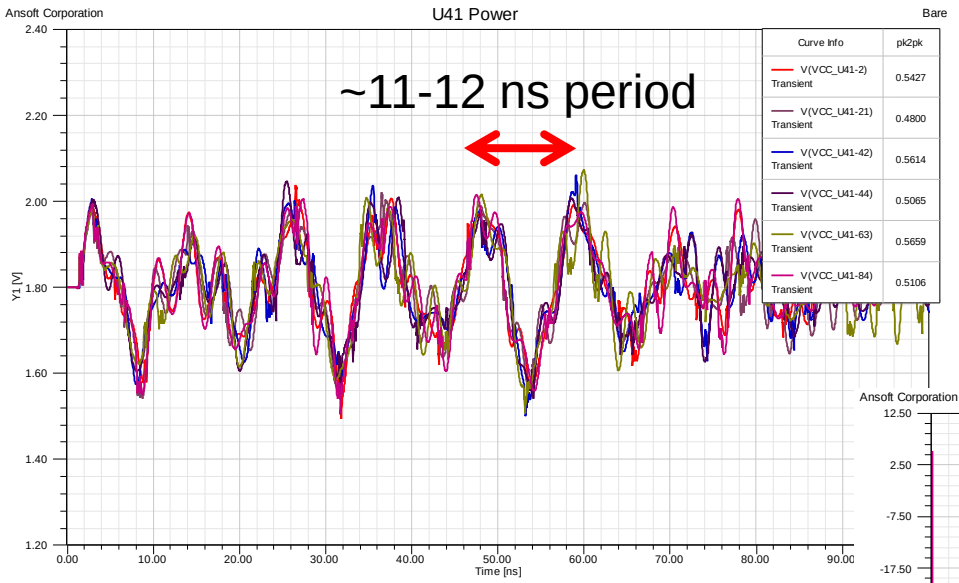
DDR2 IBIS driver into ideal termination used as load for PDS

Package decoupling modeled using a capacitor w/ ESR, ESL

Switching Power Noise

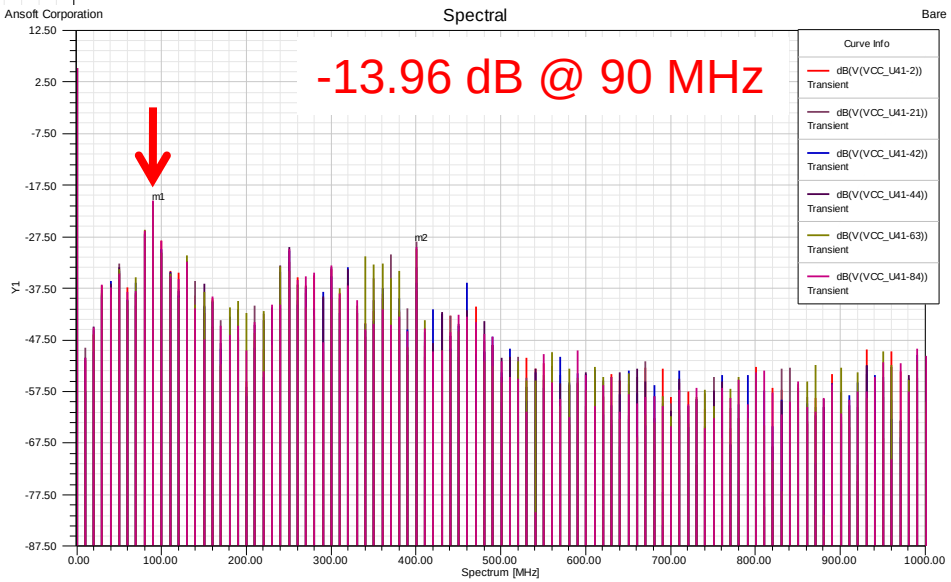


Spectral Analysis

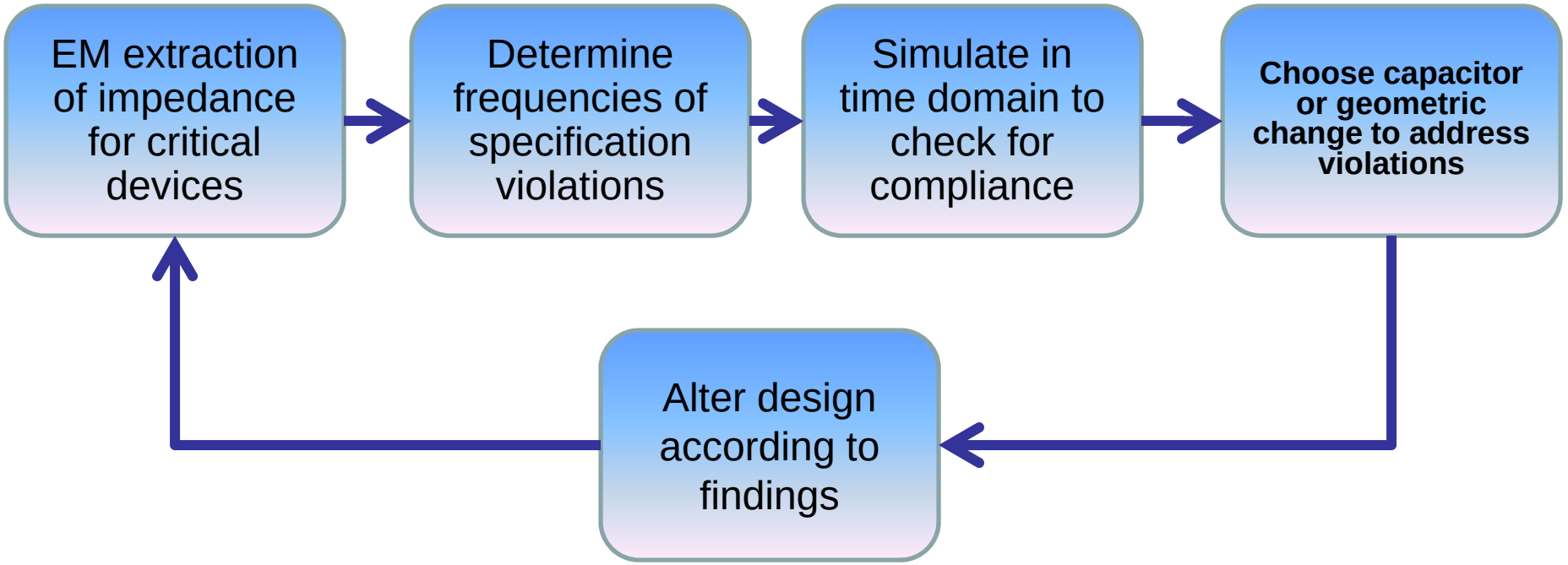


11-12 ns period corresponds to frequency of 80-90 MHz

This is confirmed by the spectral plot and correlates with the ideal driver simulation shown earlier (peak @ 83 MHz)

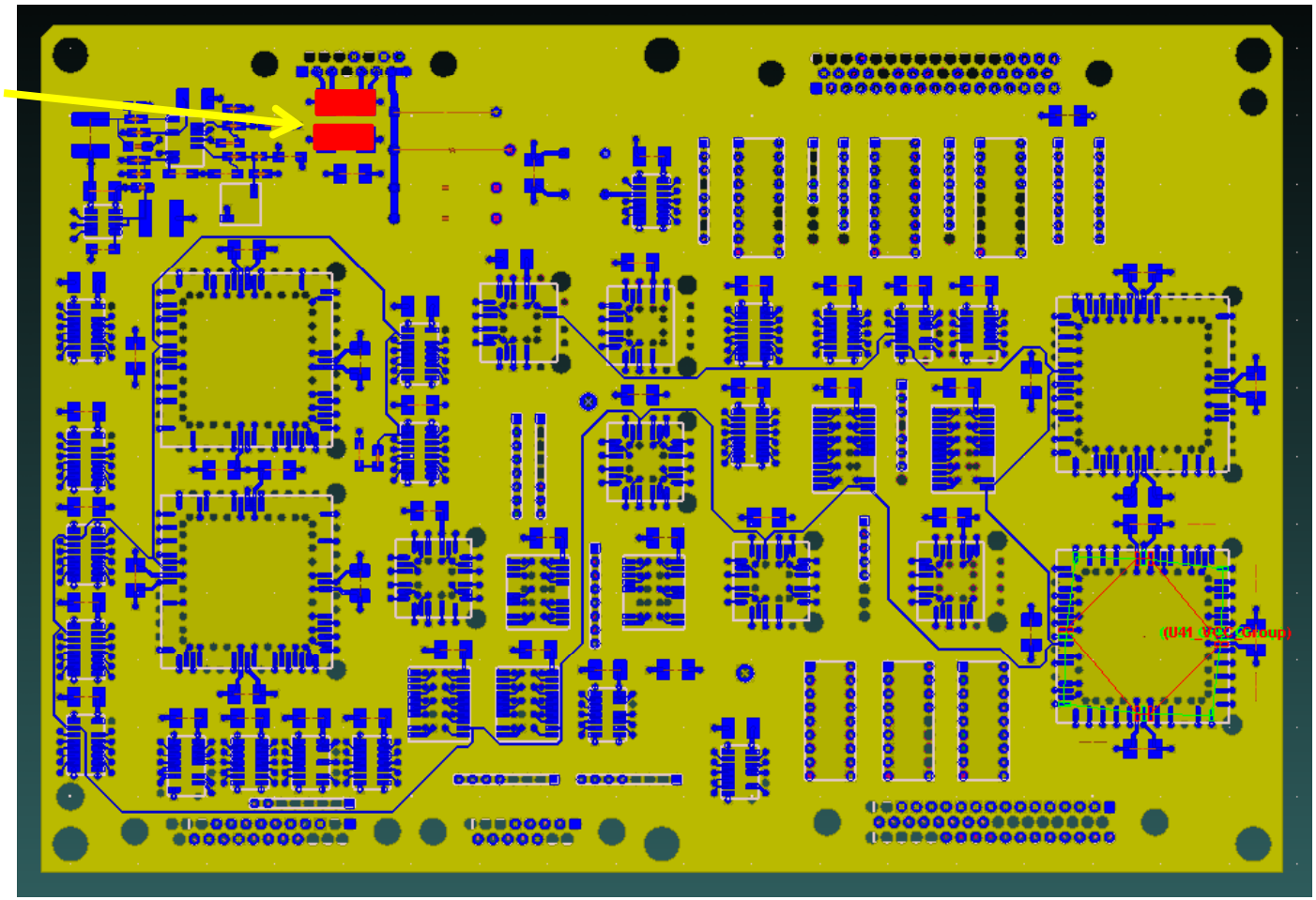


PDS Design Flow

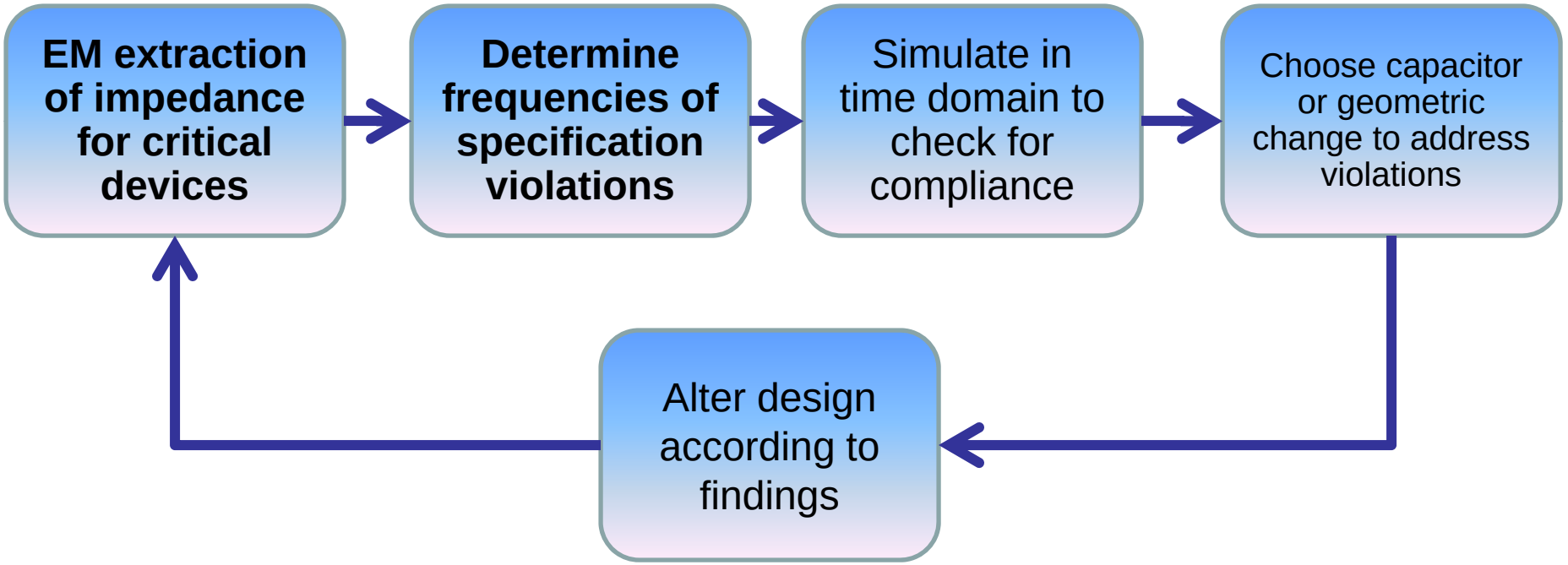


Adding Bulk Capacitors

Added two 47 uF capacitors as specified by VRM manufacturer

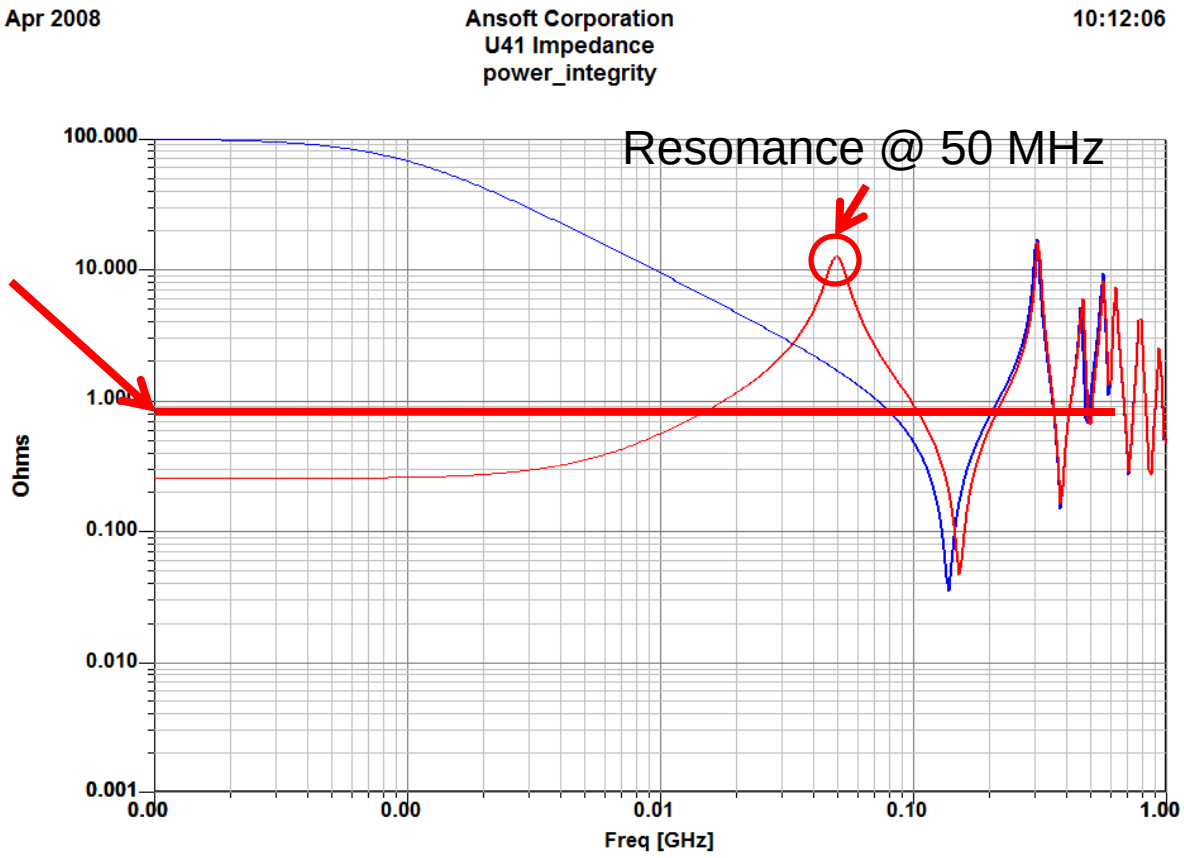


PDS Design Flow



Bare Board vs. Bulk Capacitors

Target impedance 800 mOhm to 667 MHz

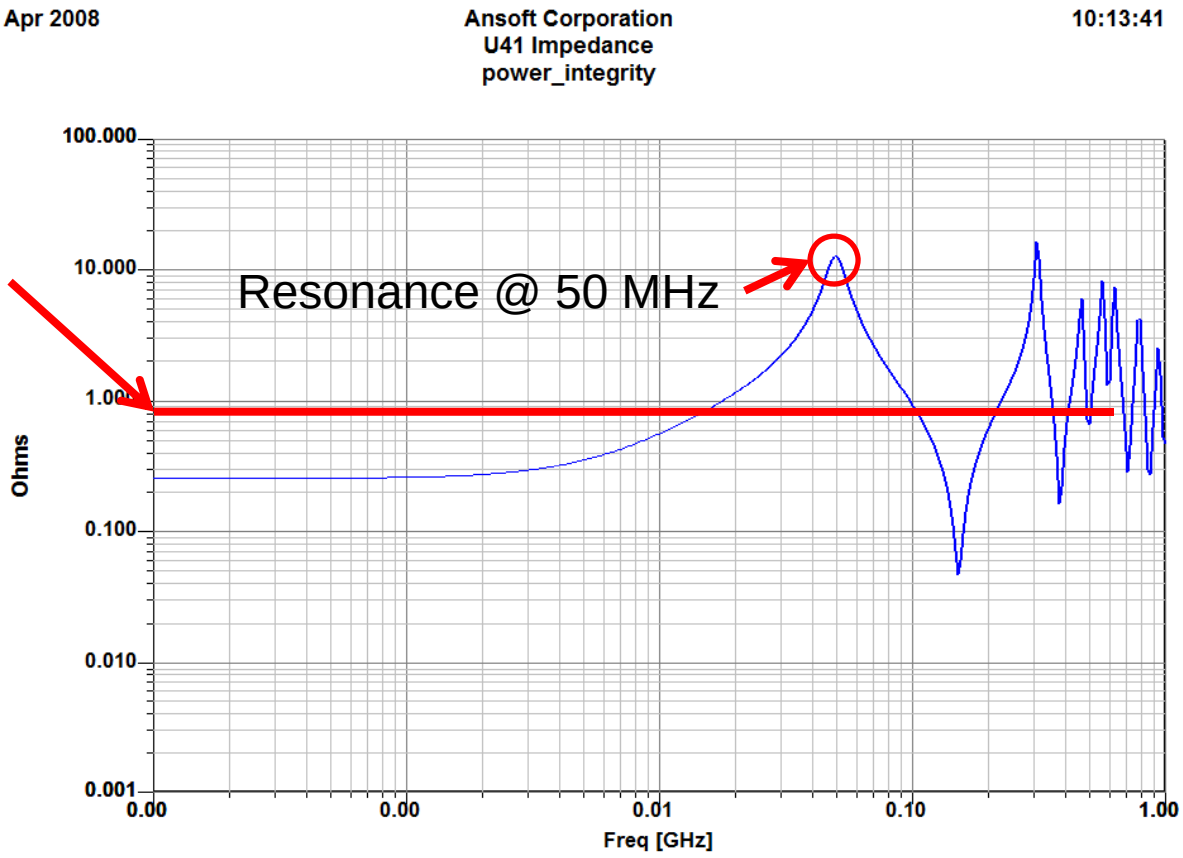


Bare Board

Board w/ Bulk Caps

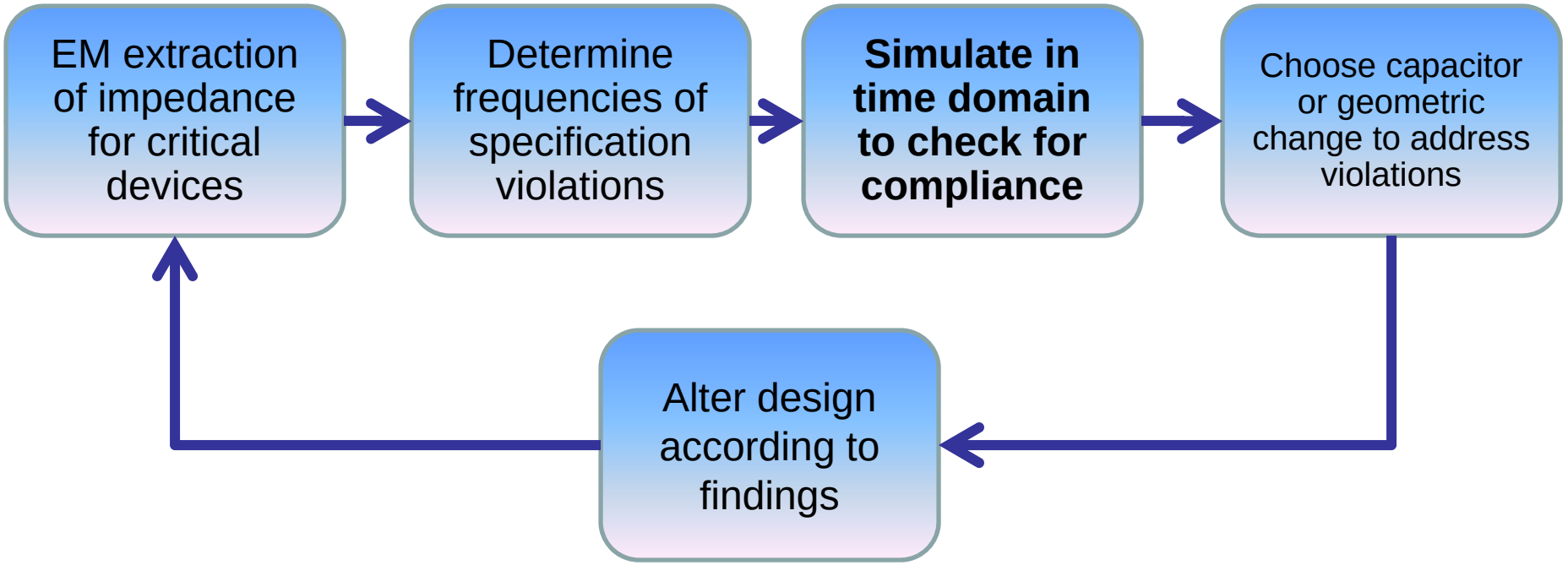
Bulk Capacitors

Target impedance 800 mOhm to 667 MHz

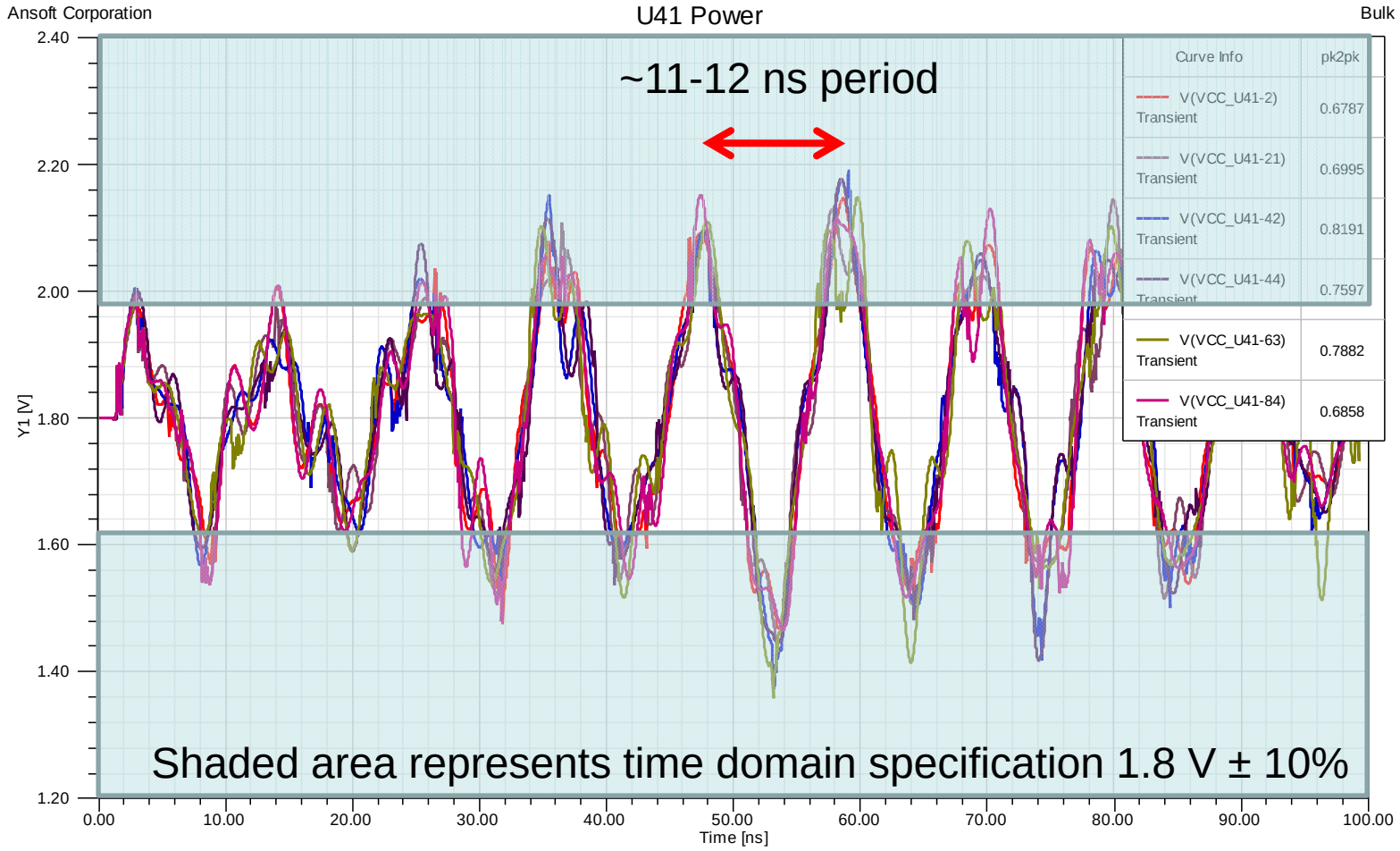


Board w/ Bulk Caps

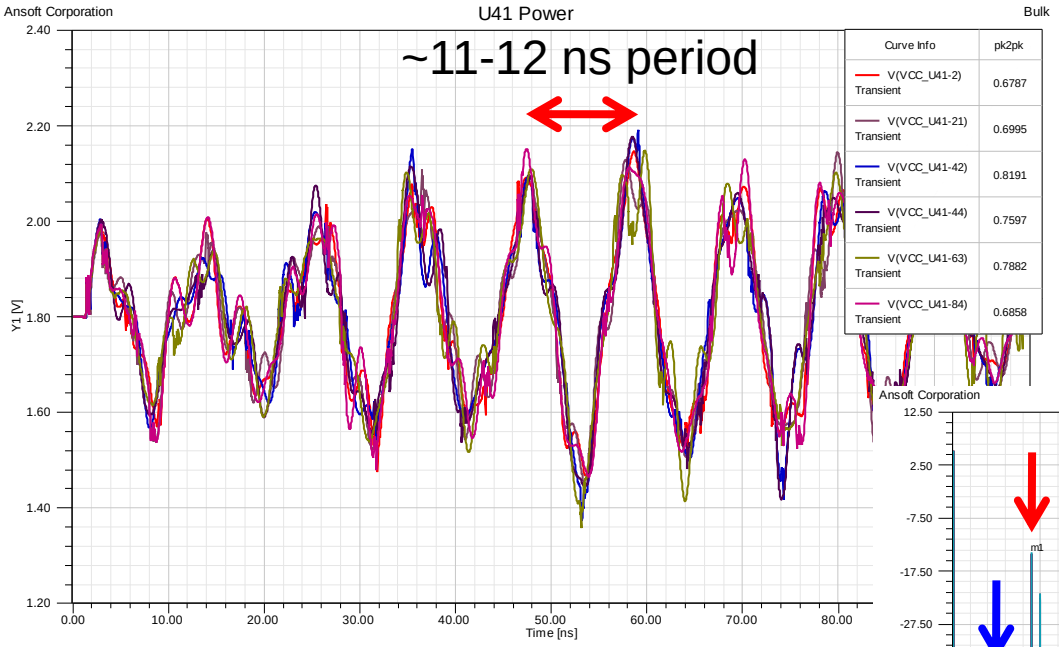
PDS Design Flow



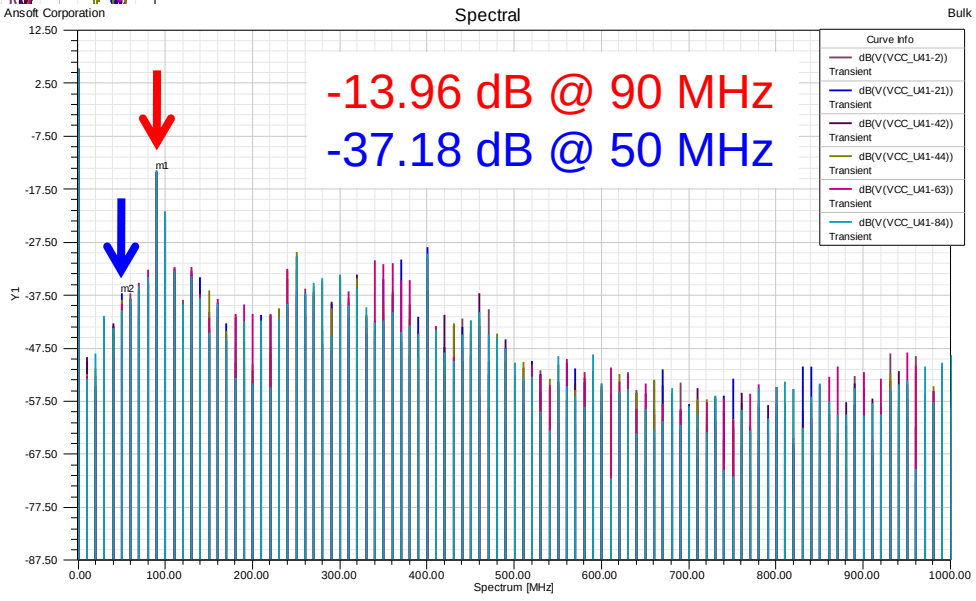
Switching Power Noise



Spectral Analysis

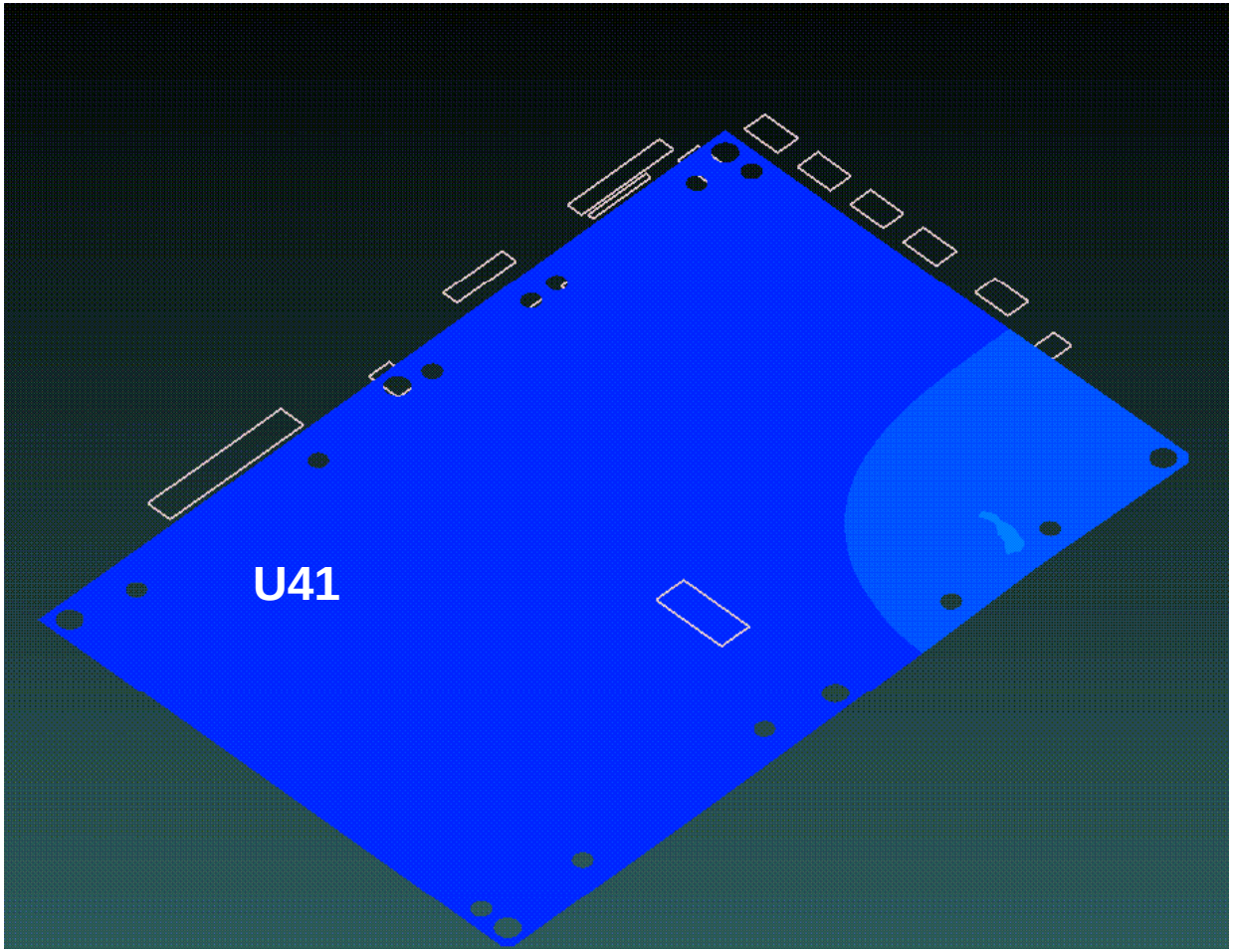


Same 11-12 ns period as exhibited by bare board

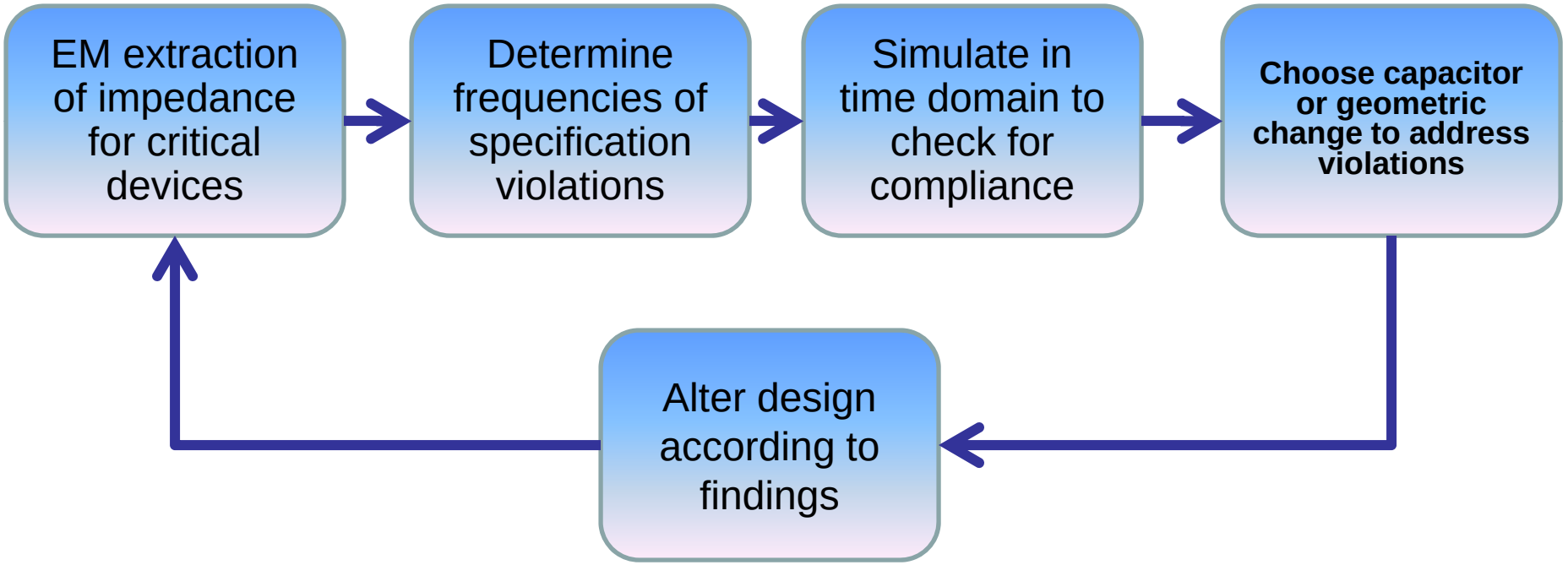


Note that resonance @ 50 MHz is not excited due as indicated by low spectral content at that frequency

Resonance at 50 MHz

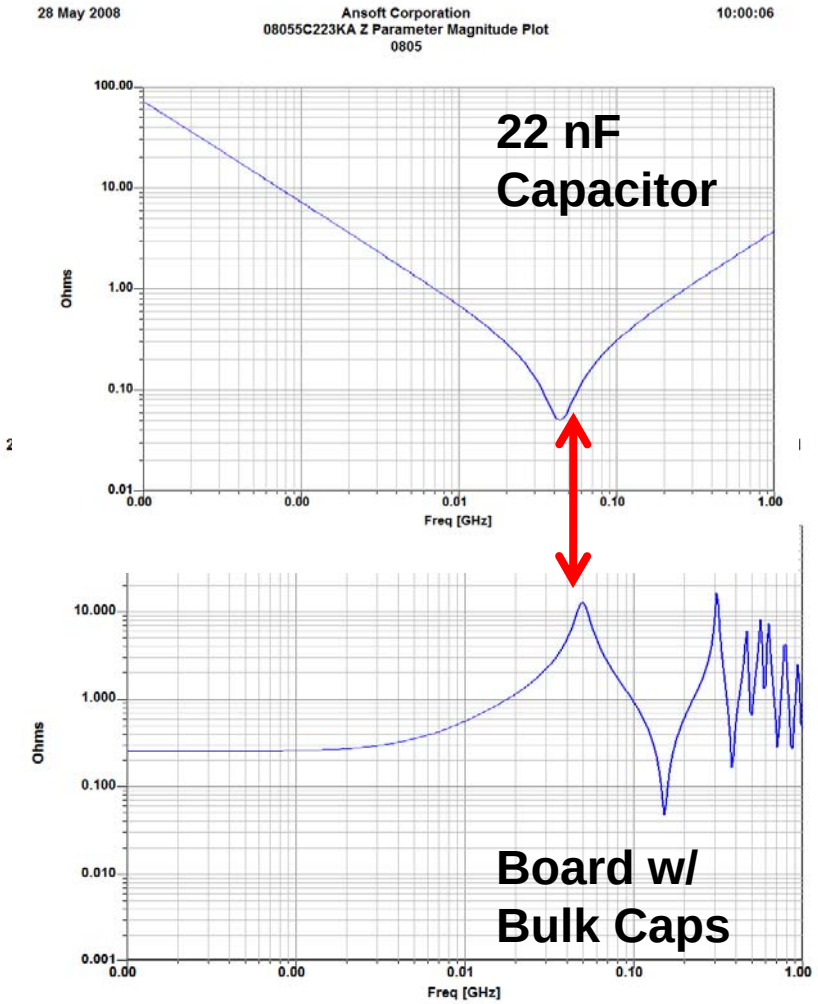


PDS Design Flow



Choosing a Capacitor

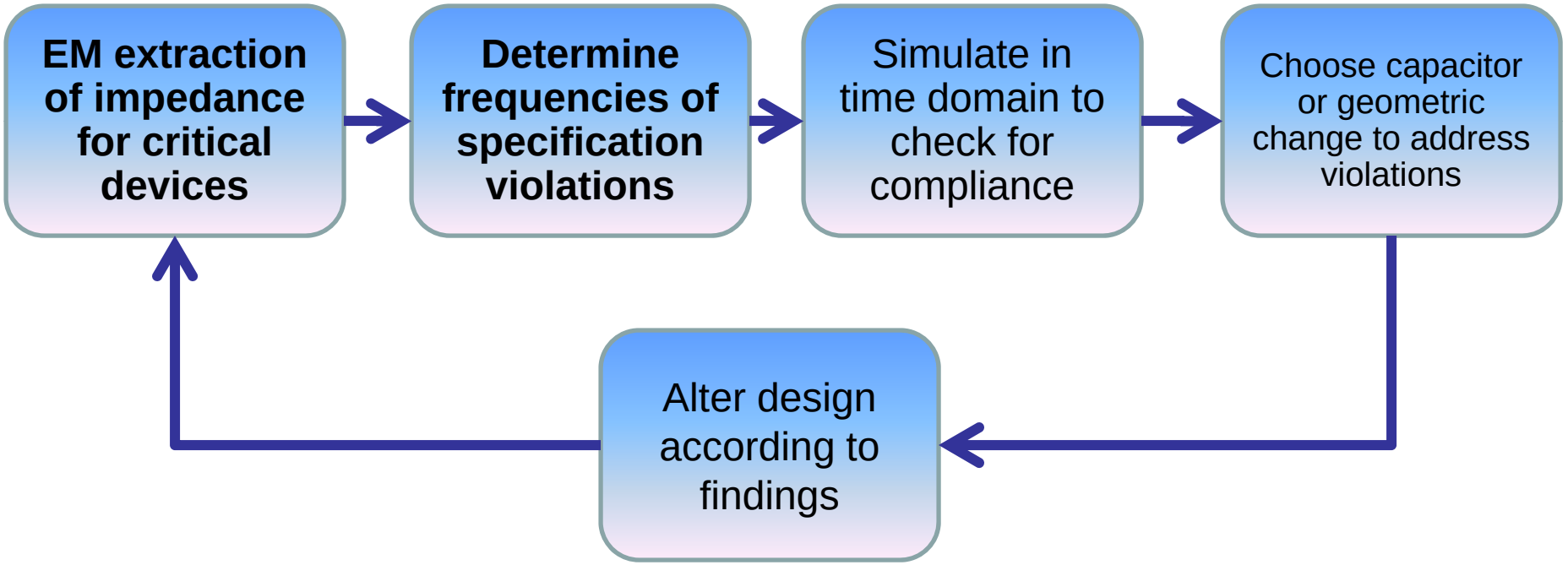
- To reduce the effect of a resonance, choose a capacitor with a low impedance at the resonant frequency



Added HF Capacitors

- 52 20 nF capacitors were added across the board to reduce high-frequency impedance and to cancel resonance at 50 MHz

PDS Design Flow



Bulk vs. HF Capacitors 1

Target impedance 800 mOhm to 667 MHz

Board w/ Bulk Caps

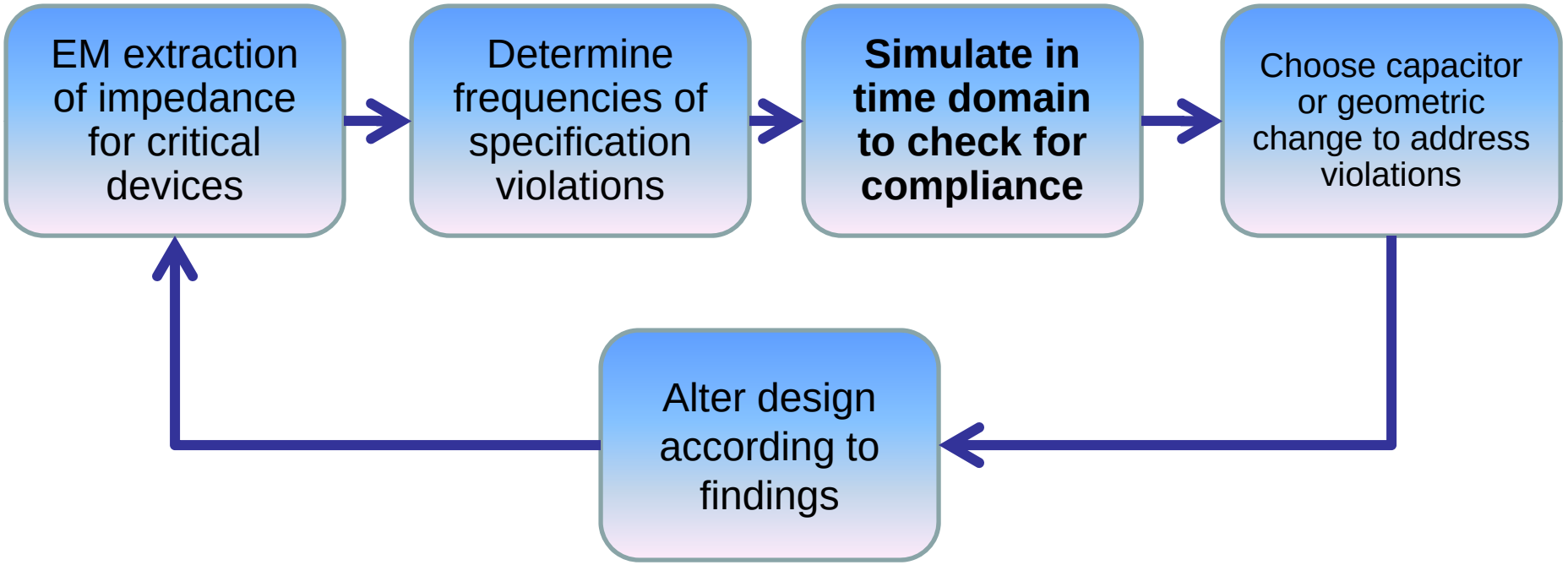
Board w/ HF Caps 1

HF Capacitors 1

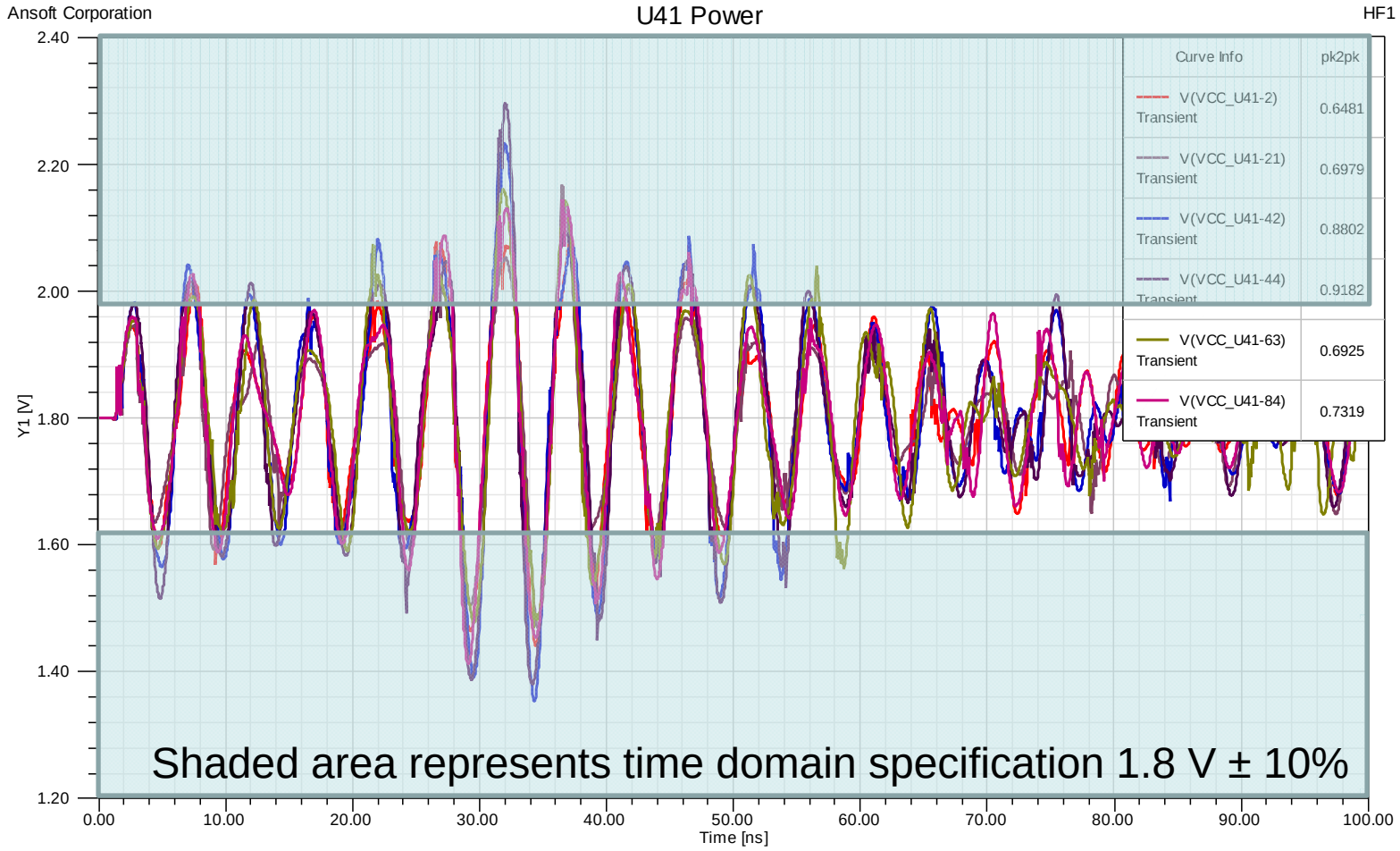
Target impedance 800 mOhm to 667 MHz

Board w/ HF Caps 1

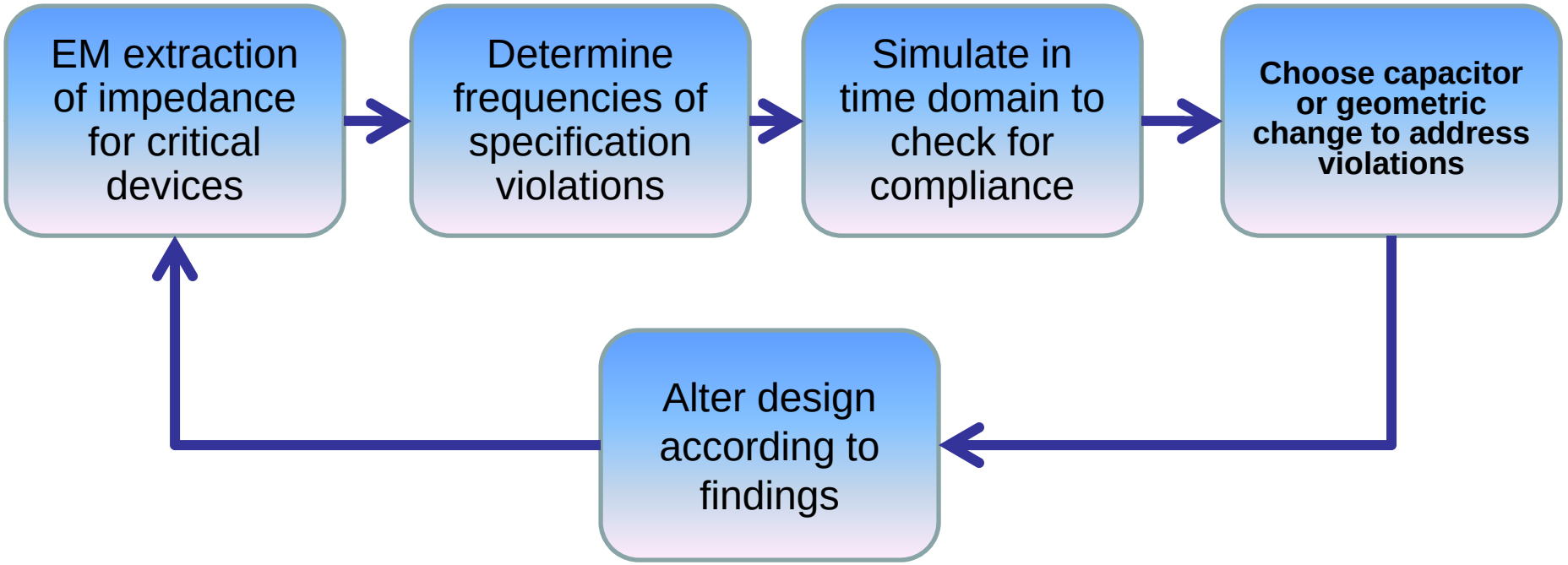
PDS Design Flow



Switching Power Noise

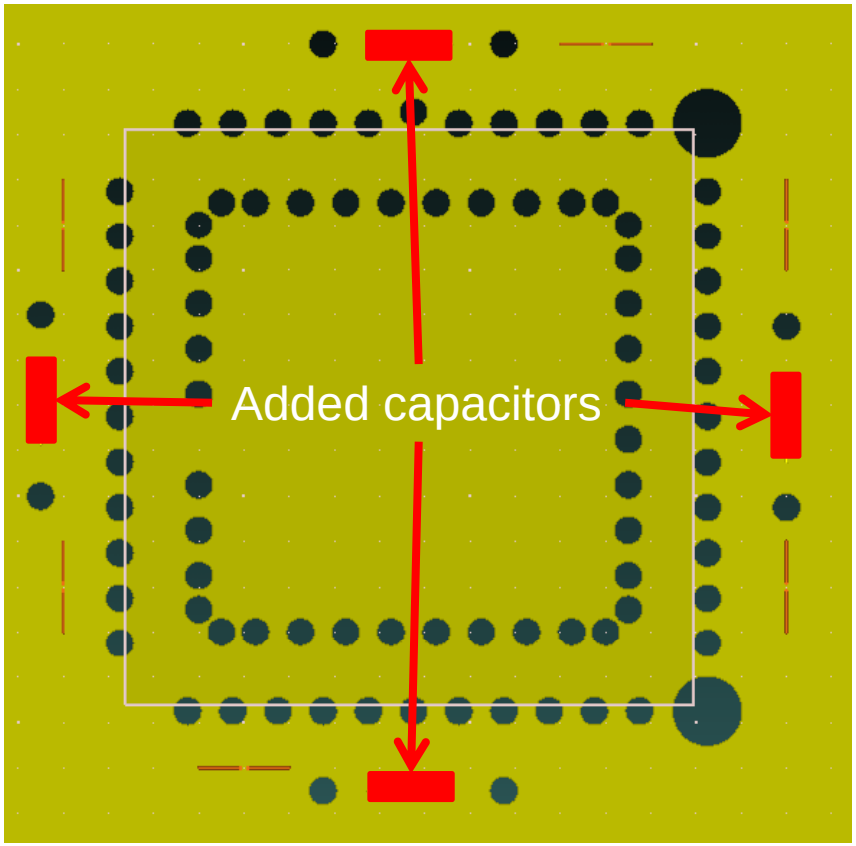


PDS Design Flow

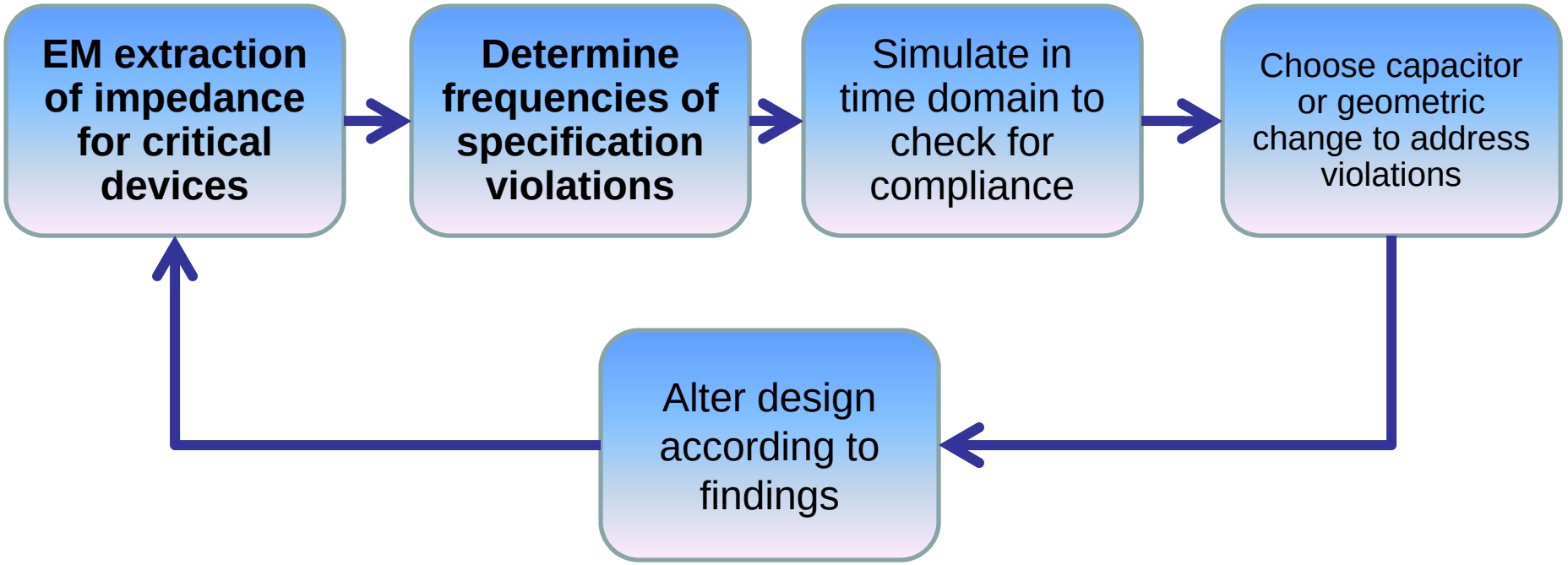


Extending Low Impedance

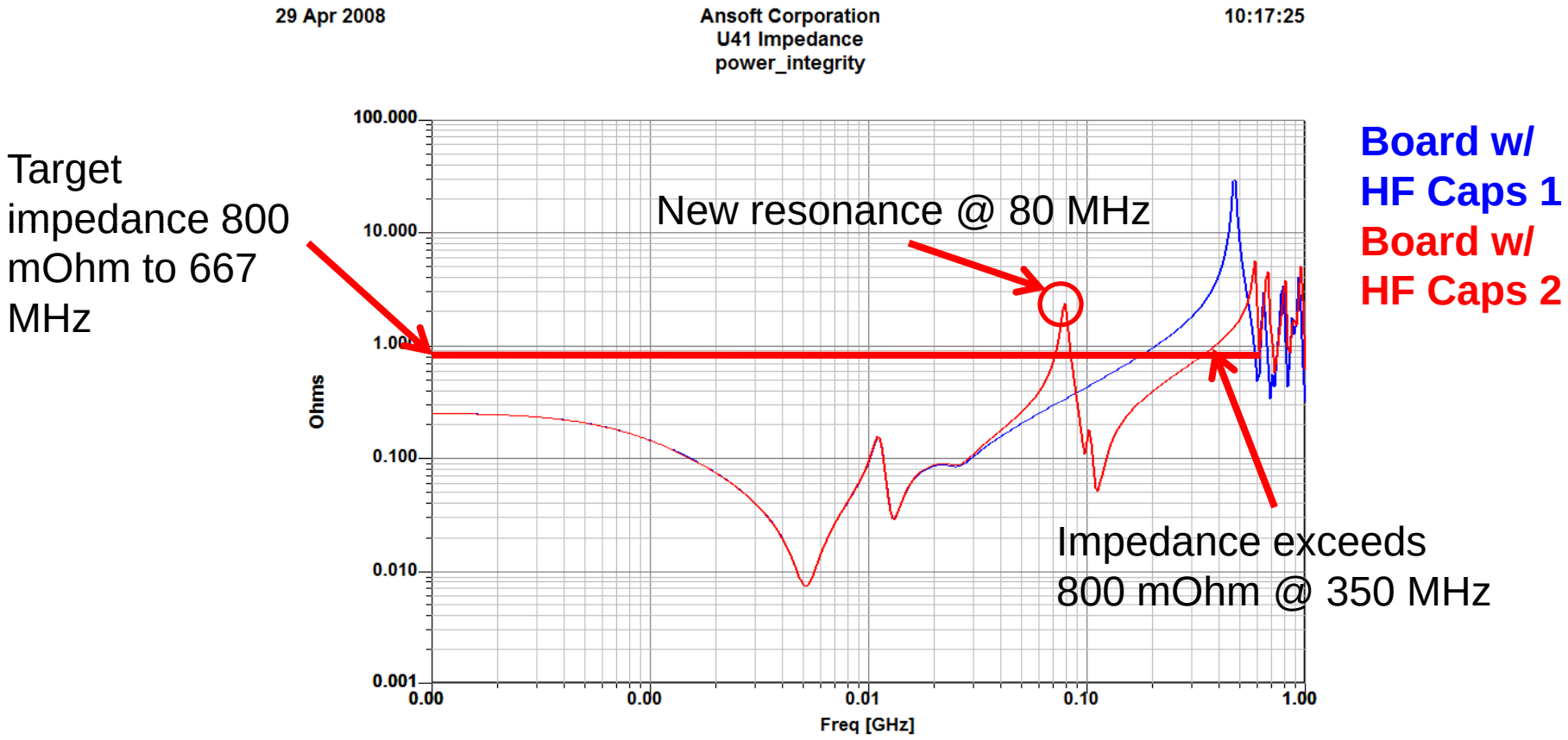
- 10 1.2 nF capacitors were added across the board to extend minimum high-frequency impedance
- 1.2 nF capacitor was chosen due to low impedance at 200 MHz
- 4 of these were located near U41



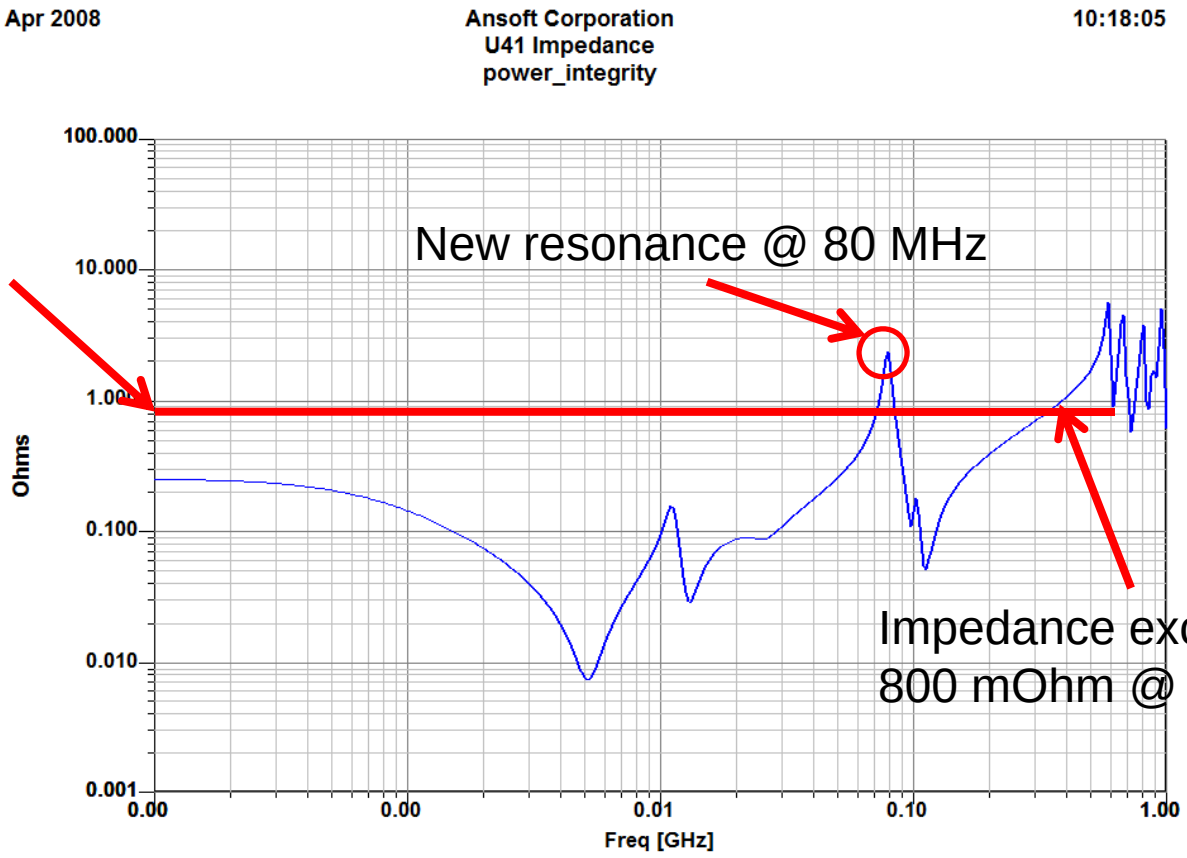
PDS Design Flow



HF 1 vs. HF 2


29 Apr 2008
Ansoft Corporation
U41 Impedance
power_integrity
10:17:25
Target impedance 800 mOhm to 667 MHz
New resonance @ 80 MHz
Board w/ HF Caps 1
Board w/ HF Caps 2
Impedance exceeds 800 mOhm @ 350 MHz
Ohms
100.000
10.000
1.000
0.100
0.010
0.001
0.00
0.00
0.01
0.10
1.00
Freq [GHz]

HF 2

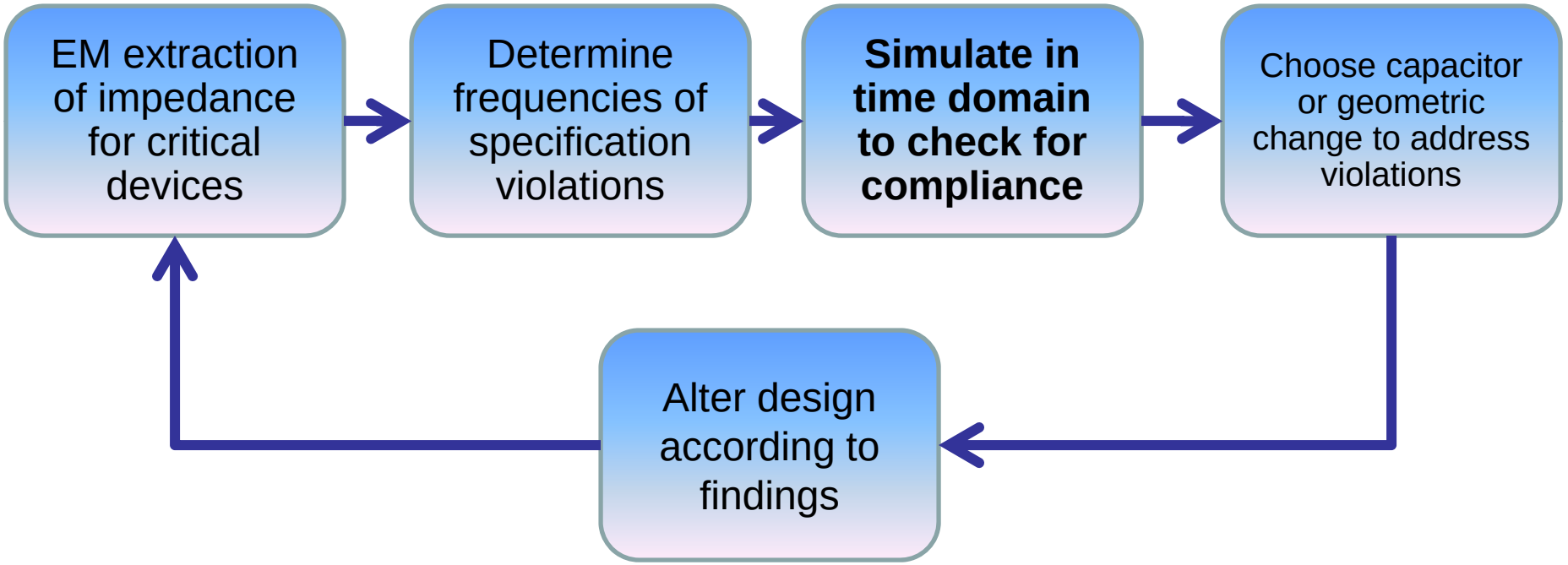


Target impedance 800 mOhm to 667 MHz

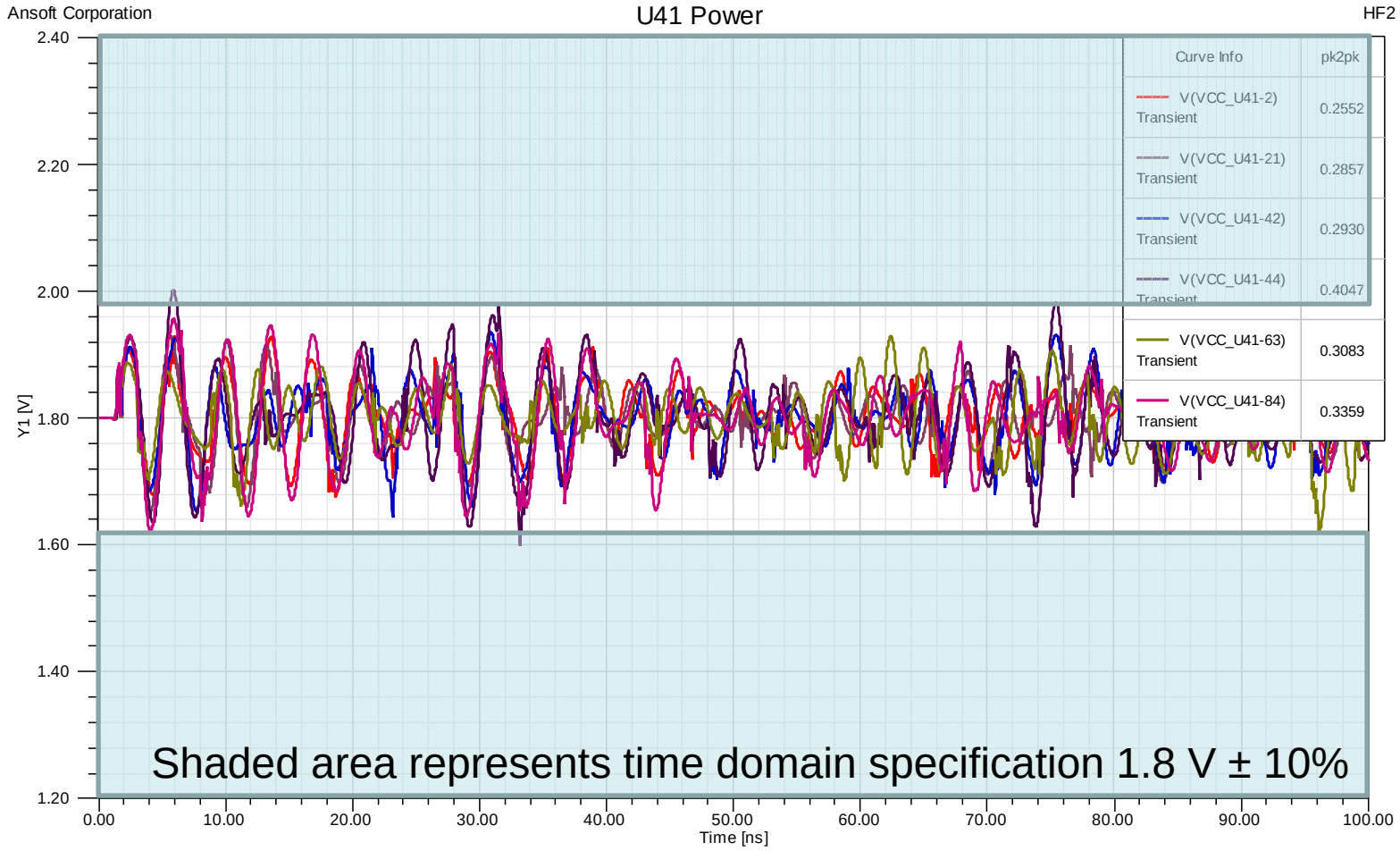
Impedance exceeds 800 mOhm @ 350 MHz

Board w/ HF Caps 2

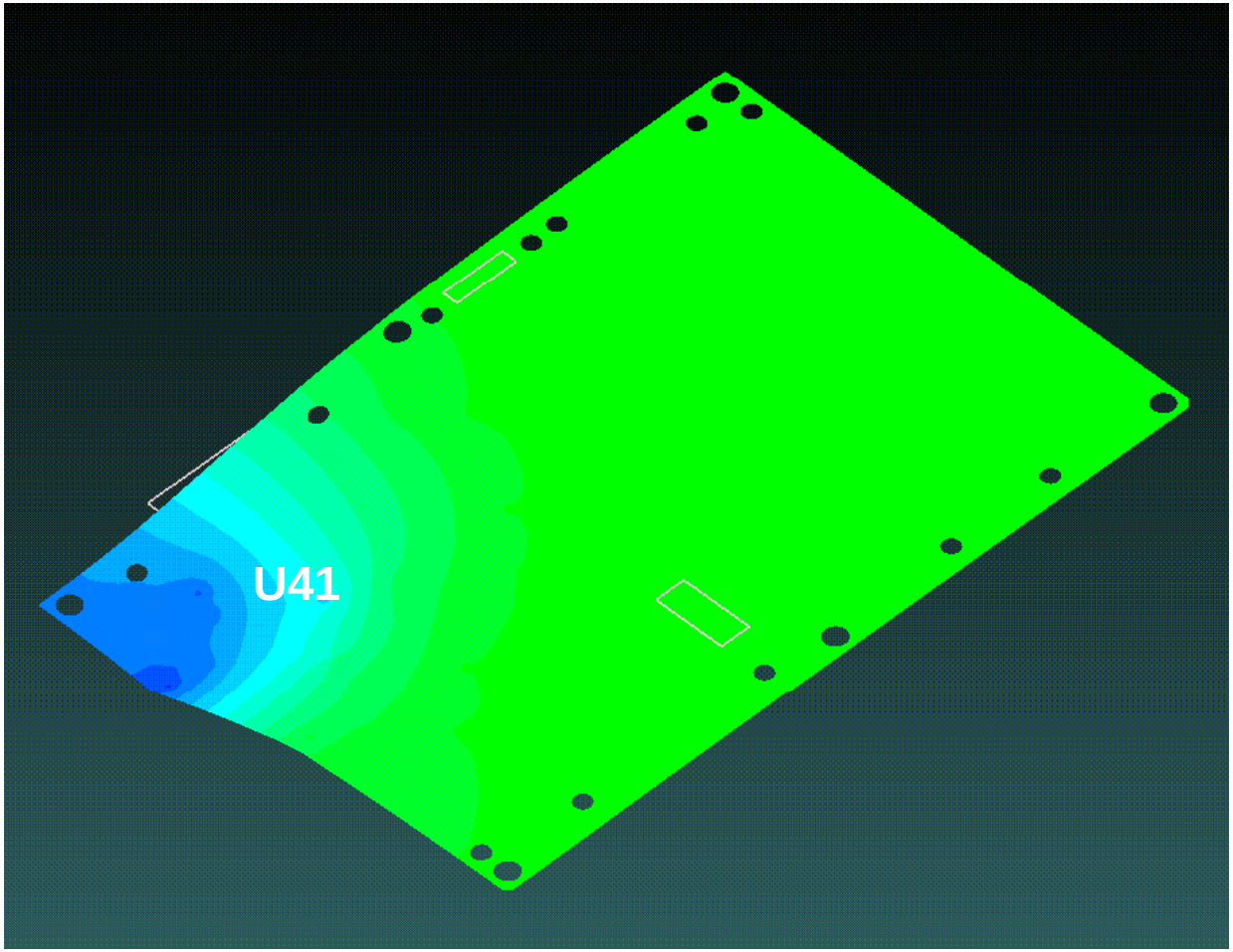
PDS Design Flow



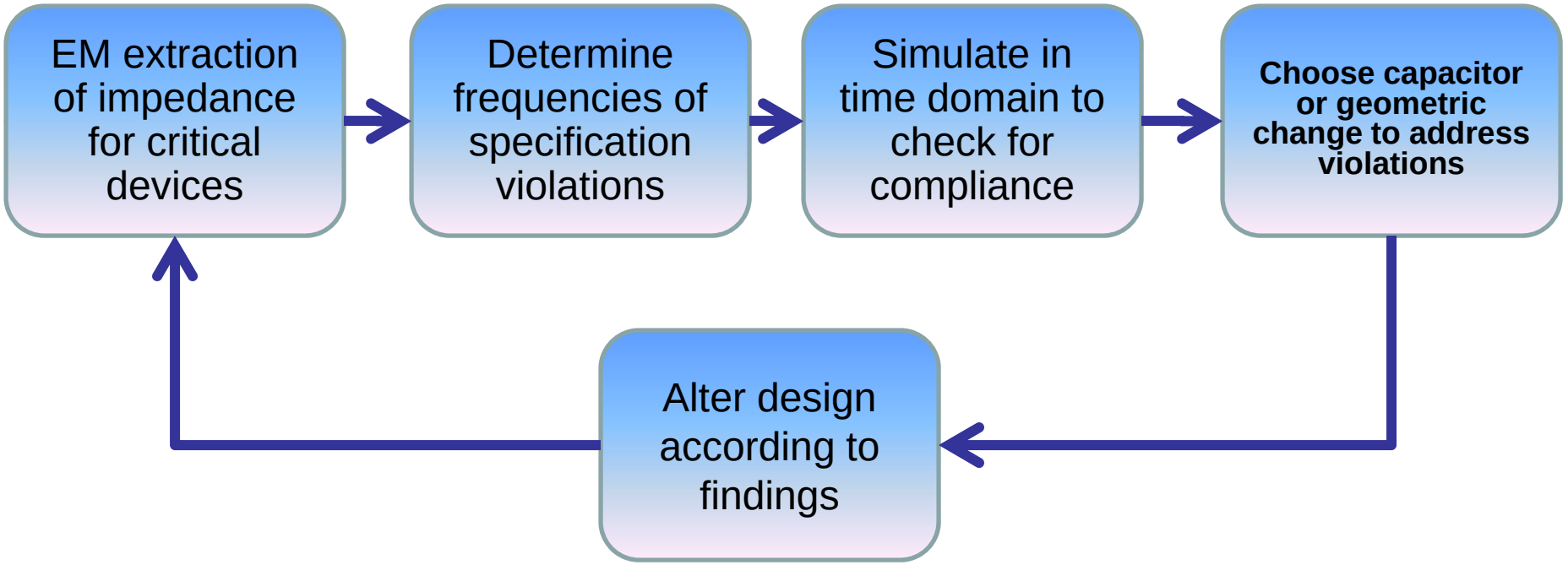
Switching Power Noise



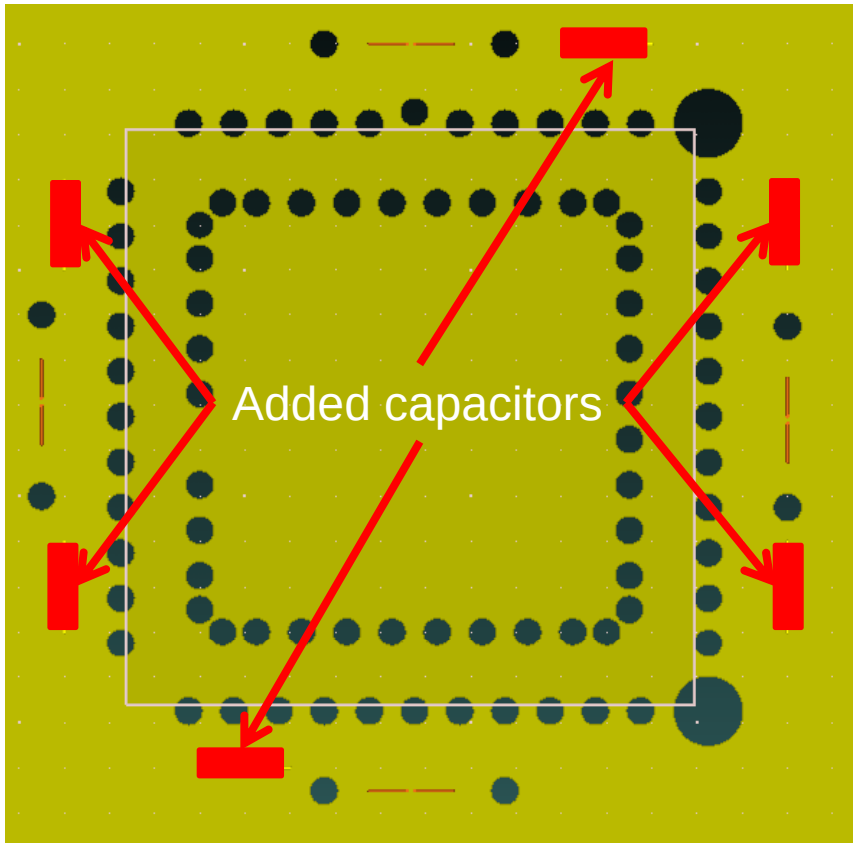
Resonance at 80 MHz



PDS Design Flow



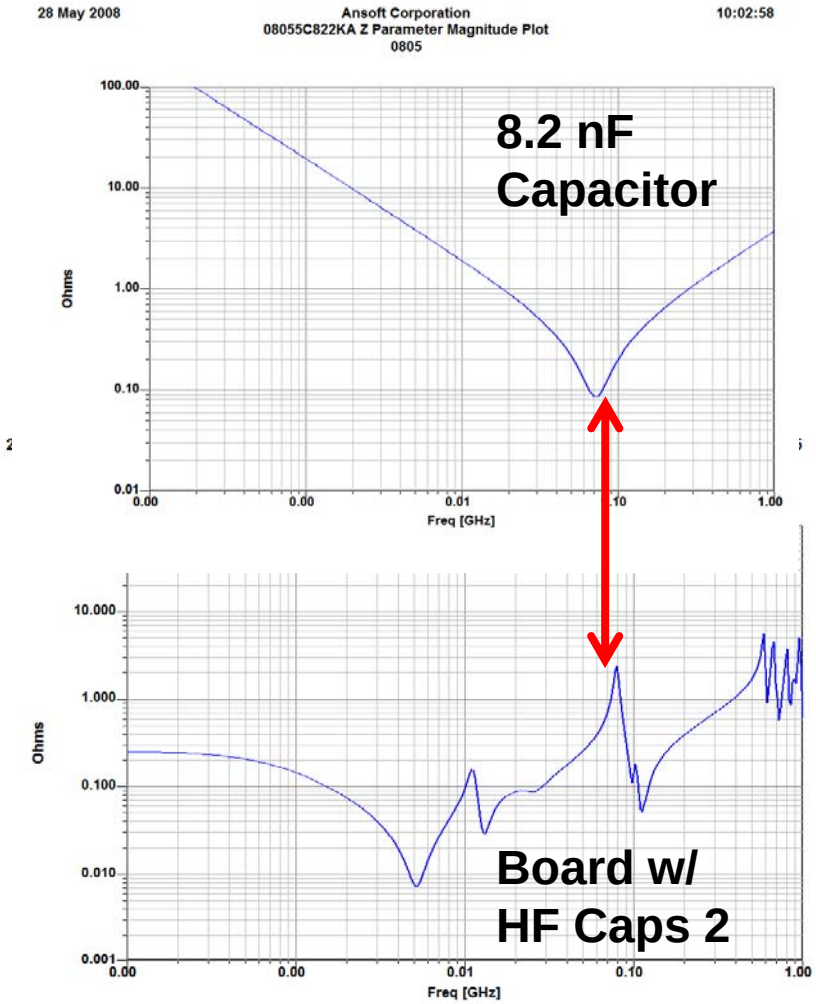
Removing a Resonance



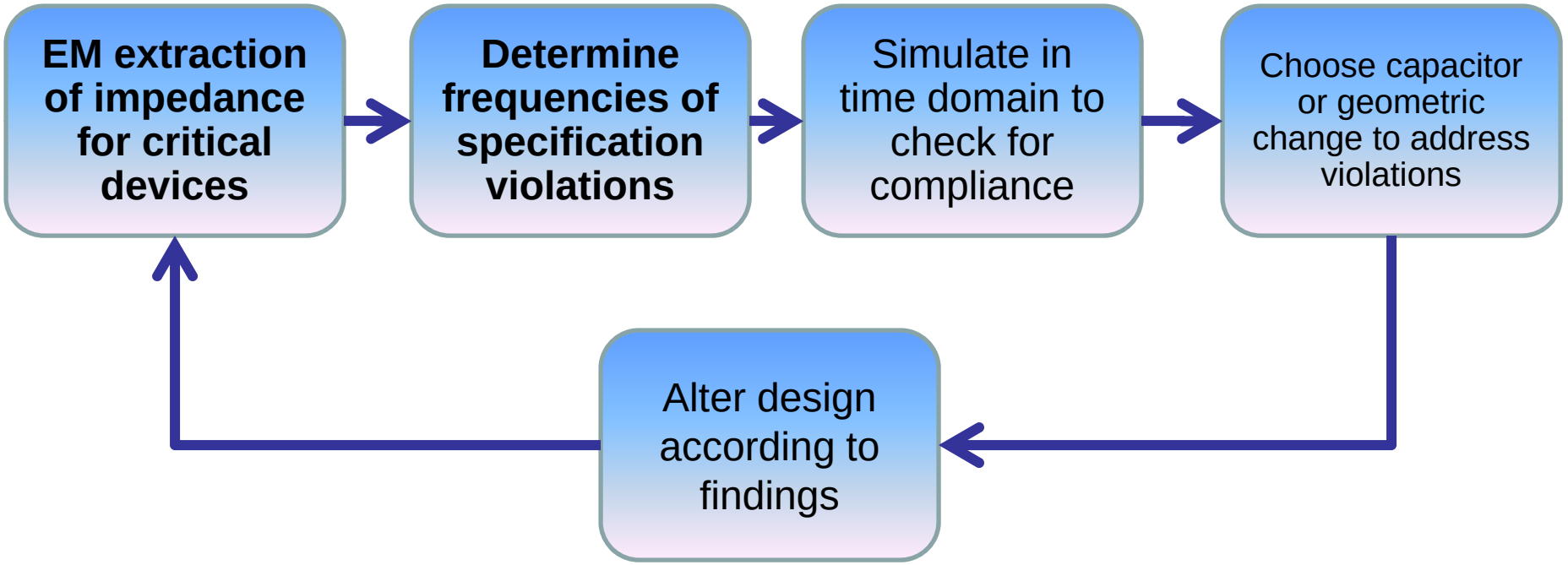
- Six 8 nF capacitors were added near U41 to cancel resonance at 80 MHz

Choosing a Capacitor

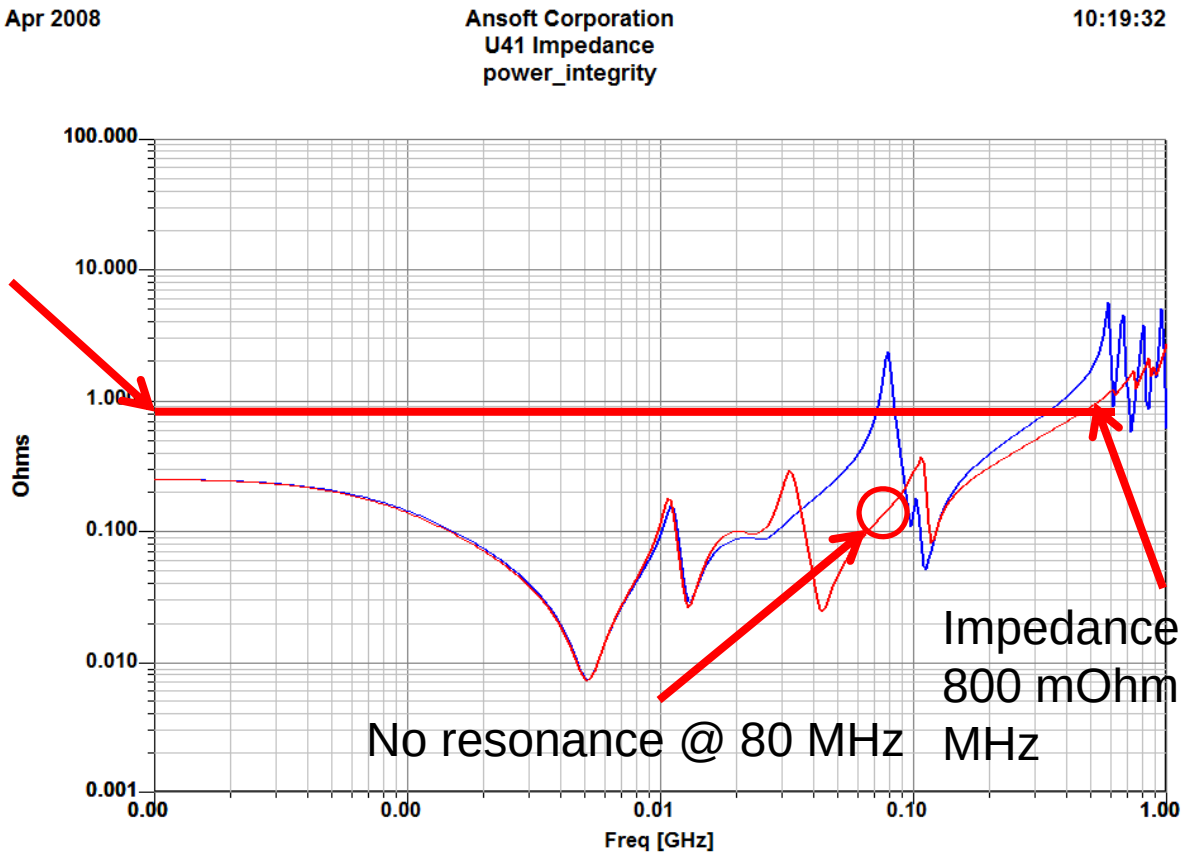
- To reduce the effect of a resonance, choose a capacitor with a low impedance at the resonant frequency



PDS Design Flow



HF 2 vs. HF 3



Target impedance 800 mOhm to 667 MHz

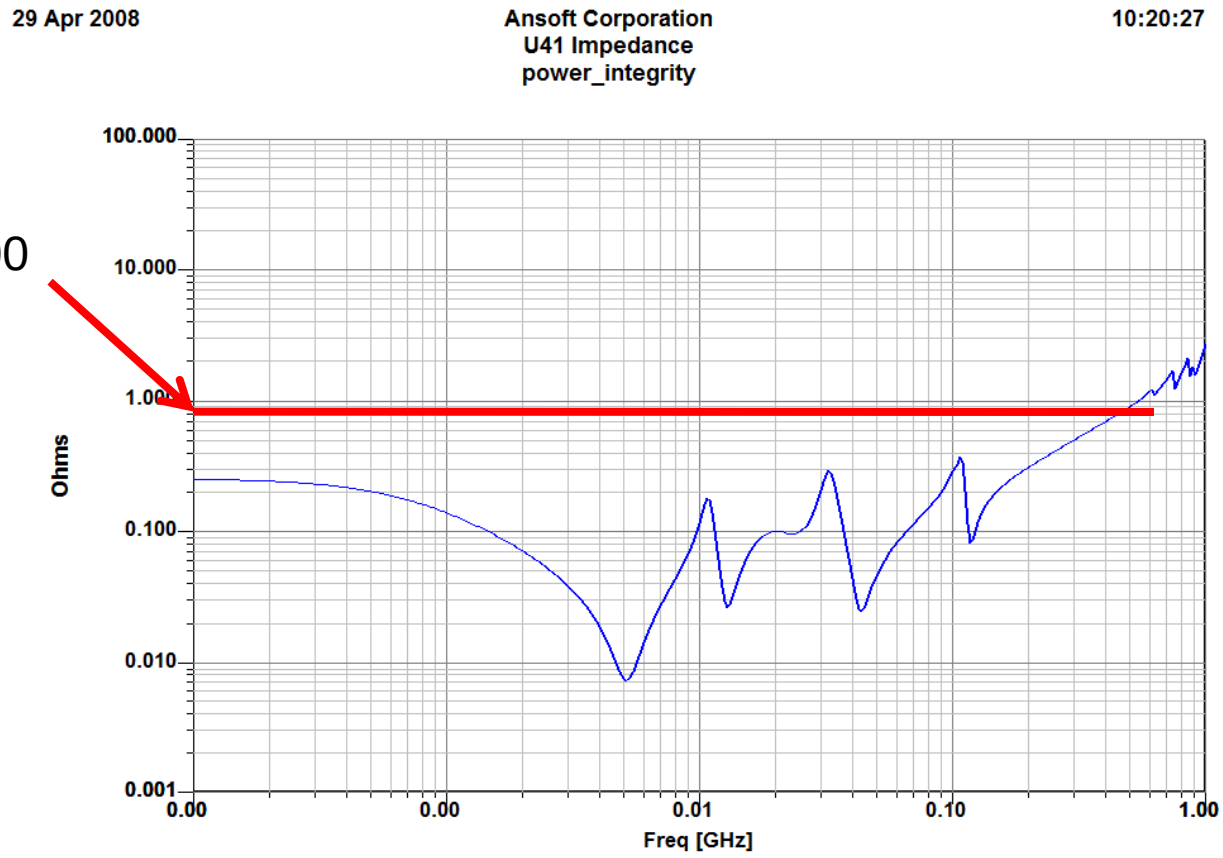
Board w/ HF Caps 2

Board w/ HF Caps 3

No resonance @ 80 MHz

Impedance crosses 800 mOhm @ 500 MHz

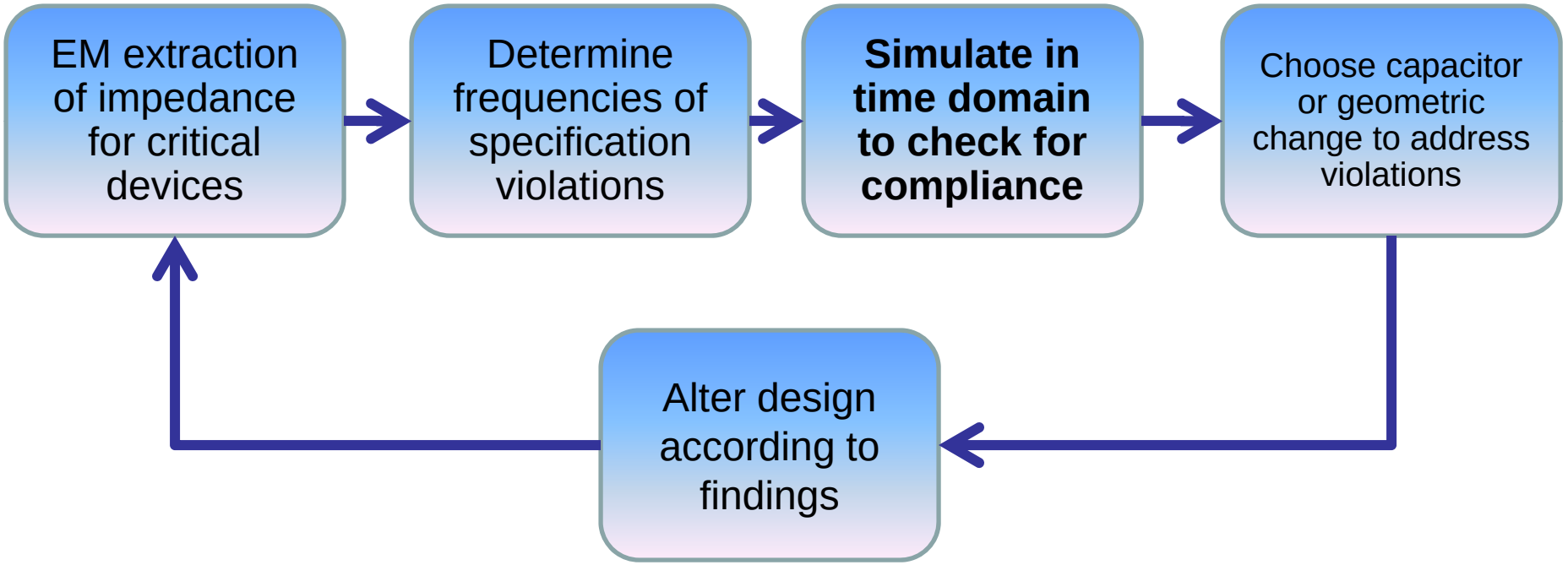
HF 3



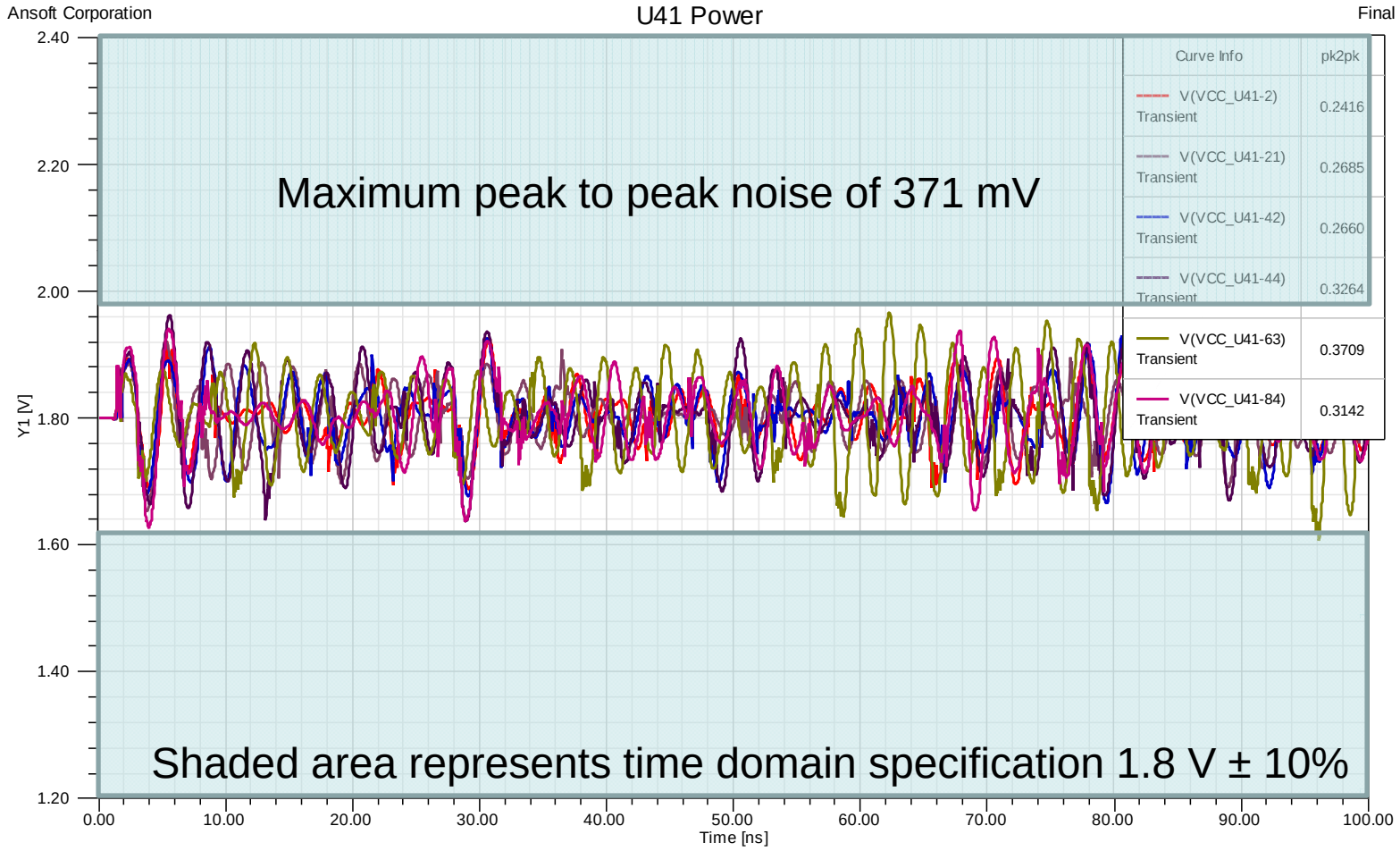
Target impedance 800 mOhm to 667 MHz

Board w/ HF Caps 3

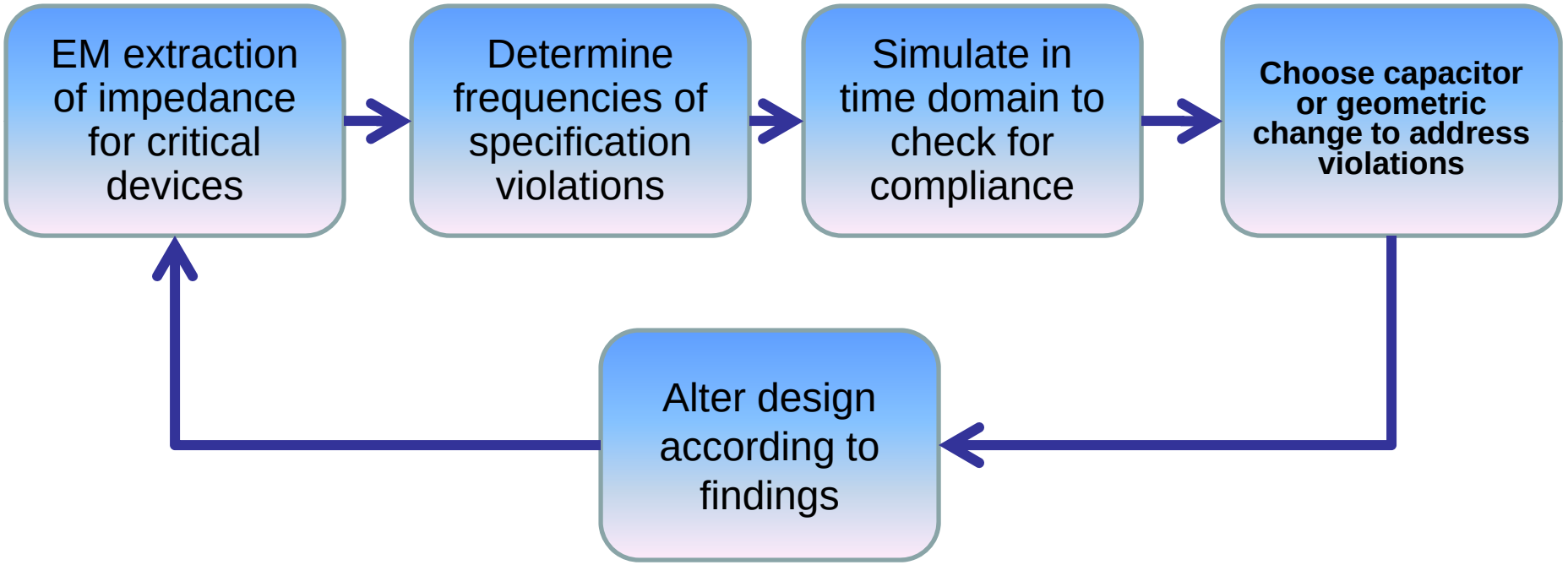
PDS Design Flow



Switching Power Noise

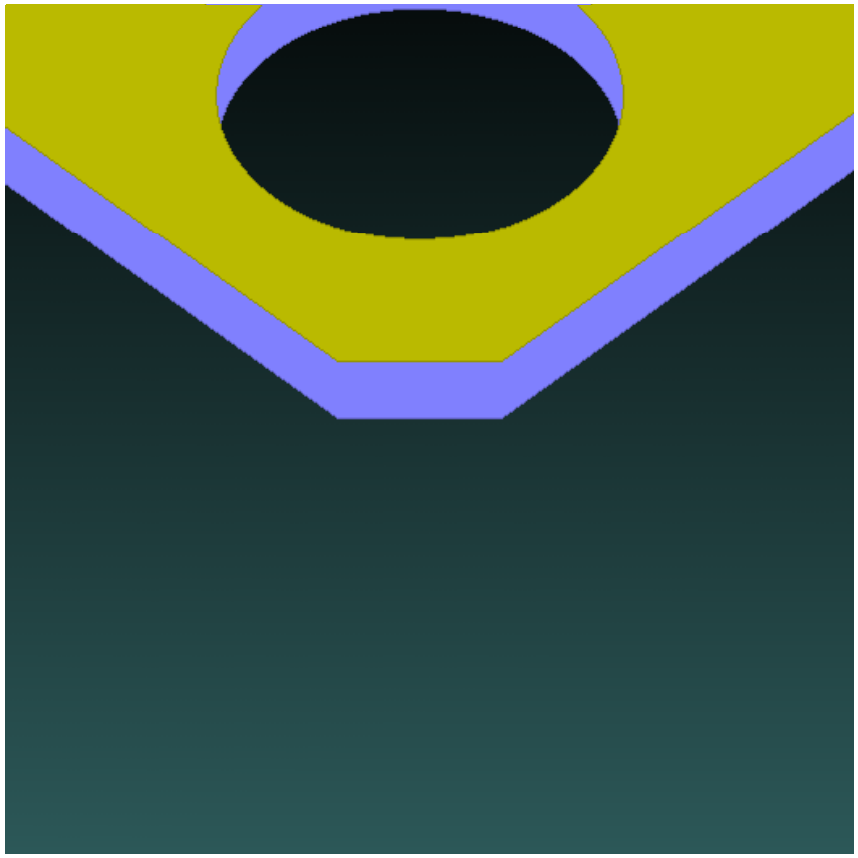


PDS Design Flow



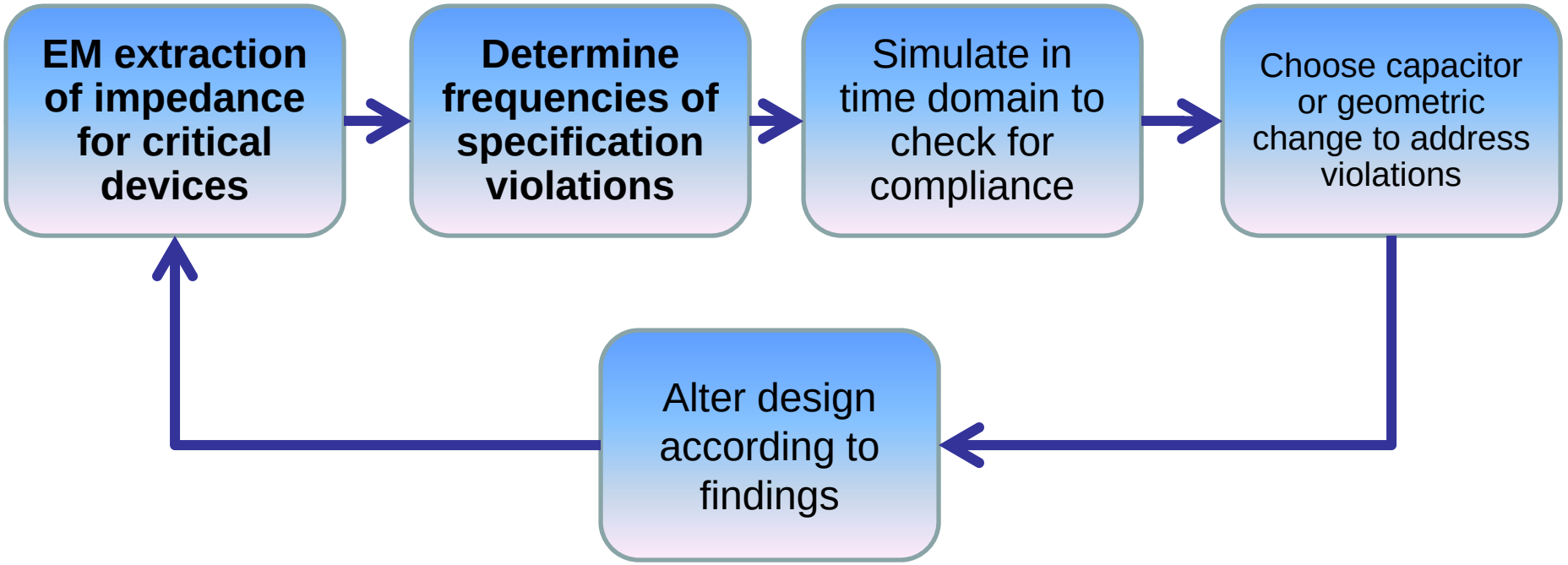
Buried Capacitance

- Due to parasitic inductance it will be impossible to further decouple the board with capacitors
- Using a thinner dielectric layer between power and ground planes introduces additional capacitance and reduces high frequency impedance



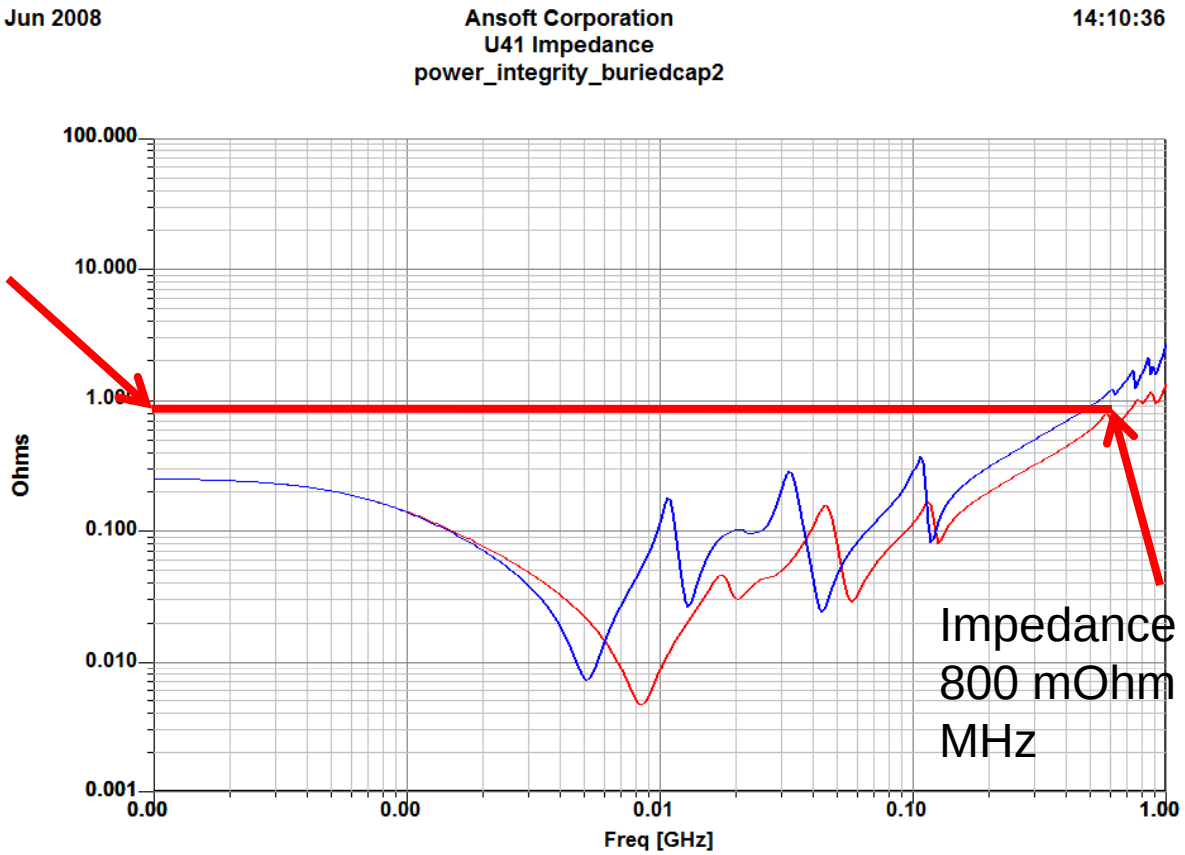
Capacitance of parallel plates: $C = \varepsilon \frac{A}{d}$

PDS Design Flow



HF 3 vs. Buried Capacitance

Target impedance 800 mOhm to 667 MHz



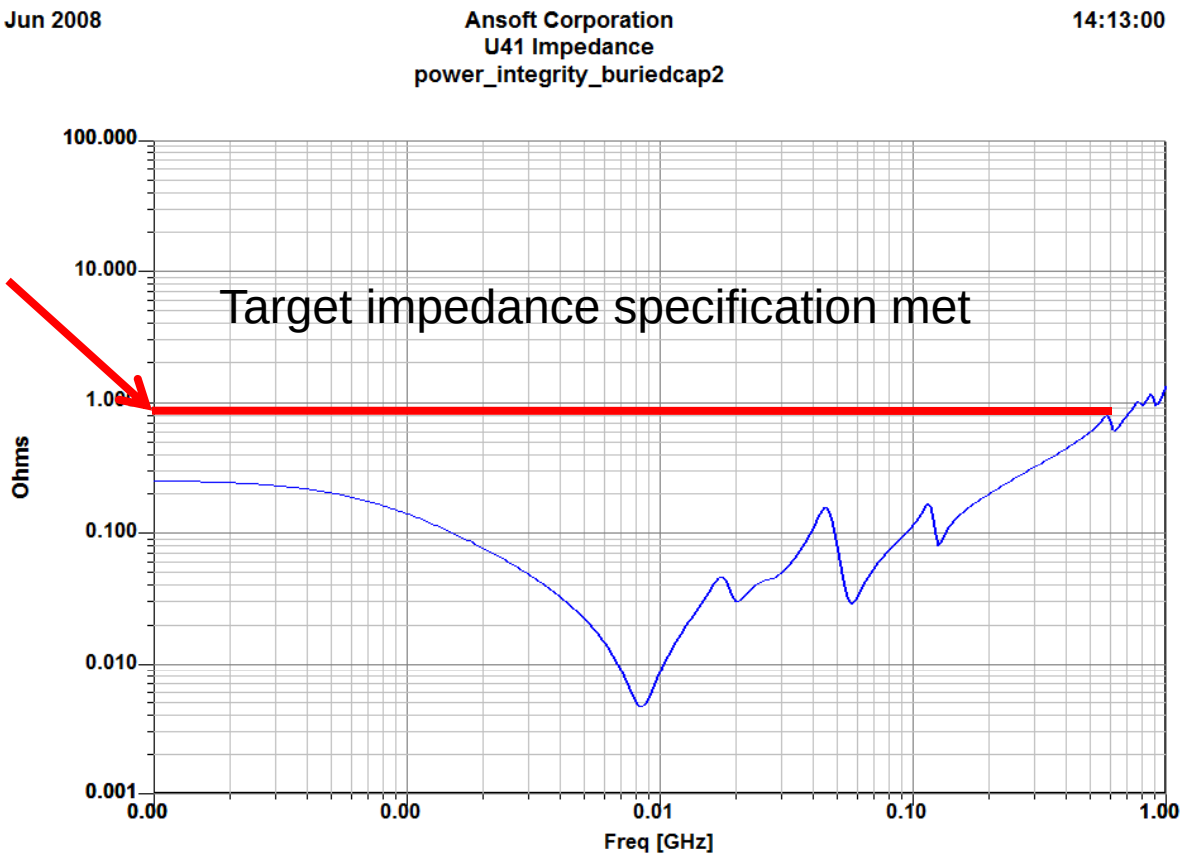
Board w/ HF Caps 3

Board w/ Buried Capacitance

Impedance crosses 800 mOhm @ >667 MHz

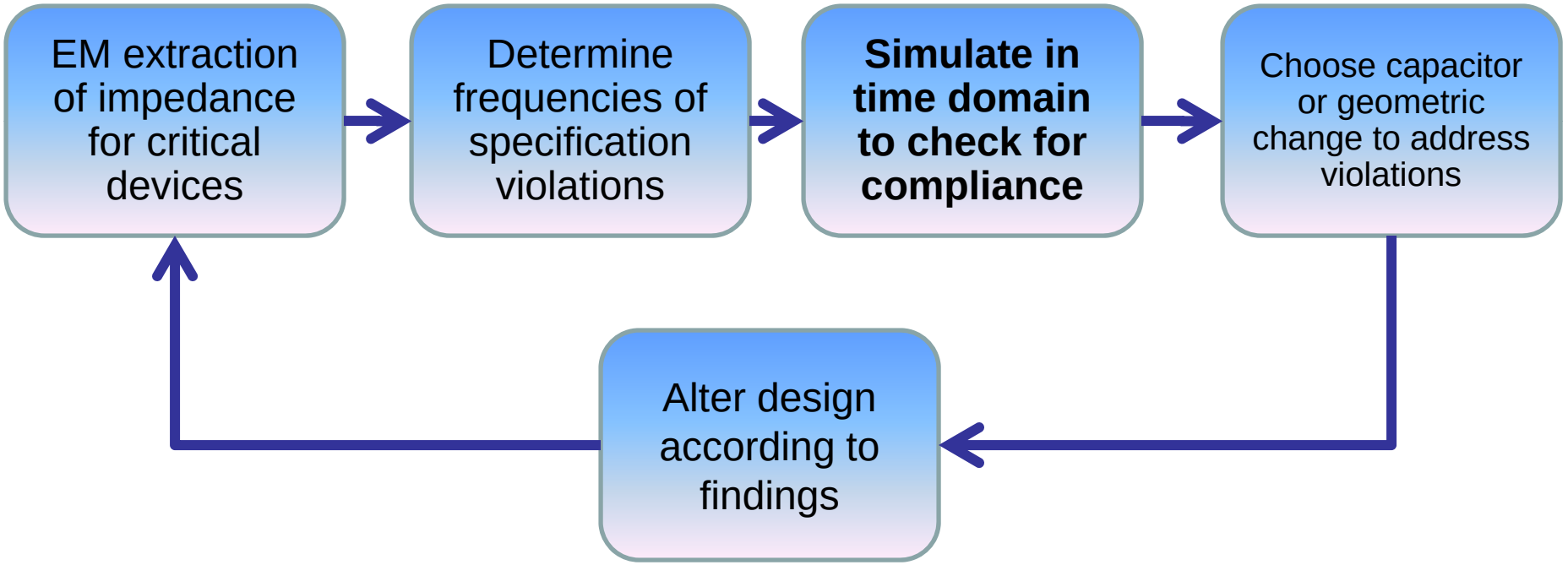
Buried Capacitance

Target impedance 800 mOhm to 667 MHz

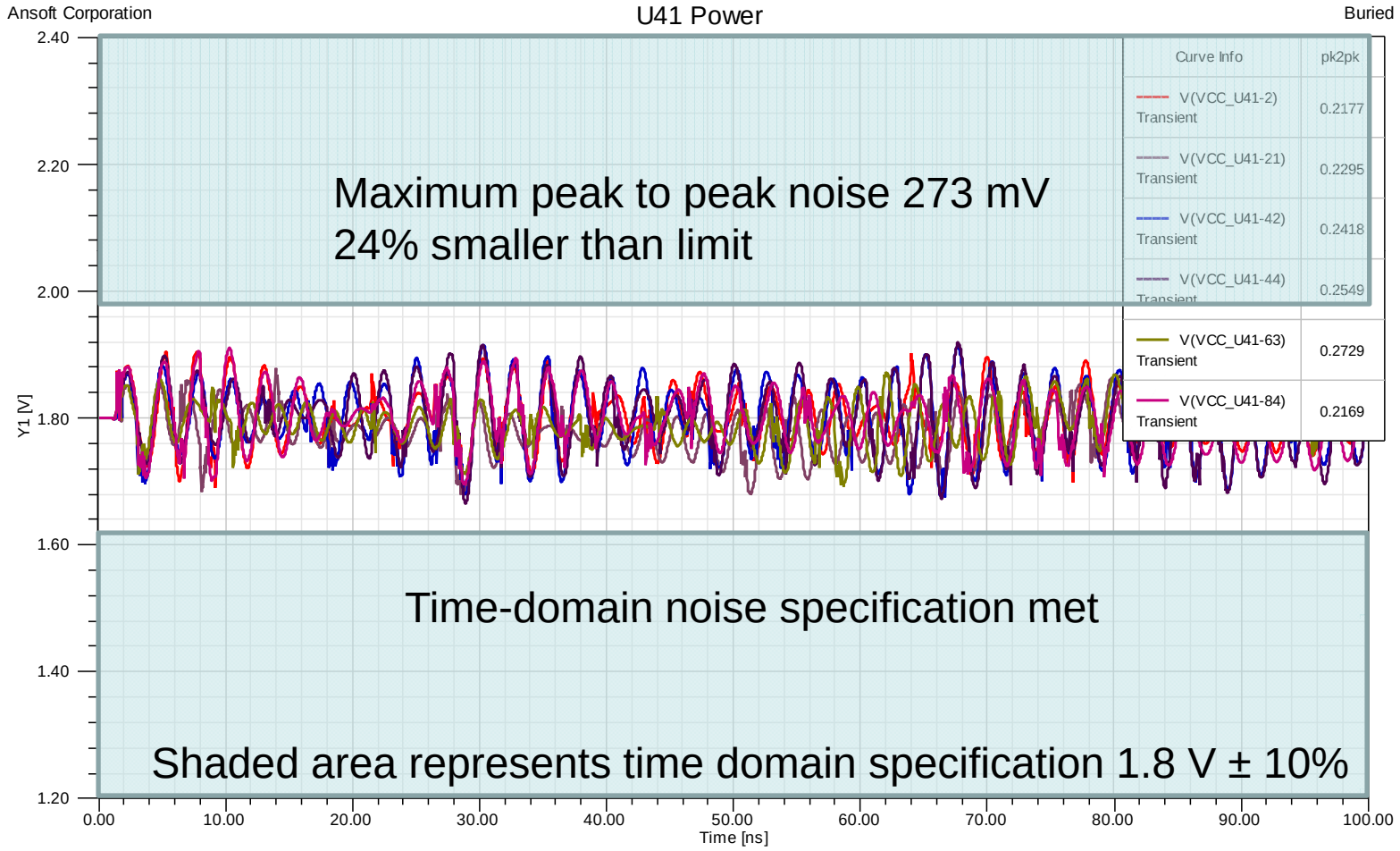


Board w/ Buried Capacitance

PDS Design Flow



Switching Power Noise



Conclusion

- Ansoft software allows PCB engineers to design effective decoupling solutions for their PCBs
- Impedance and resonant mode simulations connect the frequency domain to the spatial domain and allow selection of capacitor value and placement
- *Frequency domain* extractions are useful for quickly optimizing PDS designs, but *time domain* simulations are necessary to ensure compliance with device specs