Power Plane and Decoupling Optimization
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Overview

- Frequency- and time-domain power distribution system specifications
- Decoupling design example
  - Bare board
  - Added capacitors
  - Buried Capacitance
- Conclusion
Frequency Domain PDS Targets

- Excessive impedance seen by a device drawing power from a PDS will cause power voltage to fluctuate.
- On a board, impedance must be below target from DC to several hundred MHz.
- Working in the frequency domain allows quick estimation of power quality.
PDS Components

Mag. of $Z$

$Z_{\text{target}}$

$|Z|$

$f$

1KHz 1MHz 100MHz 1 GHz

Switching Power Supply
Electrolytic Bulk Capacitors
High Frequency Ceramic Capacitors
Power/Ground Planes Buried Capacitance
Time Domain PDS Targets

- S-parameters and impedance are calculated in the frequency domain.
- Device specifications are typically given in the time domain.
- Example: maximum VCC excursion 10% of nominal value
  - 1.8 V VCC has an allowable range of 1.62 V to 1.98 V.
PDS Design Flow

1. EM extraction of impedance for critical devices
2. Determine frequencies of specification violations
3. Simulate in time domain to check for compliance
4. Choose capacitor or geometric change to address violations
5. Alter design according to findings

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EM extraction of impedance for critical devices → Determine frequencies of specification violations → Simulate in time domain to check for compliance → Choose capacitor or geometric change to address violations → Alter design according to findings

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ANSOFT
Board Imported from Layout

Measuring impedance at the six VCC pins on U41
Defining the Target Impedance

To define the target impedance we need to consider two factors:

- Peak current
  - Determines maximum impedance
- Spectral power
  - Determines cutoff frequency
Peak Current

- Peak current 37.87 mA
- Six drivers and 0.18 V maximum voltage swing:

\[
\frac{0.18 \text{ V}}{6(37.87 \text{ mA})} = 800 \text{ m}\Omega
\]
95% of driver power is below 667 MHz

-46.11 dB @ 400 MHz

-51.59 dB @ 83 MHz
PDS Design Flow

- EM extraction of impedance for critical devices
- Determine frequencies of specification violations
- Simulate in time domain to check for compliance
- Choose capacitor or geometric change to address violations
- Alter design according to findings
Bare Board

Target impedance 800 mOhm to 667 MHz
EM extraction of impedance for critical devices

Determine frequencies of specification violations

Simulate in time domain to check for compliance

Choose capacitor or geometric change to address violations

Alter design according to findings
Time Domain Schematic

Driver

VRM

800 Mbps data rate

DDR2 IBIS driver into ideal termination used as load for PDS

Package decoupling modeled using a capacitor with ESR, ESL
Switching Power Noise

Shaded area represents time domain specification 1.8 V ± 10%
Spectral Analysis

11-12 ns period corresponds to frequency of 80-90 MHz

This is confirmed by the spectral plot and correlates with the ideal driver simulation shown earlier (peak @ 83 MHz)
PDS Design Flow

1. EM extraction of impedance for critical devices
2. Determine frequencies of specification violations
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4. Choose capacitor or geometric change to address violations
5. Alter design according to findings
Adding Bulk Capacitors

Added two 47 uF capacitors as specified by VRM manufacturer.
PDS Design Flow

1. EM extraction of impedance for critical devices
2. Determine frequencies of specification violations
3. Simulate in time domain to check for compliance
4. Choose capacitor or geometric change to address violations

Alter design according to findings
Bare Board vs. Bulk Capacitors

Resonance @ 50 MHz

Target impedance 800 mOhm to 667 MHz
Bulk Capacitors

Target impedance 800 mOhm to 667 MHz

Resonance @ 50 MHz
PDS Design Flow

- EM extraction of impedance for critical devices
- Determine frequencies of specification violations
- Simulate in time domain to check for compliance
- Choose capacitor or geometric change to address violations

Alter design according to findings
Switching Power Noise

~11-12 ns period

Shaded area represents time domain specification 1.8 V ± 10%
Spectral Analysis

~11-12 ns period

Same 11-12 ns period as exhibited by bare board

Note that resonance @ 50 MHz is not excited due as indicated by low spectral content at that frequency

-13.96 dB @ 90 MHz
-37.18 dB @ 50 MHz
Resonance at 50 MHz
EM extraction
of impedance
for critical
devices

Determine
frequencies of
specification
violations

Simulate in
time domain to
check for
compliance

Choose capacitor
or geometric
change to address
violations

Alter design
according to
findings
Choosing a Capacitor

- To reduce the effect of a resonance, choose a capacitor with a low impedance at the resonant frequency.
Added HF Capacitors

- 52 20 nF capacitors were added across the board to reduce high-frequency impedance and to cancel resonance at 50 MHz
PDS Design Flow

1. EM extraction of impedance for critical devices
2. Determine frequencies of specification violations
3. Simulate in time domain to check for compliance
4. Choose capacitor or geometric change to address violations

Alter design according to findings
Bulk vs. HF Capacitors 1

Target impedance 800 mOhm to 667 MHz

No Resonance @ 50 MHz
HF Capacitors 1

Target impedance 800 mOhm to 667 MHz

Exceeds 800 mOhm @ 200 MHz

No resonance @ 50 MHz

Board w/ HF Caps 1
PDS Design Flow

EM extraction of impedance for critical devices

Determine frequencies of specification violations

Simulate in time domain to check for compliance

Choose capacitor or geometric change to address violations

Alter design according to findings
Switching Power Noise

Shaded area represents time domain specification 1.8 V ± 10%
EM extraction of impedance for critical devices

Determine frequencies of specification violations

Simulate in time domain to check for compliance

Choose capacitor or geometric change to address violations

Alter design according to findings
Extending Low Impedance

- 10 1.2 nF capacitors were added across the board to extend minimum high-frequency impedance
- 1.2 nF capacitor was chosen due to low impedance at 200 MHz
- 4 of these were located near U41
PDS Design Flow

1. EM extraction of impedance for critical devices
2. Determine frequencies of specification violations
3. Simulate in time domain to check for compliance
4. Choose capacitor or geometric change to address violations
5. Alter design according to findings
HF 1 vs. HF 2

Target impedance 800 mOhm to 667 MHz

New resonance @ 80 MHz

Impedance exceeds 800 mOhm @ 350 MHz
Target impedance 800 mOhm to 667 MHz

New resonance @ 80 MHz

Impedance exceeds 800 mOhm @ 350 MHz
PDS Design Flow

EM extraction of impedance for critical devices

Determine frequencies of specification violations

Simulate in time domain to check for compliance

Choose capacitor or geometric change to address violations

Alter design according to findings
Switching Power Noise

Shaded area represents time domain specification 1.8 V ± 10%
Resonance at 80 MHz
PDS Design Flow

EM extraction of impedance for critical devices

Determine frequencies of specification violations

Simulate in time domain to check for compliance

Choose capacitor or geometric change to address violations

Alter design according to findings
Removing a Resonance

- Six 8 nF capacitors were added near U41 to cancel resonance at 80 MHz
Choosing a Capacitor

- To reduce the effect of a resonance, choose a capacitor with a low impedance at the resonant frequency.
PDS Design Flow

1. EM extraction of impedance for critical devices
2. Determine frequencies of specification violations
3. Simulate in time domain to check for compliance
4. Choose capacitor or geometric change to address violations
5. Alter design according to findings
HF 2 vs. HF 3

Target impedance 800 mOhm to 667 MHz

Board w/ HF Caps 2

Board w/ HF Caps 3

Impedance crosses 800 mOhm @ 500 MHz

No resonance @ 80 MHz
HF 3

Target impedance 800 mOhm to 667 MHz

Board w/ HF Caps 3
PDS Design Flow

1. EM extraction of impedance for critical devices
2. Determine frequencies of specification violations
3. Simulate in time domain to check for compliance
4. Choose capacitor or geometric change to address violations
5. Alter design according to findings

The flowchart illustrates the design process, starting with EM extraction and progressing through the steps of determining frequencies, simulating in the time domain, choosing components, and finally altering the design based on findings.
Switching Power Noise

Maximum peak to peak noise of 371 mV

Shaded area represents time domain specification 1.8 V ± 10%
PDS Design Flow

1. EM extraction of impedance for critical devices
2. Determine frequencies of specification violations
3. Simulate in time domain to check for compliance
4. Choose capacitor or geometric change to address violations
5. Alter design according to findings
Buried Capacitance

- Due to parasitic inductance it will be impossible to further decouple the board with capacitors.
- Using a thinner dielectric layer between power and ground planes introduces additional capacitance and reduces high frequency impedance.

Capacitance of parallel plates:

\[ C = \varepsilon \frac{A}{d} \]
PDS Design Flow

1. EM extraction of impedance for critical devices
2. Determine frequencies of specification violations
3. Simulate in time domain to check for compliance
4. Choose capacitor or geometric change to address violations
5. Alter design according to findings
HF 3 vs. Buried Capacitance

Target impedance 800 mOhm to 667 MHz

Impedance crosses 800 mOhm @ >667 MHz
Buried Capacitance

Target impedance specification met

Board w/ Buried Capacitance

Target impedance 800 mOhm to 667 MHz
PDS Design Flow

- EM extraction of impedance for critical devices
- Determine frequencies of specification violations
- Simulate in time domain to check for compliance
- Choose capacitor or geometric change to address violations
- Alter design according to findings
Switching Power Noise

Maximum peak to peak noise 273 mV
24% smaller than limit

Time-domain noise specification met

Shaded area represents time domain specification 1.8 V ± 10%
Conclusion

- Ansoft software allows PCB engineers to design effective decoupling solutions for their PCBs
- Impedance and resonant mode simulations connect the frequency domain to the spatial domain and allow selection of capacitor value and placement
- *Frequency domain* extractions are useful for quickly optimizing PDS designs, but *time domain* simulations are necessary to ensure compliance with device specs