SIwave 5.0 PI Advisor for Optimized DDR3 Memory Design

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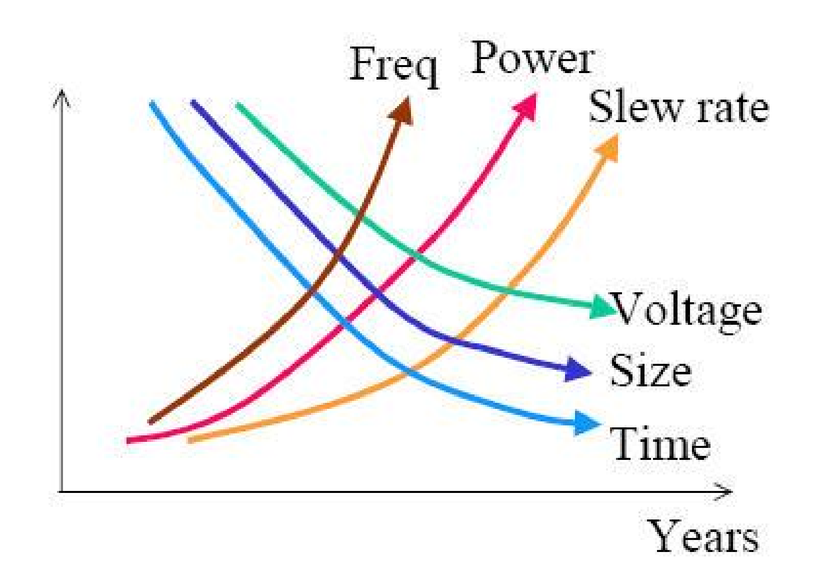
Agenda

- Design Overview and Challenges
- How to define Target impedance ?
- PI Advisor
- Summary

Design Challenges

- **New deep sub-micron technologies**
  - Increased device speeds
  - Lower power supply voltages
- **Device miniaturization**
  - Decreasing design cycles
- **Delta-I noise on whole PDS system**

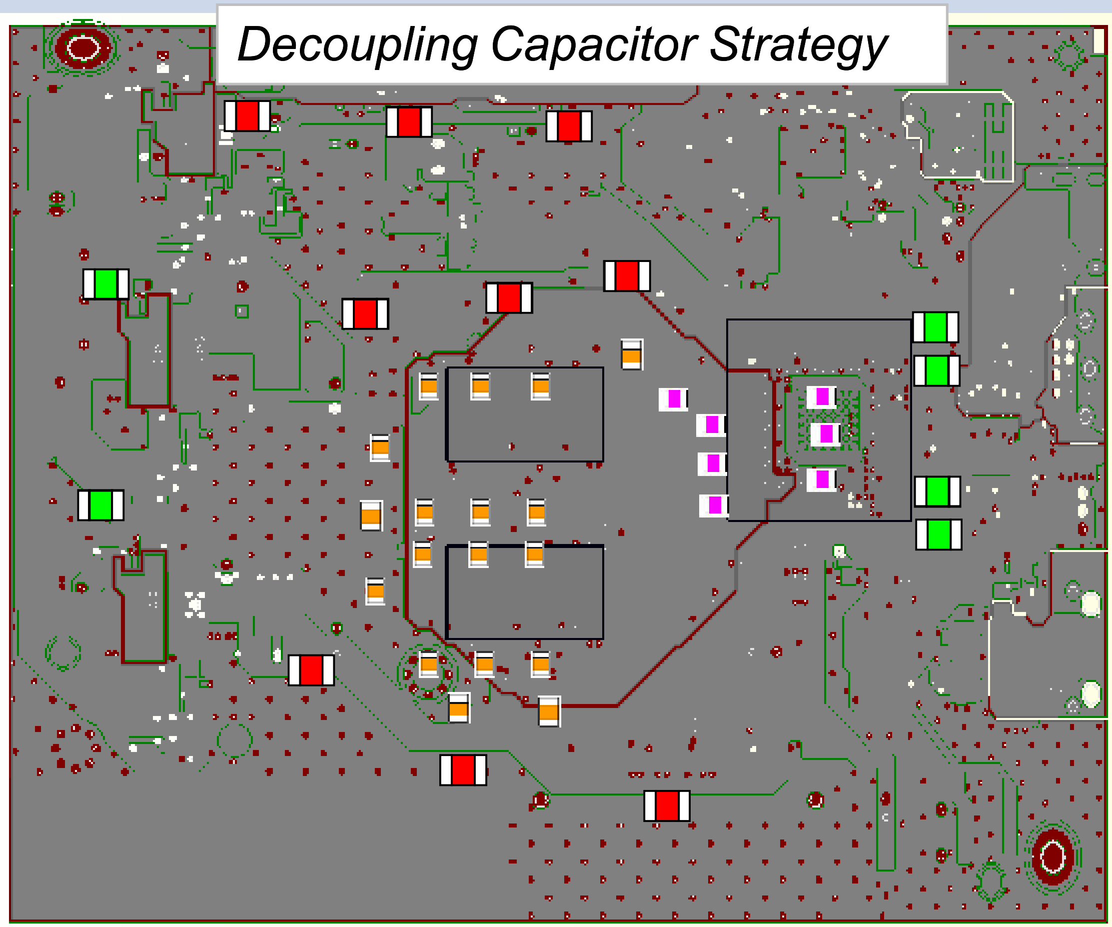


A Typical Scenario

- *Customer X* has a PCB with possible SI/PI related issues
- Management is asking for quick fix and cost reduction
- The Challenge: How to achieve target impedances without compromising SI/PI performance?

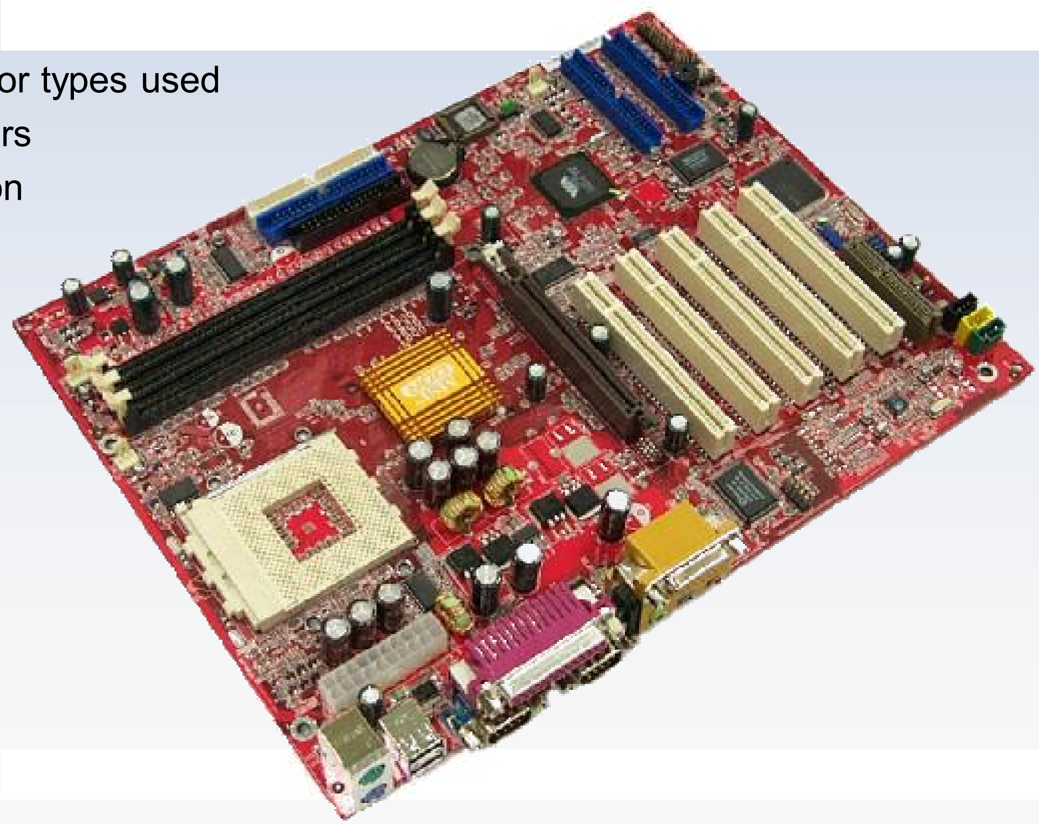
High Volume Production

Decoupling Capacitor Strategy



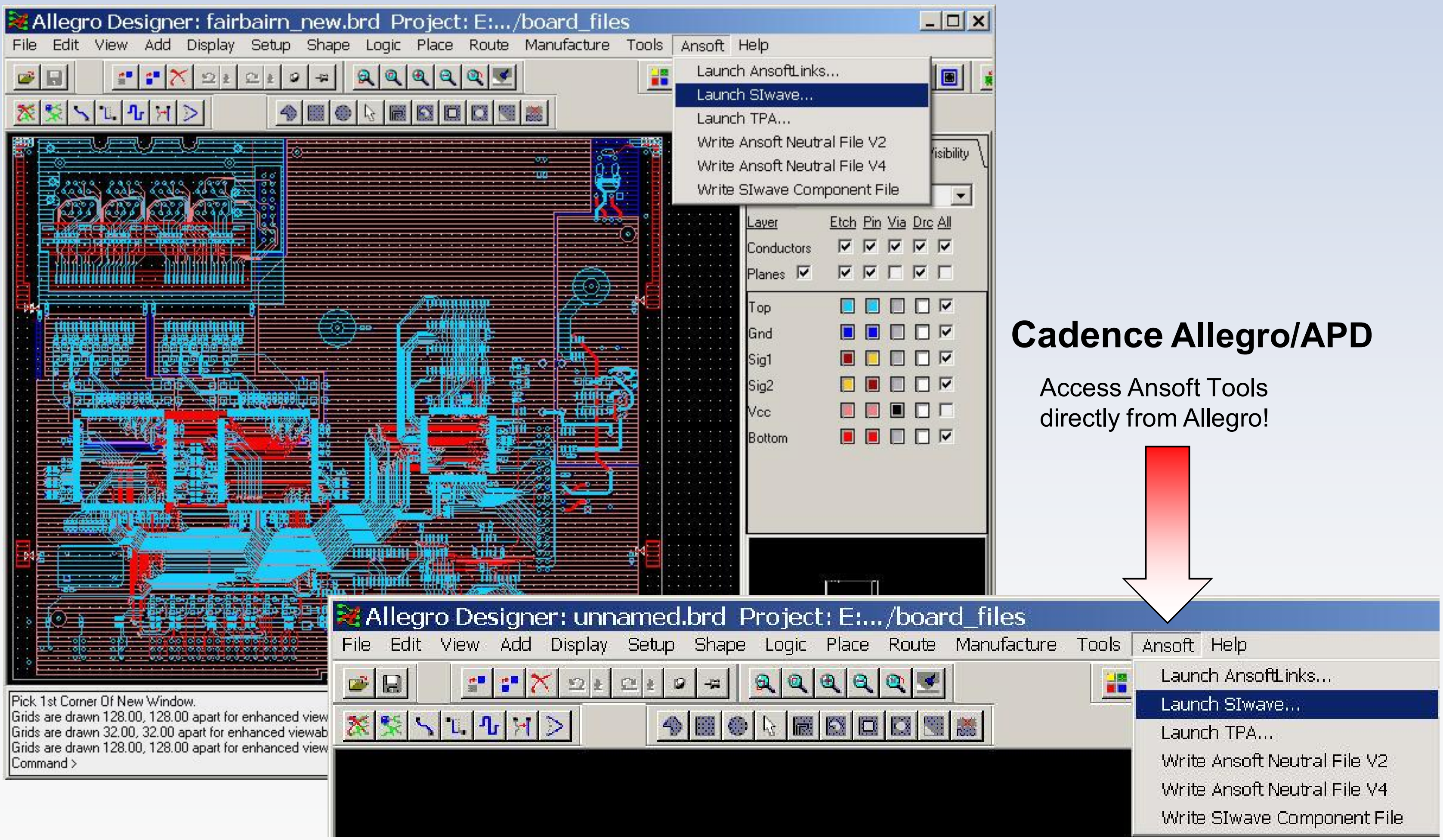
Power Integrity Design

- **PCB Geometry present**
  - A functional design, with all decoupling capacitors already placed on PCB
  - PI Engineer may want to:
    - Increase capacitor count in order to make design more robust (i.e. overclocking, etc.)
    - Reduce the capacitor count
    - Reduce number of different capacitor types used
    - Redesign using lower cost capacitors
    - Chose appropriate capacitor location



Layout Import and Translation

- **Direct access to Ansoft tools from Cadence environment**
  - Allegro layout is directly translated and imported in SIwave
  - Component file is also imported



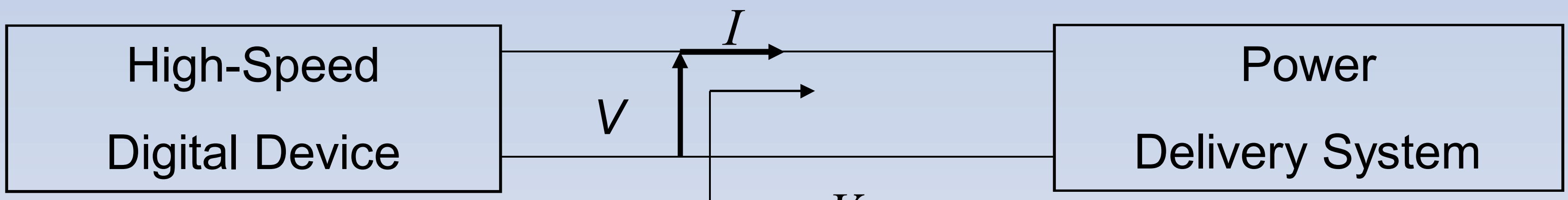
Cadence Allegro/APD

Access Ansoft Tools directly from Allegro!

ECAD Databases Supported

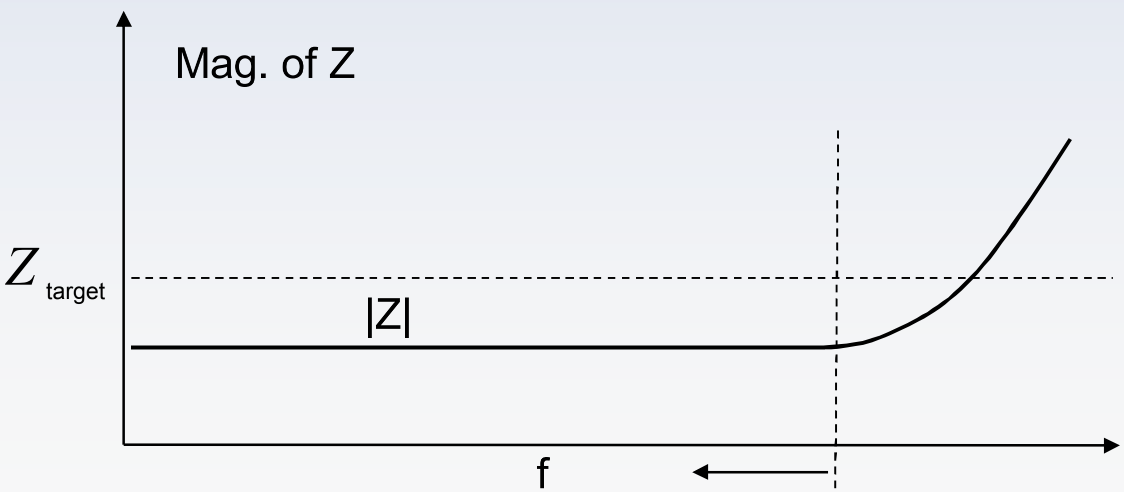
1.	Cadence Allegro and APD	15.0, 15.1, 15.2, 15.5.x, 15.7, 16.0, 16.1, 16.2, and 16.3
2.	Cadence SiP Digital/RF	15.7, 16.0, 16.1, 16.2, and 16.3
3.	Mentor BoardStation	8.x
4.	Mentor BoardStation XE/RE	v2007.1 and v2007.2
5.	Mentor Expedition	v2004, v2005, v2007.1, v2007.2 and v2007.3
6.	Mentor PADS (PowerPCB)	v5.2a, v2005 (2007 with 2005 export format)
7.	Synopsys Encore ICPD	2001.x, 2002.x, 2003.x, 2004.x and 2005.x
8.	Sigrity UPD	9.0 and lower
9.	Zuken CR5000	10.x and lower
10.	Altium Designer	Summer 2010 Beta2 or later

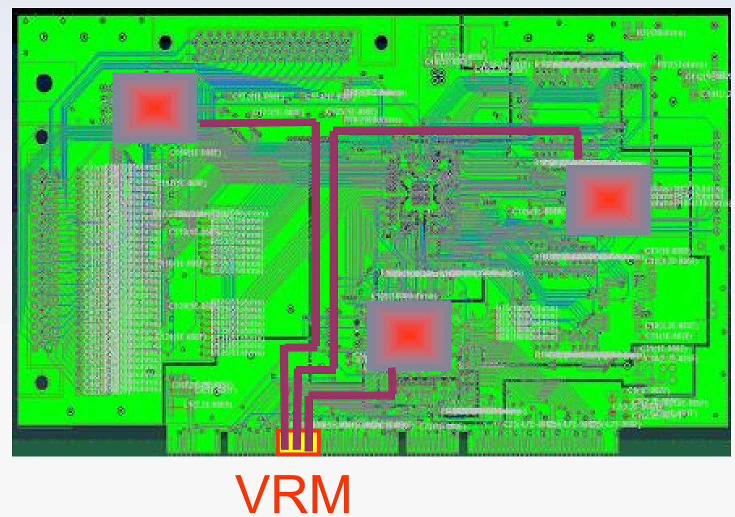
PI Design Goal : Target Impedance of PDS



$$Z = \frac{V}{I}$$

The Impedance looking into PDS at the device should be kept low over a broad frequency range (from DC to several harmonics of clock frequency).





Target Impedance Trends

$$Z_{\text{Target}} = \frac{(Power\_Supply\_Voltage) \times (Allowed\_Ripple)}{Current}$$

$$Z_{\text{Target(2.5v)}} = \frac{(2.5V) \times (5\%)}{40.3A} = 3.1m\Omega$$

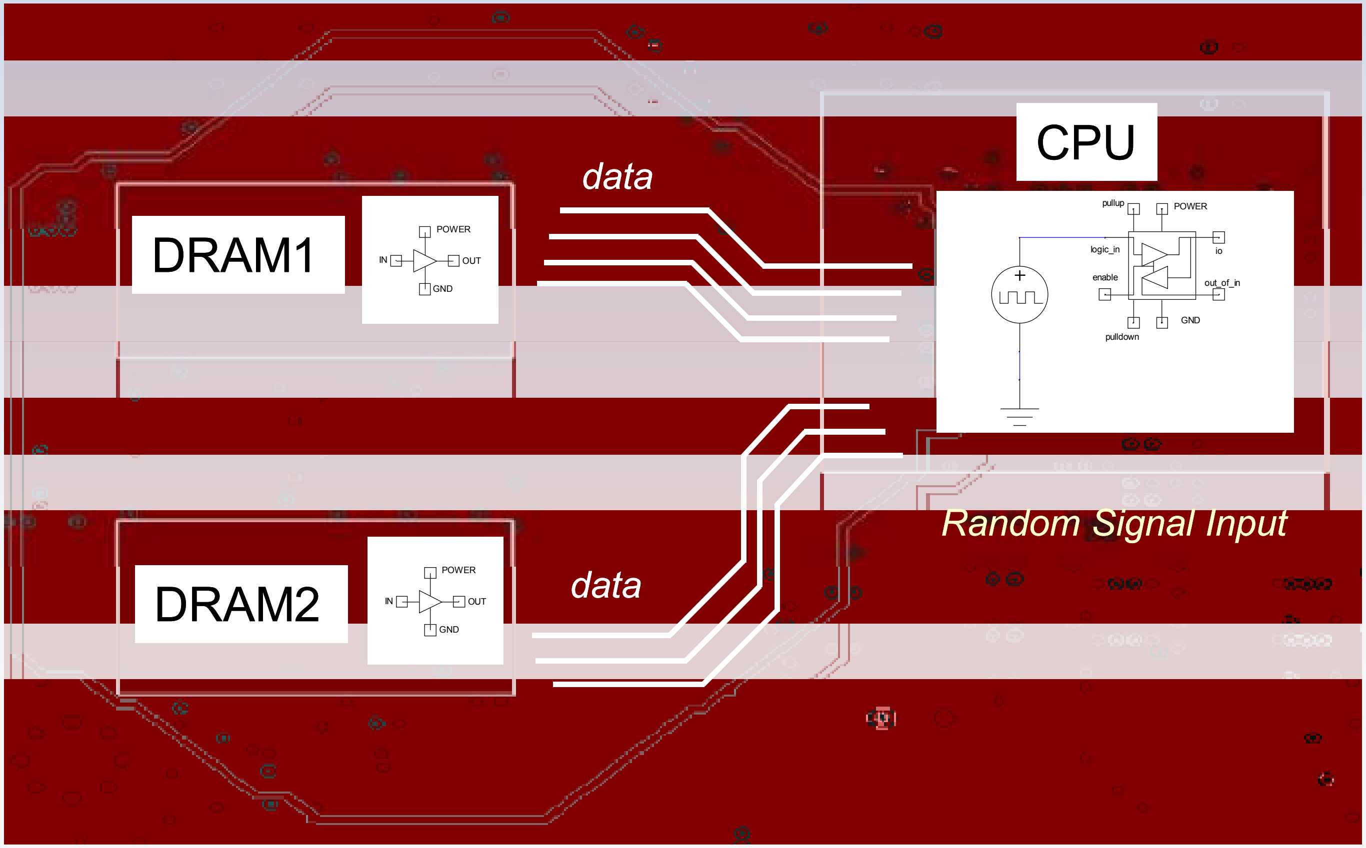
- *Target Impedance is falling ~ 1.6x, every 3 years

Year of first production	1997	1999	2002	2005	2008
Chip technology	0.25um	0.18um	0.13um	0.10um	0.07um
Across Chip Frequency (MHz)	450	600	800	1000	1100
Max. Chip Power (W)	100	120	140	160	180
Max current (A)	40.3	66.7	93.3	133.3	180.0
Power Supply (V)	2.5	1.8	1.5	1.2	0.9
Target Impedance (mΩ)	3.1	1.3	0.8	0.45	0.25

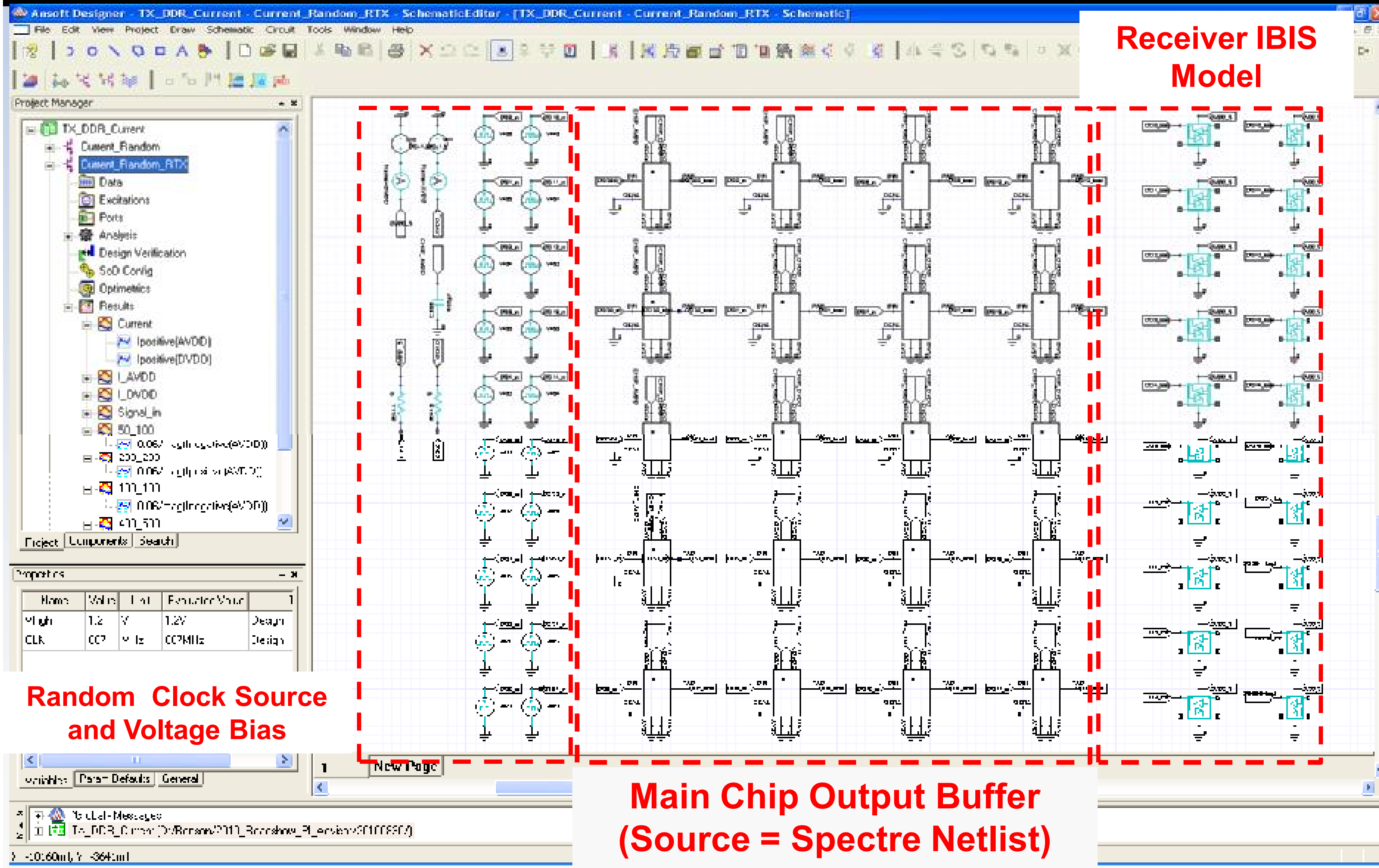
*Source: International Technology Roadmap for Semiconductors

Define Target Impedance

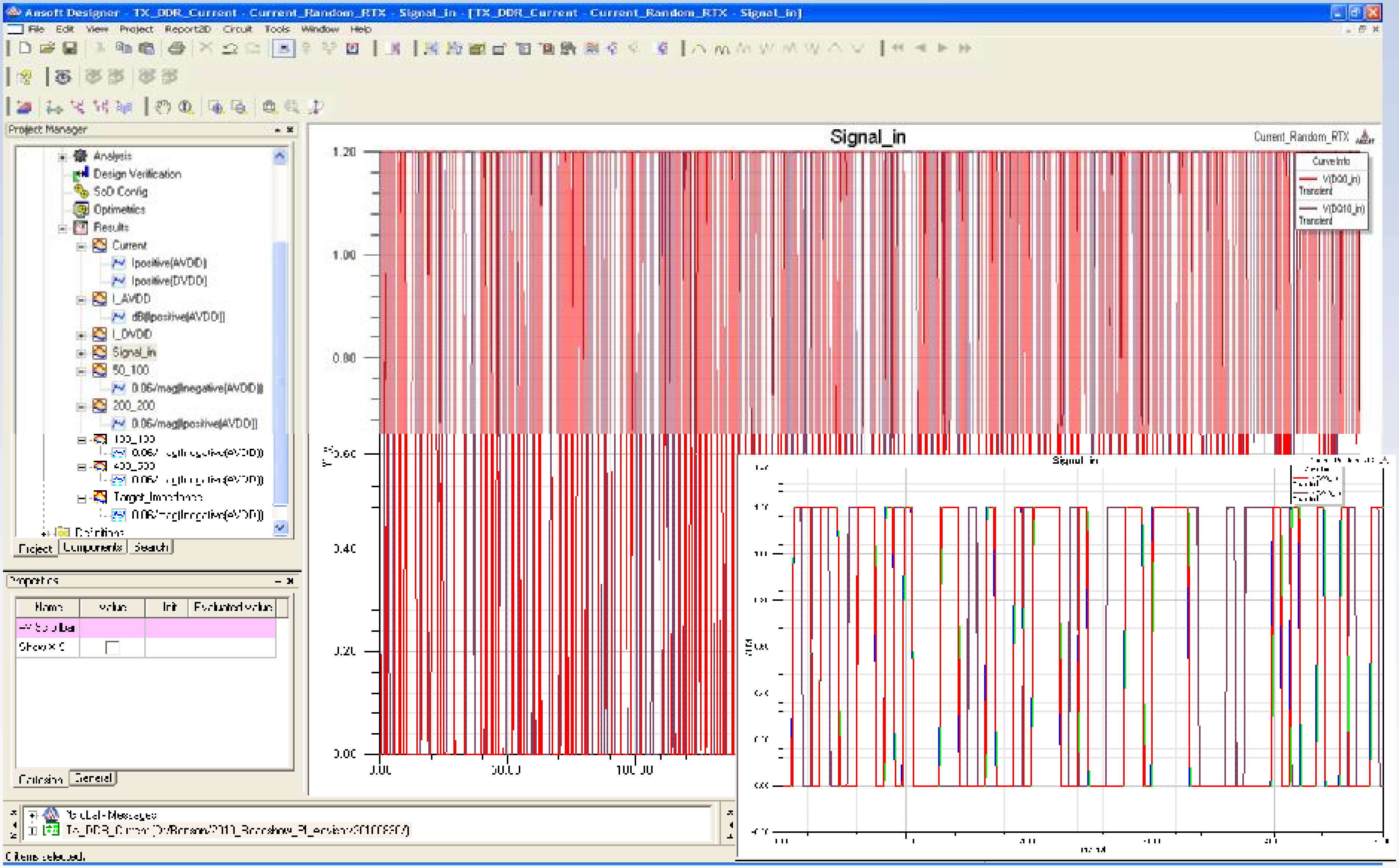
- Target Impedance
  - Get TX/Rx models for DRAM and CPU modules
  - Use Random Signal Input from CPU
  - Get time/frequency domain current profile



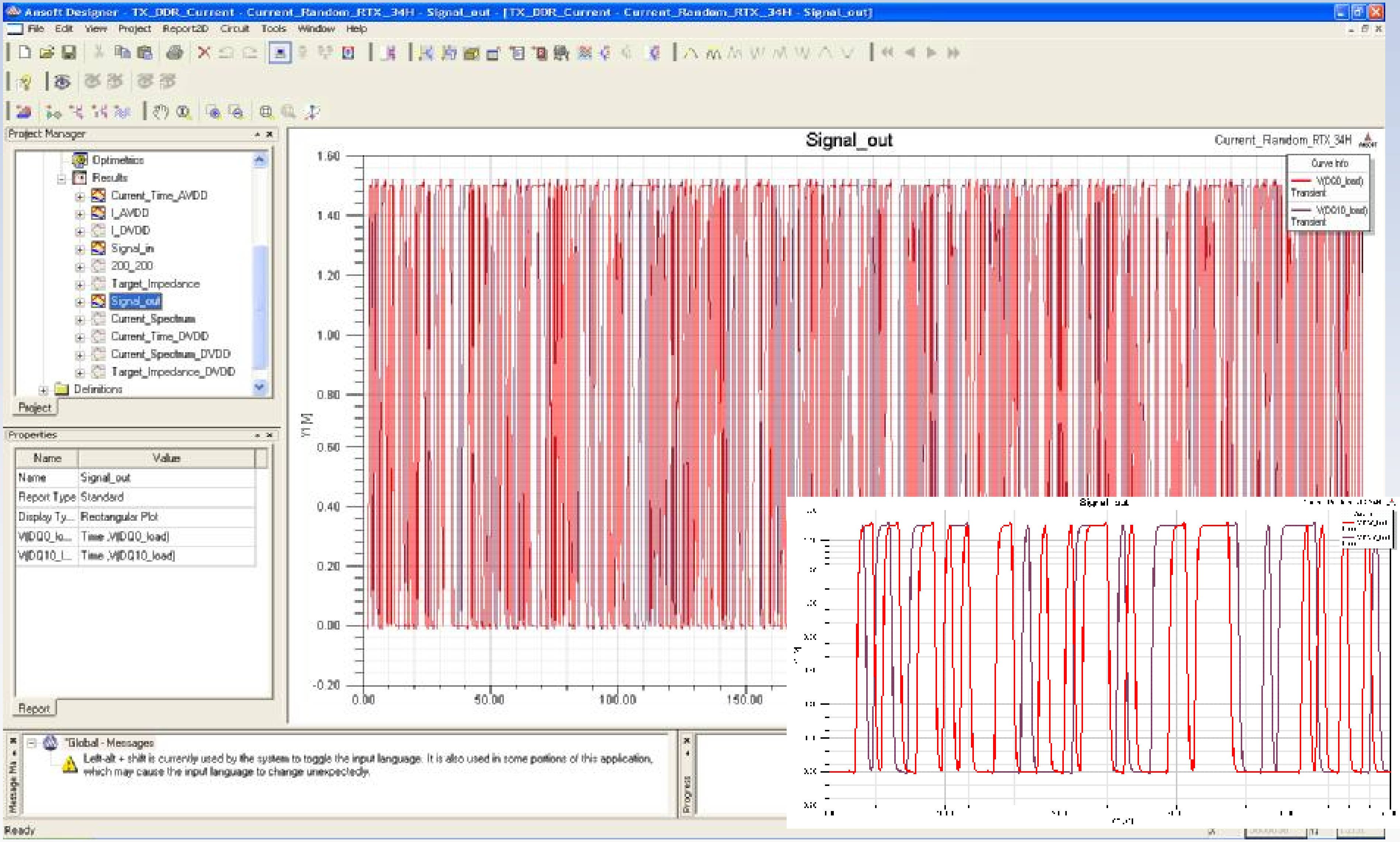
Simulation Schematic



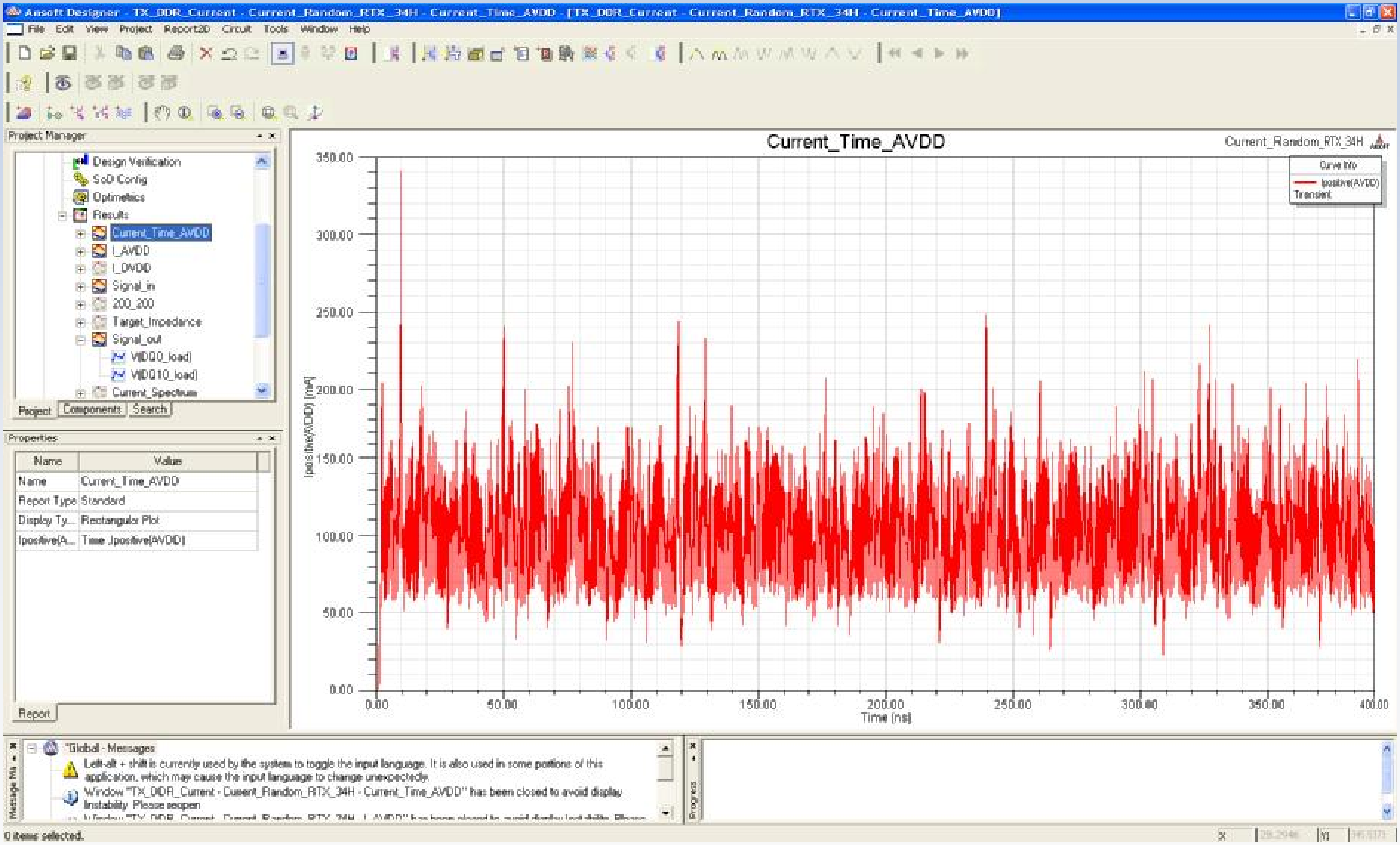
Signal Input – Random Clock



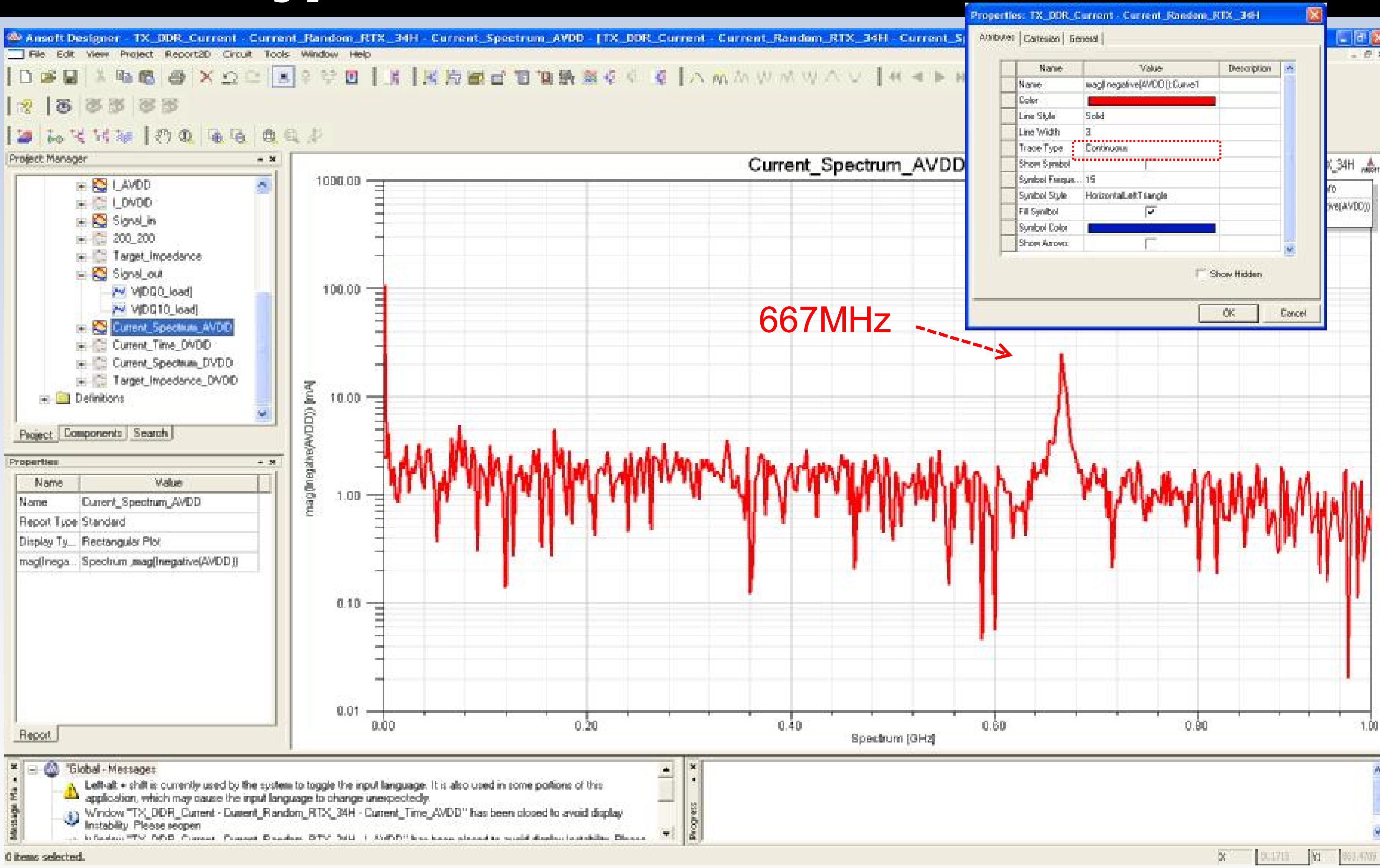
Signal Output



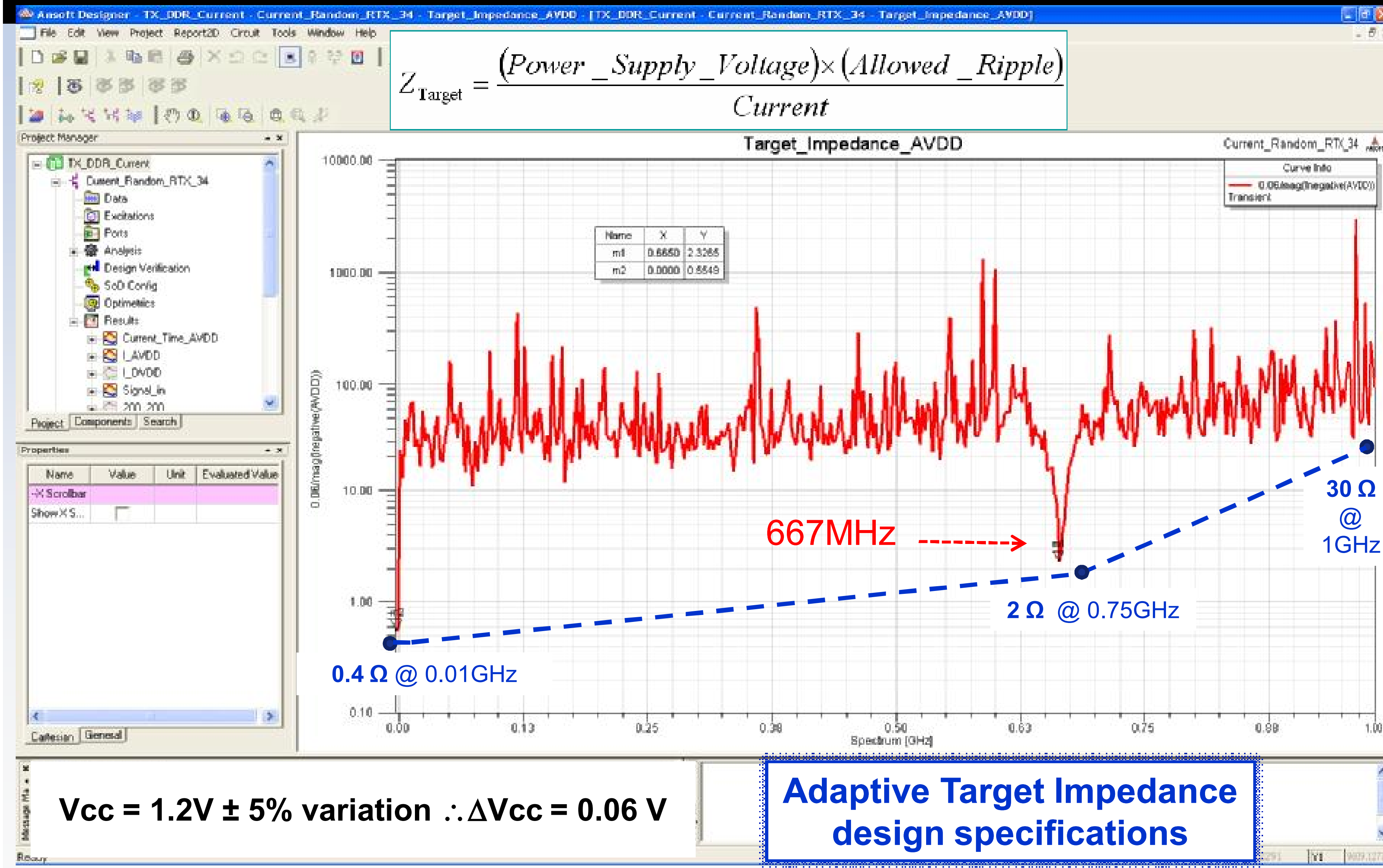
Simulation Results – Time domain Current Profile



Current Spectrum output Trace type - Continuous



Adaptive Target Impedance



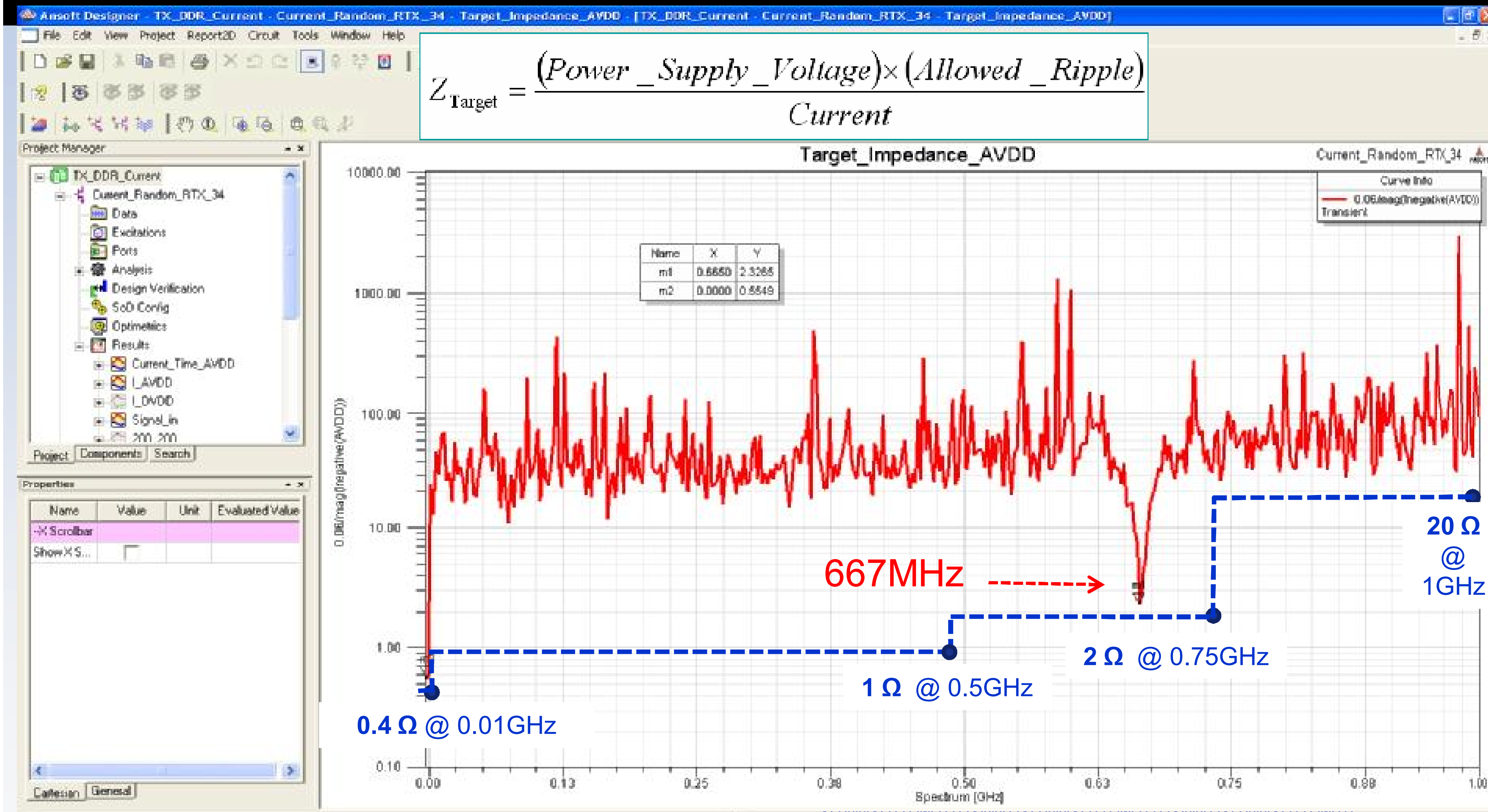
$$Z_{Target} = \frac{(Power\_Supply\_Voltage) \times (Allowed\_Ripple)}{Current}$$

Vcc = 1.2V ± 5% variation ∴ ΔVcc = 0.06 V

Adaptive Target Impedance design specifications

Or .... Adaptive Target Impedance

$$Z_{Target} = \frac{(Power\_Supply\_Voltage) \times (Allowed\_Ripple)}{Current}$$



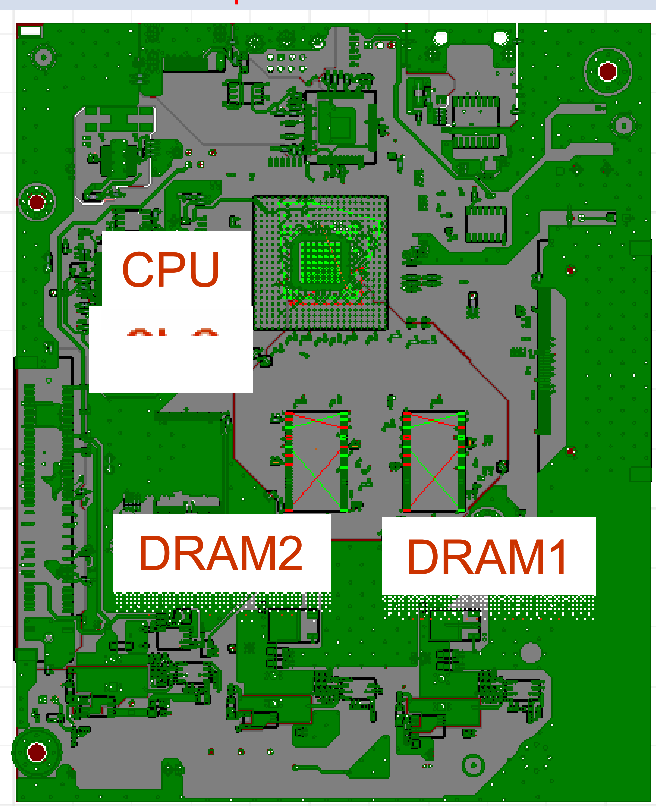
Vcc = 1.2V ± 5% variation ∴ΔVcc = 0.06 V

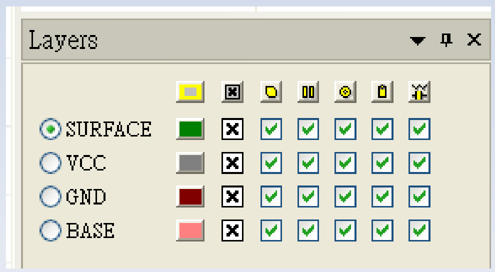
Adaptive Target Impedance design specifications

PCB Layer Structure

- High-speed signals are routed between CPU and DRAM
  - Minimize noise voltage distribution on the VCC/GND plane pair
    - Design of this Power/Ground plane is the most important aspect of design
  - Low power bus impedance over frequency

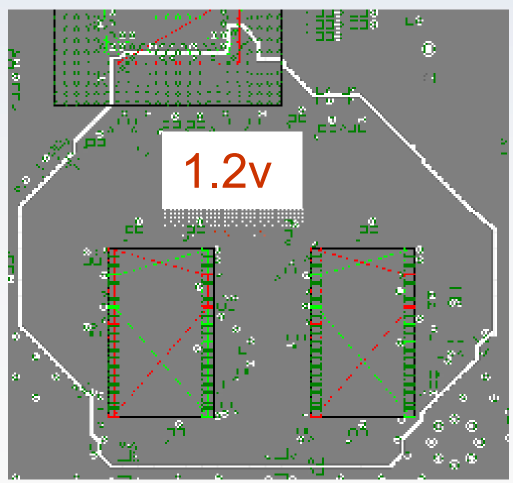
3 ports defined



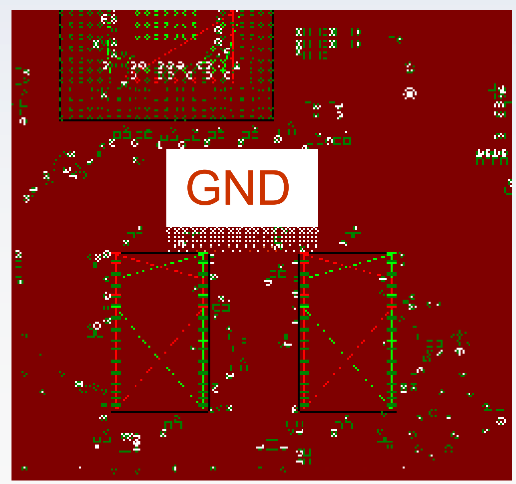


4 Layer PCB
Board Size : 5.3'' x 6.5''
(13.5cm x 16.5cm)

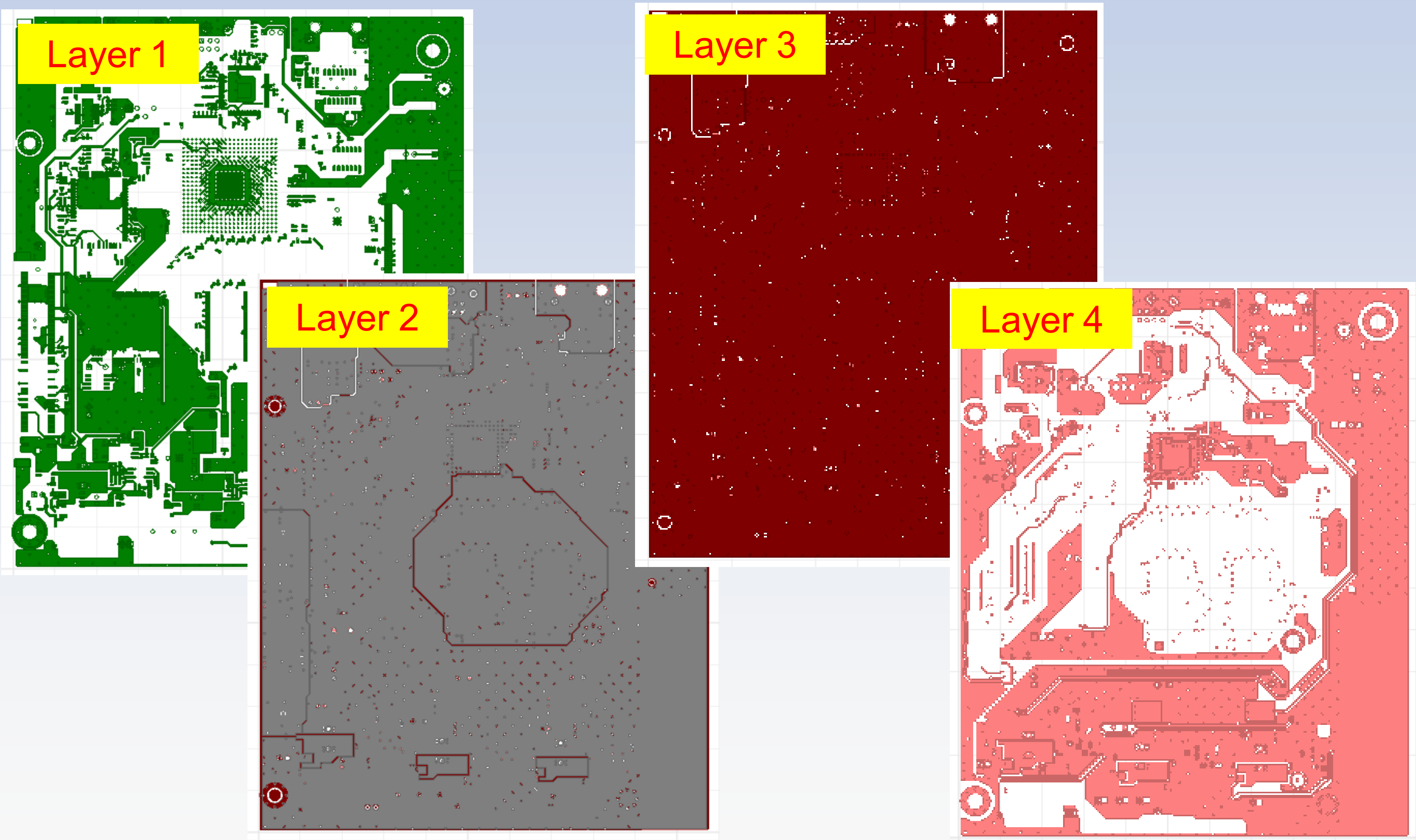
Power Plane



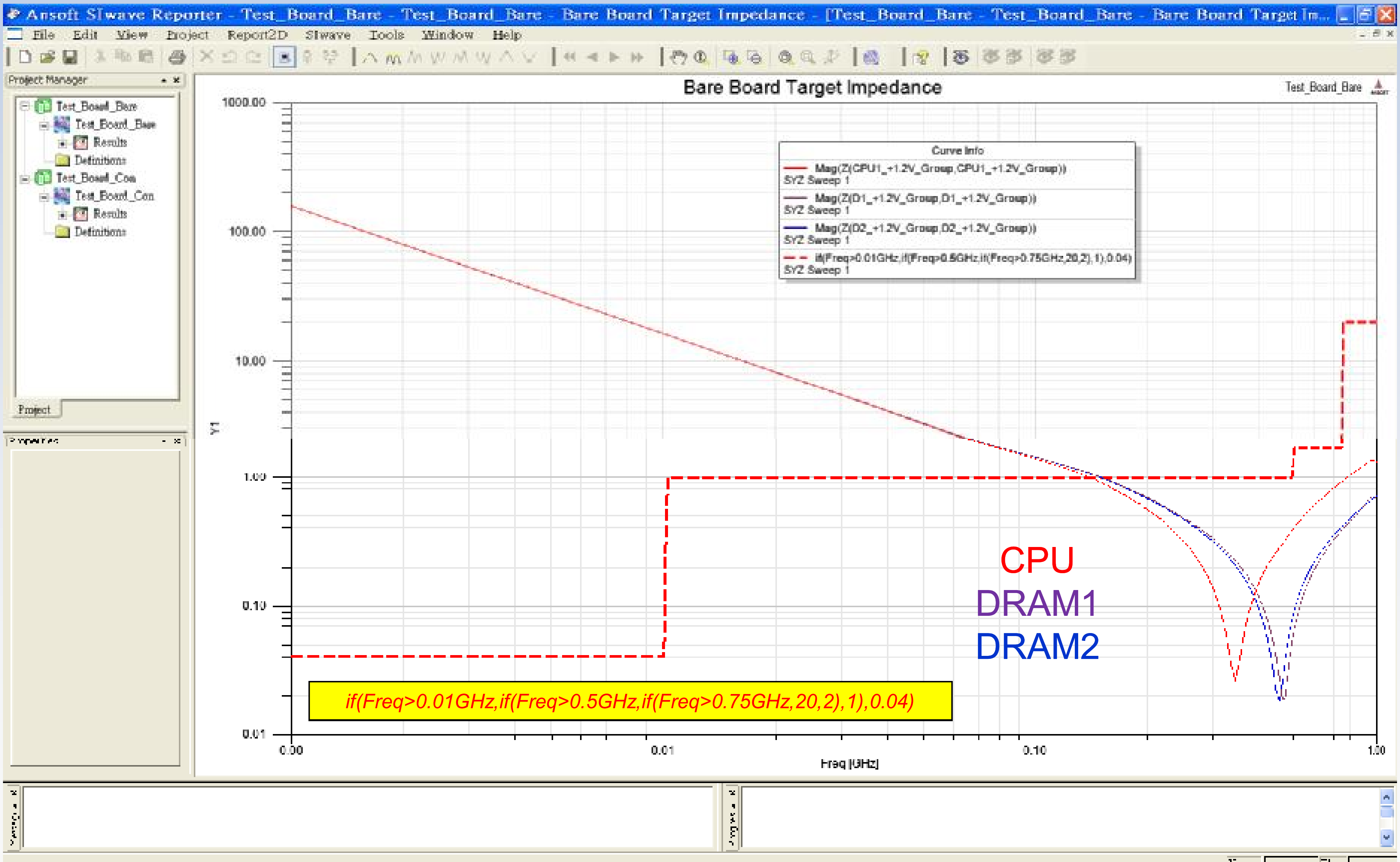
Ground Plane



PCB Layer Structure



Bare Board Impedance

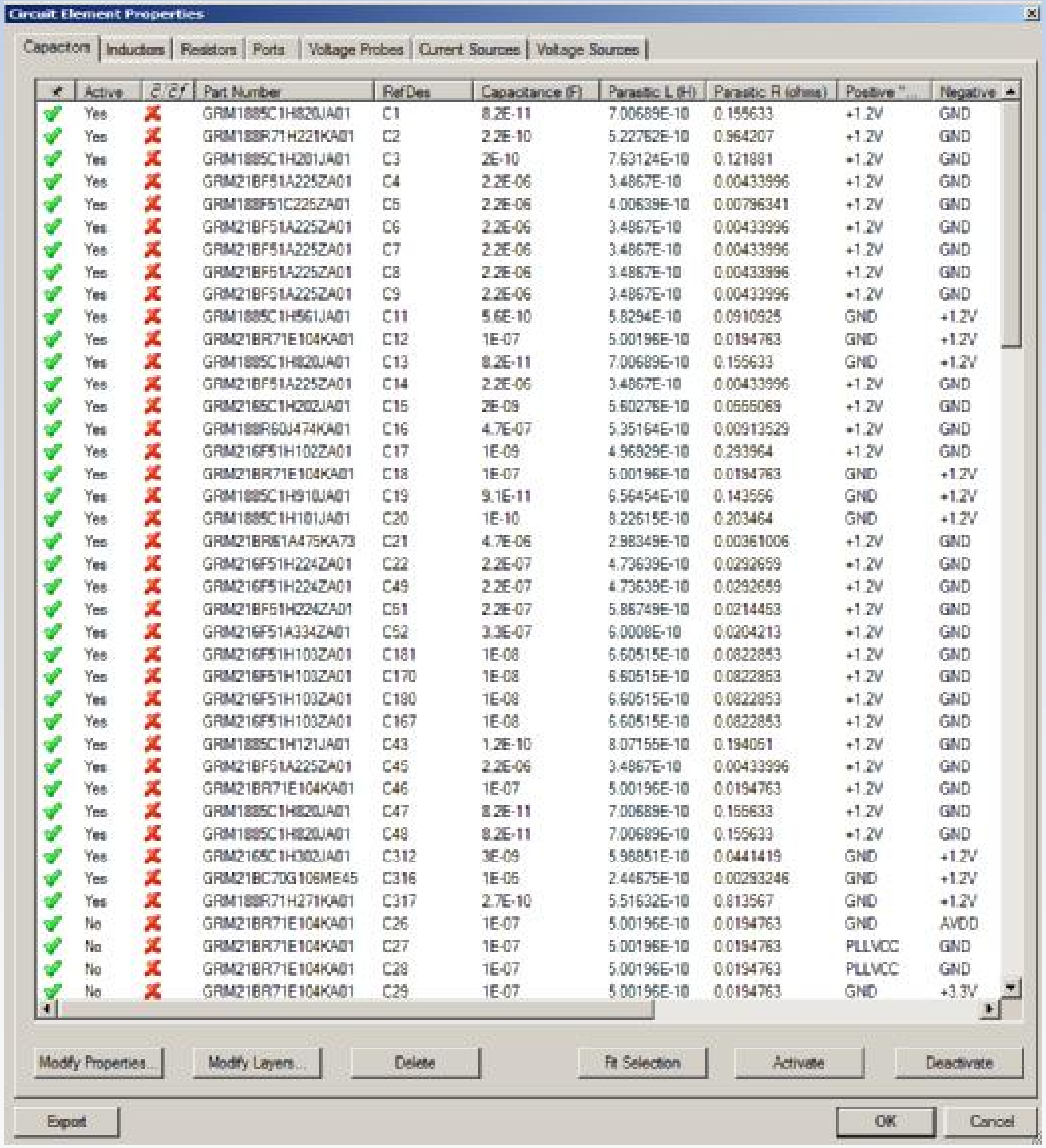


Original Design
All 1.2V to GND 36 Capacitors ON

Original Design - Total 36 Caps

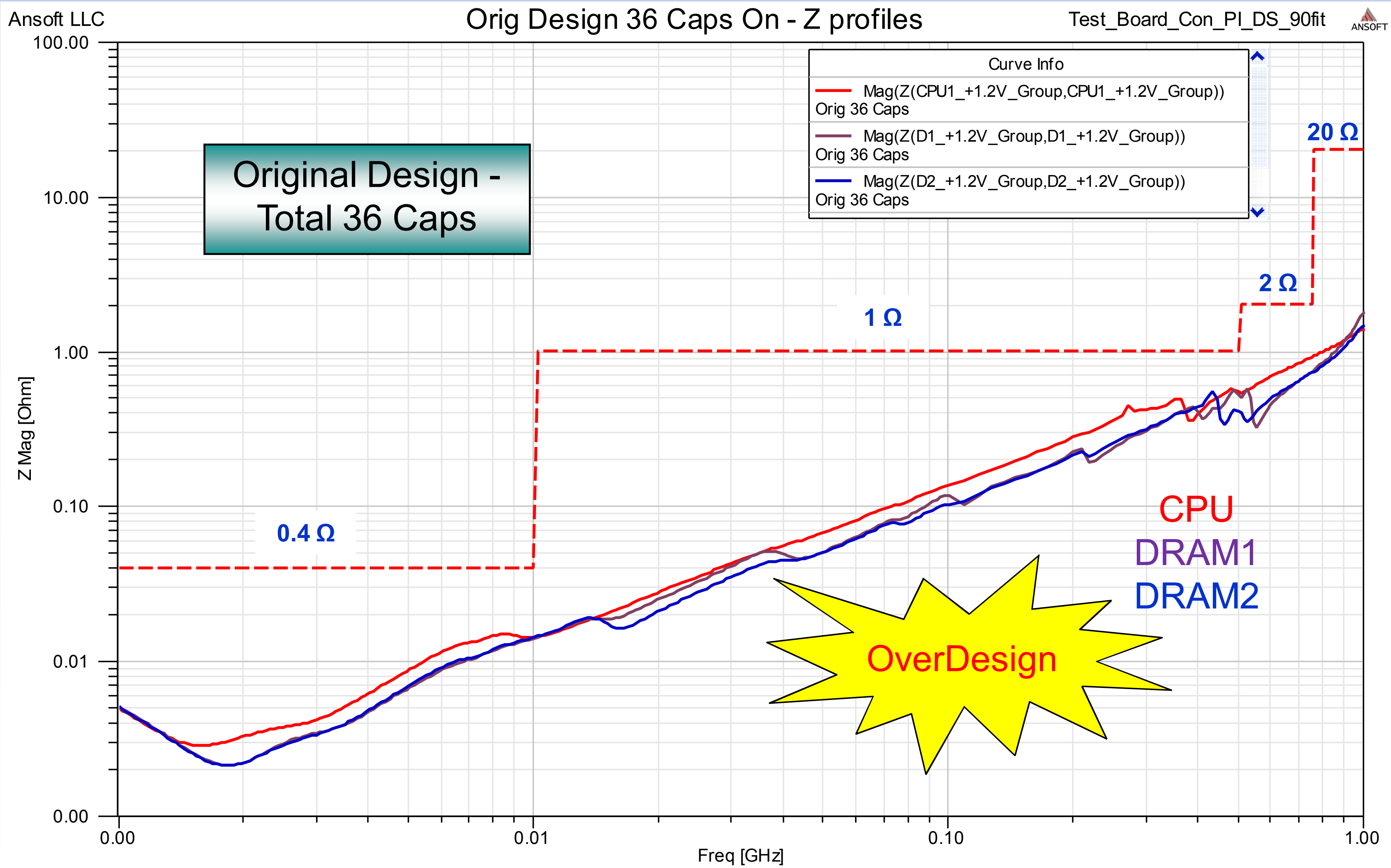
Types of Capacitors

GRM21BC70G106ME45
GRM21BF51A225ZA01
GRM21BF51H224ZA01
GRM21BR71E104KA01
GRM216F51H103ZA01
GRM216F51H224ZA01
GRM1885C1H201JA01
GRM1885C1H820JA01

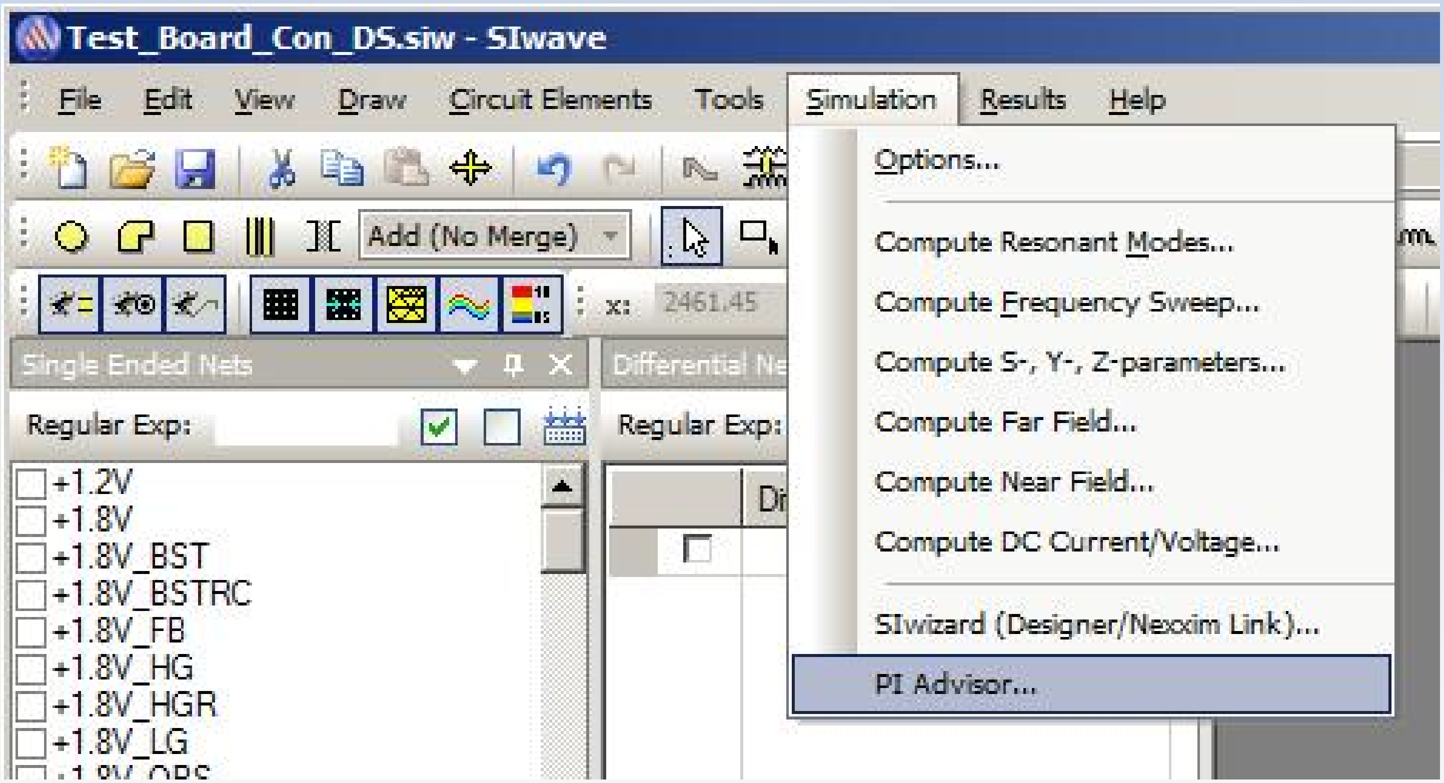


	Active		Part Number	RefDes	Capacitance (F)	Parasitic L (H)	Parasitic R (ohms)	Positive	Negative
✓	Yes	✗	GRM1885C1H820JA01	C1	8.2E-11	7.00689E-10	0.155633	+1.2V	GND
✓	Yes	✗	GRM188R71H221KA01	C2	2.2E-10	5.22762E-10	0.964207	+1.2V	GND
✓	Yes	✗	GRM1885C1H201JA01	C3	2E-10	7.63124E-10	0.121881	+1.2V	GND
✓	Yes	✗	GRM21BF51A225ZA01	C4	2.2E-06	3.4867E-10	0.00433996	+1.2V	GND
✓	Yes	✗	GRM188F51C225ZA01	C5	2.2E-06	4.00639E-10	0.00796341	+1.2V	GND
✓	Yes	✗	GRM21BF51A225ZA01	C6	2.2E-06	3.4867E-10	0.00433996	+1.2V	GND
✓	Yes	✗	GRM21BF51A225ZA01	C7	2.2E-06	3.4867E-10	0.00433996	+1.2V	GND
✓	Yes	✗	GRM21BF51A225ZA01	C8	2.2E-06	3.4867E-10	0.00433996	+1.2V	GND
✓	Yes	✗	GRM21BF51A225ZA01	C9	2.2E-06	3.4867E-10	0.00433996	+1.2V	GND
✓	Yes	✗	GRM1885C1H561JA01	C11	5.6E-10	5.8294E-10	0.0910925	GND	+1.2V
✓	Yes	✗	GRM21BR71E104KA01	C12	1E-07	5.00196E-10	0.0194763	GND	+1.2V
✓	Yes	✗	GRM1885C1H820JA01	C13	8.2E-11	7.00689E-10	0.155633	GND	+1.2V
✓	Yes	✗	GRM21BF51A225ZA01	C14	2.2E-06	3.4867E-10	0.00433996	+1.2V	GND
✓	Yes	✗	GRM2165C1H202JA01	C15	2E-09	5.60276E-10	0.0555069	+1.2V	GND
✓	Yes	✗	GRM188R60J474KA01	C16	4.7E-07	5.35164E-10	0.00913529	+1.2V	GND
✓	Yes	✗	GRM216F51H102ZA01	C17	1E-09	4.96929E-10	0.253964	+1.2V	GND
✓	Yes	✗	GRM21BR71E104KA01	C18	1E-07	5.00196E-10	0.0194763	GND	+1.2V
✓	Yes	✗	GRM1885C1H910JA01	C19	9.1E-11	6.56454E-10	0.143556	GND	+1.2V
✓	Yes	✗	GRM1885C1H101JA01	C20	1E-10	8.22615E-10	0.203464	GND	+1.2V
✓	Yes	✗	GRM21BR61A475KA73	C21	4.7E-06	2.98349E-10	0.00361006	+1.2V	GND
✓	Yes	✗	GRM216F51H224ZA01	C22	2.2E-07	4.73639E-10	0.0292659	+1.2V	GND
✓	Yes	✗	GRM216F51H224ZA01	C49	2.2E-07	4.73639E-10	0.0292659	+1.2V	GND
✓	Yes	✗	GRM21BF51H224ZA01	C51	2.2E-07	5.86749E-10	0.0214453	+1.2V	GND
✓	Yes	✗	GRM216F51A334ZA01	C52	3.3E-07	6.0008E-10	0.0204213	+1.2V	GND
✓	Yes	✗	GRM216F51H103ZA01	C181	1E-08	6.60515E-10	0.0822853	+1.2V	GND
✓	Yes	✗	GRM216F51H103ZA01	C170	1E-08	6.60515E-10	0.0822853	+1.2V	GND
✓	Yes	✗	GRM216F51H103ZA01	C180	1E-08	6.60515E-10	0.0822853	+1.2V	GND
✓	Yes	✗	GRM216F51H103ZA01	C167	1E-08	6.60515E-10	0.0822853	+1.2V	GND
✓	Yes	✗	GRM1885C1H121JA01	C43	1.2E-10	8.07155E-10	0.194051	+1.2V	GND
✓	Yes	✗	GRM21BF51A225ZA01	C45	2.2E-06	3.4867E-10	0.00433996	+1.2V	GND
✓	Yes	✗	GRM21BR71E104KA01	C46	1E-07	5.00196E-10	0.0194763	+1.2V	GND
✓	Yes	✗	GRM1885C1H820JA01	C47	8.2E-11	7.00689E-10	0.155633	+1.2V	GND
✓	Yes	✗	GRM1885C1H820JA01	C48	8.2E-11	7.00689E-10	0.155633	+1.2V	GND
✓	Yes	✗	GRM2165C1H302JA01	C312	3E-09	5.98851E-10	0.0441419	GND	+1.2V
✓	Yes	✗	GRM21BC70G106ME45	C316	1E-05	2.44675E-10	0.00293246	GND	+1.2V
✓	Yes	✗	GRM188R71H271KA01	C317	2.7E-10	5.51632E-10	0.813567	GND	+1.2V
✓	No	✗	GRM21BR71E104KA01	C26	1E-07	5.00196E-10	0.0194763	GND	AVDD
✓	No	✗	GRM21BR71E104KA01	C27	1E-07	5.00196E-10	0.0194763	PLLVCC	GND
✓	No	✗	GRM21BR71E104KA01	C28	1E-07	5.00196E-10	0.0194763	PLLVCC	GND
✓	No	✗	GRM21BR71E104KA01	C29	1E-07	5.00196E-10	0.0194763	GND	+3.3V

Original Design
All 36 Capacitors Enabled

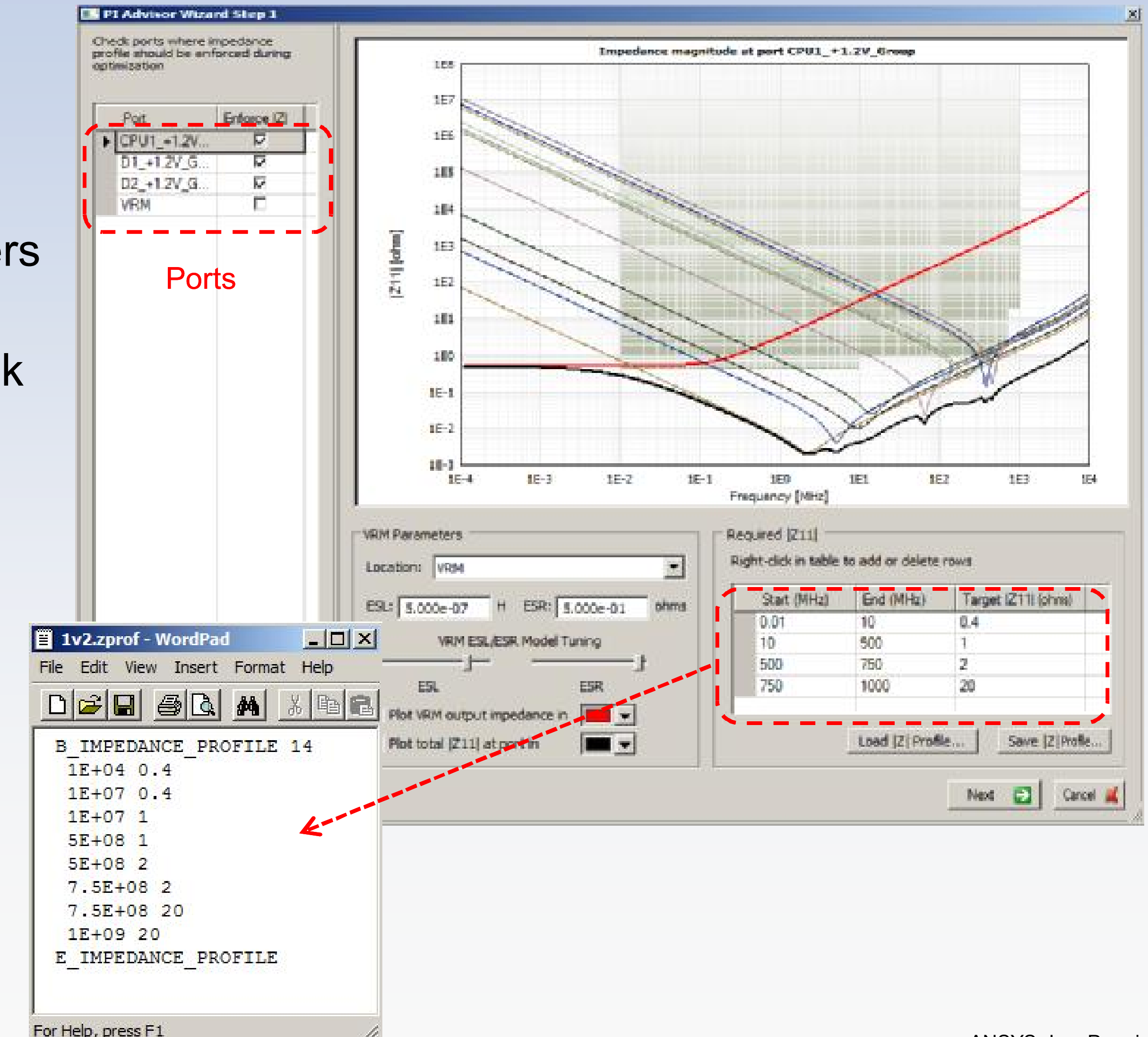


Launch SIwave PI Advisor…



Step 1 : Define Ports and Target Impedance Profile

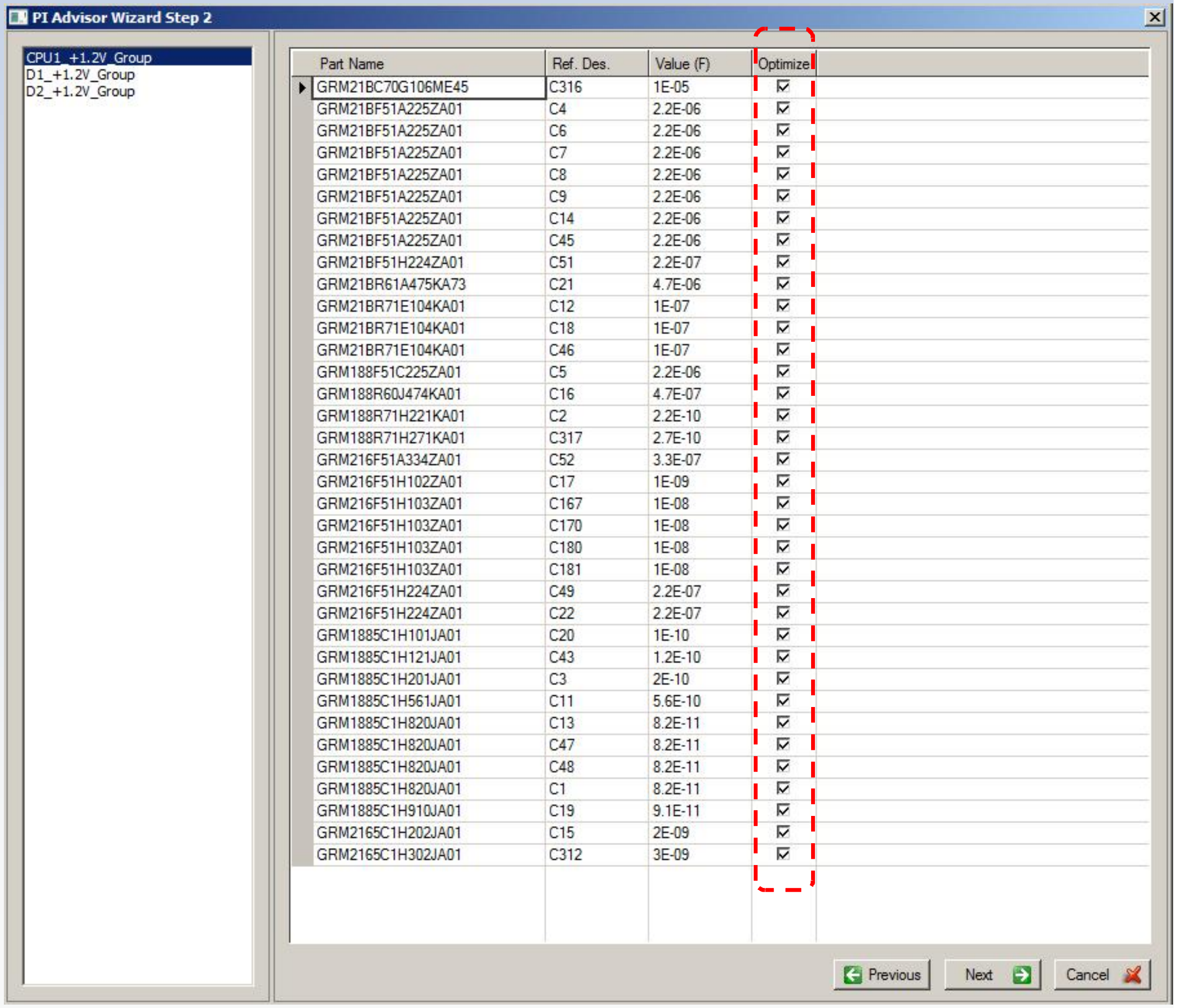
- **PI Advisor**
  - Select Reference Port Locations
  - Set the VRM Parameters including ESL & ESR
  - Define Impedance Mask



Step 2 : Select Capacitors for Automated Optimization

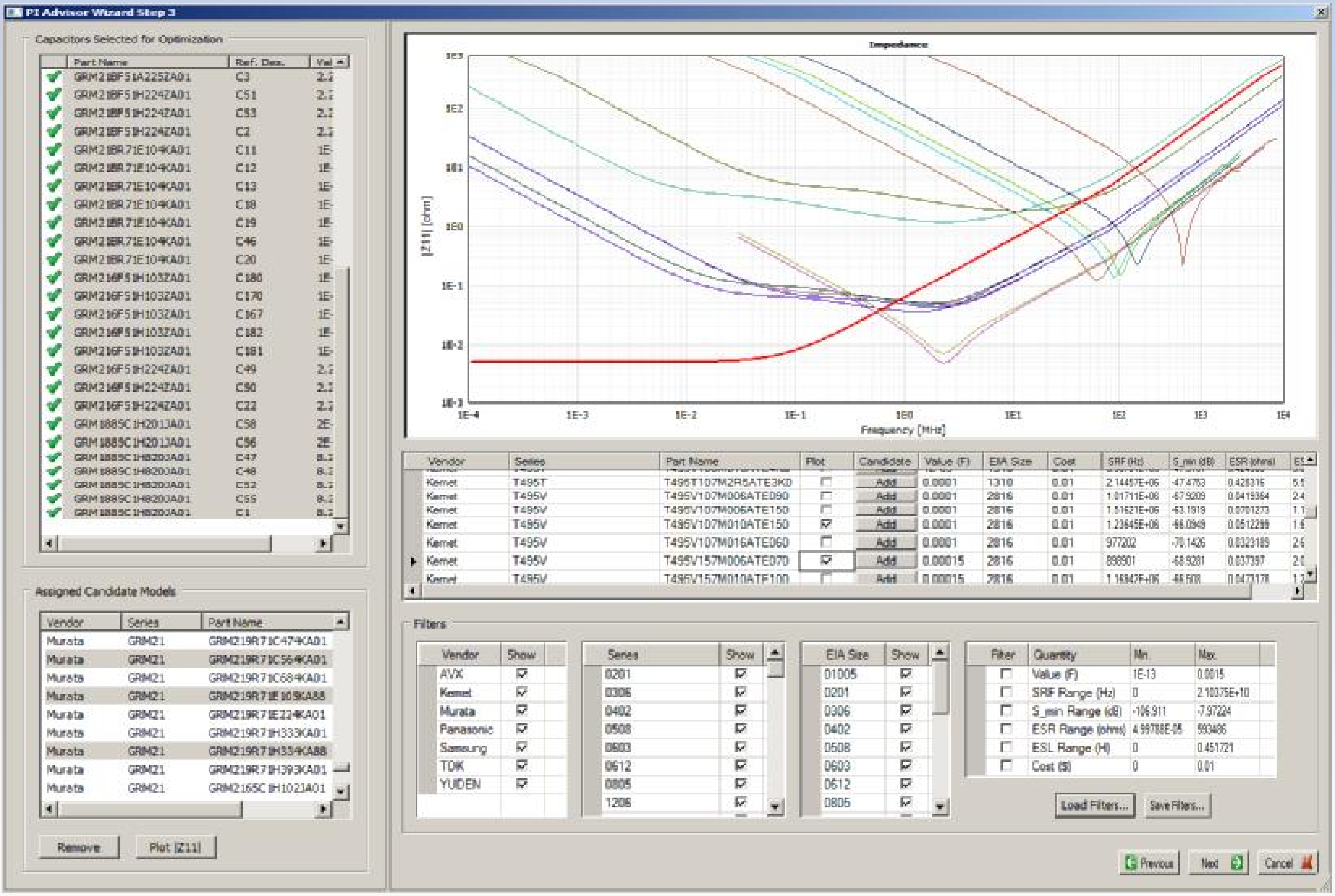
ANSYS

- **PI Advisor**
  - Select Capacitor set that needs to be optimized
  - All 36 caps selected



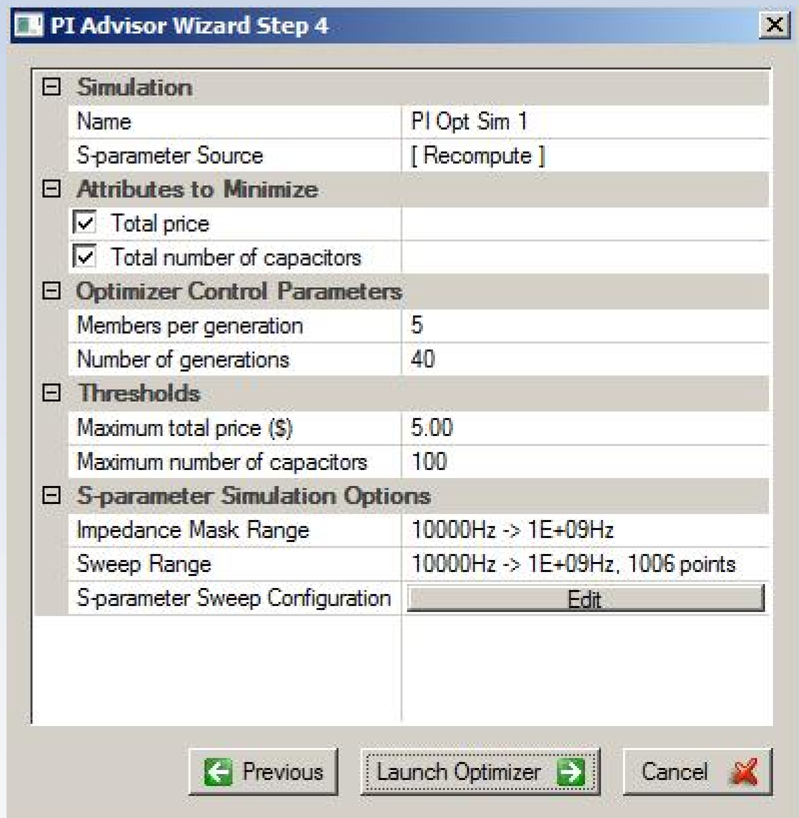
Part Name	Ref. Des.	Value (F)	Optimize
GRM21BC70G106ME45	C316	1E-05	☑
GRM21BF51A225ZA01	C4	2.2E-06	☑
GRM21BF51A225ZA01	C6	2.2E-06	☑
GRM21BF51A225ZA01	C7	2.2E-06	☑
GRM21BF51A225ZA01	C8	2.2E-06	☑
GRM21BF51A225ZA01	C9	2.2E-06	☑
GRM21BF51A225ZA01	C14	2.2E-06	☑
GRM21BF51A225ZA01	C45	2.2E-06	☑
GRM21BF51H224ZA01	C51	2.2E-07	☑
GRM21BR61A475KA73	C21	4.7E-06	☑
GRM21BR71E104KA01	C12	1E-07	☑
GRM21BR71E104KA01	C18	1E-07	☑
GRM21BR71E104KA01	C46	1E-07	☑
GRM188F51C225ZA01	C5	2.2E-06	☑
GRM188R60J474KA01	C16	4.7E-07	☑
GRM188R71H221KA01	C2	2.2E-10	☑
GRM188R71H271KA01	C317	2.7E-10	☑
GRM216F51A334ZA01	C52	3.3E-07	☑
GRM216F51H102ZA01	C17	1E-09	☑
GRM216F51H103ZA01	C167	1E-08	☑
GRM216F51H103ZA01	C170	1E-08	☑
GRM216F51H103ZA01	C180	1E-08	☑
GRM216F51H103ZA01	C181	1E-08	☑
GRM216F51H224ZA01	C49	2.2E-07	☑
GRM216F51H224ZA01	C22	2.2E-07	☑
GRM1885C1H101JA01	C20	1E-10	☑
GRM1885C1H121JA01	C43	1.2E-10	☑
GRM1885C1H201JA01	C3	2E-10	☑
GRM1885C1H561JA01	C11	5.6E-10	☑
GRM1885C1H820JA01	C13	8.2E-11	☑
GRM1885C1H820JA01	C47	8.2E-11	☑
GRM1885C1H820JA01	C48	8.2E-11	☑
GRM1885C1H820JA01	C1	8.2E-11	☑
GRM1885C1H910JA01	C19	9.1E-11	☑
GRM2165C1H202JA01	C15	2E-09	☑
GRM2165C1H302JA01	C312	3E-09	☑

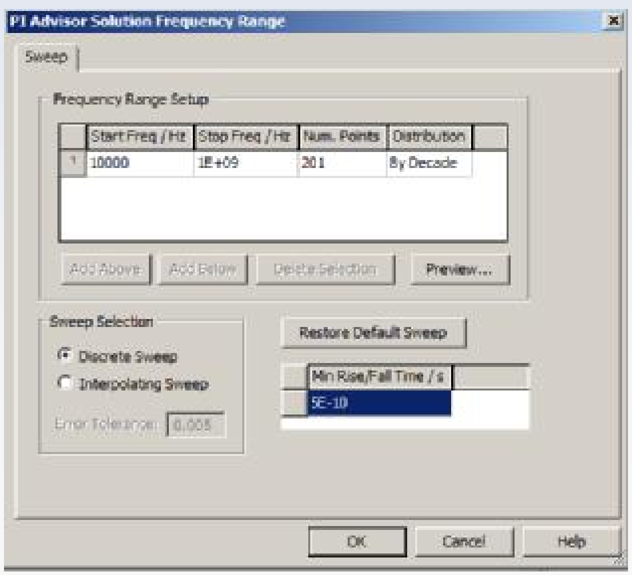
Step 3 : Select Candidate Capacitors for Optimization



Step 4 : Setup Optimization Criteria

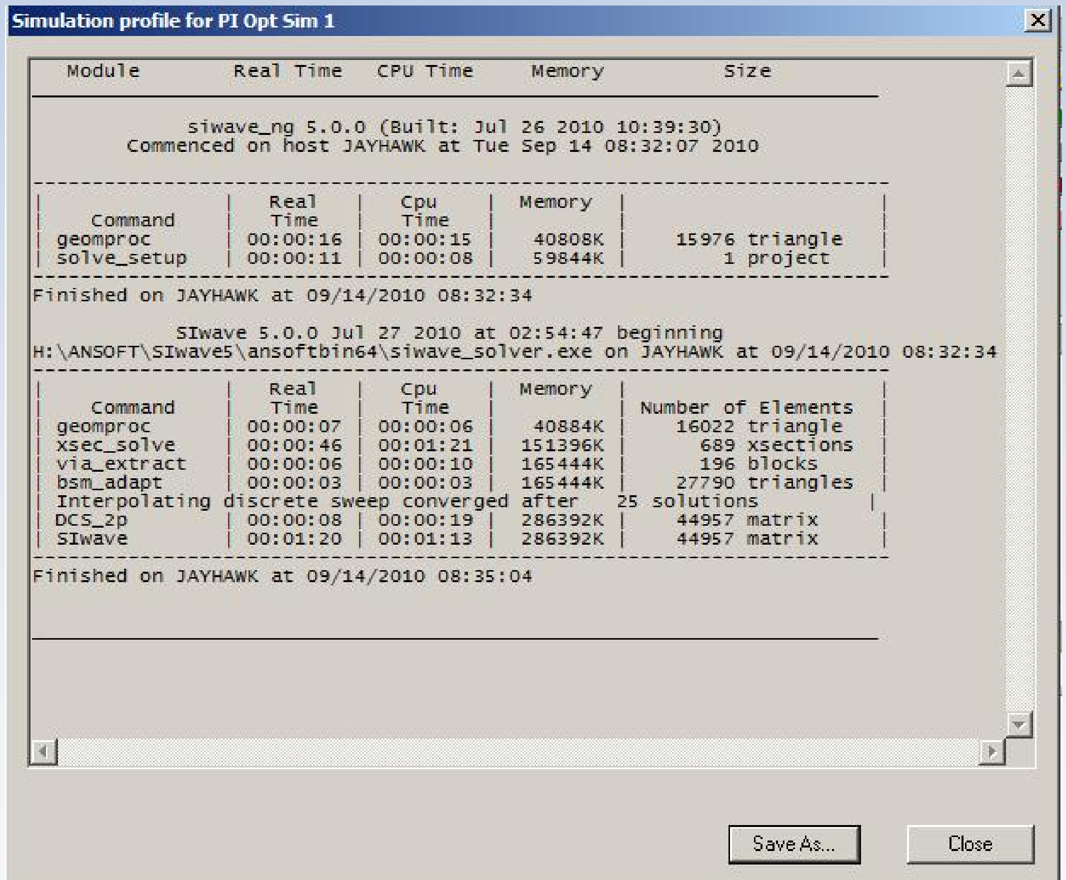
- **PI Advisor**
  - Launch PI Advisor Wizard
  - Set Optimizer Goal Parameters
  - Set Thresholds
    - Total price $$$
    - Total number of capacitors
  - Genetic Algorithm is used for optimization
  - SYZ sweep





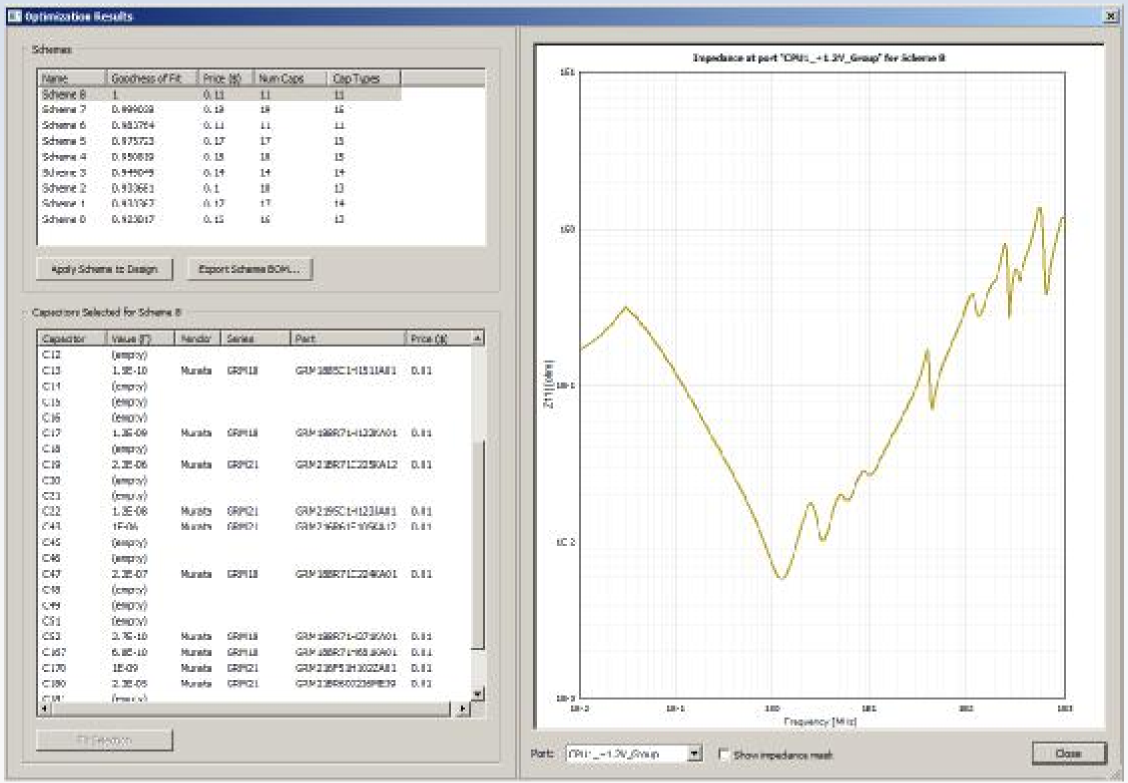
Step 5 : Launch Optimizer and Analyze Results

- **Time = 2 minutes 56 seconds**
- **RAM = 286 MB**
  - Frequency Setup
    - 10KHz < f < 1GHz
    - 201 Points/decade
  - Genetic Algorithm Setup
    - **Optimized for Impedance**
    - **Optimized for # of Caps**
    - **Optimized for Price**



PI Advisor – Step 5

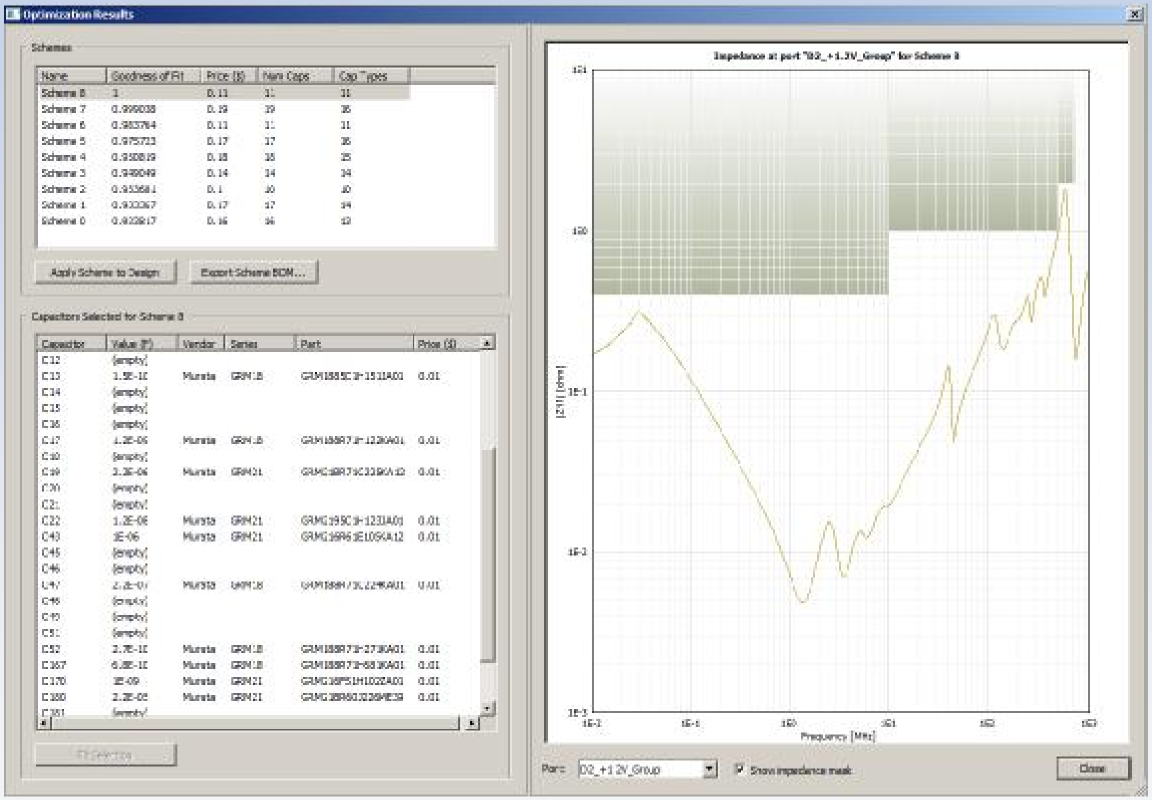
- **PI Advisor Results**
  - PI Advisor provides multiple different Schemes
  - Sort solutions by **Price ($), Num Caps** and **Goodness of Fit**
  - You can display Impedance Mask . Etc
  - Apply optimized capacitor scheme to the existing design
  - Export BOM file back to layout database



Step 5 : Launch Optimizer and Analyze Results

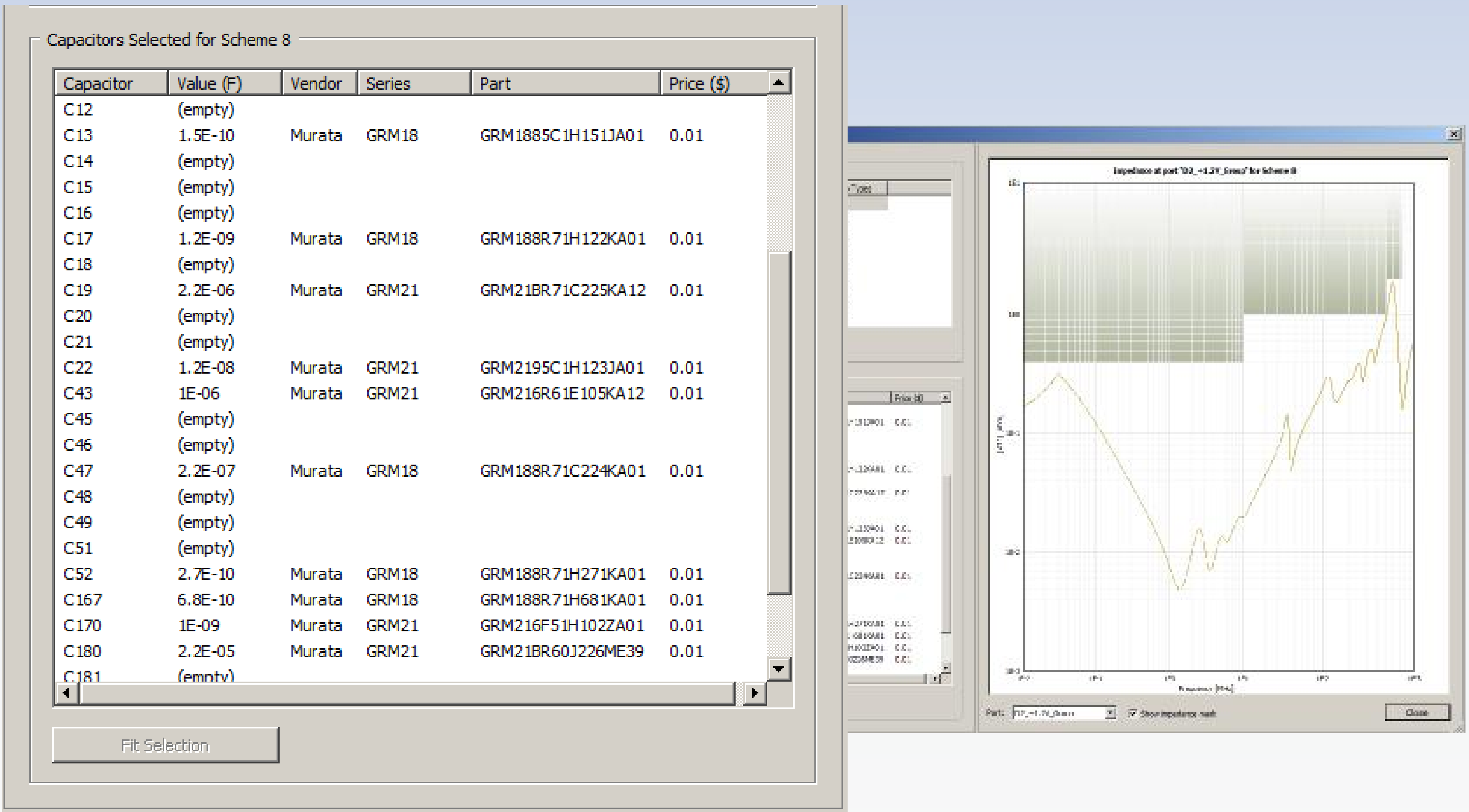
- **Original solution**
  – Total # Caps: 36

- **Optimized Solution**
  – Total # Caps: from 10 to 19
  – **9** Schemes available
  – **6** Capacitor Types: 10 to 16



PI Advisor Simulation Results

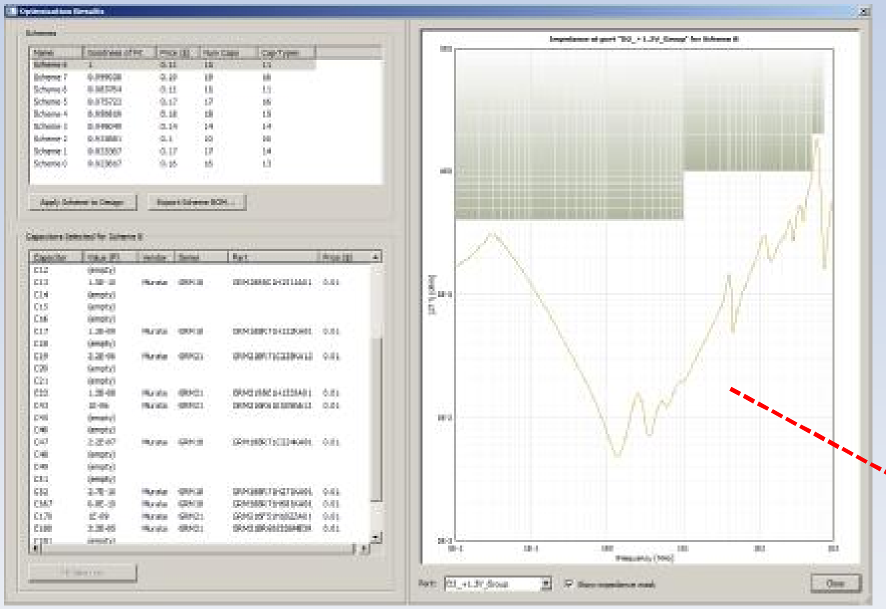
- **Scheme 8 Capacitors Selection information**
  – 11 capacitors and 11 different types



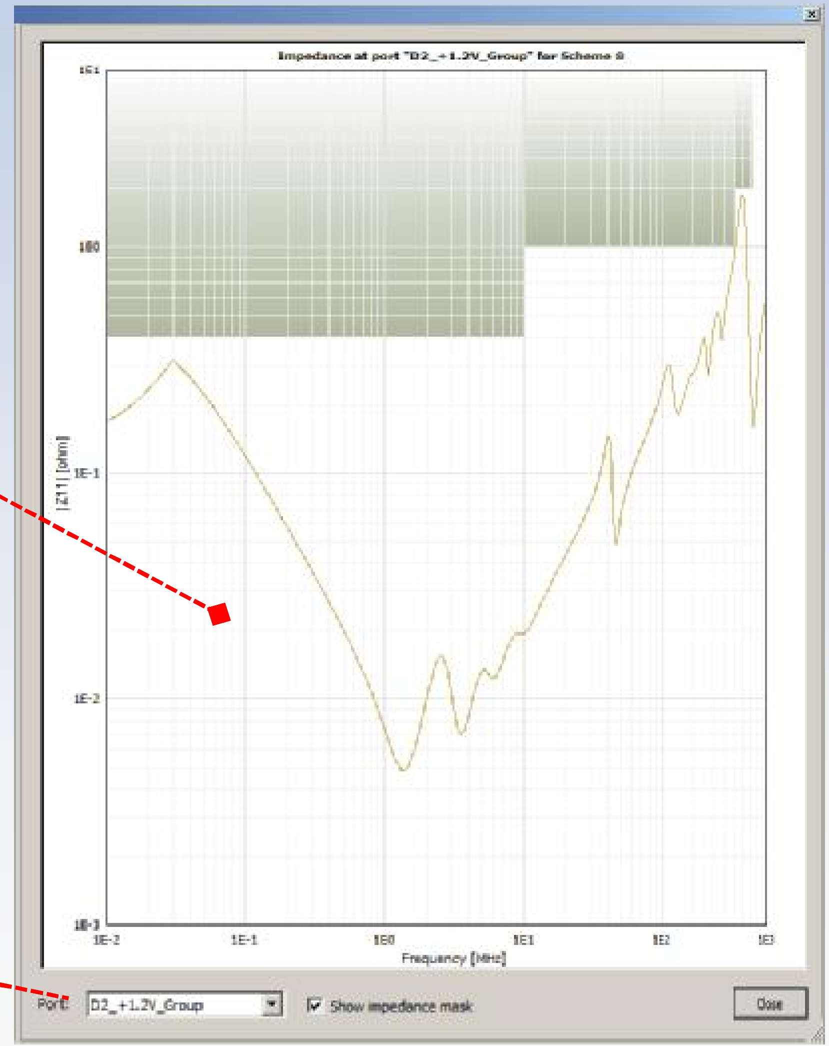
Capacitors Selected for Scheme 8

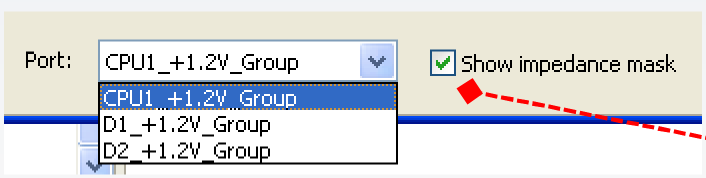
Capacitor	Value (F)	Vendor	Series	Part	Price ($)
C12	(empty)				
C13	1.5E-10	Murata	GRM18	GRM1885C1H151JA01	0.01
C14	(empty)				
C15	(empty)				
C16	(empty)				
C17	1.2E-09	Murata	GRM18	GRM188R71H122KA01	0.01
C18	(empty)				
C19	2.2E-06	Murata	GRM21	GRM21BR71C225KA12	0.01
C20	(empty)				
C21	(empty)				
C22	1.2E-08	Murata	GRM21	GRM2195C1H123JA01	0.01
C43	1E-06	Murata	GRM21	GRM216R61E105KA12	0.01
C45	(empty)				
C46	(empty)				
C47	2.2E-07	Murata	GRM18	GRM188R71C224KA01	0.01
C48	(empty)				
C49	(empty)				
C51	(empty)				
C52	2.7E-10	Murata	GRM18	GRM188R71H271KA01	0.01
C167	6.8E-10	Murata	GRM18	GRM188R71H681KA01	0.01
C170	1E-09	Murata	GRM21	GRM216F51H102ZA01	0.01
C180	2.2E-05	Murata	GRM21	GRM21BR60J226ME39	0.01
C181	(empty)				

PI Advisor Simulation Results



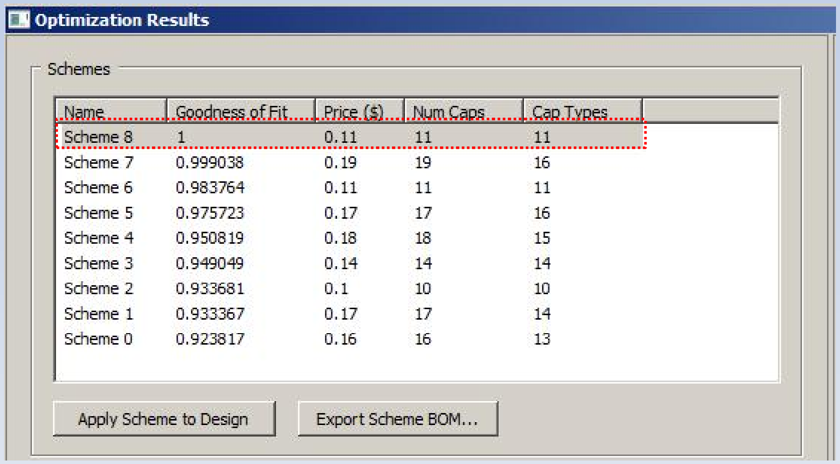
Scheme 8 Target impedance information





Port Selection

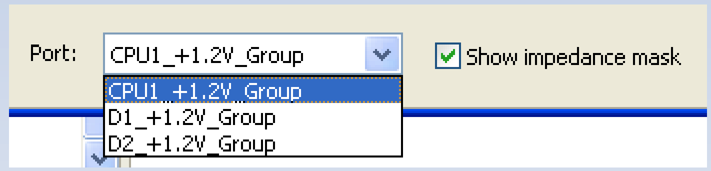
Scheme 8 Results – All three ports

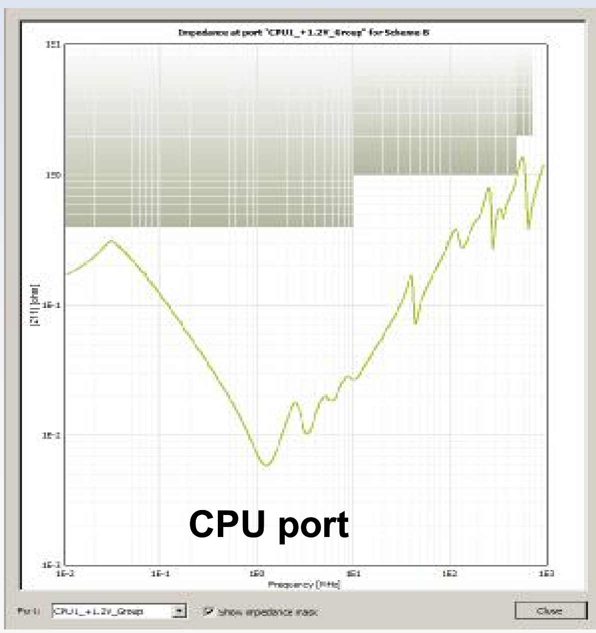

Optimization Results

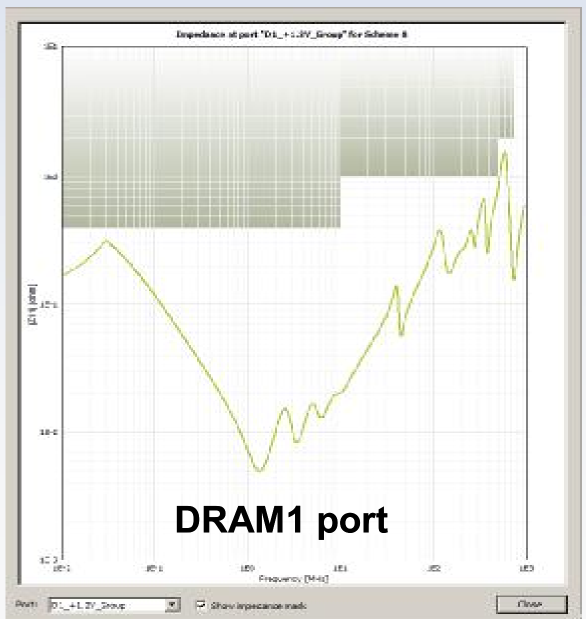
Schemes

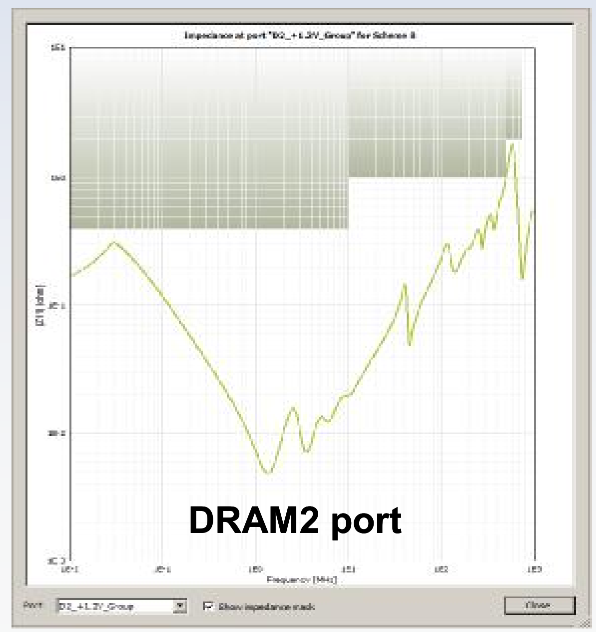
Name	Goodness of Fit	Price ($)	Num Caps	Cap Types
Scheme 8	1	0.11	11	11
Scheme 7	0.999038	0.19	19	16
Scheme 6	0.983764	0.11	11	11
Scheme 5	0.975723	0.17	17	16
Scheme 4	0.950819	0.18	18	15
Scheme 3	0.949049	0.14	14	14
Scheme 2	0.933681	0.1	10	10
Scheme 1	0.933367	0.17	17	14
Scheme 0	0.923817	0.16	16	13

Apply Scheme to Design | Export Scheme BOM...









Capacitor Count Reduction

Optimization Results

Schemes

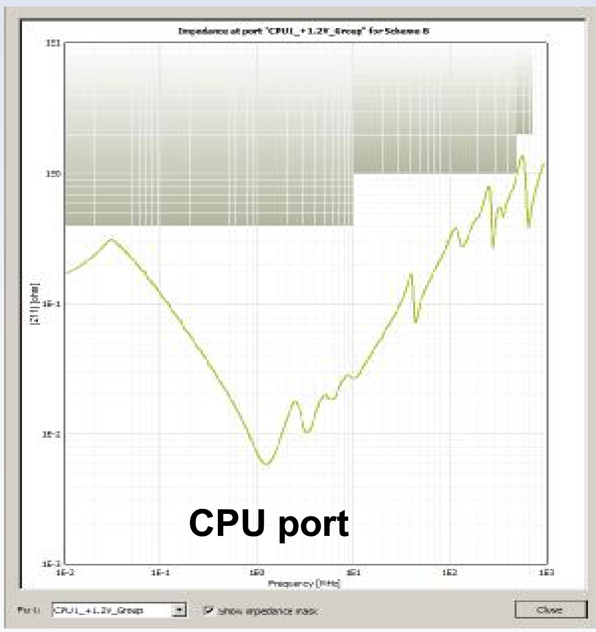
Name	Goodness of Fit	Price ($)	Num Caps	Cap Types
Scheme 8	1	0.11	11	11
Scheme 7	0.999038	0.19	19	16
Scheme 6	0.983764	0.11	11	11
Scheme 5	0.975723	0.17	17	16
Scheme 4	0.950819	0.18	18	15
Scheme 3	0.949049	0.14	14	14
Scheme 2	0.933681	0.1	10	10
Scheme 1	0.933367	0.17	17	14
Scheme 0	0.923817	0.16	16	13

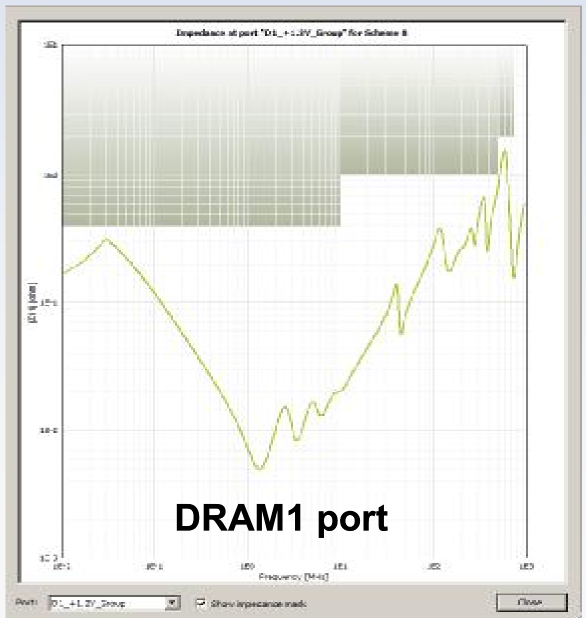
Apply Scheme to Design | Export Scheme BOM...

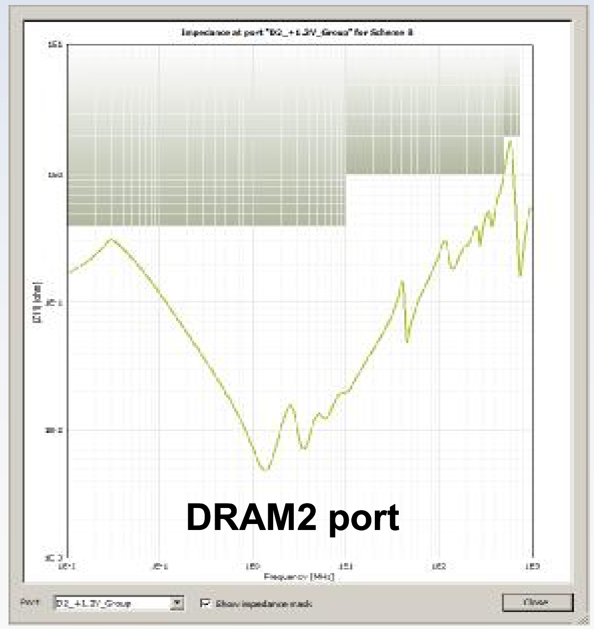
Original Design - Total of 36 Caps

New Design – Total of 11 Caps

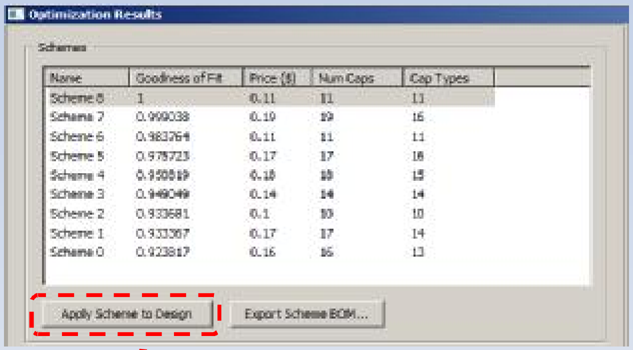
Capacitor Count **69% Reduction**



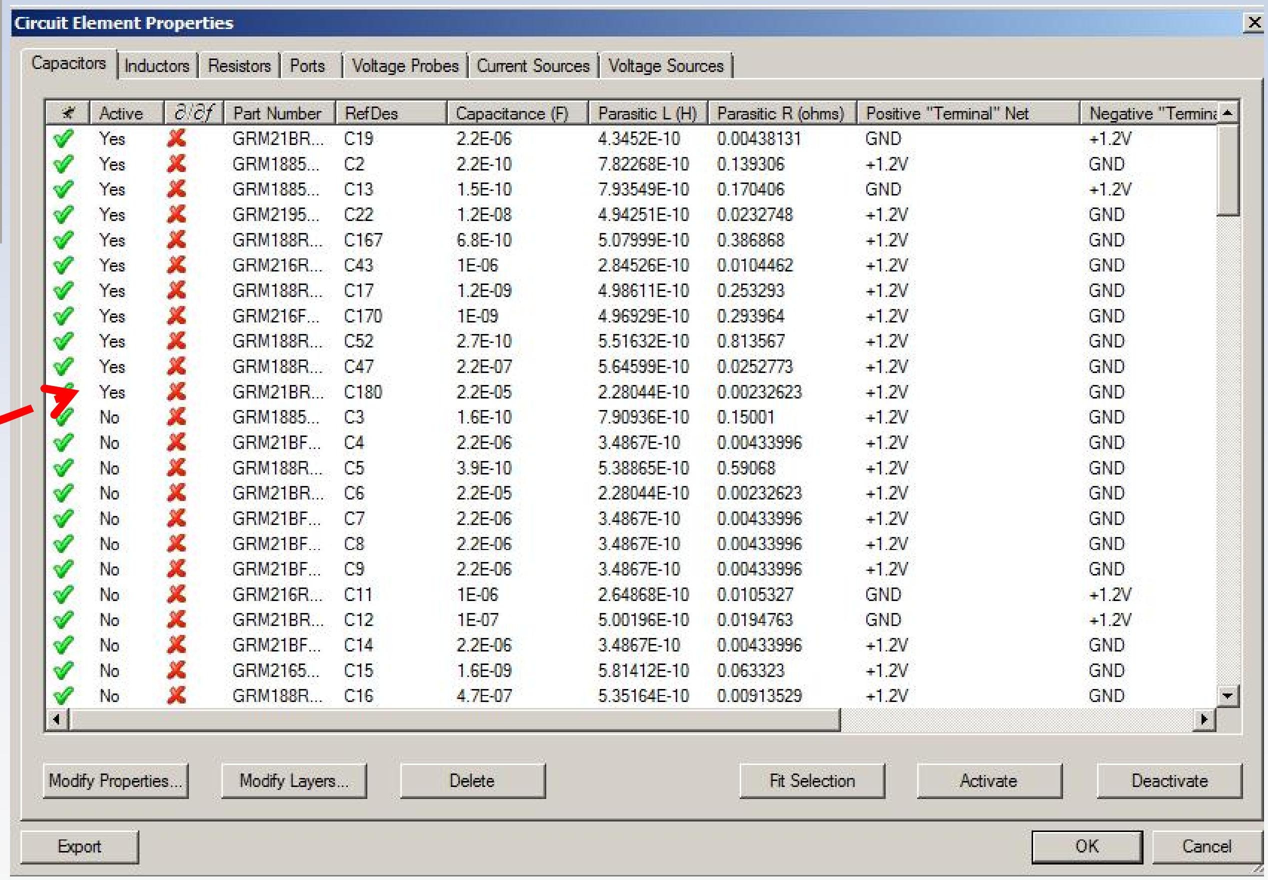




Apply Scheme 8 to Original Design



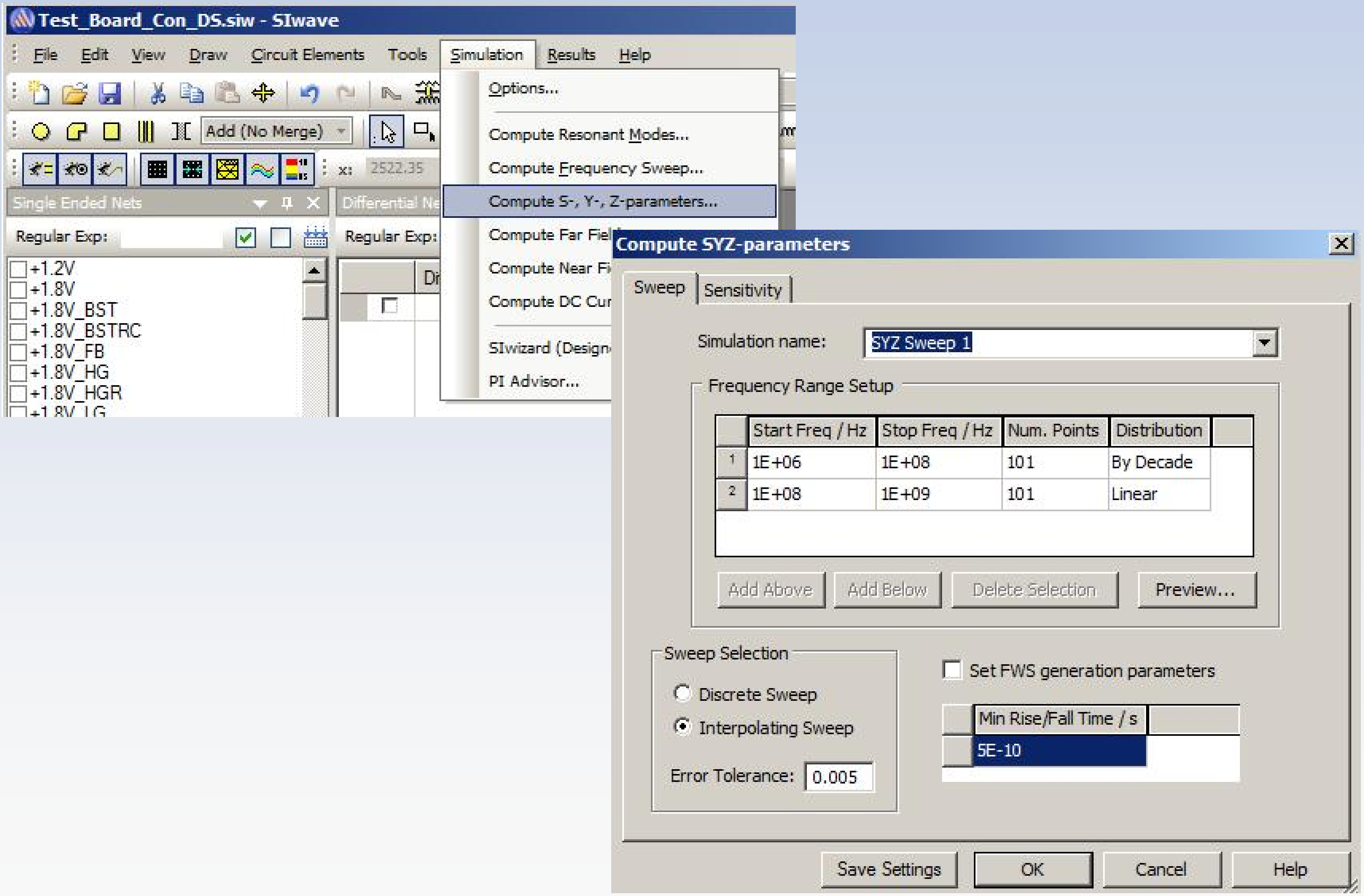
Name	Goodness of Fit	Price ($)	Num Caps	Cap Types
Scheme 8	1	0.11	11	11
Scheme 7	0.999038	0.19	19	16
Scheme 6	0.983764	0.11	11	11
Scheme 5	0.978723	0.17	17	18
Scheme 4	0.950819	0.18	18	15
Scheme 3	0.949049	0.14	14	14
Scheme 2	0.933681	0.1	10	10
Scheme 1	0.933367	0.17	17	14
Scheme 0	0.923817	0.16	16	13



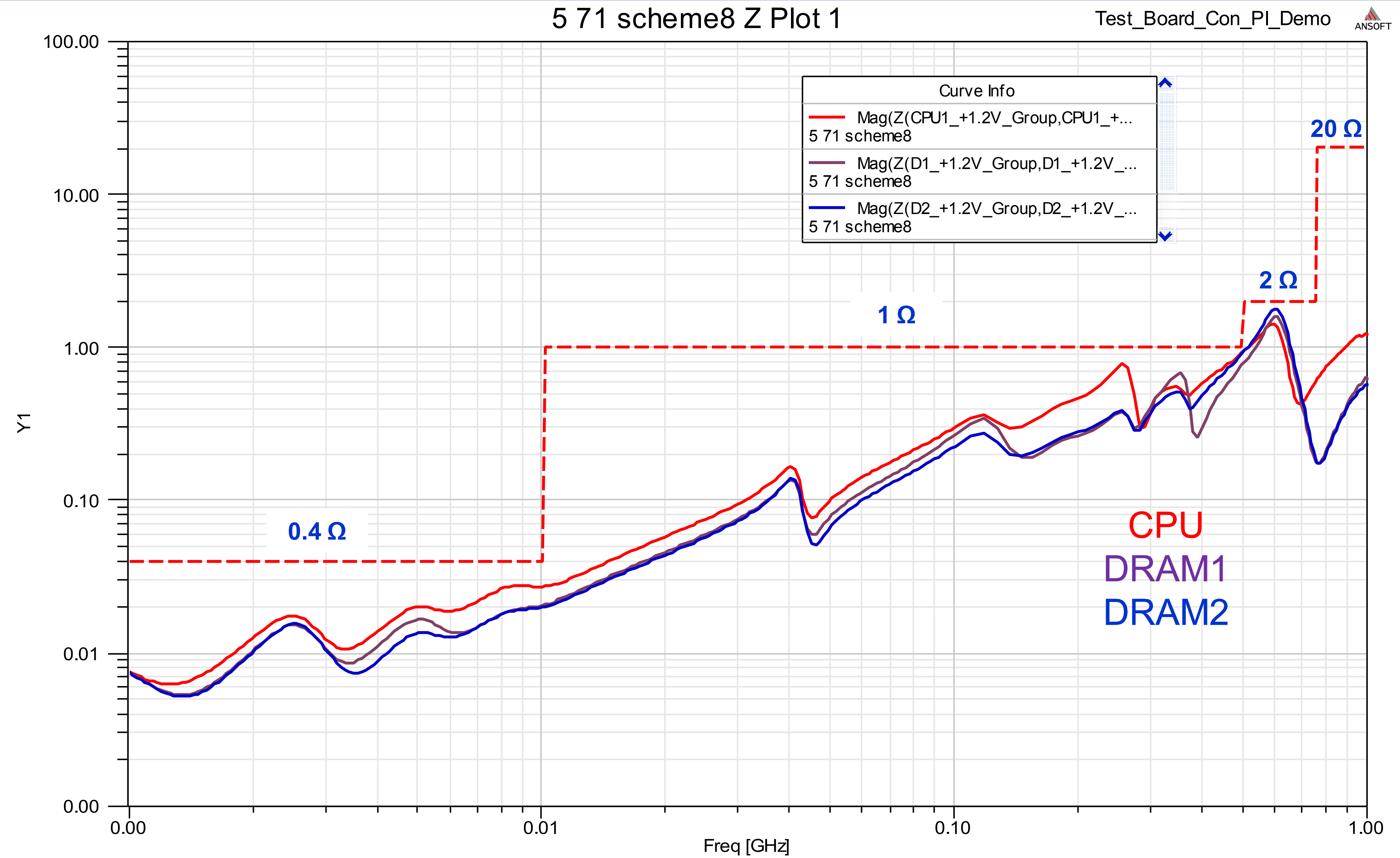
Active	Part Number	RefDes	Capacitance (F)	Parasitic L (H)	Parasitic R (ohms)	Positive "Terminal" Net	Negative "Termin
Yes	GRM21BR...	C19	2.2E-06	4.3452E-10	0.00438131	GND	+1.2V
Yes	GRM1885...	C2	2.2E-10	7.82268E-10	0.139306	+1.2V	GND
Yes	GRM1885...	C13	1.5E-10	7.93549E-10	0.170406	GND	+1.2V
Yes	GRM2195...	C22	1.2E-08	4.94251E-10	0.0232748	+1.2V	GND
Yes	GRM188R...	C167	6.8E-10	5.07999E-10	0.386868	+1.2V	GND
Yes	GRM216R...	C43	1E-06	2.84526E-10	0.0104462	+1.2V	GND
Yes	GRM188R...	C17	1.2E-09	4.98611E-10	0.253293	+1.2V	GND
Yes	GRM216F...	C170	1E-09	4.96929E-10	0.293964	+1.2V	GND
Yes	GRM188R...	C52	2.7E-10	5.51632E-10	0.813567	+1.2V	GND
Yes	GRM188R...	C47	2.2E-07	5.64599E-10	0.0252773	+1.2V	GND
Yes	GRM21BR...	C180	2.2E-05	2.28044E-10	0.00232623	+1.2V	GND
No	GRM1885...	C3	1.6E-10	7.90936E-10	0.15001	+1.2V	GND
No	GRM21BF...	C4	2.2E-06	3.4867E-10	0.00433996	+1.2V	GND
No	GRM188R...	C5	3.9E-10	5.38865E-10	0.59068	+1.2V	GND
No	GRM21BR...	C6	2.2E-05	2.28044E-10	0.00232623	+1.2V	GND
No	GRM21BF...	C7	2.2E-06	3.4867E-10	0.00433996	+1.2V	GND
No	GRM21BF...	C8	2.2E-06	3.4867E-10	0.00433996	+1.2V	GND
No	GRM21BF...	C9	2.2E-06	3.4867E-10	0.00433996	+1.2V	GND
No	GRM216R...	C11	1E-06	2.64868E-10	0.0105327	GND	+1.2V
No	GRM21BR...	C12	1E-07	5.00196E-10	0.0194763	GND	+1.2V
No	GRM21BF...	C14	2.2E-06	3.4867E-10	0.00433996	+1.2V	GND
No	GRM2165...	C15	1.6E-09	5.81412E-10	0.063323	+1.2V	GND
No	GRM188R...	C16	4.7E-07	5.35164E-10	0.00913529	+1.2V	GND

Circuit Element Properties auto defined !

Re- Compute S,Y,Z parameters

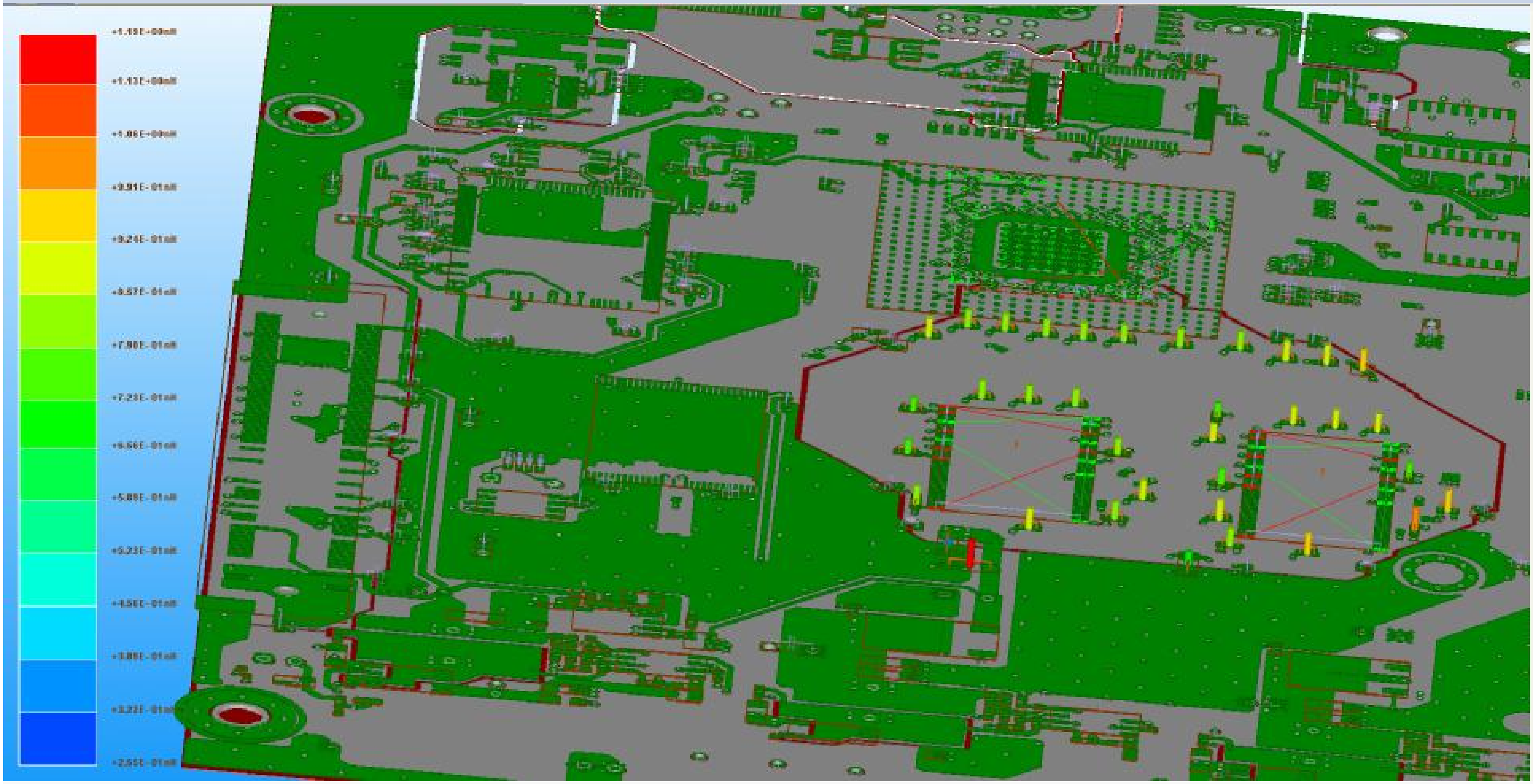


Final Simulation Results



Loop Inductance Plot

- **Provides intuitive plot to analyze capacitor layout thereby minimizing loop inductance (all 36 caps displayed)**



Efficient Simulation = Design Productivity

[*]2005 ITRS: *"Cost of design is the greatest threat to the continuation of the semiconductor roadmap… [and] design productivity… is the most massive and critical [design challenge facing the industry today]."*

[*]Source: International Technology Roadmap for Semiconductors

Delivering productivity:

- **Assume 4 to 5 changes per board**
  - Single PI Advisor simulation time ~ 3 min
  - Simulation time is approximately 10-15 min.
- **Result: Your design team meets project performance requirements on time and, therefore, within budget.**

Summary

- **Achieving *Adaptive Target Impedance* Specifications is critical for overall system performance**
- **The advantages of *PI Advisor* were shown here.**
  - Increase capacitor count in order to make design more robust
  - Reduce the capacitor count
  - Reduce number of different capacitor types used
  - Redesign using lower cost capacitors
- **Efficient Power Integrity PCB Capacitor Optimization analysis and *"What-if…"* type analysis is utilized using:**
  - SIwave
  - DesignerSI