



# *Siwave 5.0 PI Advisor for Optimized DDR3 Memory Design*

**Presented by  
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Senior R&D Manager**



# Agenda

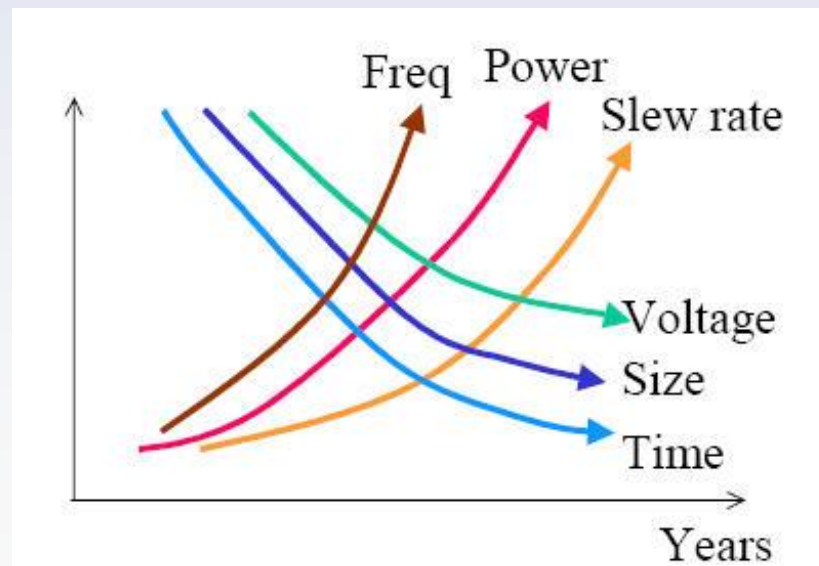


- Design Overview and Challenges
- How to define Target impedance ?
- PI Advisor
- Summary

# Design Challenges



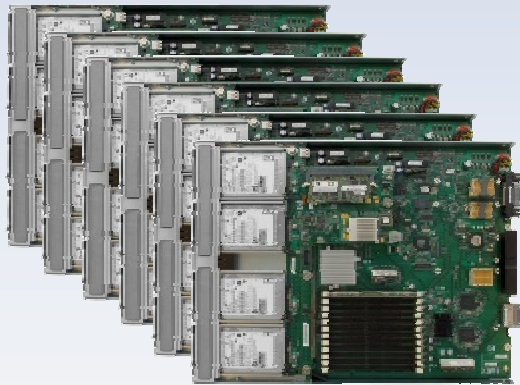
- **New deep sub-micron technologies**
  - Increased device speeds
  - Lower power supply voltages
- **Device miniaturization**
  - Decreasing design cycles
- **Delta-I noise on whole PDS system**



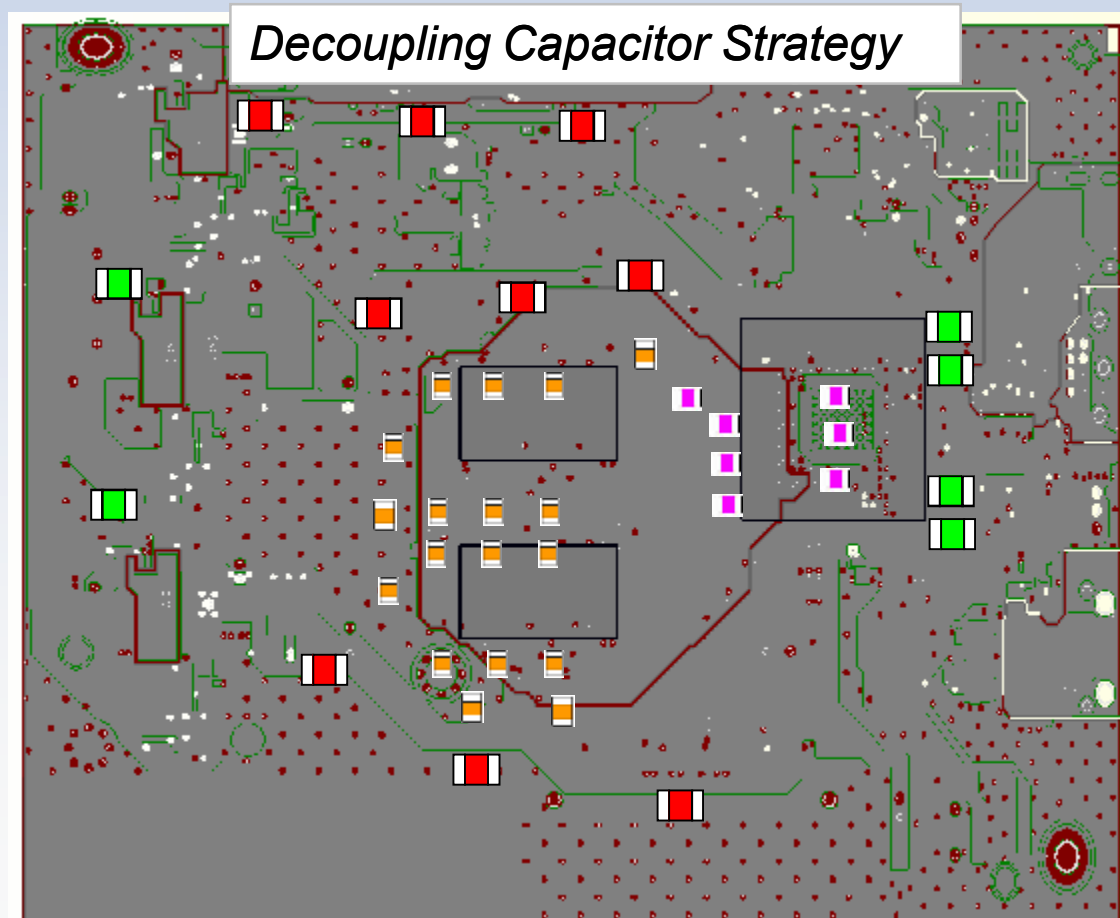
# A Typical Scenario



- *Customer X* has a PCB with possible SI/PI related issues
- Management is asking for quick fix and cost reduction
- **The Challenge:** How to achieve target impedances without compromising SI/PI performance?

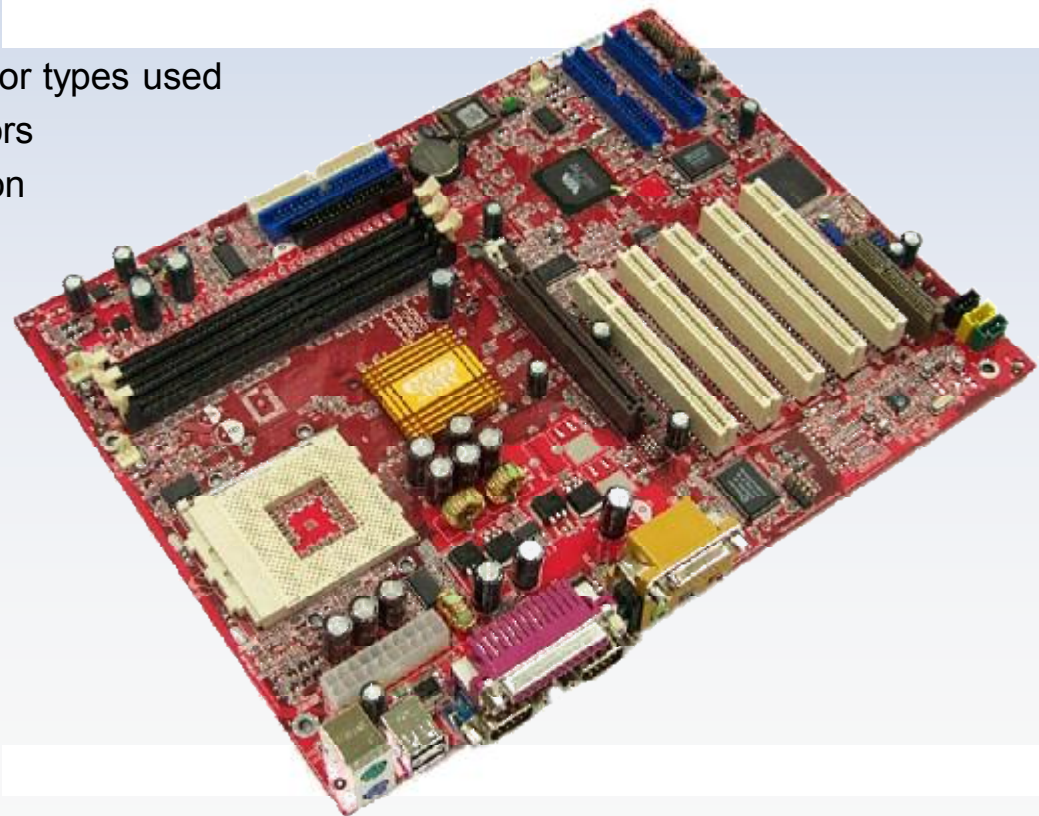


High Volume Production



- **PCB Geometry present**

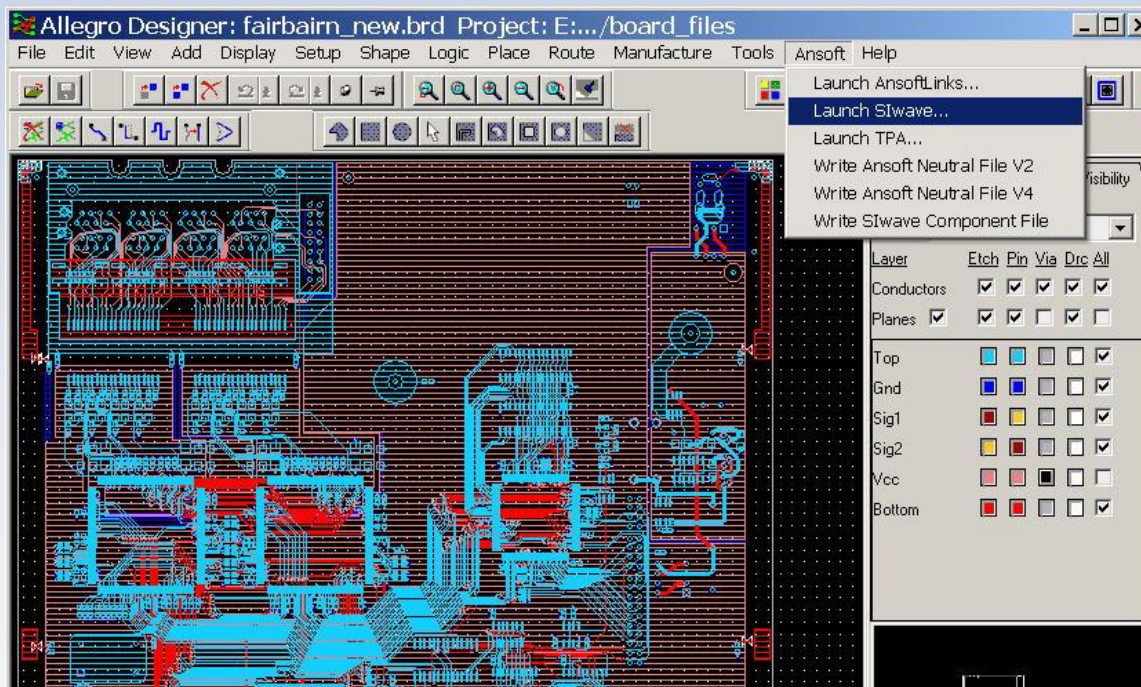
- A functional design, with all decoupling capacitors already placed on PCB
- PI Engineer may want to:
  - Increase capacitor count in order to make design more robust (i.e. overclocking, etc.)
  - Reduce the capacitor count
  - Reduce number of different capacitor types used
  - Redesign using lower cost capacitors
  - Chose appropriate capacitor location



# Layout Import and Translation



- Direct access to Ansoft tools from Cadence environment
  - Allegro layout is directly translated and imported in SIwave
  - Component file is also imported



**Cadence Allegro/APD**

Access Ansoft Tools  
directly from Allegro!

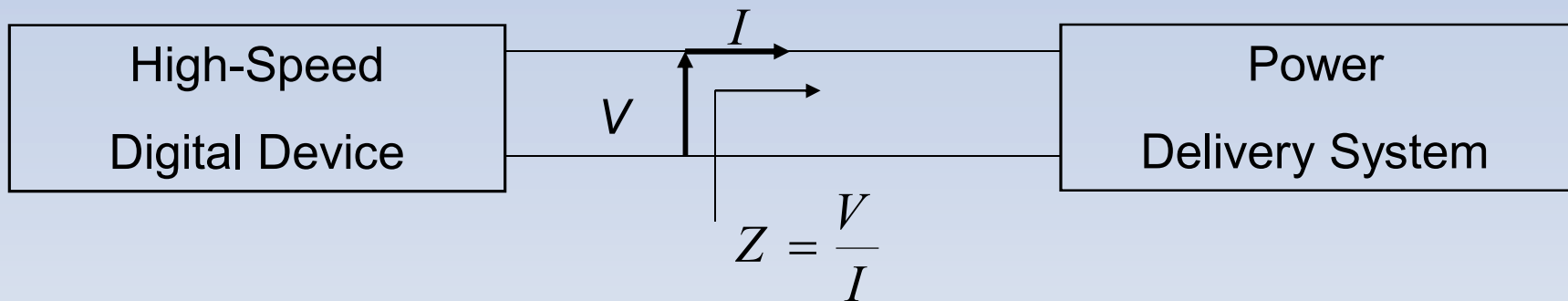


# ***ECAD Databases Supported***

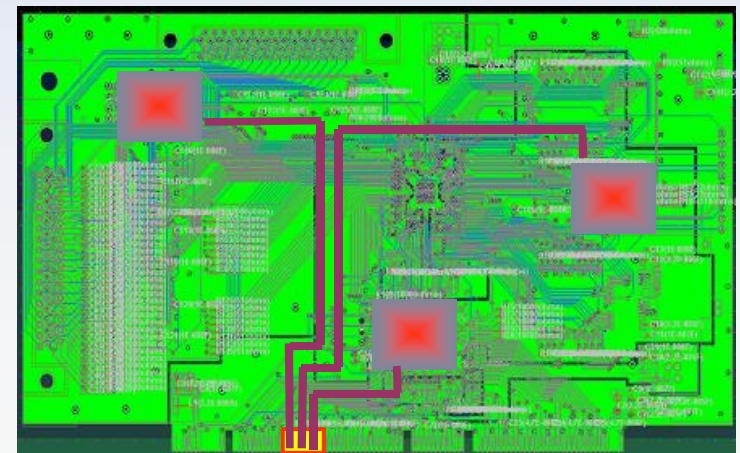
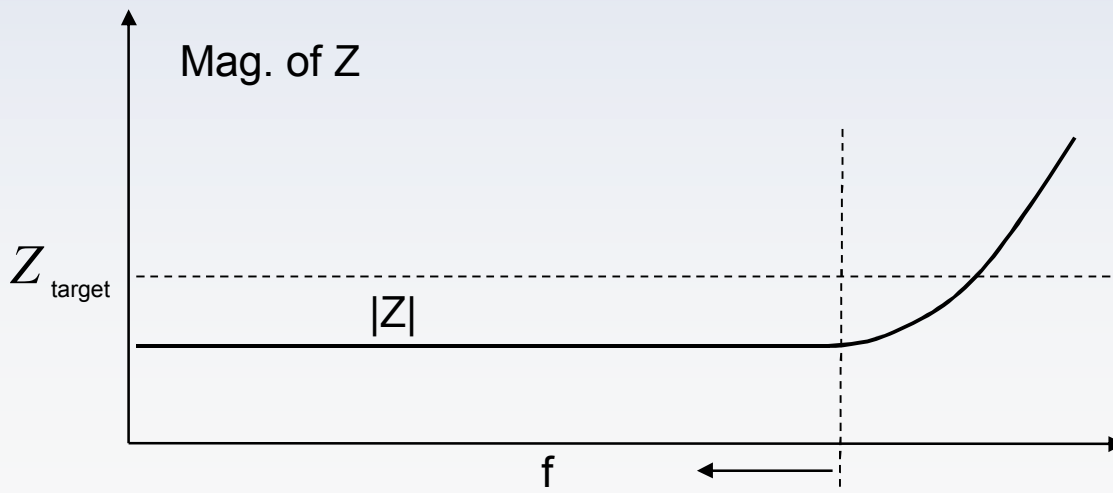


- |                                     |   |
|-------------------------------------|---|
| <b>1. Cadence Allegro and APD</b>   | <b>15.0, 15.1, 15.2, 15.5.x, 15.7, 16.0, 16.1, 16.2, and 16.3</b> |
| <b>2. Cadence SiP Digital/RF</b>    | <b>15.7, 16.0, 16.1, 16.2, and 16.3</b>                           |
| <b>3. Mentor BoardStation</b>       | <b>8.x</b>  |
| <b>4. Mentor BoardStation XE/RE</b> | <b>v2007.1 and v2007.2</b>  |
| <b>5. Mentor Expedition</b>         | <b>v2004, v2005, v2007.1, v2007.2 and v2007.3</b>                 |
| <b>6. Mentor PADS (PowerPCB)</b>    | <b>v5.2a, v2005 (2007 with 2005 export format)</b>                |
| <b>7. Synopsys Encore ICPD</b>      | <b>2001.x, 2002.x, 2003.x, 2004.x and 2005.x</b>                  |
| <b>8. Sigrity UPD</b>               | <b>9.0 and lower</b>  |
| <b>9. Zuken CR5000</b>              | <b>10.x and lower</b>   |
| <b>10. Altium Designer</b>          | <b>Summer 2010 Beta2 or later</b>                                 |

# PI Design Goal : Target Impedance of PDS



The Impedance looking into PDS at the device should be kept low over a broad frequency range (from DC to several harmonics of clock frequency).



VRM



# Target Impedance Trends



$$Z_{\text{Target}} = \frac{(\text{Power\_Supply\_Voltage}) \times (\text{Allowed\_Ripple})}{\text{Current}}$$

$$Z_{\text{Target}(2.5\text{v})} = \frac{(2.5\text{V}) \times (5\%)}{40.3\text{A}} = 3.1\text{m}\Omega$$

- \*Target Impedance is falling ~ 1.6x, every 3 years

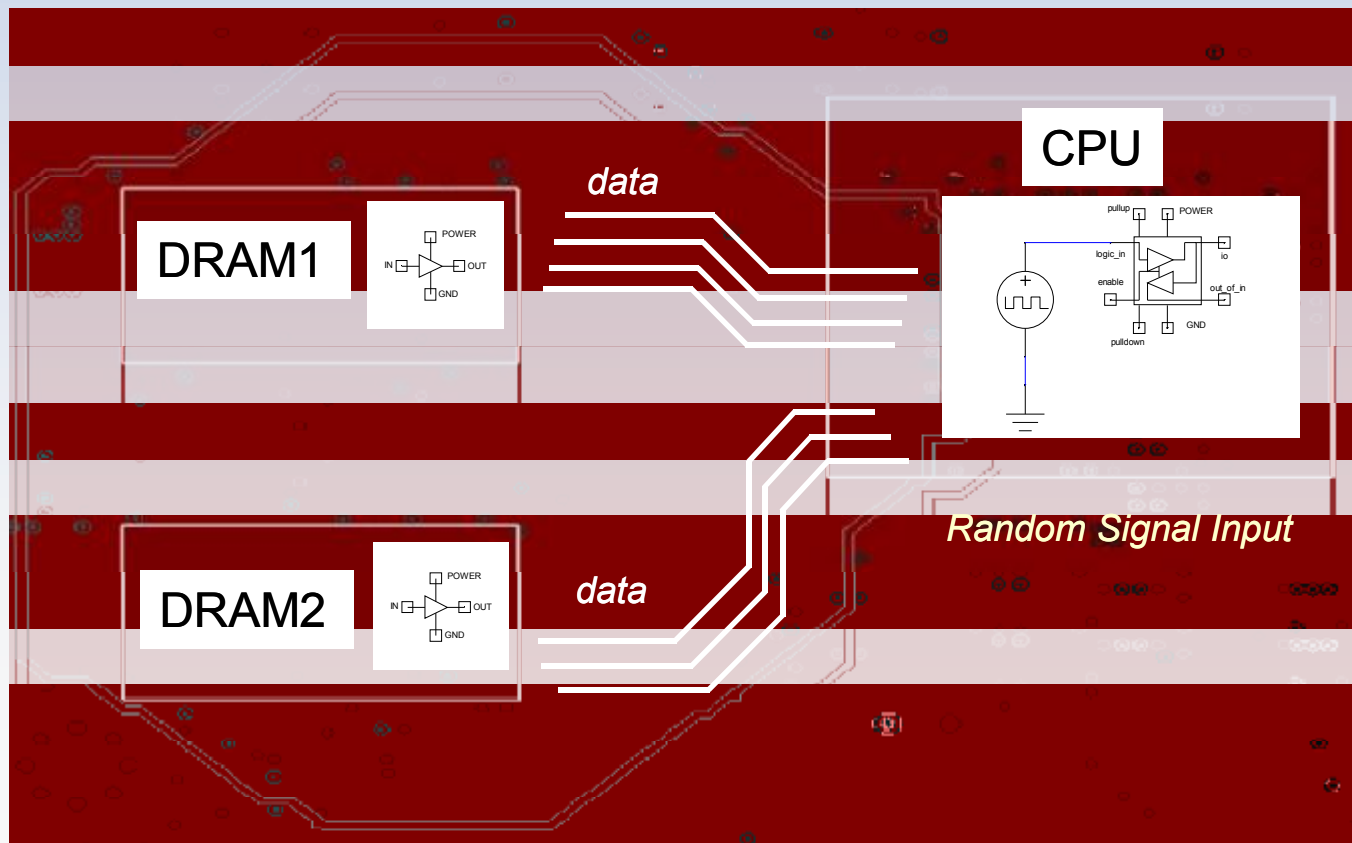
Year of first production	1997	1999	2002	2005	2008
Chip technology	0.25um	0.18um	0.13um	0.10um	0.07um
Across Chip Frequency (MHz)	450	600	800	1000	1100
Max. Chip Power (W)	100	120	140	160	180
Max current (A)	40.3	66.7	93.3	133.3	180.0
Power Supply (V)	2.5	1.8	1.5	1.2	0.9
Target Impedance (mΩ)	3.1	1.3	0.8	0.45	0.25

\*Source: International Technology Roadmap for Semiconductors

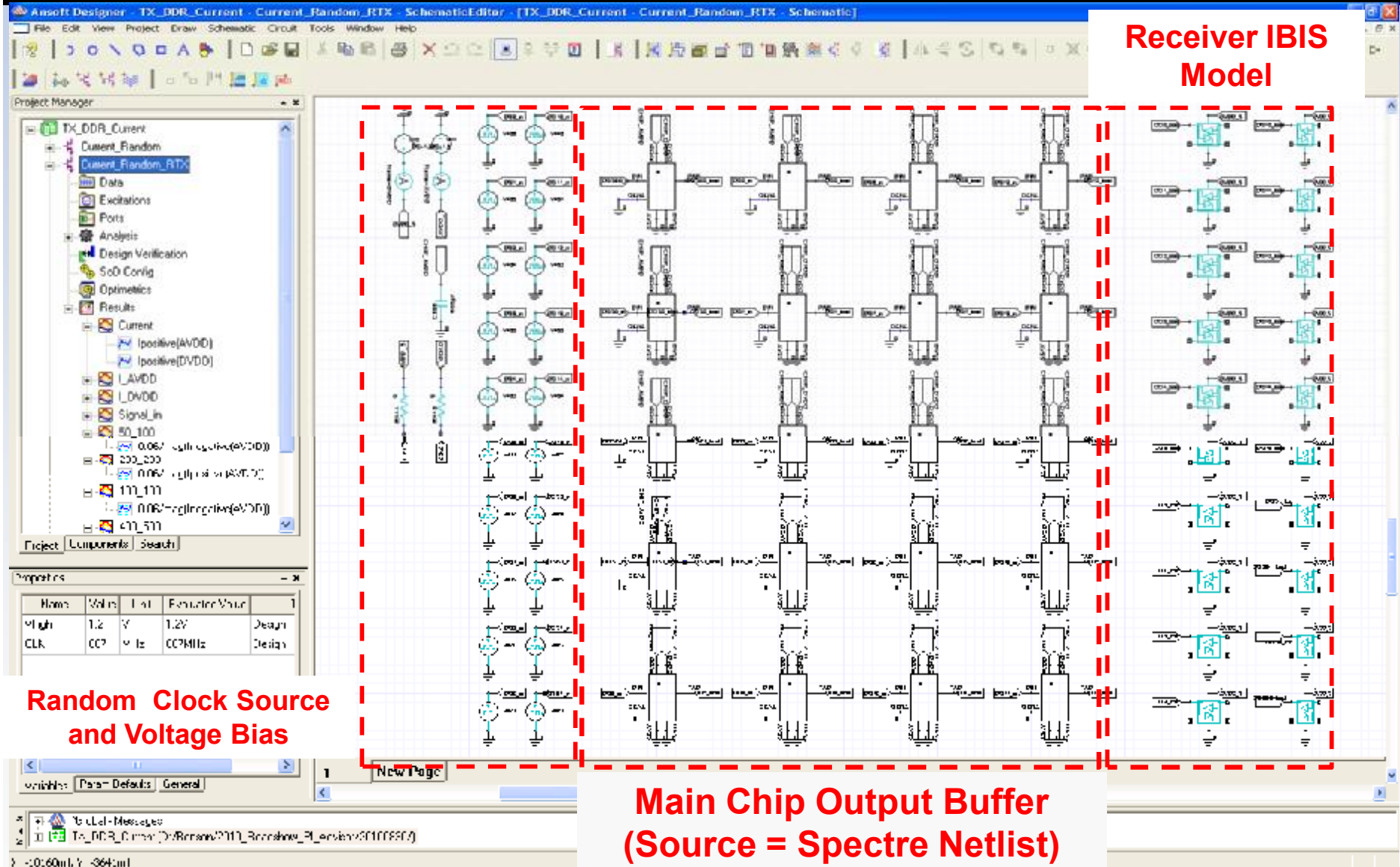
# Define Target Impedance



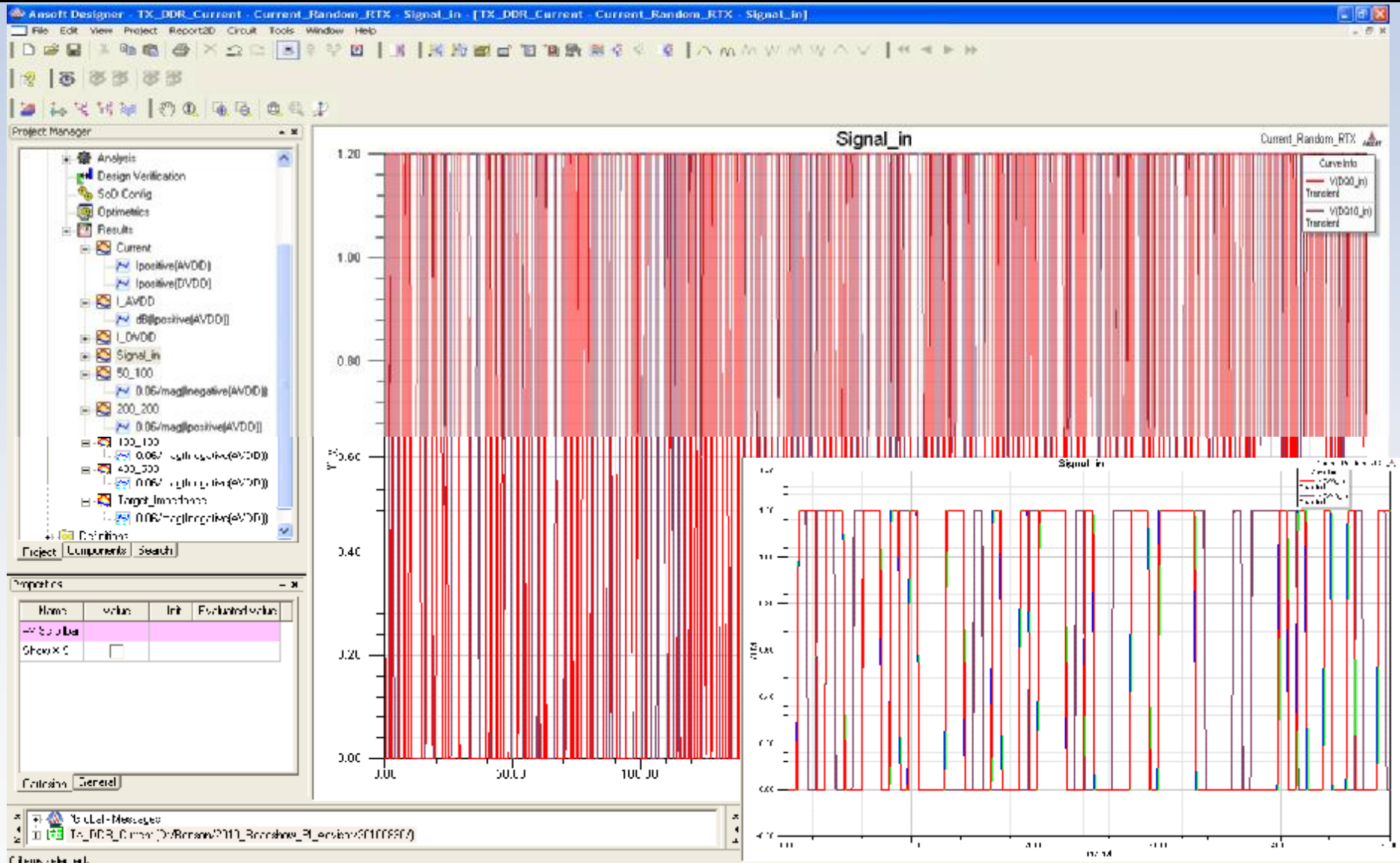
- Target Impedance
  - Get TX/Rx models for DRAM and CPU modules
  - Use Random Signal Input from CPU
  - Get time/frequency domain current profile



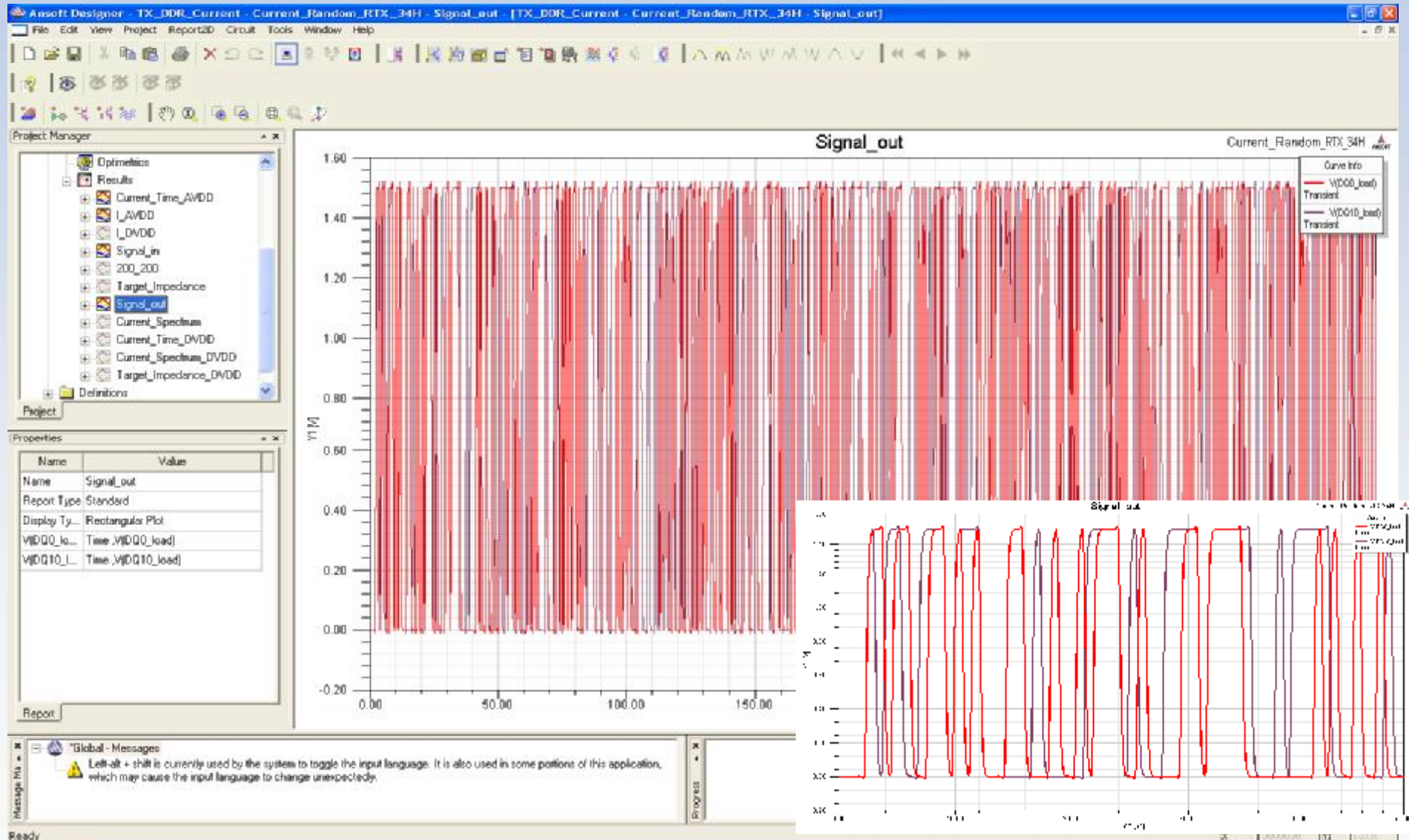
# Simulation Schematic



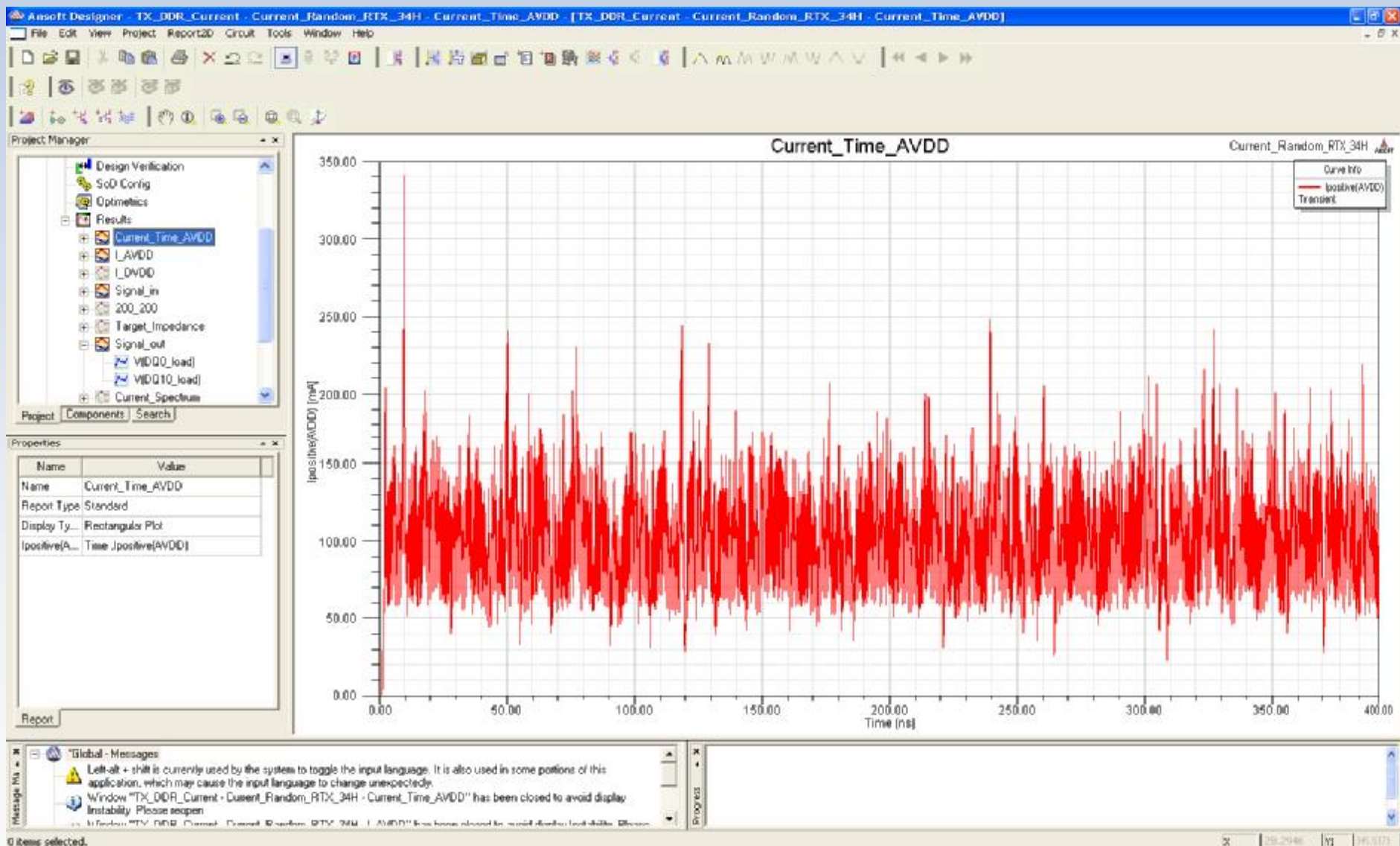
# Signal Input – Random Clock



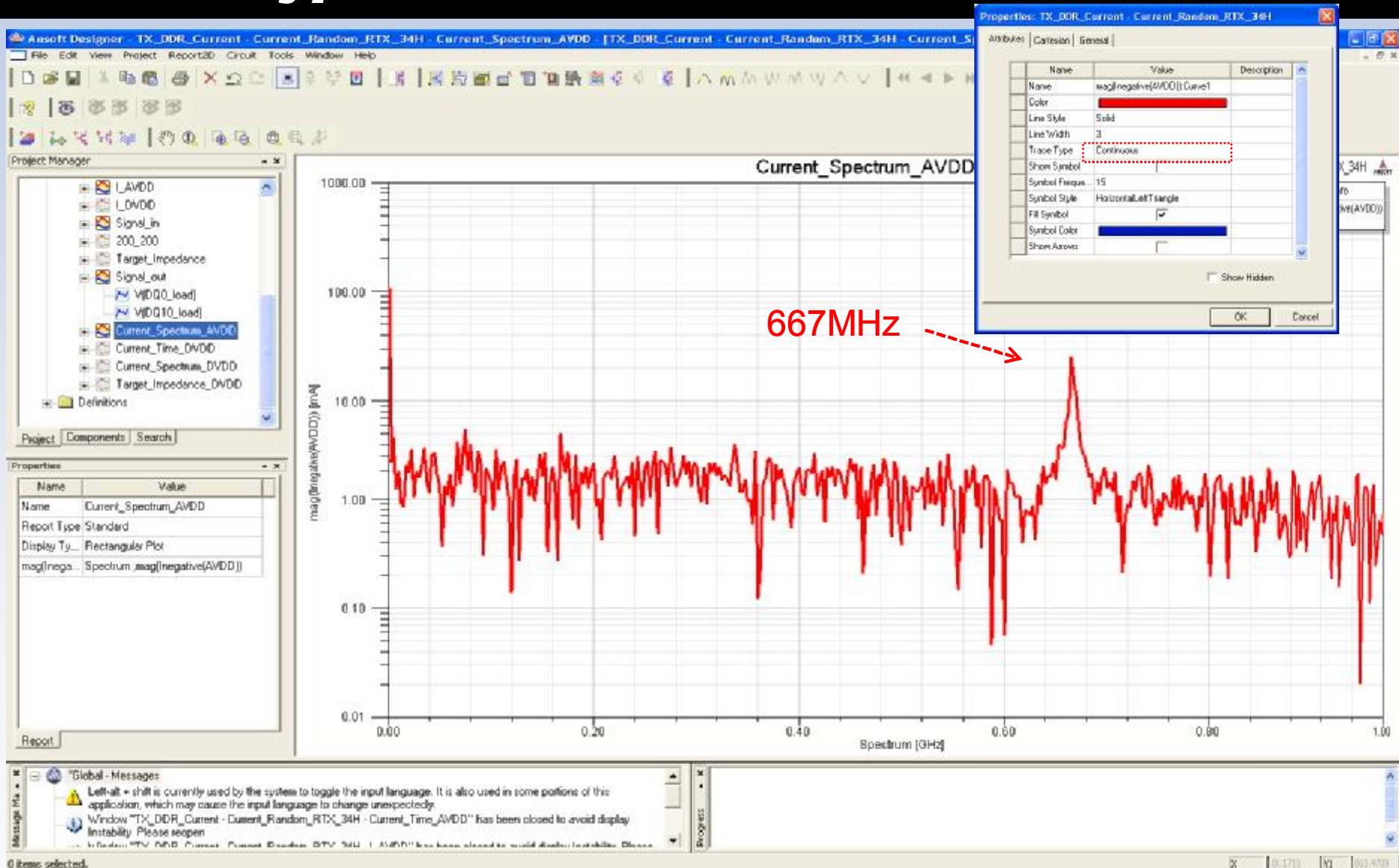
# Signal Output



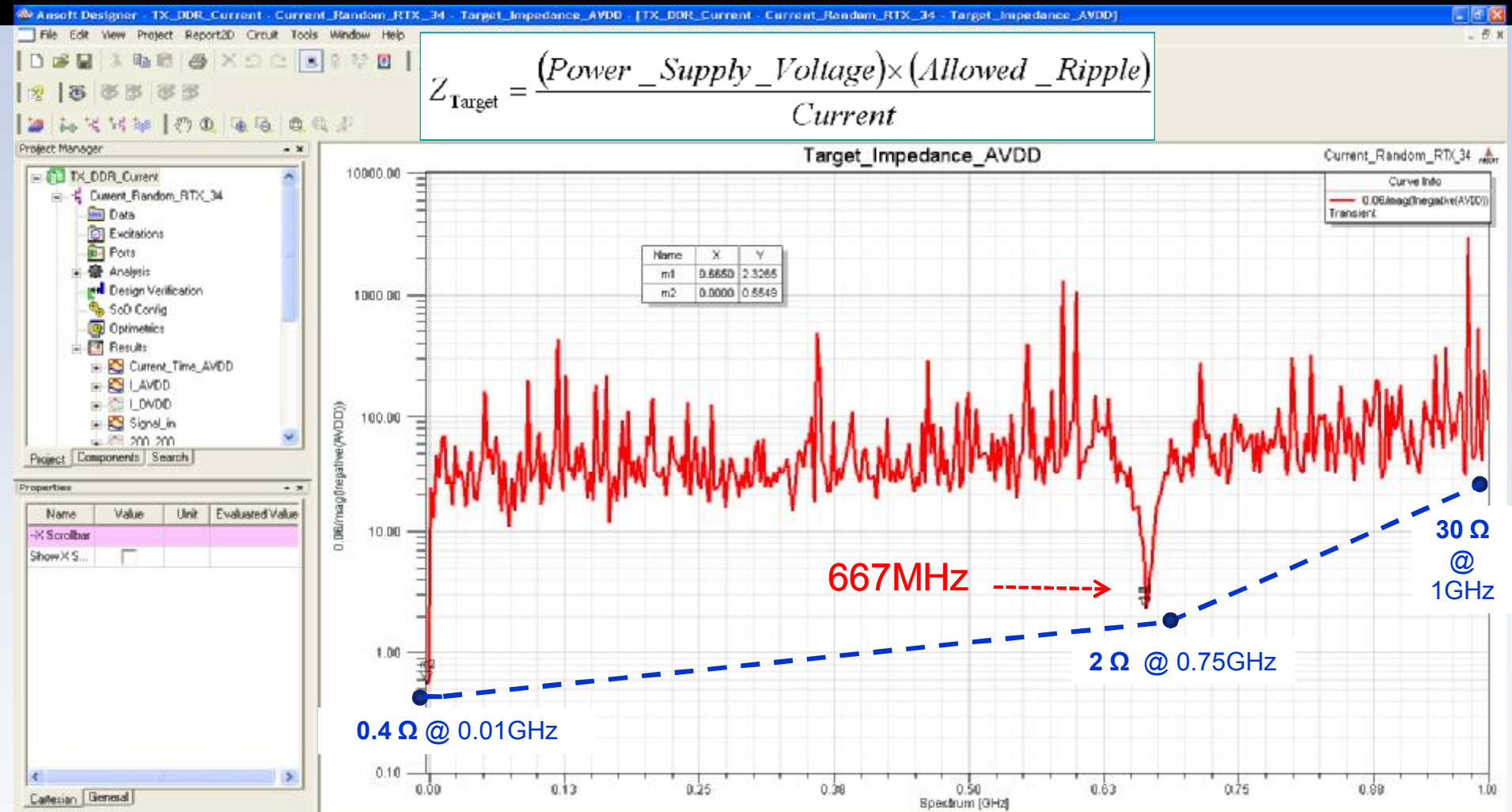
# Simulation Results – Time domain Current Profile



# Current Spectrum output Trace type - Continuous



# Adaptive Target Impedance

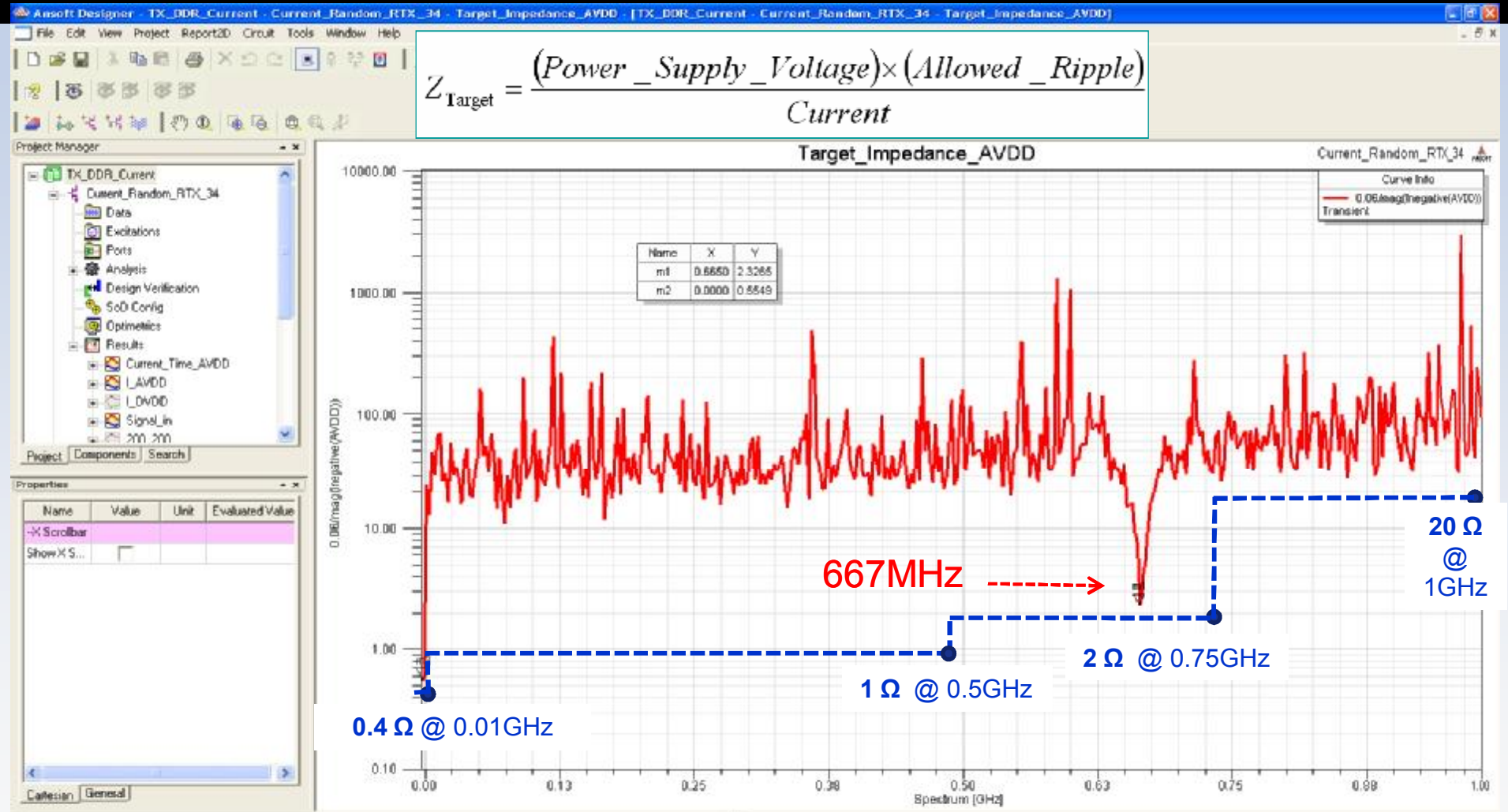


Vcc = 1.2V ± 5% variation ∴ ΔVcc = 0.06 V

**Adaptive Target Impedance design specifications**



# Or .... Adaptive Target Impedance



Vcc = 1.2V ± 5% variation ∴ ΔVcc = 0.06 V

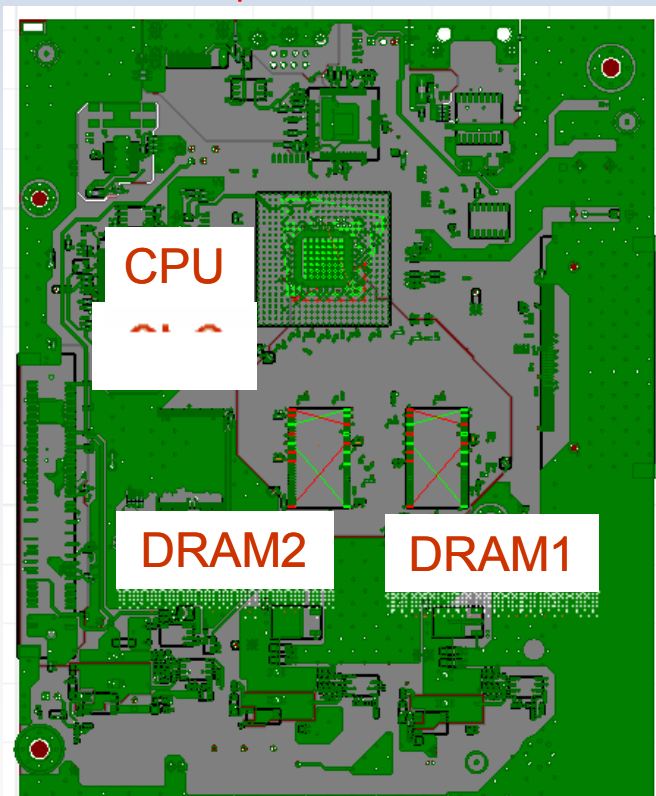
**Adaptive Target Impedance design specifications**

# PCB Layer Structure



- High-speed signals are routed between CPU and DRAM
  - Minimize noise voltage distribution on the VCC/GND plane pair
    - Design of this Power/Ground plane is the most important aspect of design
  - Low power bus impedance over frequency

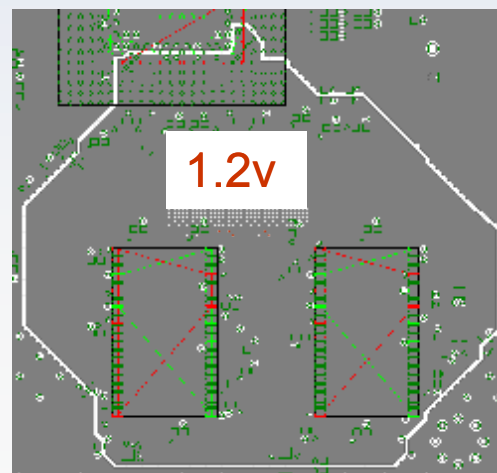
3 ports defined



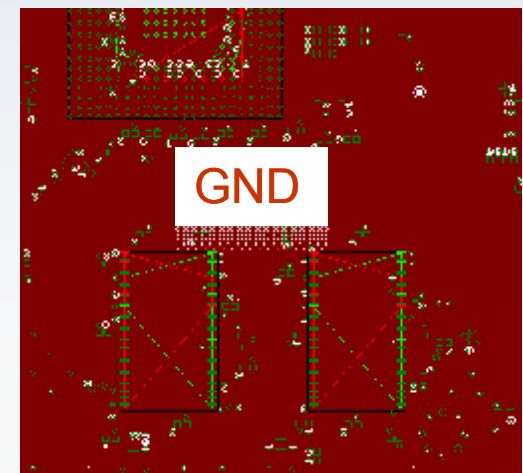
Layers	
<input type="checkbox"/> SURFACE	<input checked="" type="checkbox"/> <input checked="" type="checkbox"/> <input checked="" type="checkbox"/> <input checked="" type="checkbox"/> <input checked="" type="checkbox"/> <input checked="" type="checkbox"/>
<input type="checkbox"/> VCC	<input checked="" type="checkbox"/> <input checked="" type="checkbox"/> <input checked="" type="checkbox"/> <input checked="" type="checkbox"/> <input checked="" type="checkbox"/> <input checked="" type="checkbox"/>
<input type="checkbox"/> GND	<input checked="" type="checkbox"/> <input checked="" type="checkbox"/> <input checked="" type="checkbox"/> <input checked="" type="checkbox"/> <input checked="" type="checkbox"/> <input checked="" type="checkbox"/>
<input type="checkbox"/> BASE	<input checked="" type="checkbox"/> <input checked="" type="checkbox"/> <input checked="" type="checkbox"/> <input checked="" type="checkbox"/> <input checked="" type="checkbox"/> <input checked="" type="checkbox"/>

4 Layer PCB  
Board Size : 5.3" x 6.5"  
(13.5cm x 16.5cm)

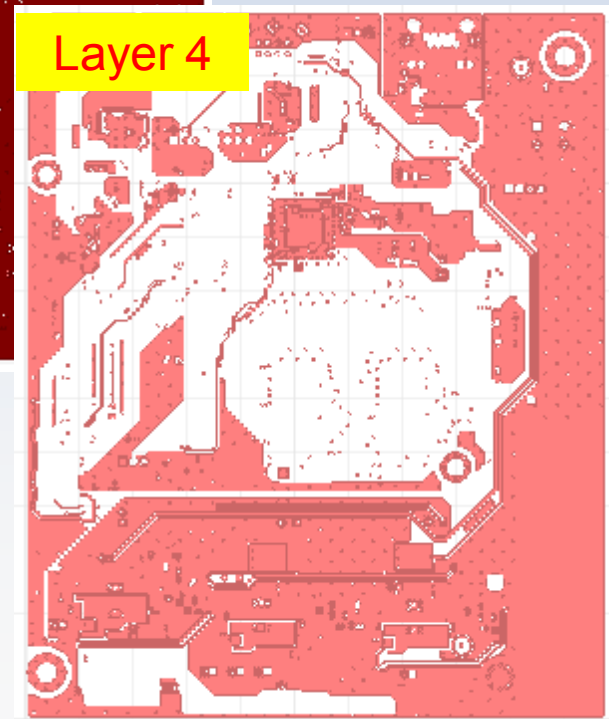
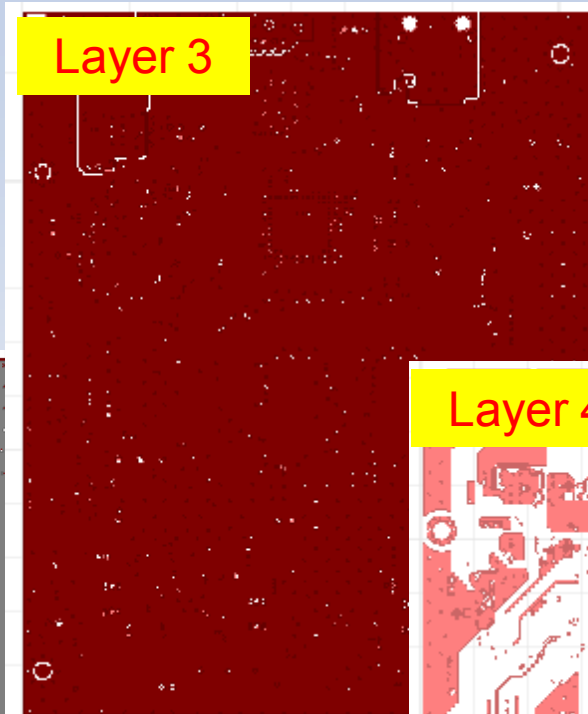
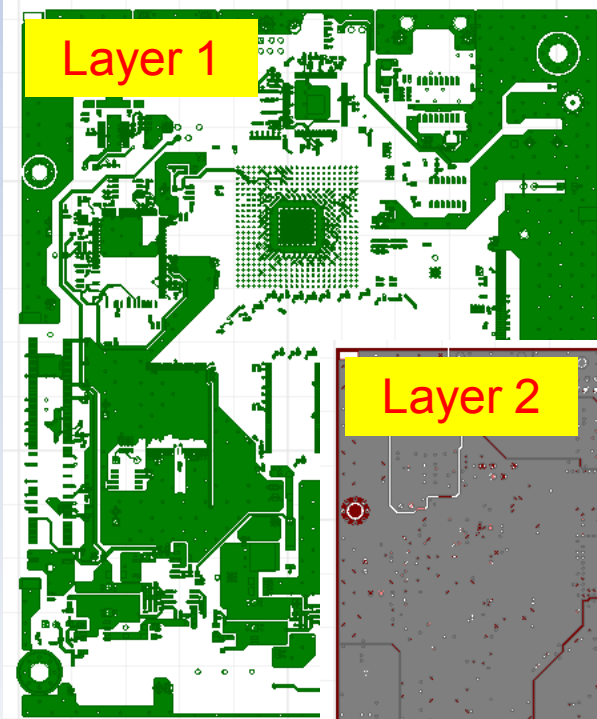
Power Plane



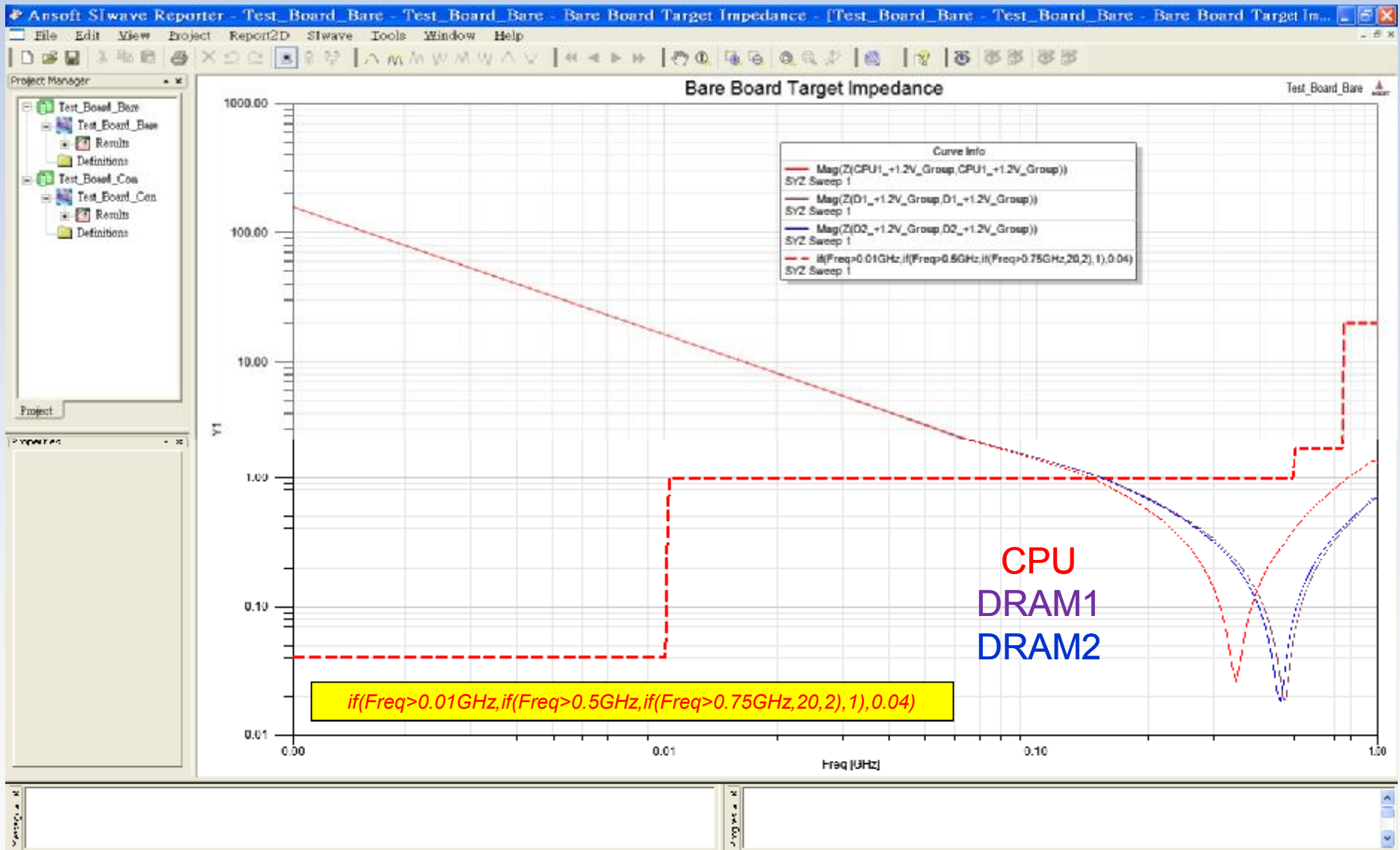
Ground Plane



# PCB Layer Structure



# Bare Board Impedance



# Original Design All 1.2V to GND 36 Capacitors ON



Original Design -  
Total 36 Caps

## Types of Capacitors

- GRM21BC70G106ME45
- GRM21BF51A225ZA01
- GRM21BF51H224ZA01
- GRM21BR71E104KA01
- GRM216F51H103ZA01
- GRM216F51H224ZA01
- GRM1885C1H201JA01
- GRM1885C1H820JA01

Active	C/F	Part Number	RefDes	Capacitance (F)	Parasitic L (H)	Parasitic R (ohms)	Positive	Negative
Yes	X	GRM1885C1H820JA01	C1	8.2E-11	7.00689E-10	0.155633	+1.2V	GND
Yes	X	GRM188R71H221KA01	C2	2.2E-10	5.22762E-10	0.964207	+1.2V	GND
Yes	X	GRM1885C1H201JA01	C3	2E-10	7.63124E-10	0.121881	+1.2V	GND
Yes	X	GRM21BF51A225ZA01	C4	2.2E-06	3.4867E-10	0.00433996	+1.2V	GND
Yes	X	GRM188F51C225ZA01	C5	2.2E-06	4.00639E-10	0.00796341	+1.2V	GND
Yes	X	GRM21BF51A225ZA01	C6	2.2E-06	3.4867E-10	0.00433996	+1.2V	GND
Yes	X	GRM21BF51A225ZA01	C7	2.2E-06	3.4867E-10	0.00433996	+1.2V	GND
Yes	X	GRM21BF51A225ZA01	C8	2.2E-06	3.4867E-10	0.00433996	+1.2V	GND
Yes	X	GRM21BF51A225ZA01	C9	2.2E-06	3.4867E-10	0.00433996	+1.2V	GND
Yes	X	GRM1885C1H561JA01	C11	5.6E-10	5.8294E-10	0.0910925	GND	+1.2V
Yes	X	GRM21BR71E104KA01	C12	1E-07	5.00196E-10	0.0194763	GND	+1.2V
Yes	X	GRM1885C1H820JA01	C13	8.2E-11	7.00689E-10	0.155633	GND	+1.2V
Yes	X	GRM21BF51A225ZA01	C14	2.2E-06	3.4867E-10	0.00433996	+1.2V	GND
Yes	X	GRM2165C1H202JA01	C15	2E-09	5.80278E-10	0.0555069	+1.2V	GND
Yes	X	GRM188R60J474KA01	C16	4.7E-07	5.35164E-10	0.00913529	+1.2V	GND
Yes	X	GRM216F51H102ZA01	C17	1E-09	4.96929E-10	0.293964	+1.2V	GND
Yes	X	GRM21BR71E104KA01	C18	1E-07	5.00196E-10	0.0194763	GND	+1.2V
Yes	X	GRM1885C1H910JA01	C19	9.1E-11	6.56454E-10	0.143556	GND	+1.2V
Yes	X	GRM1885C1H101JA01	C20	1E-10	8.22615E-10	0.203464	GND	+1.2V
Yes	X	GRM21BR61A475KA73	C21	4.7E-06	2.98349E-10	0.00361006	+1.2V	GND
Yes	X	GRM216F51H224ZA01	C22	2.2E-07	4.73639E-10	0.0292659	+1.2V	GND
Yes	X	GRM216F51H224ZA01	C49	2.2E-07	4.73639E-10	0.0292659	+1.2V	GND
Yes	X	GRM21BF51H224ZA01	C51	2.2E-07	5.88749E-10	0.0214453	+1.2V	GND
Yes	X	GRM216F51A334ZA01	C52	3.3E-07	6.0008E-10	0.0204213	+1.2V	GND
Yes	X	GRM216F51H103ZA01	C181	1E-08	6.60515E-10	0.0822853	+1.2V	GND
Yes	X	GRM216F51H103ZA01	C170	1E-08	6.60515E-10	0.0822853	+1.2V	GND
Yes	X	GRM216F51H103ZA01	C180	1E-08	6.60515E-10	0.0822853	+1.2V	GND
Yes	X	GRM216F51H103ZA01	C167	1E-08	6.60515E-10	0.0822853	+1.2V	GND
Yes	X	GRM1885C1H121JA01	C43	1.2E-10	8.07155E-10	0.194051	+1.2V	GND
Yes	X	GRM21BF51A225ZA01	C45	2.2E-06	3.4867E-10	0.00433996	+1.2V	GND
Yes	X	GRM21BR71E104KA01	C46	1E-07	5.00196E-10	0.0194763	+1.2V	GND
Yes	X	GRM1885C1H820JA01	C47	8.2E-11	7.00689E-10	0.155633	+1.2V	GND
Yes	X	GRM1885C1H820JA01	C48	8.2E-11	7.00689E-10	0.155633	+1.2V	GND
Yes	X	GRM2165C1H302JA01	C312	3E-09	5.98851E-10	0.0441419	GND	+1.2V
Yes	X	GRM21BC70G106ME45	C316	1E-05	2.44875E-10	0.00293246	GND	+1.2V
Yes	X	GRM188R71H271KA01	C317	2.7E-10	5.51632E-10	0.813567	GND	+1.2V
No	X	GRM21BR71E104KA01	C26	1E-07	5.00196E-10	0.0194763	GND	AVDD
No	X	GRM21BR71E104KA01	C27	1E-07	5.00196E-10	0.0194763	PLLVC	GND
No	X	GRM21BR71E104KA01	C28	1E-07	5.00196E-10	0.0194763	PLLVC	GND
No	X	GRM21BR71E104KA01	C29	1E-07	5.00196E-10	0.0194763	GND	+3.3V

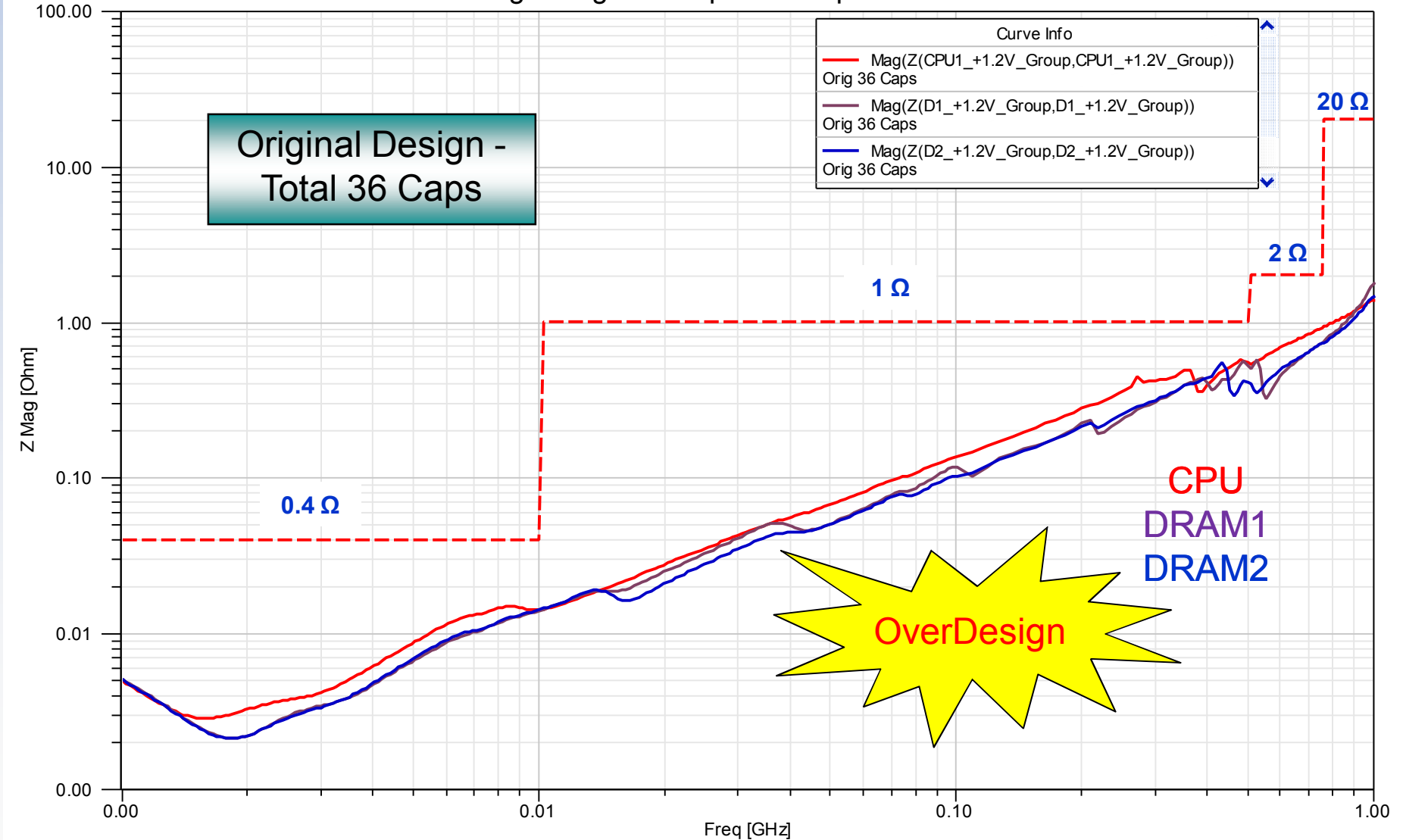
# Original Design All 36 Capacitors Enabled



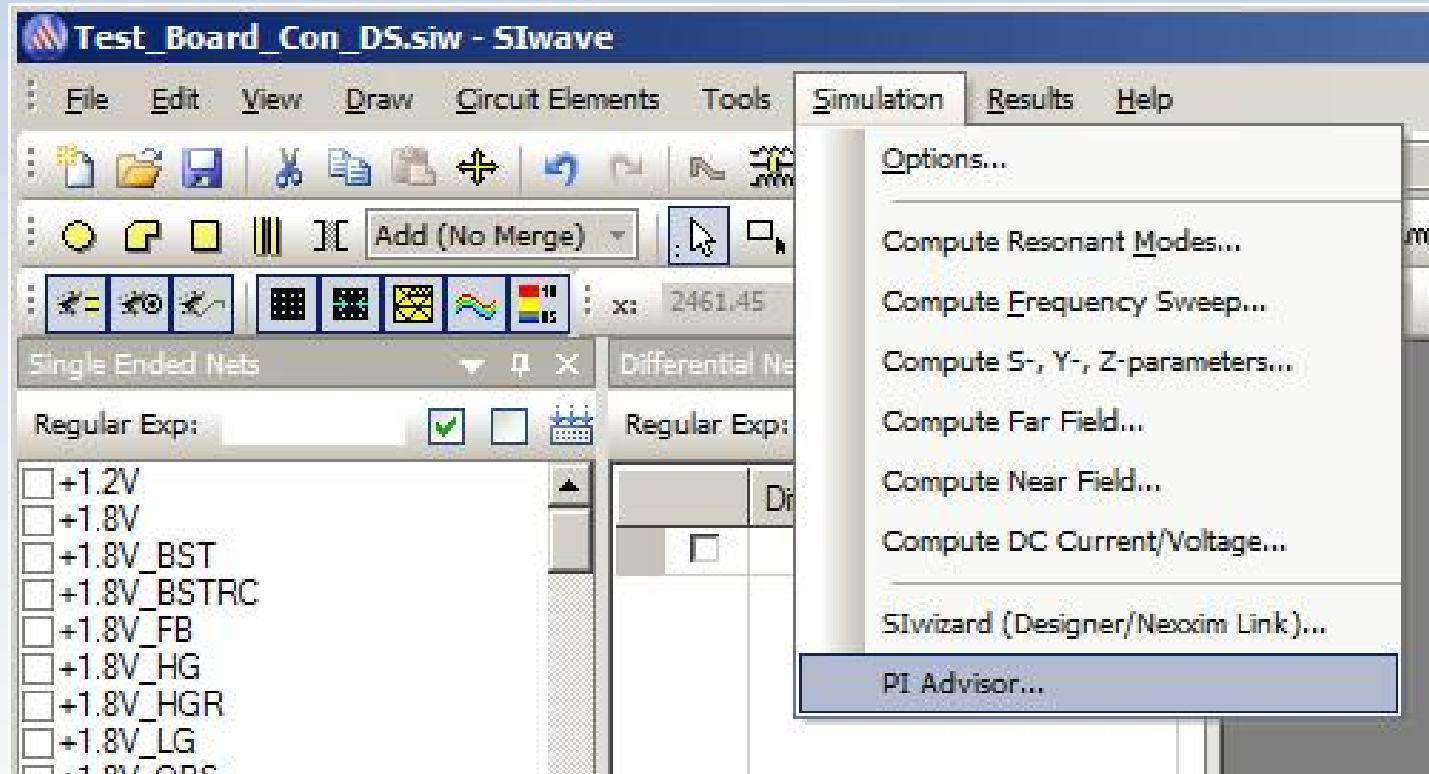
Ansoft LLC

Orig Design 36 Caps On - Z profiles

Test\_Board\_Con\_PI\_DS\_90fit



# Launch SIwave PI Advisor...



# Step 1 : Define Ports and Target Impedance Profile



## • PI Advisor

- Select Reference Port Locations
- Set the VRM Parameters including ESL & ESR
- Define Impedance Mask

The screenshot displays the ANSYS PI Advisor Wizard Step 1 interface. On the left, a table lists ports for selection:

Port	Enforce (Z)
CPU1_+1.2V...	<input checked="" type="checkbox"/>
D1_+1.2V_G...	<input checked="" type="checkbox"/>
D2_+1.2V_G...	<input checked="" type="checkbox"/>
VRM	<input type="checkbox"/>

A red dashed box highlights this table, with the word "Ports" written below it. The main window shows a plot of "Impedance magnitude at port CPU1\_+1.2V\_Group" with the y-axis labeled  $|Z_{11}|$  [ohms] and the x-axis labeled Frequency [MHz]. The plot shows several curves representing different components, with a red curve indicating the target impedance profile. Below the plot, the "VRM Parameters" section shows "Location: VRM" and "ESL: 5.000e-07 H" and "ESR: 5.000e-01 ohms". To the right, the "Required  $|Z_{11}|$ " table is highlighted with a red dashed box:

Start (MHz)	End (MHz)	Target $ Z_{11} $ (ohms)
0.01	10	0.4
10	500	1
500	750	2
750	1000	20

At the bottom, a WordPad window titled "1v2.zprof - WordPad" displays the generated impedance profile:

```
B_IMPEDANCE_PROFILE 14
1E+04 0.4
1E+07 0.4
1E+07 1
5E+08 1
5E+08 2
7.5E+08 2
7.5E+08 20
1E+09 20
E_IMPEDANCE_PROFILE
```

A red arrow points from the "Required  $|Z_{11}|$ " table to the WordPad window. The bottom of the wizard shows "VRM ESL/ESR Model Tuning" options and "Plot VRM output impedance in" and "Plot total  $|Z_{11}|$  at ports" dropdowns. The "Next" and "Cancel" buttons are visible at the bottom right.

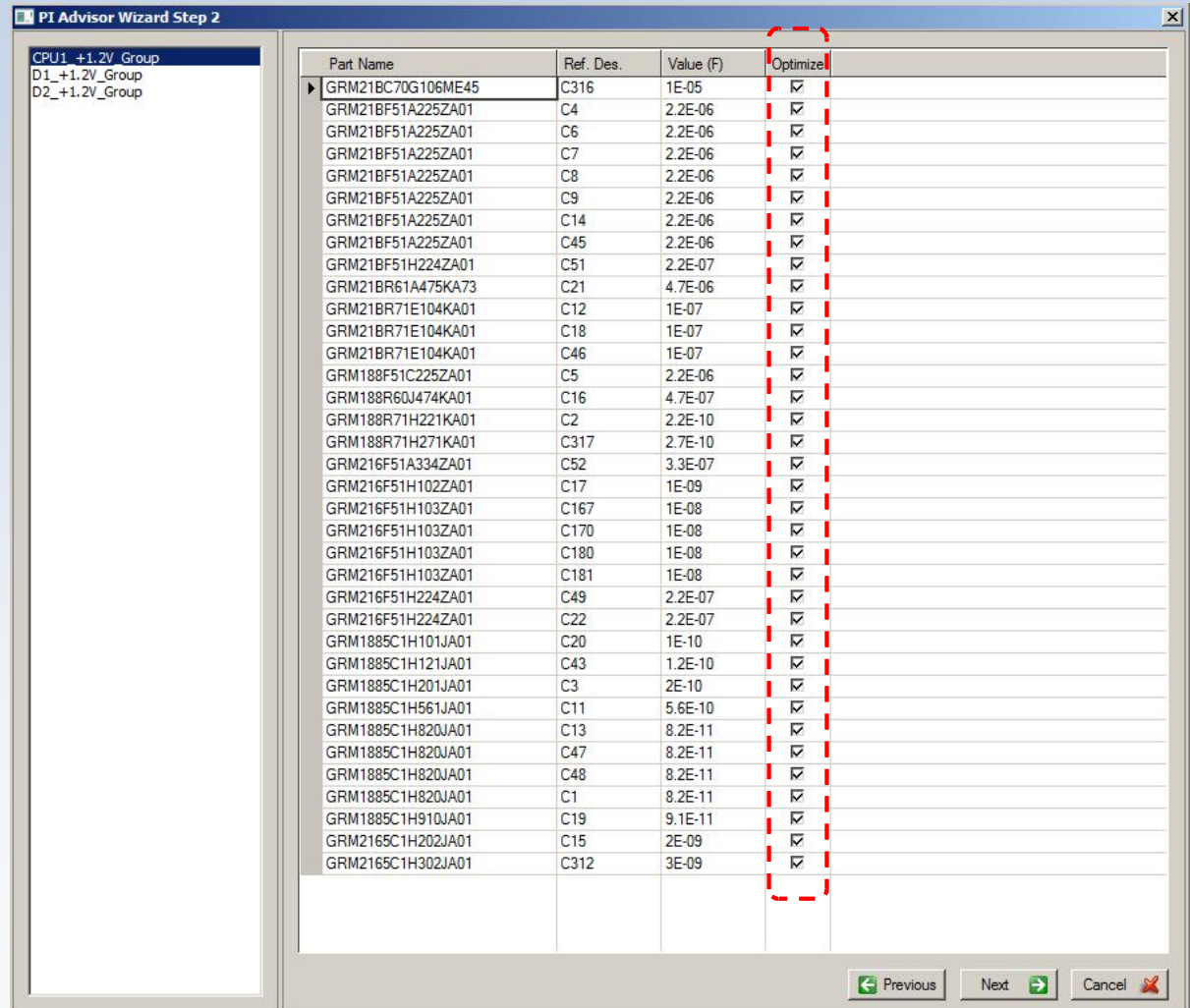


# Step 2 : Select Capacitors for Automated Optimization



## • PI Advisor

- Select Capacitor set that needs to be optimized
- All 36 caps selected



# Step 3 : Select Candidate Capacitors for Optimization



PI Advisor Wizard Step 3

Capacitors Selected for Optimization

Part Name	Ref. Des.	Val
GRM21BF51A225ZAD1	C3	2.2
GRM21BF51H224ZAD1	C51	2.2
GRM21BF51H224ZAD1	C53	2.2
GRM21BF51H224ZAD1	C2	2.2
GRM21BR71E104KA01	C11	1E
GRM21BR71E104KA01	C12	1E
GRM21BR71E104KA01	C13	1E
GRM21BR71E104KA01	C18	1E
GRM21BR71E104KA01	C19	1E
GRM21BR71E104KA01	C46	1E
GRM21BR71E104KA01	C20	1E
GRM21BF51H103ZAD1	C180	1E
GRM21BF51H103ZAD1	C170	1E
GRM21BF51H103ZAD1	C167	1E
GRM21BF51H103ZAD1	C182	1E
GRM21BF51H103ZAD1	C181	1E
GRM21BF51H224ZAD1	C49	2.2
GRM21BF51H224ZAD1	C50	2.2
GRM21BF51H224ZAD1	C22	2.2
GRM1885C1H201JA01	C58	2E
GRM1885C1H201JA01	C56	2E
GRM1885C1H820JA01	C47	B.2
GRM1885C1H820JA01	C48	B.2
GRM1885C1H820JA01	C52	B.2
GRM1885C1H820JA01	C55	B.2
GRM1885C1H820JA01	C4	B.2

Assigned Candidate Models

Vendor	Series	Part Name
Murata	GRM21	GRM219R71C474KA01
Murata	GRM21	GRM219R71C564KA01
Murata	GRM21	GRM219R71C684KA01
Murata	GRM21	GRM219R71E104KA88
Murata	GRM21	GRM219R71E224KA01
Murata	GRM21	GRM219R71H333KA01
Murata	GRM21	GRM219R71H354KA88
Murata	GRM21	GRM219R71H393KA01
Murata	GRM21	GRM2165C1H102JA01

Impedance

Vendor	Series	Part Name	Plot	Candidate	Value (F)	EIA Size	Cost	SRF (Hz)	S_min (dB)	ESR (ohm)	ESL
Kemet	T495T	T495T107M2R5ATE3K0	<input type="checkbox"/>	Add	0.0001	1310	0.01	2.14457E+06	-47.4703	0.428316	5.1
Kemet	T495V	T495V107M006ATE090	<input type="checkbox"/>	Add	0.0001	2816	0.01	1.01711E+06	-67.9009	0.0419364	2.4
Kemet	T495V	T495V107M006ATE150	<input type="checkbox"/>	Add	0.0001	2816	0.01	1.01621E+06	-63.1919	0.0701273	1.1
Kemet	T495V	T495V107M010ATE150	<input checked="" type="checkbox"/>	Add	0.0001	2816	0.01	1.23645E+06	-66.0949	0.0512289	1.6
Kemet	T495V	T495V107M016ATE060	<input type="checkbox"/>	Add	0.0001	2816	0.01	977202	-70.1426	0.0323189	2.6
Kemet	T495V	T495V157M006ATE070	<input checked="" type="checkbox"/>	Add	0.00015	2816	0.01	898901	-68.9281	0.037397	2.0
Kemet	T495V	T495V157M010ATE100	<input type="checkbox"/>	Add	0.00015	2816	0.01	1.16947E+06	-66.5008	0.0471178	1.3

Filters

Vendor	Show	Series	Show	EIA Size	Show	Filter	Quantity	Min	Max
AVX	<input checked="" type="checkbox"/>	0201	<input checked="" type="checkbox"/>	01005	<input checked="" type="checkbox"/>	<input type="checkbox"/> Value (F)		1E-13	0.0015
Kemet	<input checked="" type="checkbox"/>	0306	<input checked="" type="checkbox"/>	0201	<input checked="" type="checkbox"/>	<input type="checkbox"/> SRF Range (Hz)		0	2.10375E+10
Murata	<input checked="" type="checkbox"/>	0402	<input checked="" type="checkbox"/>	0306	<input checked="" type="checkbox"/>	<input type="checkbox"/> S_min Range (dB)		-106.911	-7.97224
Panasonic	<input checked="" type="checkbox"/>	0508	<input checked="" type="checkbox"/>	0402	<input checked="" type="checkbox"/>	<input type="checkbox"/> ESR Range (ohms)		4.99788E-06	593486
Samsung	<input checked="" type="checkbox"/>	0603	<input checked="" type="checkbox"/>	0508	<input checked="" type="checkbox"/>	<input type="checkbox"/> ESL Range (nH)		0	0.451721
TDK	<input checked="" type="checkbox"/>	0612	<input checked="" type="checkbox"/>	0603	<input checked="" type="checkbox"/>	<input type="checkbox"/> Cost (\$)		0	0.01
YUJIDEN	<input checked="" type="checkbox"/>	0805	<input checked="" type="checkbox"/>	0612	<input checked="" type="checkbox"/>				
		1206	<input checked="" type="checkbox"/>	0805	<input checked="" type="checkbox"/>				

Remove Plot [Z11]

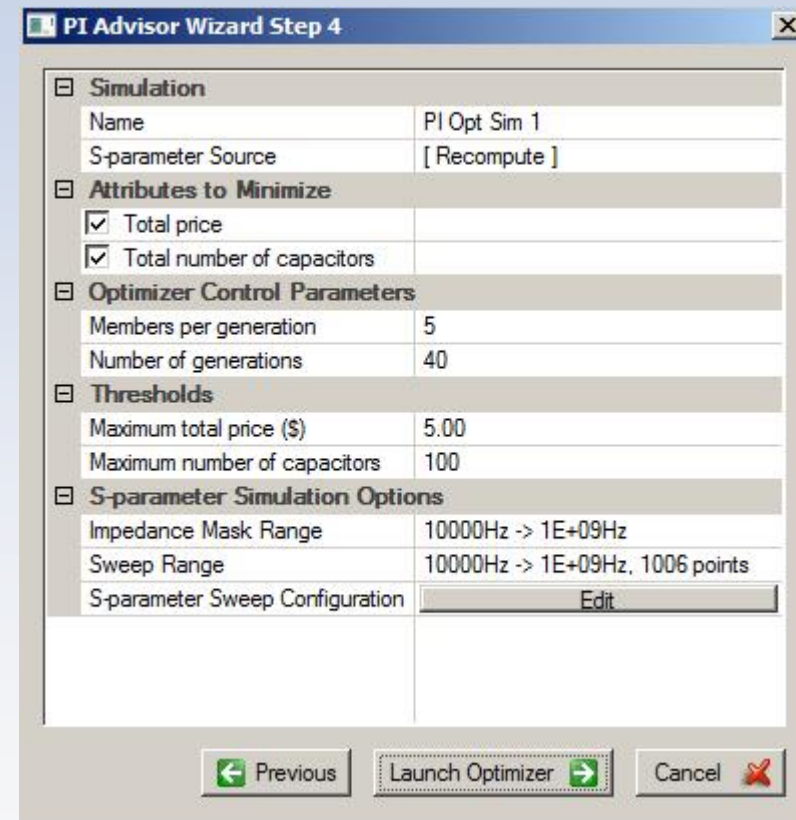
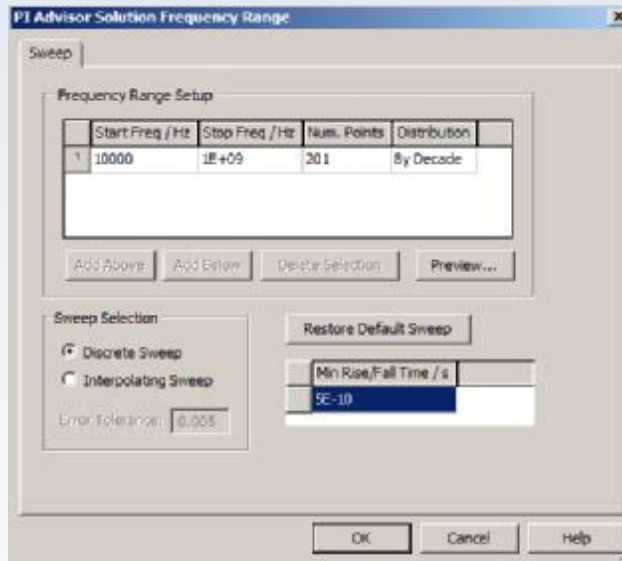
Previous Next Cancel

# Step 4 : Setup Optimization Criteria



## • PI Advisor

- Launch PI Advisor Wizard
- Set Optimizer Goal Parameters
- Set Thresholds
  - Total price \$\$\$
  - Total number of capacitors
- Genetic Algorithm is used for optimization
- SYZ sweep



# Step 5 : Launch Optimizer and Analyze Results



- Time = 2 minutes 56 seconds
- RAM = 286 MB
  - Frequency Setup
    - 10KHz < f < 1GHz
    - 201 Points/decade
  - Genetic Algorithm Setup
    - **Optimized for Impedance**
    - **Optimized for # of Caps**
    - **Optimized for Price**

Simulation profile for PI Opt Sim 1

Module	Real Time	CPU Time	Memory	Size
siwave_ng 5.0.0 (Built: Jul 26 2010 10:39:30) Commenced on host JAYHAWK at Tue Sep 14 08:32:07 2010				
-----				
Command	Real Time	Cpu Time	Memory	Size
geomproc	00:00:16	00:00:15	40808K	15976 triangle
solve_setup	00:00:11	00:00:08	59844K	1 project
-----				
Finished on JAYHAWK at 09/14/2010 08:32:34				
SIwave 5.0.0 Jul 27 2010 at 02:54:47 beginning H:\ANSOFT\SIwave5\ansoftbin64\siwave_solver.exe on JAYHAWK at 09/14/2010 08:32:34				
Command	Real Time	Cpu Time	Memory	Number of Elements
geomproc	00:00:07	00:00:06	40884K	16022 triangle
xsec_solve	00:00:46	00:01:21	151396K	689 xsections
via_extract	00:00:06	00:00:10	165444K	196 blocks
bsm_adapt	00:00:03	00:00:03	165444K	27790 triangles
Interpolating discrete sweep converged after 25 solutions				
DCS_2p	00:00:08	00:00:19	286392K	44957 matrix
SIwave	00:01:20	00:01:13	286392K	44957 matrix
-----				
Finished on JAYHAWK at 09/14/2010 08:35:04				

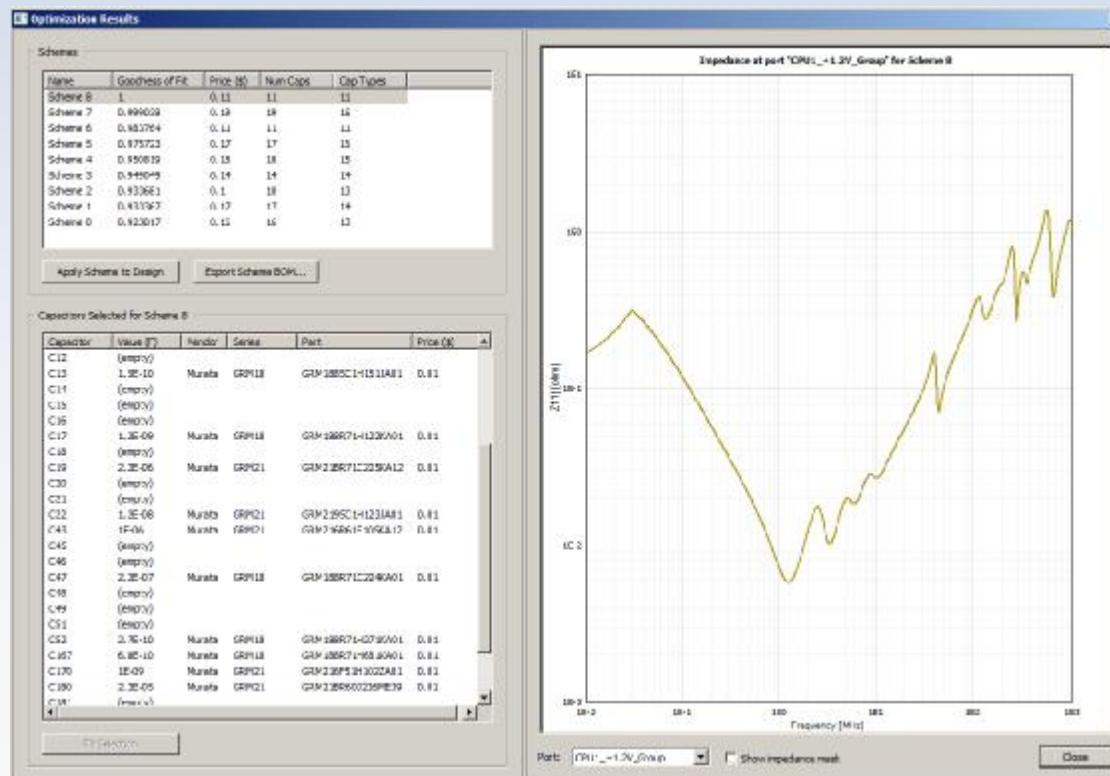
Save As... Close

# PI Advisor – Step 5



## PI Advisor Results

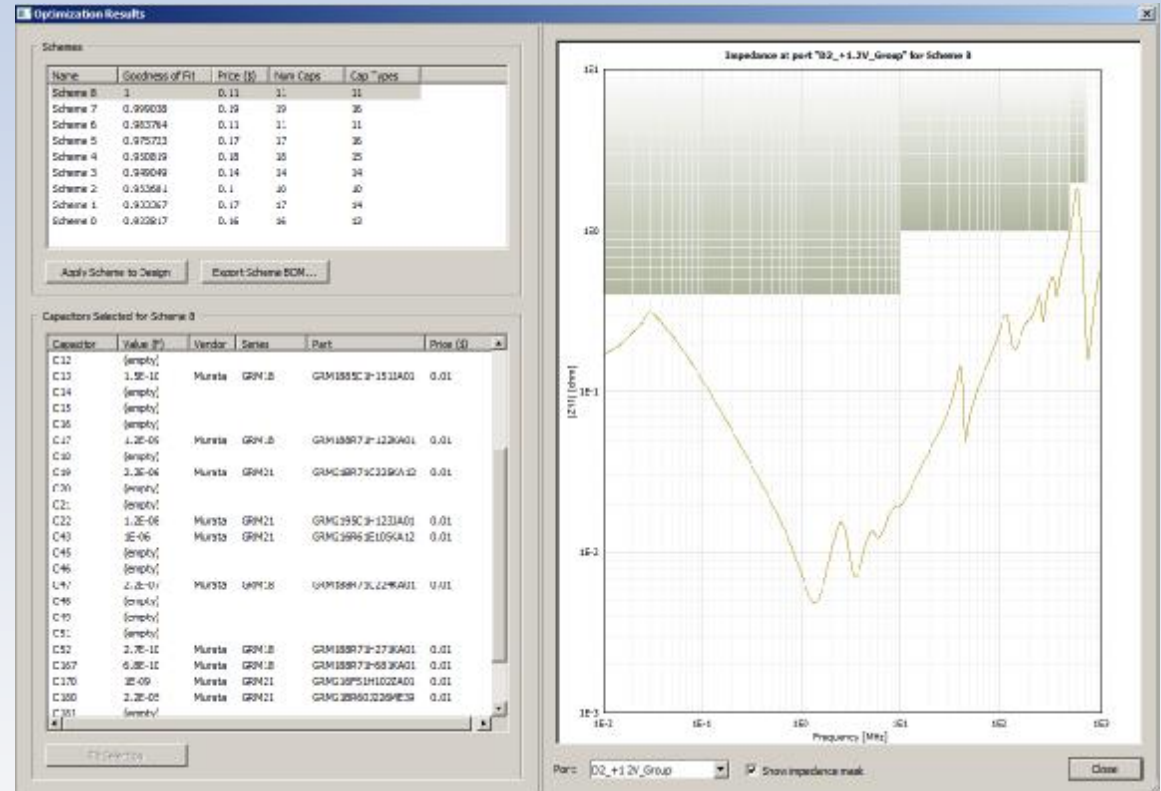
- PI Advisor provides multiple different Schemes
- Sort solutions by **Price (\$)**, **Num Caps** and **Goodness of Fit**
- You can display Impedance Mask . Etc
- Apply optimized capacitor scheme to the existing design
- Export BOM file back to layout database



# Step 5 : Launch Optimizer and Analyze Results



- Original solution
  - Total # Caps: 36
- Optimized Solution
  - Total # Caps: from 10 to 19
  - 9 Schemes available
  - 6 Capacitor Types: 10 to 16



# PI Advisor Simulation Results

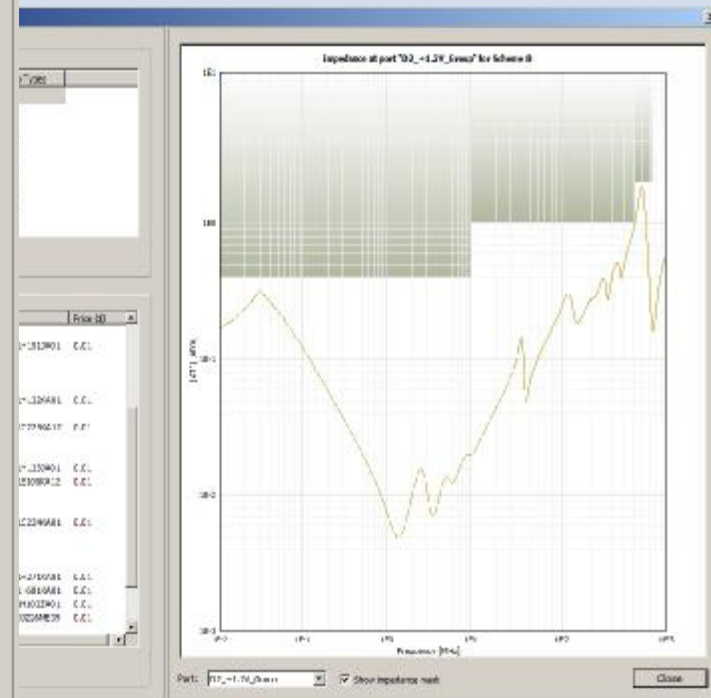


- **Scheme 8 Capacitors Selection information**
  - 11 capacitors and 11 different types

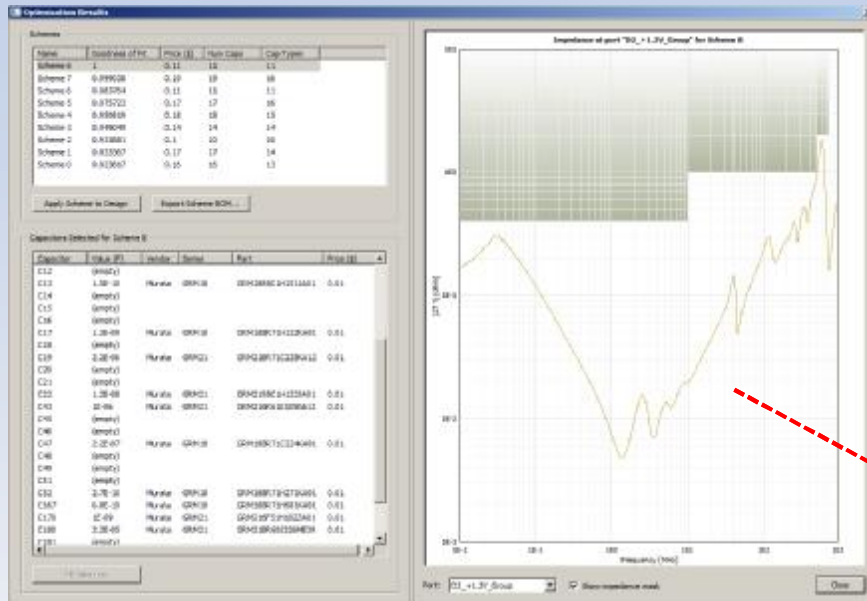
Capacitors Selected for Scheme 8

Capacitor	Value (F)	Vendor	Series	Part	Price (\$)
C12	(empty)				
C13	1.5E-10	Murata	GRM18	GRM1885C1H151JA01	0.01
C14	(empty)				
C15	(empty)				
C16	(empty)				
C17	1.2E-09	Murata	GRM18	GRM188R71H122KA01	0.01
C18	(empty)				
C19	2.2E-06	Murata	GRM21	GRM21BR71C225KA12	0.01
C20	(empty)				
C21	(empty)				
C22	1.2E-08	Murata	GRM21	GRM2195C1H123JA01	0.01
C43	1E-06	Murata	GRM21	GRM216R61E105KA12	0.01
C45	(empty)				
C46	(empty)				
C47	2.2E-07	Murata	GRM18	GRM188R71C224KA01	0.01
C48	(empty)				
C49	(empty)				
C51	(empty)				
C52	2.7E-10	Murata	GRM18	GRM188R71H271KA01	0.01
C167	6.8E-10	Murata	GRM18	GRM188R71H681KA01	0.01
C170	1E-09	Murata	GRM21	GRM216F51H102ZA01	0.01
C180	2.2E-05	Murata	GRM21	GRM21BR60J226ME39	0.01
C181	(empty)				

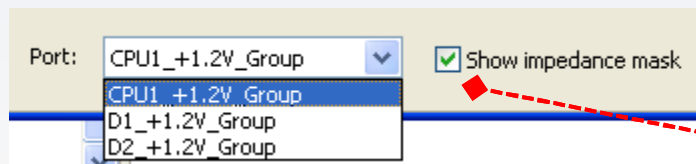
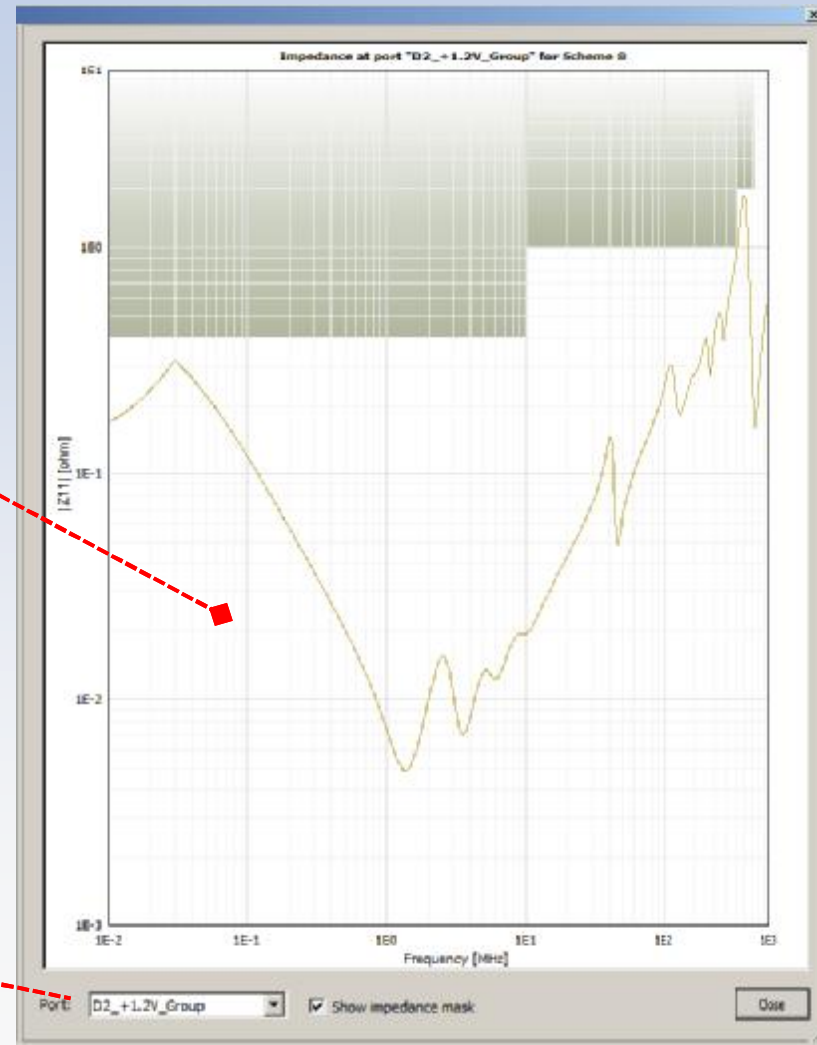
Fit Selection



# PI Advisor Simulation Results



Scheme 8 Target impedance information



Port Selection



# Scheme 8 Results – All three ports



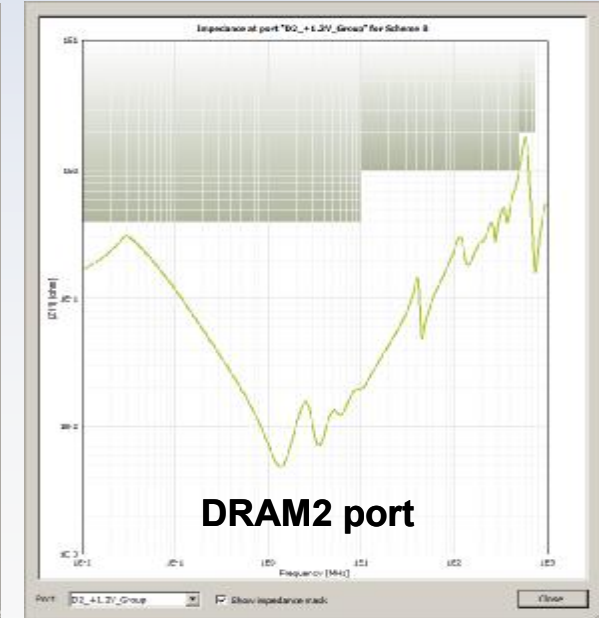
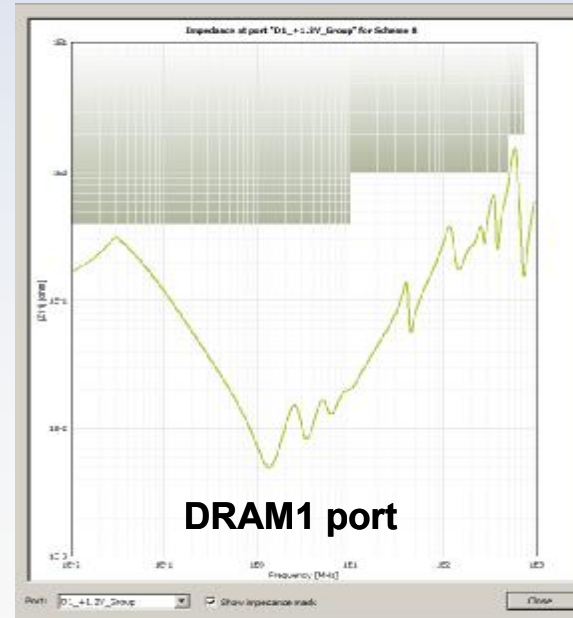
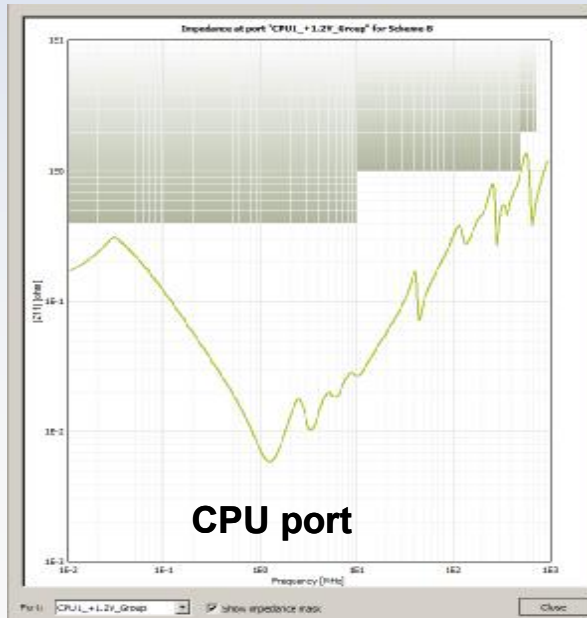
Optimization Results

Name	Goodness of Fit	Price (\$)	Num Caps	Cap Types
Scheme 8	1	0.11	11	11
Scheme 7	0.999038	0.19	19	16
Scheme 6	0.983764	0.11	11	11
Scheme 5	0.975723	0.17	17	16
Scheme 4	0.950819	0.18	18	15
Scheme 3	0.949049	0.14	14	14
Scheme 2	0.933681	0.1	10	10
Scheme 1	0.933367	0.17	17	14
Scheme 0	0.923817	0.16	16	13

Apply Scheme to Design    Export Scheme BOM...

Port: CPU1\_+1.2V\_Group  Show impedance mask

- CPU1\_+1.2V\_Group
- D1\_+1.2V\_Group
- D2\_+1.2V\_Group



# Capacitor Count Reduction



Optimization Results

Schemes

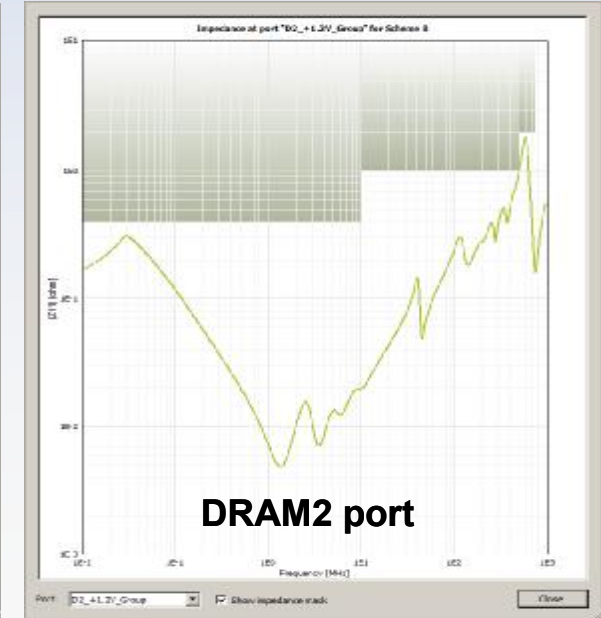
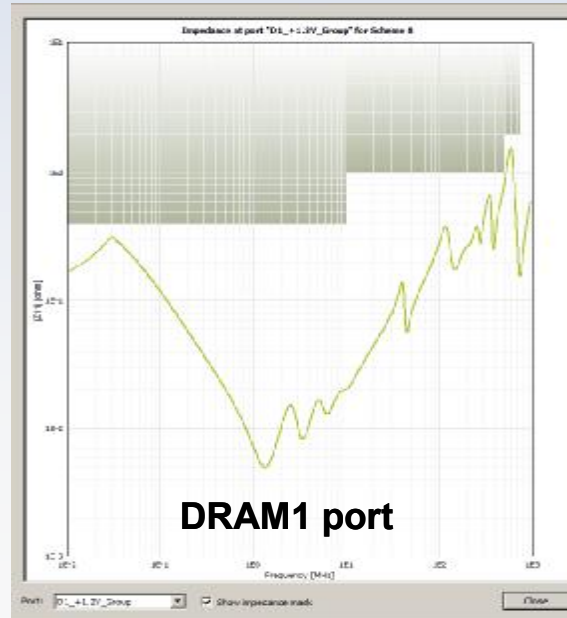
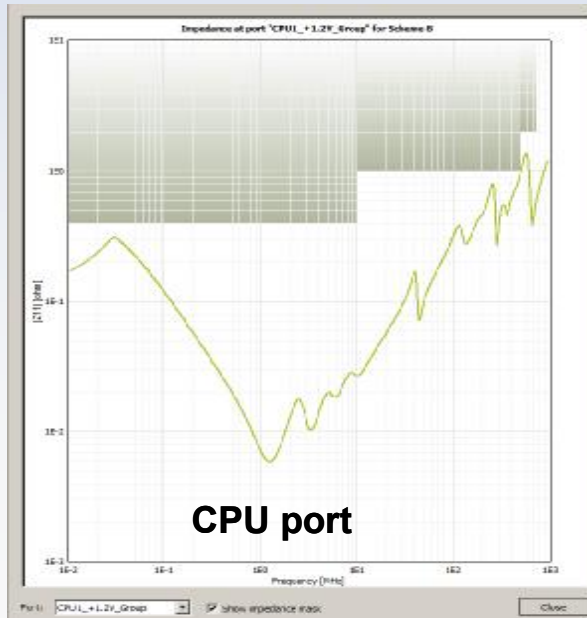
Name	Goodness of Fit	Price (\$)	Num Caps	Cap Types
Scheme 8	1	0.11	11	11
Scheme 7	0.999038	0.19	19	16
Scheme 6	0.983764	0.11	11	11
Scheme 5	0.975723	0.17	17	16
Scheme 4	0.950819	0.18	18	15
Scheme 3	0.949049	0.14	14	14
Scheme 2	0.933681	0.1	10	10
Scheme 1	0.933367	0.17	17	14
Scheme 0	0.923817	0.16	16	13

Apply Scheme to Design    Export Scheme BOM...

Original Design -  
Total of 36 Caps

New Design -  
Total of 11 Caps

Capacitor Count  
**69% Reduction**



# Apply Scheme 8 to Original Design



Optimization Results

Name	Goodness of Fit	Price (\$)	Num Caps	Cap Types
Scheme 8	1	0.11	11	13
Scheme 7	0.999038	0.19	19	16
Scheme 6	0.983764	0.11	11	11
Scheme 5	0.978723	0.17	17	18
Scheme 4	0.950819	0.18	18	15
Scheme 3	0.949049	0.14	14	14
Scheme 2	0.933681	0.1	10	10
Scheme 1	0.933367	0.17	17	14
Scheme 0	0.923817	0.16	16	13

Apply Scheme to Design    Export Scheme BOM...

Circuit Element Properties

Active	∂/∂f	Part Number	RefDes	Capacitance (F)	Parasitic L (H)	Parasitic R (ohms)	Positive "Terminal" Net	Negative "Terminal" Net
Yes	X	GRM21BR...	C19	2.2E-06	4.3452E-10	0.00438131	GND	+1.2V
Yes	X	GRM1885...	C2	2.2E-10	7.82268E-10	0.139306	+1.2V	GND
Yes	X	GRM1885...	C13	1.5E-10	7.93549E-10	0.170406	GND	+1.2V
Yes	X	GRM2195...	C22	1.2E-08	4.94251E-10	0.0232748	+1.2V	GND
Yes	X	GRM188R...	C167	6.8E-10	5.07999E-10	0.386868	+1.2V	GND
Yes	X	GRM216R...	C43	1E-06	2.84526E-10	0.0104462	+1.2V	GND
Yes	X	GRM188R...	C17	1.2E-09	4.98611E-10	0.253293	+1.2V	GND
Yes	X	GRM216F...	C170	1E-09	4.96929E-10	0.293964	+1.2V	GND
Yes	X	GRM188R...	C52	2.7E-10	5.51632E-10	0.813567	+1.2V	GND
Yes	X	GRM188R...	C47	2.2E-07	5.64599E-10	0.0252773	+1.2V	GND
Yes	X	GRM21BR...	C180	2.2E-05	2.28044E-10	0.00232623	+1.2V	GND
No	X	GRM1885...	C3	1.6E-10	7.90936E-10	0.15001	+1.2V	GND
No	X	GRM21BF...	C4	2.2E-06	3.4867E-10	0.00433996	+1.2V	GND
No	X	GRM188R...	C5	3.9E-10	5.38865E-10	0.59068	+1.2V	GND
No	X	GRM21BR...	C6	2.2E-05	2.28044E-10	0.00232623	+1.2V	GND
No	X	GRM21BF...	C7	2.2E-06	3.4867E-10	0.00433996	+1.2V	GND
No	X	GRM21BF...	C8	2.2E-06	3.4867E-10	0.00433996	+1.2V	GND
No	X	GRM21BF...	C9	2.2E-06	3.4867E-10	0.00433996	+1.2V	GND
No	X	GRM216R...	C11	1E-06	2.64868E-10	0.0105327	GND	+1.2V
No	X	GRM21BR...	C12	1E-07	5.00196E-10	0.0194763	GND	+1.2V
No	X	GRM21BF...	C14	2.2E-06	3.4867E-10	0.00433996	+1.2V	GND
No	X	GRM2165...	C15	1.6E-09	5.81412E-10	0.063323	+1.2V	GND
No	X	GRM188R...	C16	4.7E-07	5.35164E-10	0.00913529	+1.2V	GND

Modify Properties...    Modify Layers...    Delete    Fit Selection    Activate    Deactivate

Export    OK    Cancel

Circuit Element Properties auto defined !

# Re- Compute S, Y, Z parameters



Simulation name: SYZ Sweep 1

	Start Freq / Hz	Stop Freq / Hz	Num. Points	Distribution
1	1E+06	1E+08	101	By Decade
2	1E+08	1E+09	101	Linear

Sweep Selection

Discrete Sweep

Interpolating Sweep

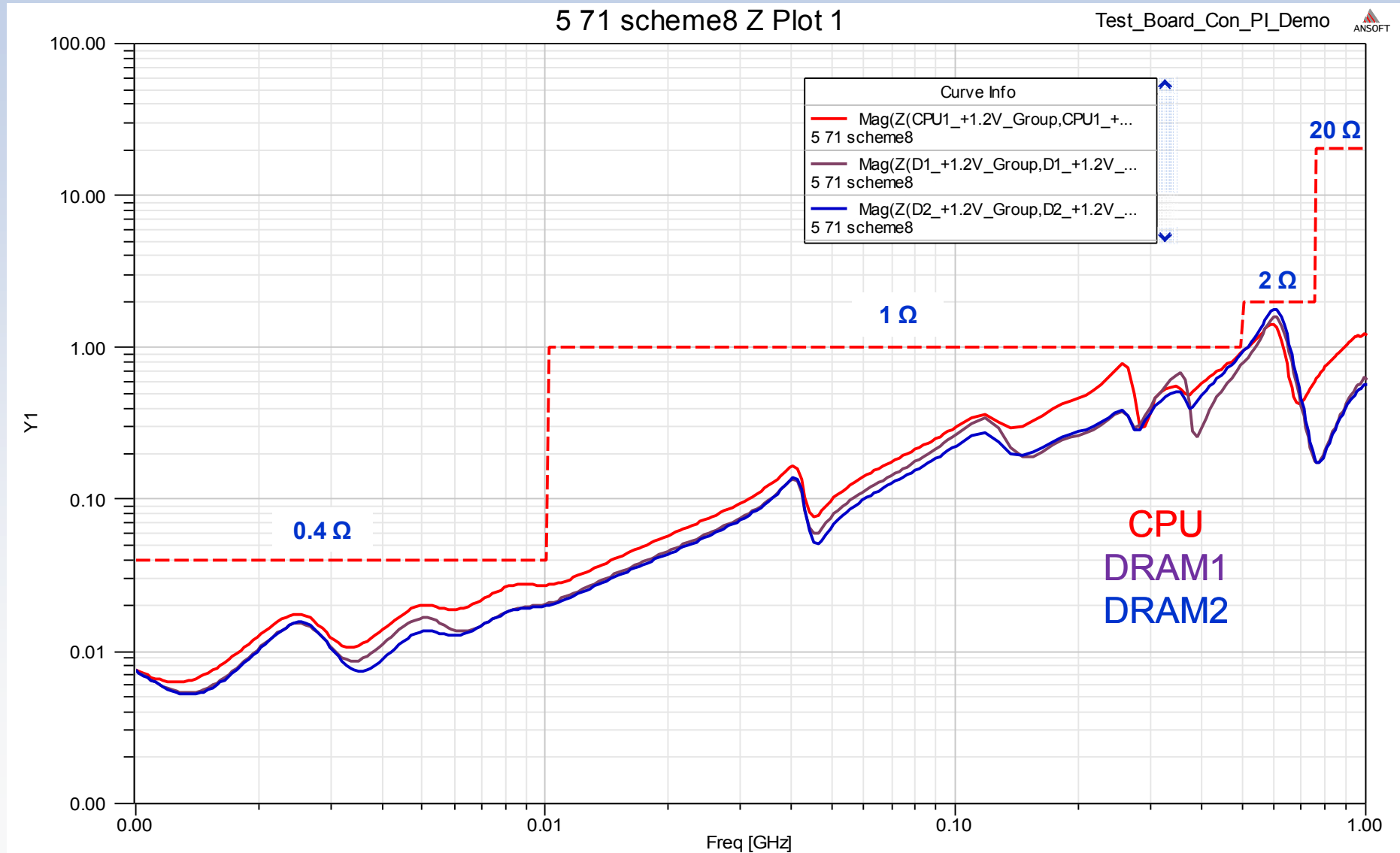
Error Tolerance: 0.005

Set FWS generation parameters

Min Rise/Fall Time / s: 5E-10

Buttons: Save Settings, OK, Cancel, Help

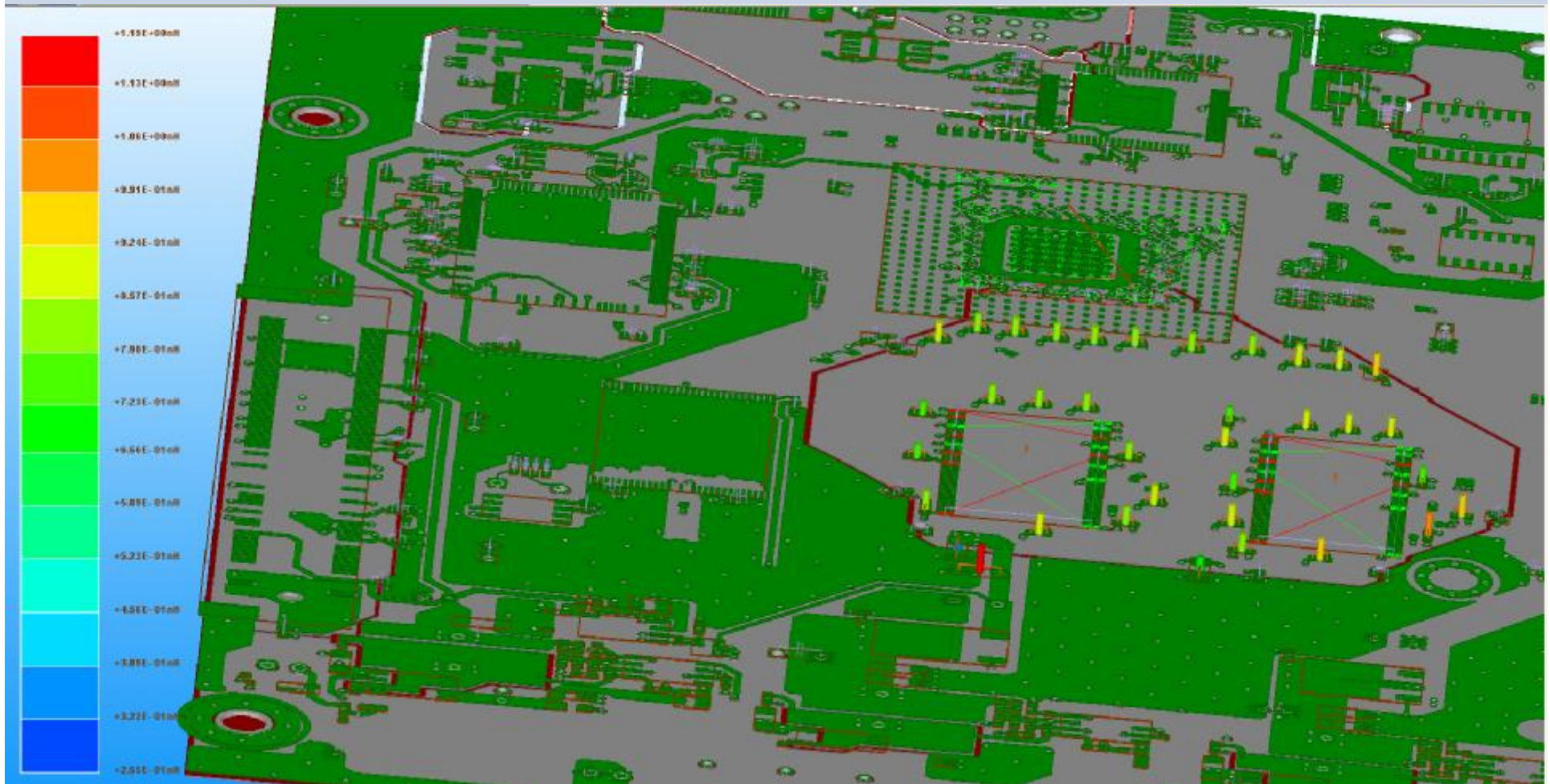
# Final Simulation Results



# Loop Inductance Plot



- Provides intuitive plot to analyze capacitor layout thereby minimizing loop inductance (all 36 caps displayed)



*\* 2005 ITRS: “Cost of design is the greatest threat to the continuation of the semiconductor roadmap... [and] design productivity... is the most massive and critical [design challenge facing the industry today].”*

*\*Source: International Technology Roadmap for Semiconductors*

## Delivering productivity:

- **Assume 4 to 5 changes per board**
  - Single PI Advisor simulation time ~ 3 min
  - Simulation time is approximately 10-15 min.
- **Result:** Your design team meets project performance requirements on time and, therefore, within budget.

- **Achieving *Adaptive Target Impedance* Specifications is critical for overall system performance**
- **The advantages of *PI Advisor* were shown here.**
  - Increase capacitor count in order to make design more robust
  - Reduce the capacitor count
  - Reduce number of different capacitor types used
  - Redesign using lower cost capacitors
- **Efficient Power Integrity PCB Capacitor Optimization analysis and “*What-if...*” type analysis is utilized using:**
  - SIwave
  - DesignerSI