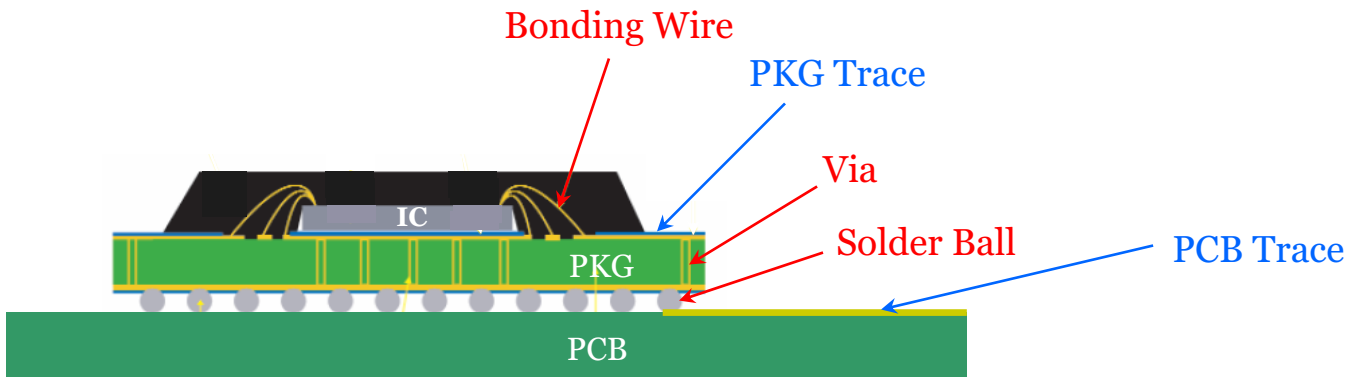
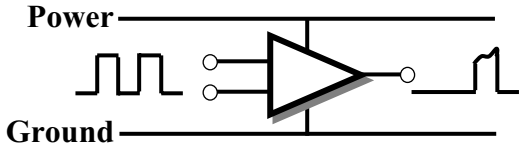
Discontinuity Regions in Package

- Channel: bonding wire → PKG trace → via → solder ball → PCB trace
- PKG traces & PCB traces: uniform transmission lines
- Bonding wires, vias & solder balls: discontinuity regions - bandwidths depend on the 3-D structure's design.

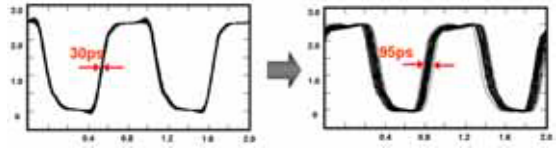


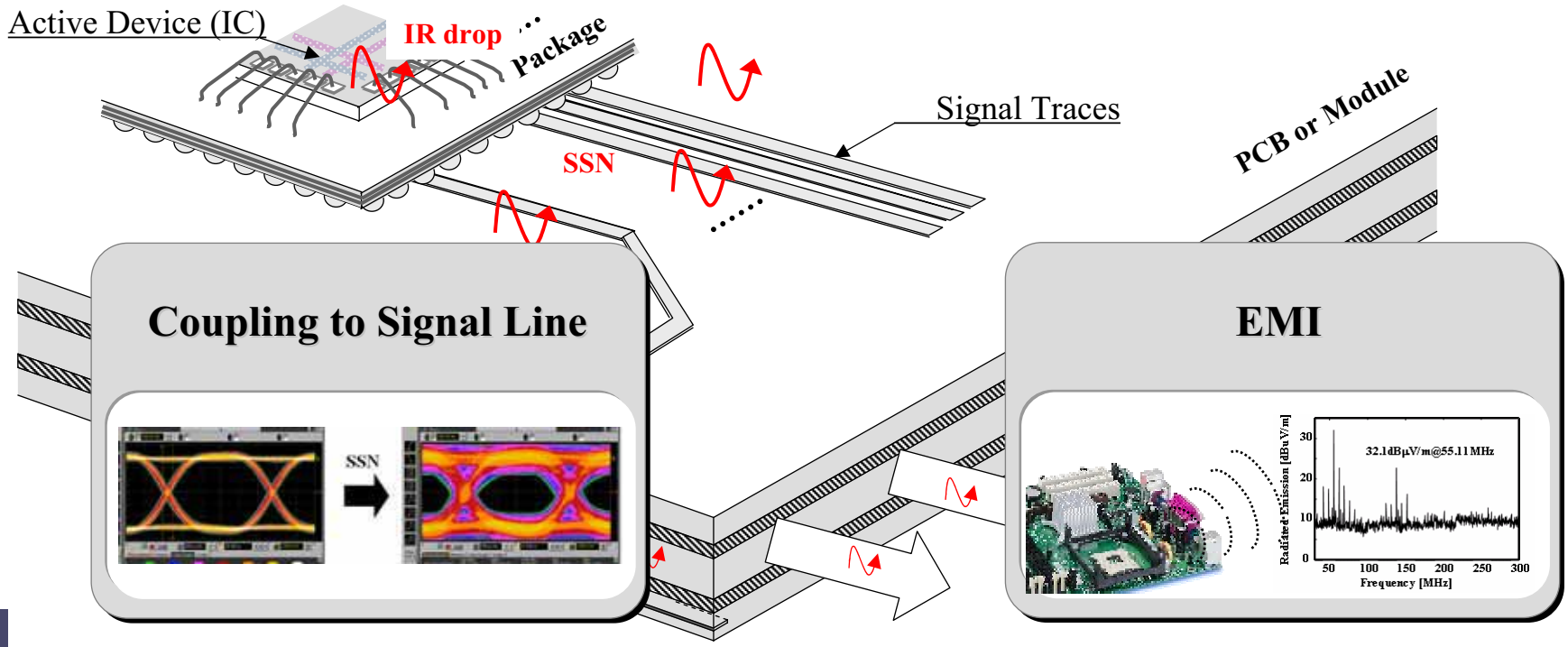
Problems by Power/Ground Noise

Logic Failure



Timing Delay, Skew

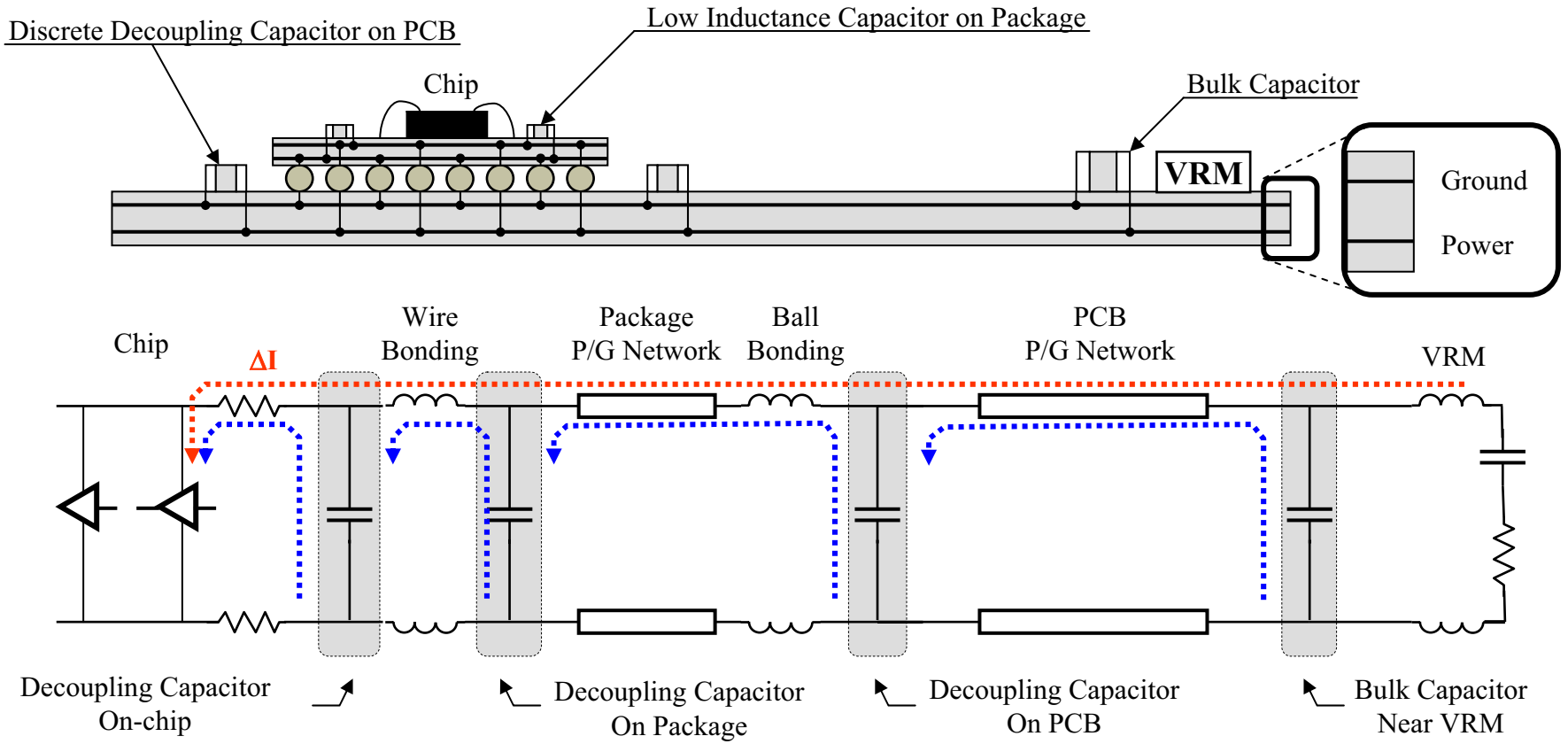




Coupling to Signal Line

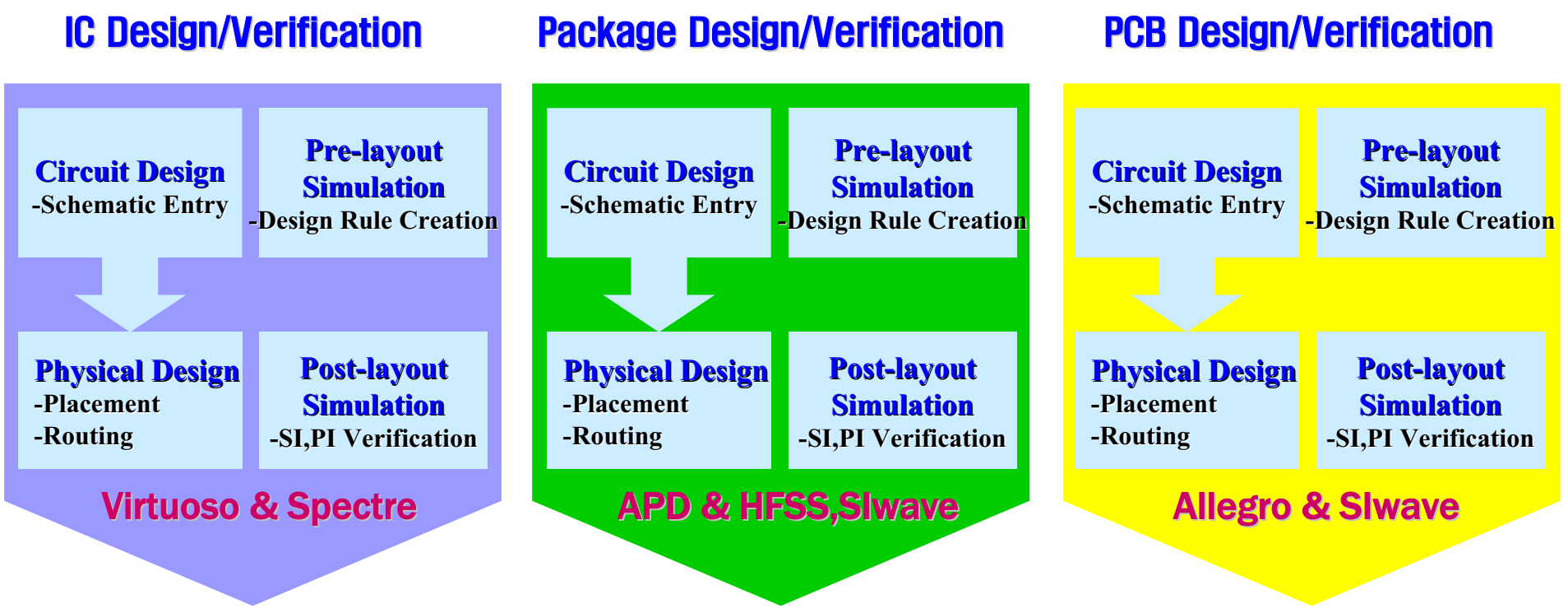
EMI

Power/Ground Noise Reduction Method



• **Decoupling Capacitors → Low Impedance Current Path**

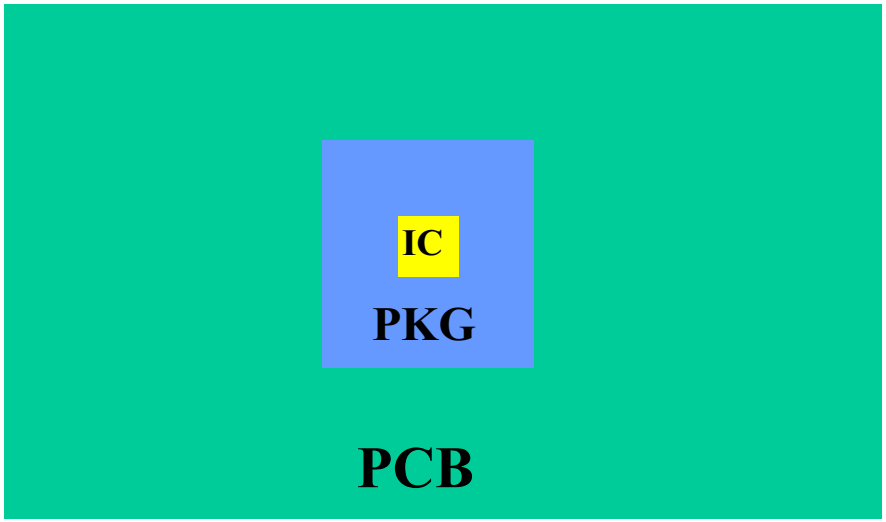
IC-Package-PCB Design and Verification Flow



System Level IC-Package-PCB Co-simulation

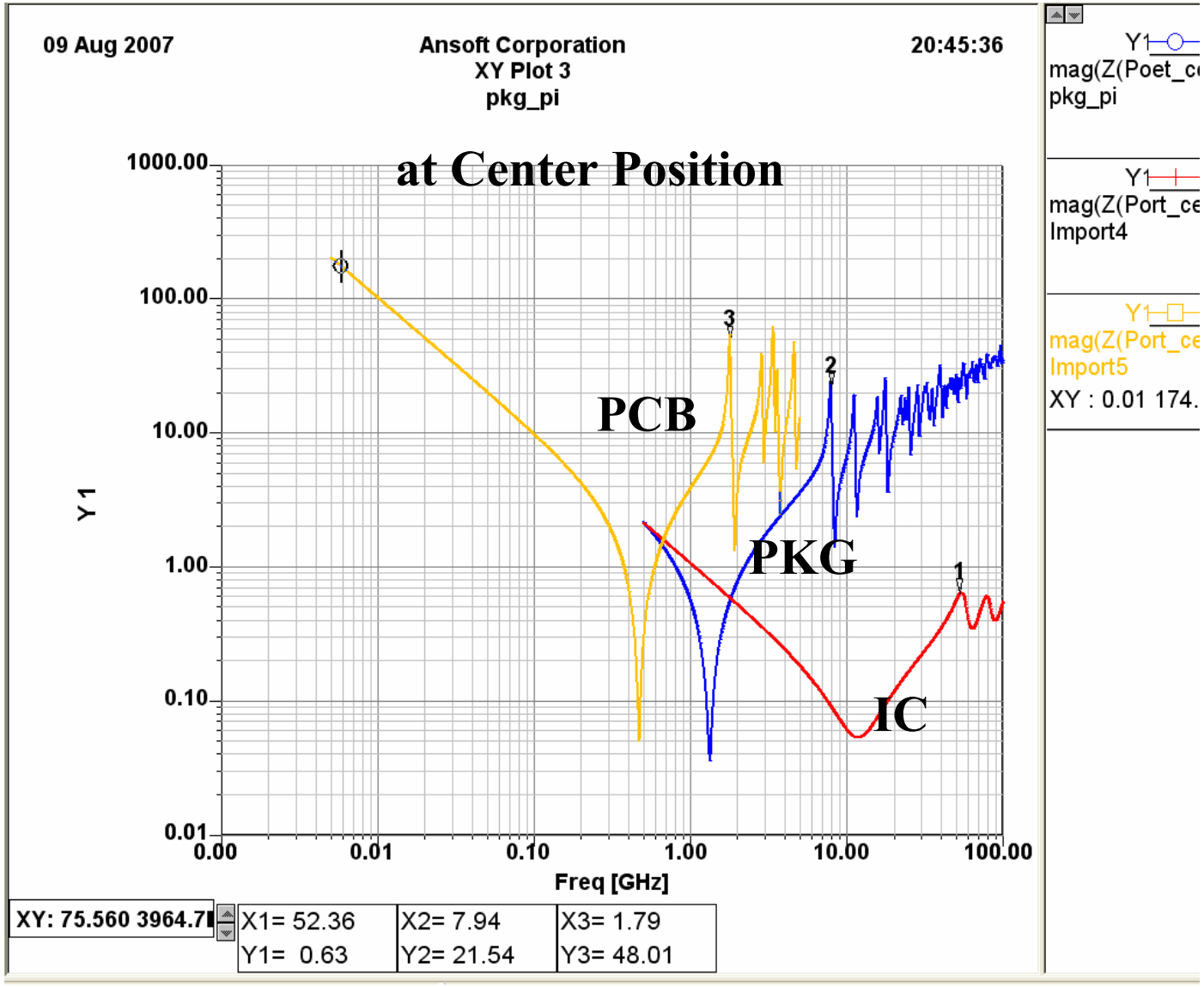
Ansoft Designer

What is different between IC, PKG, and PCB

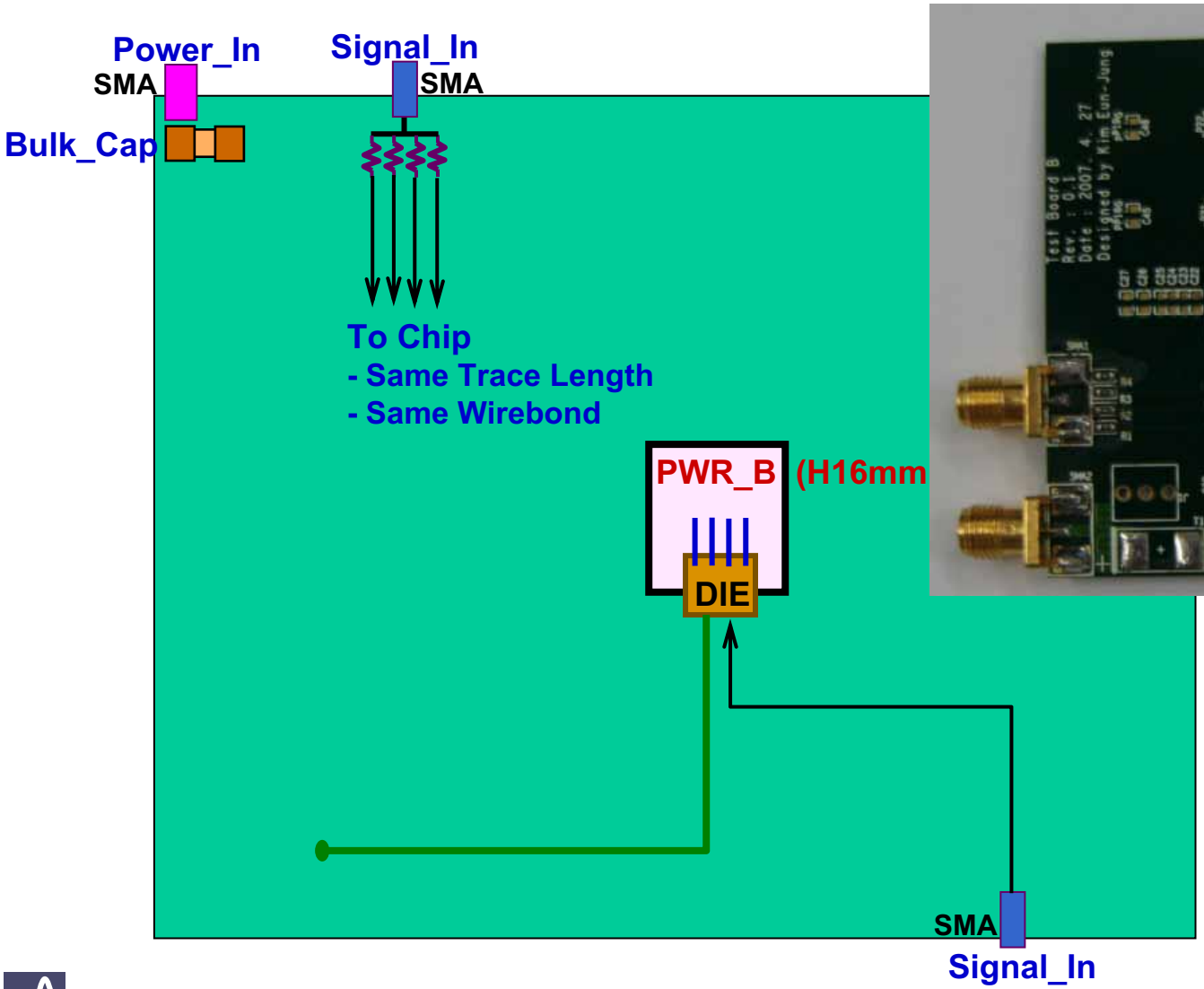


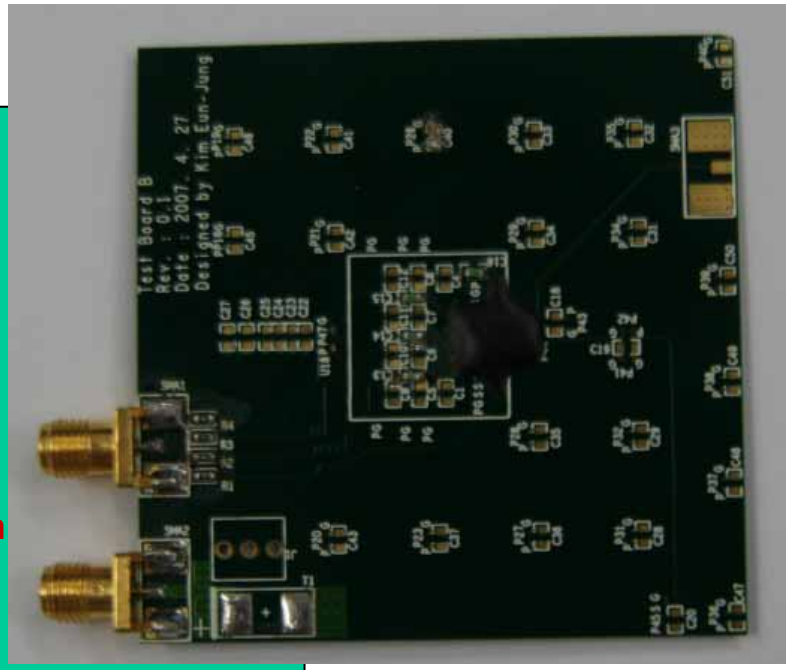
TYPE	H x V (mm)	P/G Height (mm)	Dielectric	Plane Capacitance
IC	2.4 x 2.4	0.00137	SIO2 (Er:4.0)	≒ 149pF
PKG	18 x 18	0.1	FR4 (Er:4.0)	≒ 115pF
PCB	80 x 50	1.0	FR4 (Er:4.0)	≒ 142pF

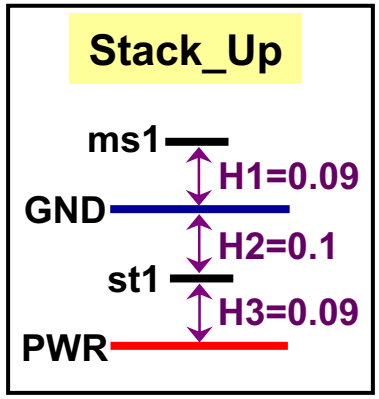
SIwave Simulation for Plane Capacitance



Test Board Design for Co-simulation







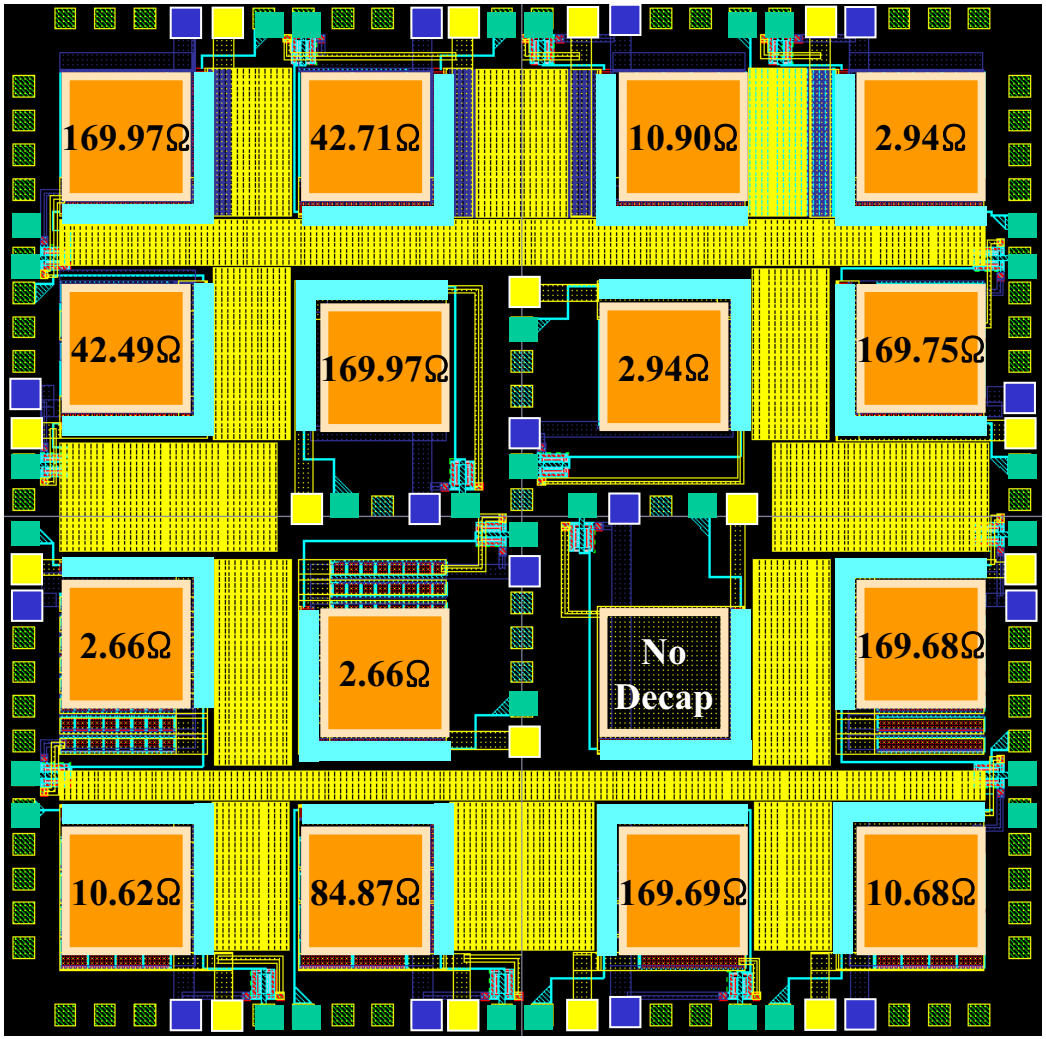
IC Deign for On-chip De-cap Test

Chip layout for Verification

Hynix 0.25 μm process

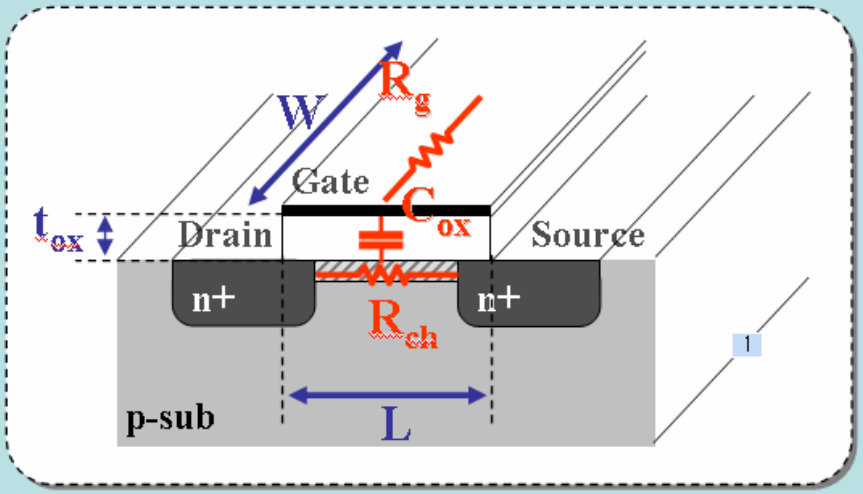
I/O voltage (V_G) : 3.3V
Gate length : 0.34μm (for I/O)
Gate Oxide (t_{ox}) : 71Å
V_T : 0.74V
R_{sheet} : 3.5Ω/□
Die Size : 2.4mm x 2.4mm

C_{total} = 778.14pF



Cell Define

Capacitor design Review

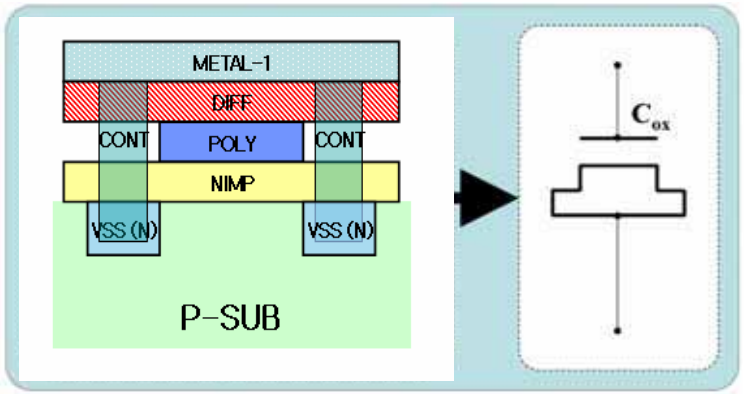


$$C_{ox} = \frac{\varepsilon_{SiO_2}\varepsilon_0}{t_{ox}} \times WL$$

$$R_g = R_{Sheet} \times \frac{W}{L}$$

$$R_{ch} = \frac{1}{\mu_n C_{ox,unit\ area}(V_G - V_T)} \times \frac{L}{W}$$

~KΩ/□



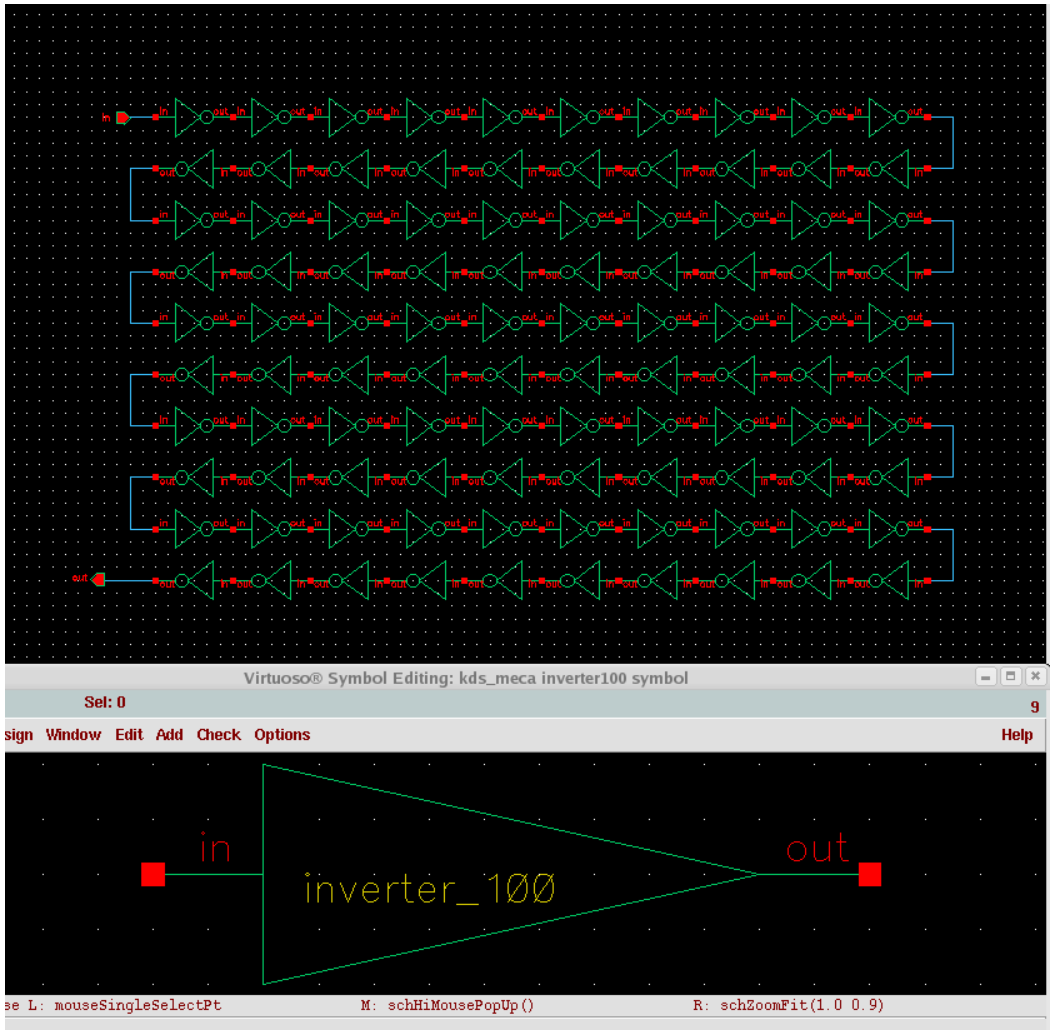
R_{ch} will be dominant unless W/L is big.

R_{sheet} : gate (ex. poly) sheet resistance
μ_n : electron mobility (~300cm²/V·s)
V_G : gate bias voltage
V_T : threshold voltage

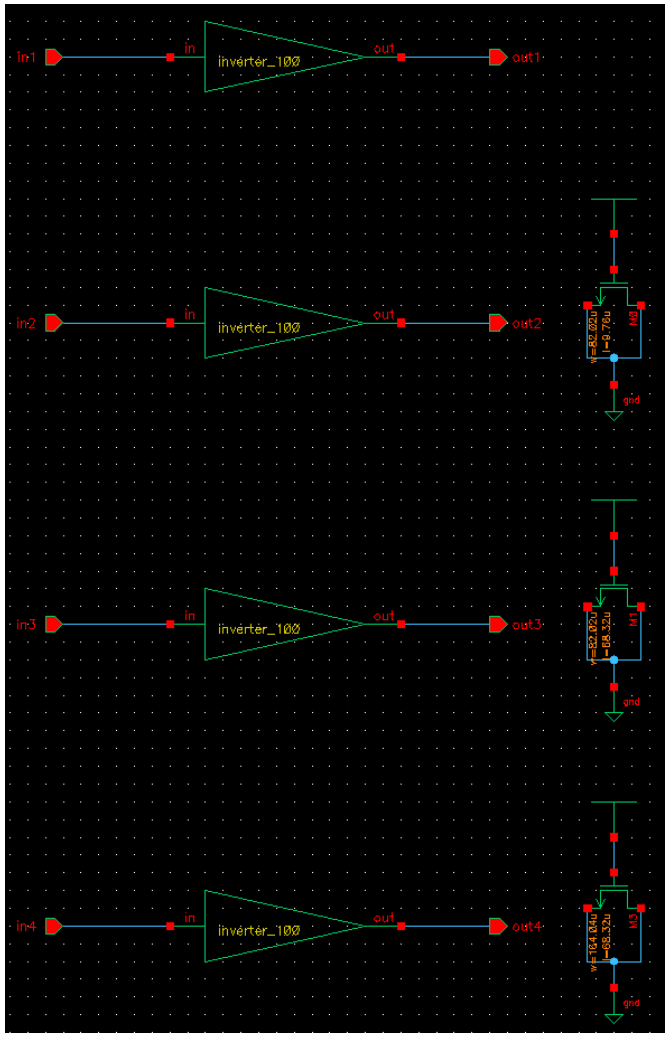
참조 : 박현정 학생 석사 논문

Schematic with Virtuoso of Cadence

Inverter 100EA & Symbol



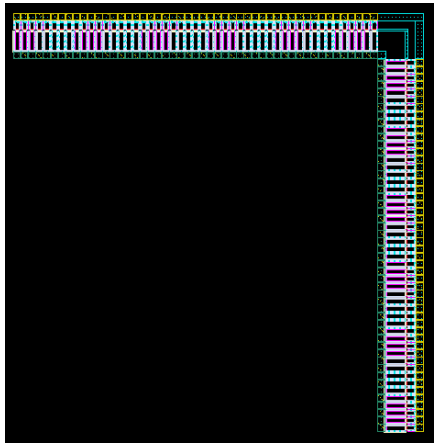
All Block Schematic



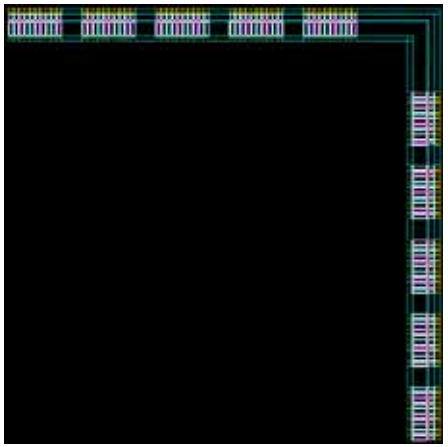
Layout with Virtuoso of Cadence

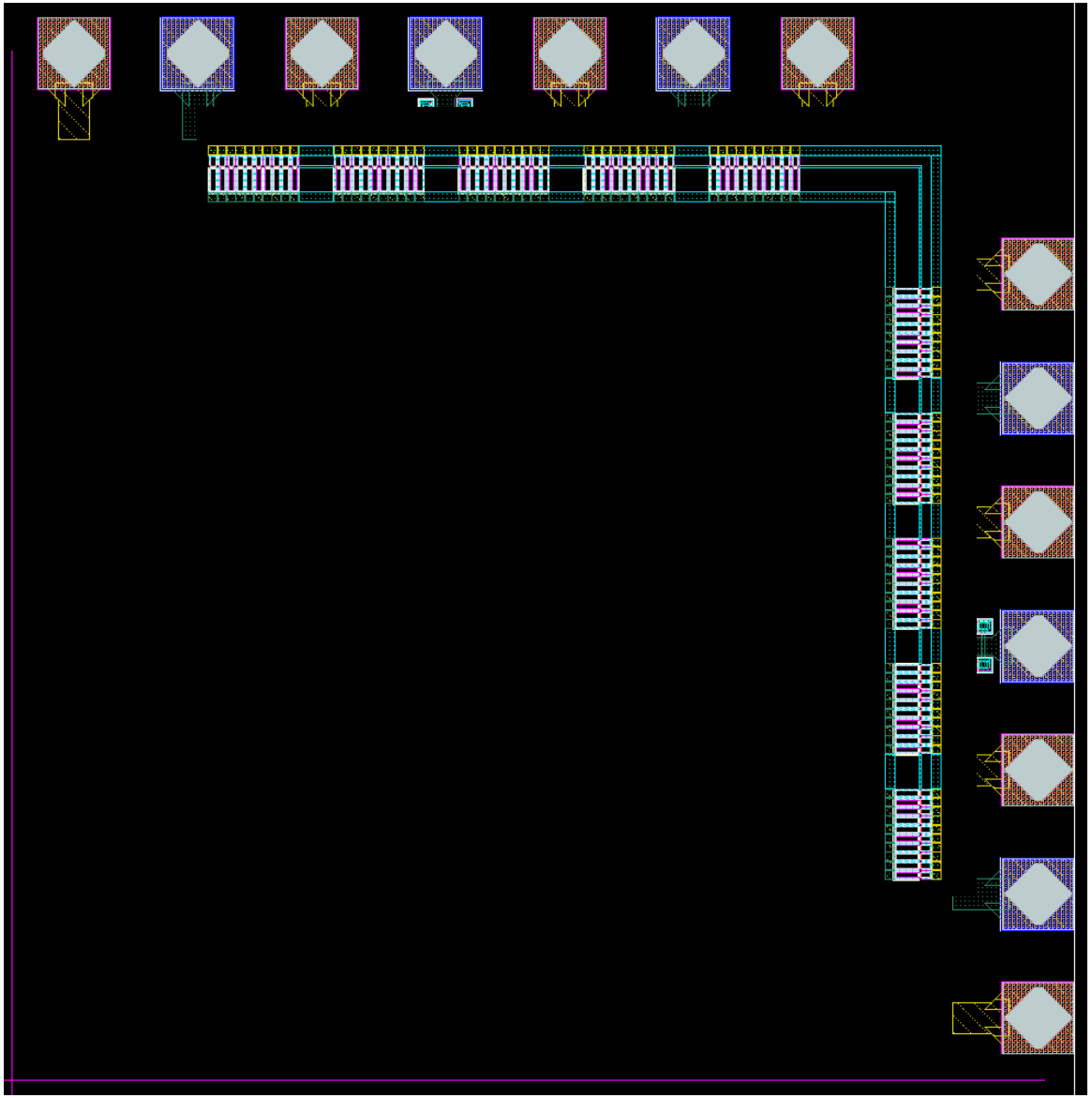
Inverter 100EA

1st Inverter 100EA

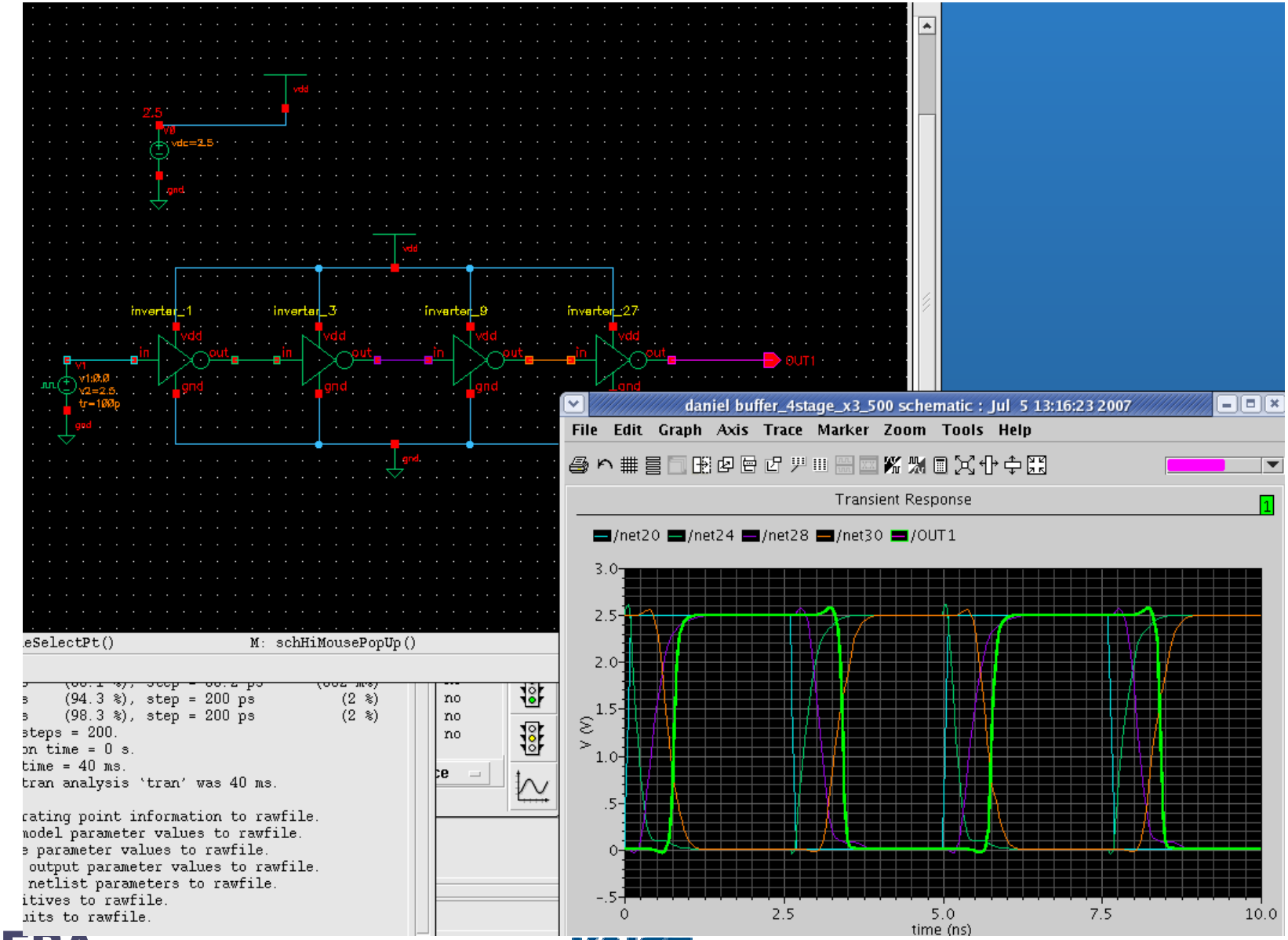


2st Inverter 100EA



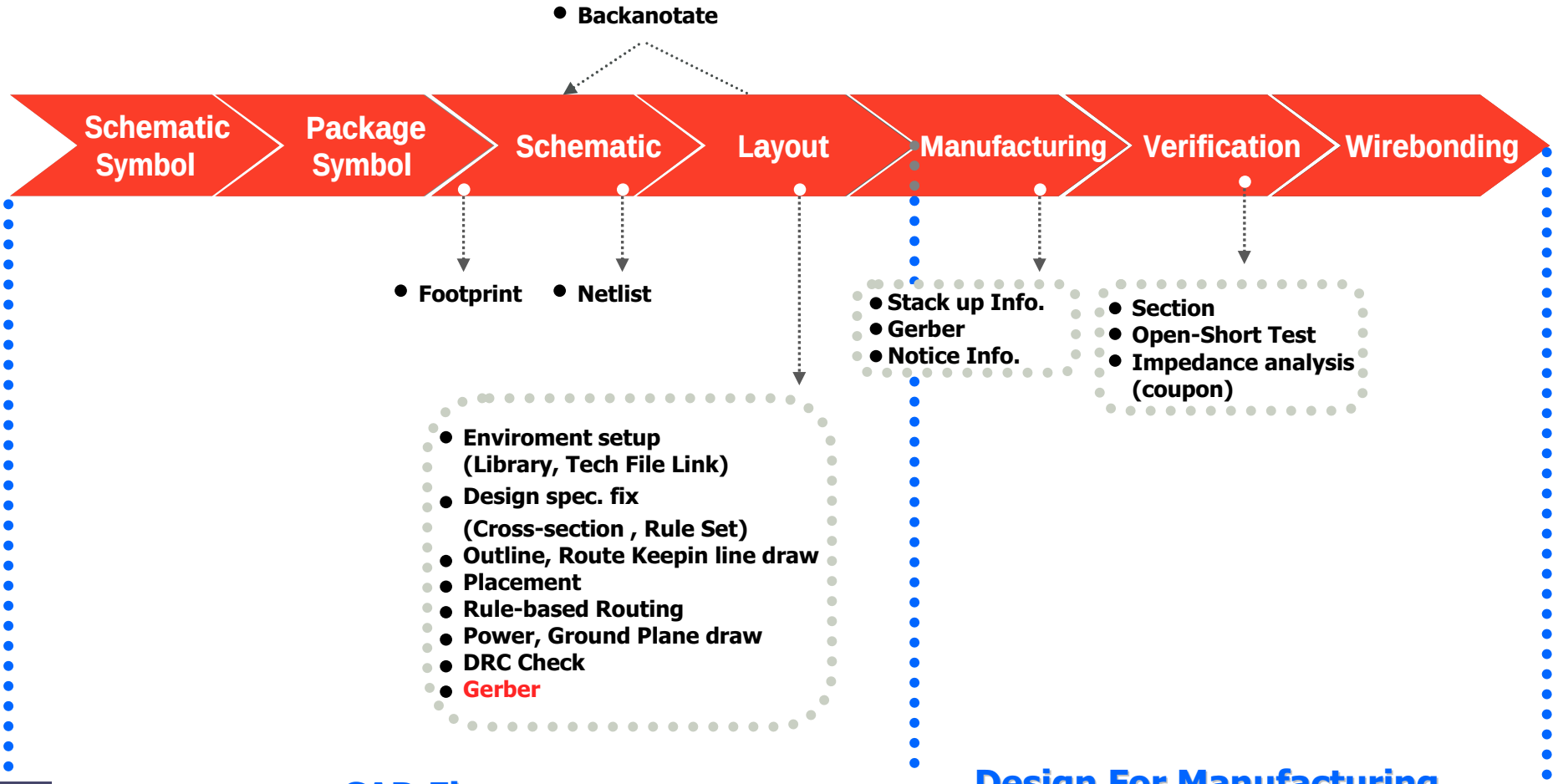


2.5V CMOS Inverter with 4 stage of 0.5u, 3x @200M

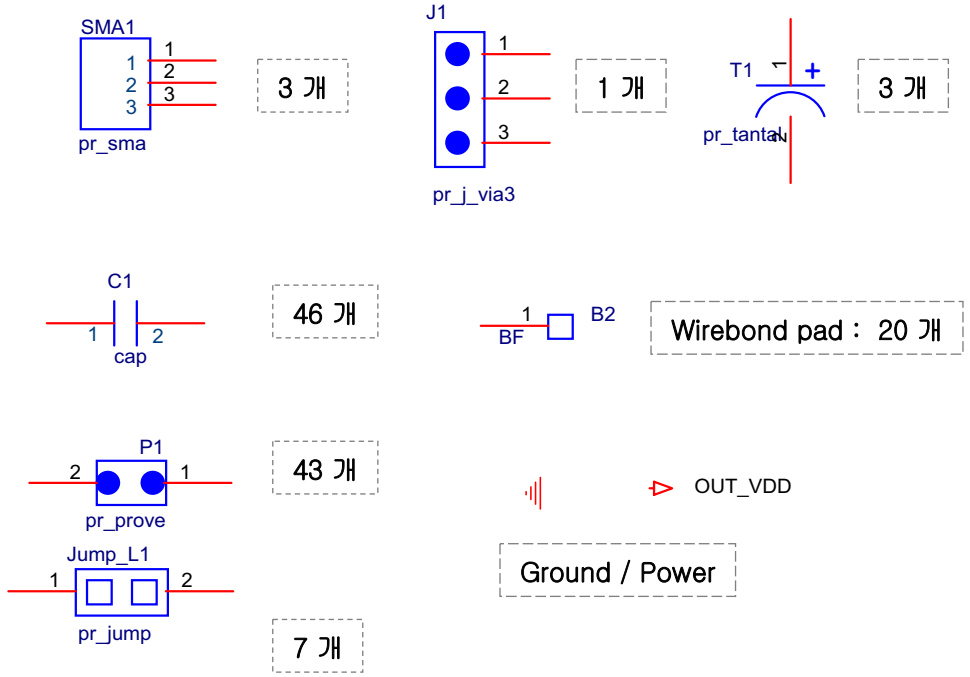


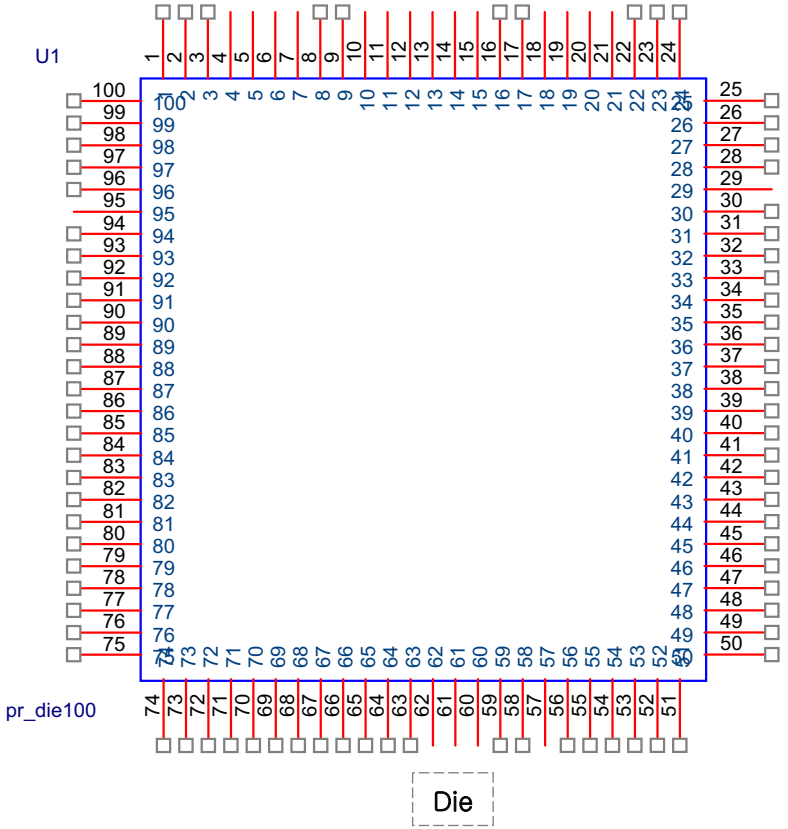
Package Design Process with Cadence Tool

- Allegro Design Entry CIS (schematic)
- Allegro PCB Editor (layout)



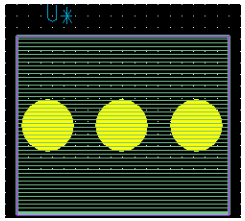
Schematic Symbol

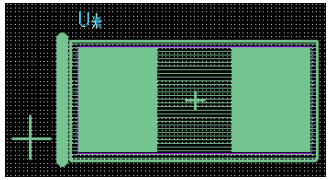




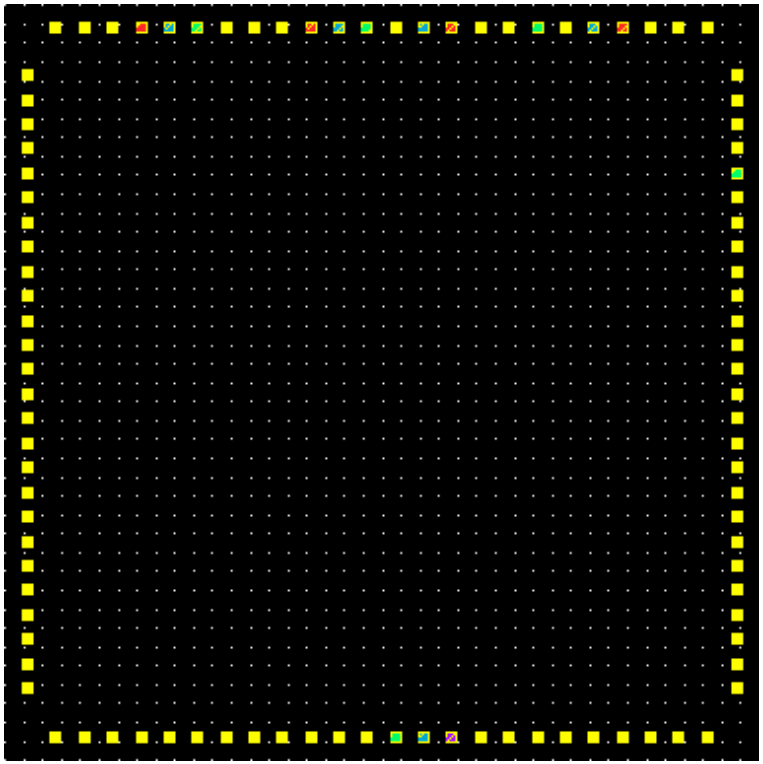
Package Symbol

SMA

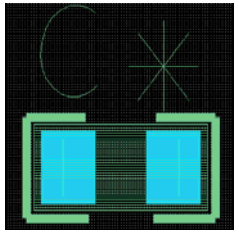


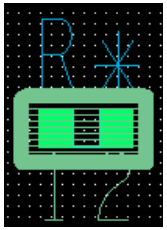


TANTAL

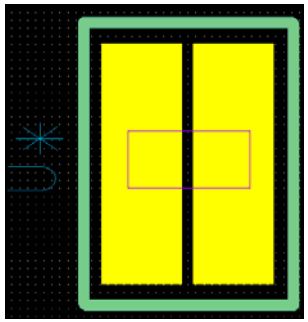


Die

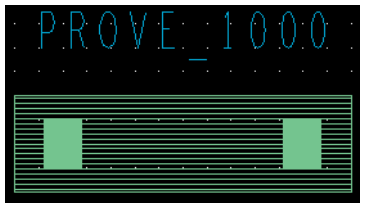




Capacitor

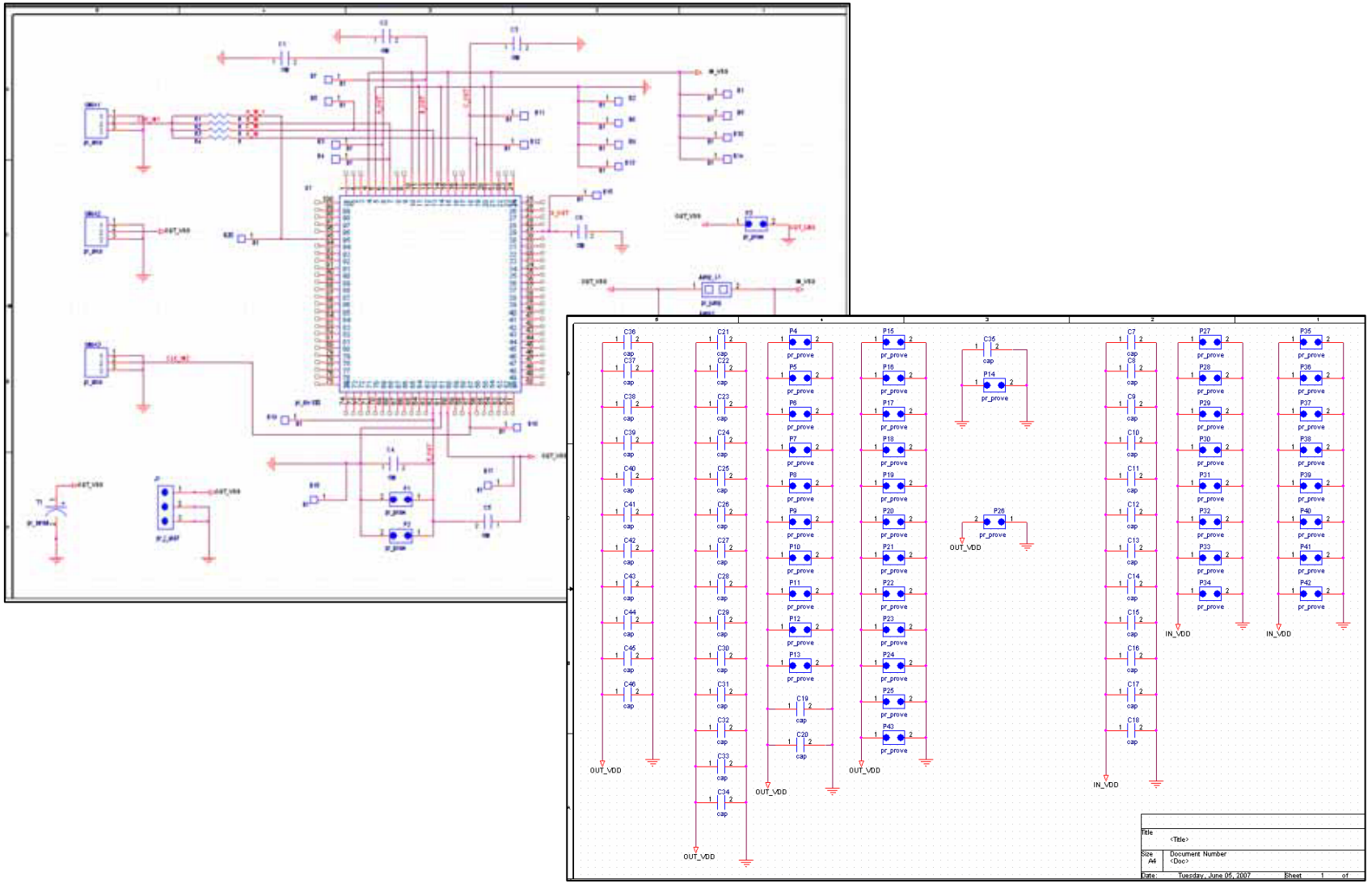


Jumper



Prove Point

Schematic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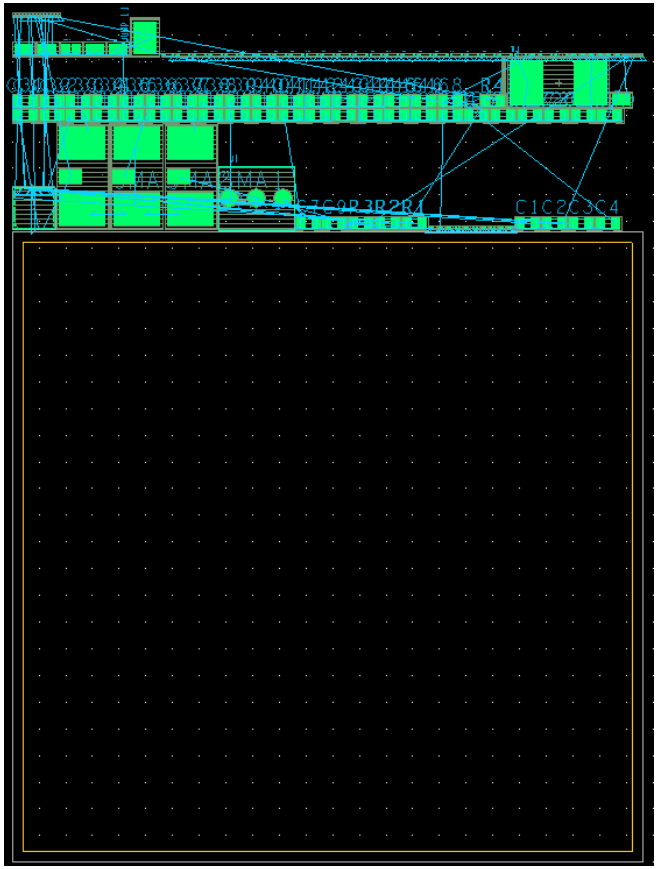
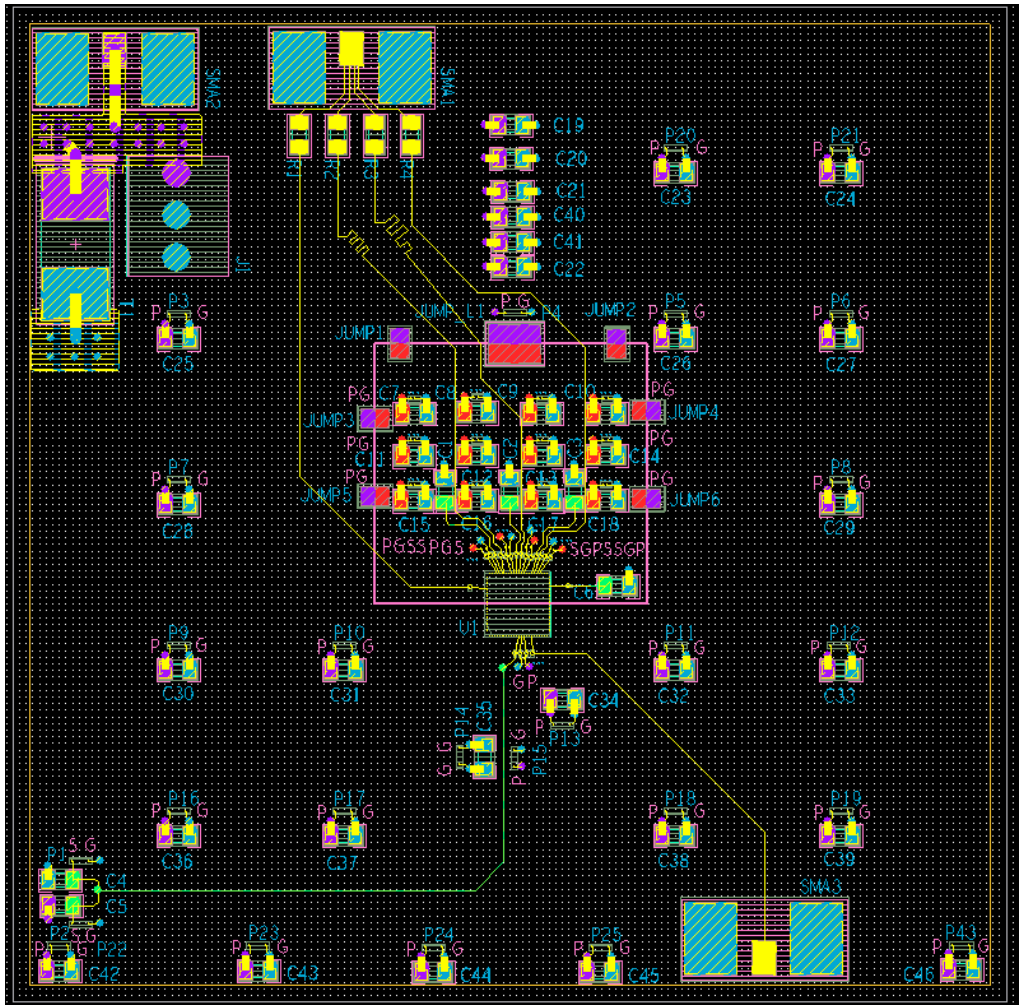
of

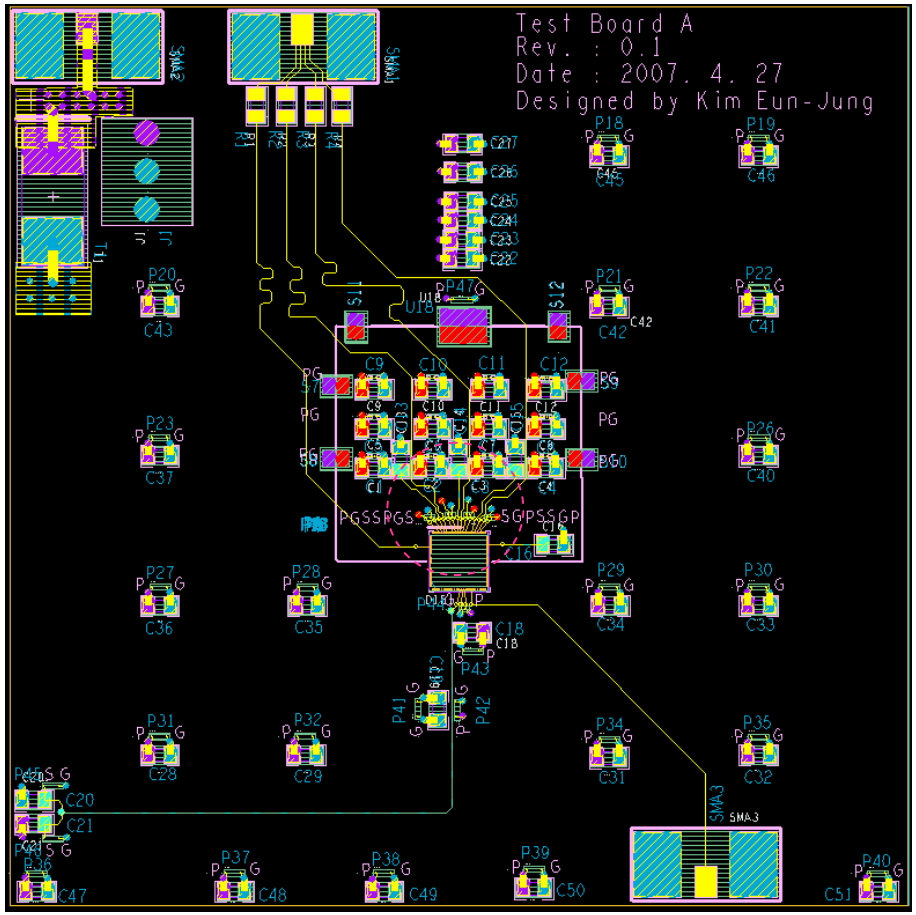
Layout





Layout (Test Board-A)

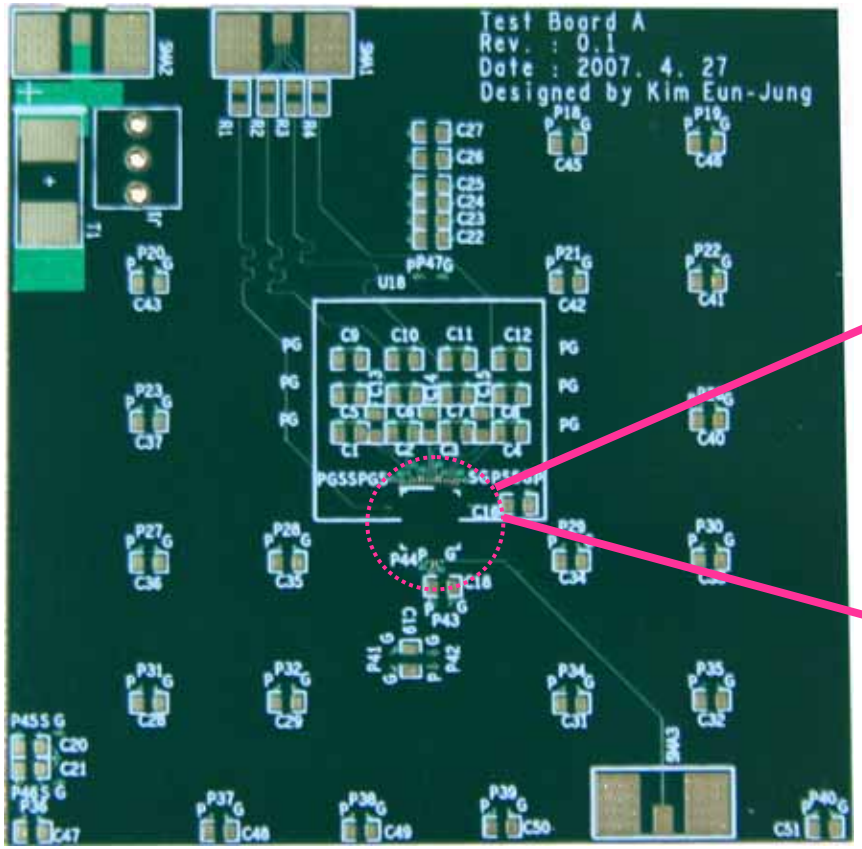
Test board A

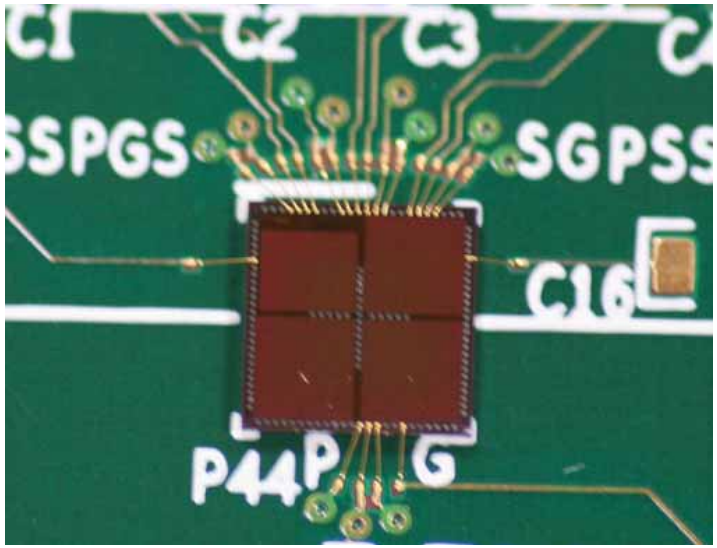


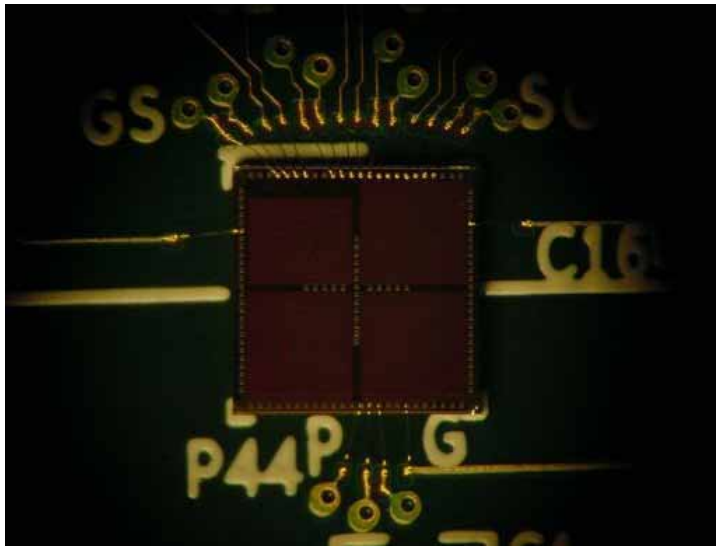
Test Board and Wire Bond

Test board A

Wire length = 1.0 mm

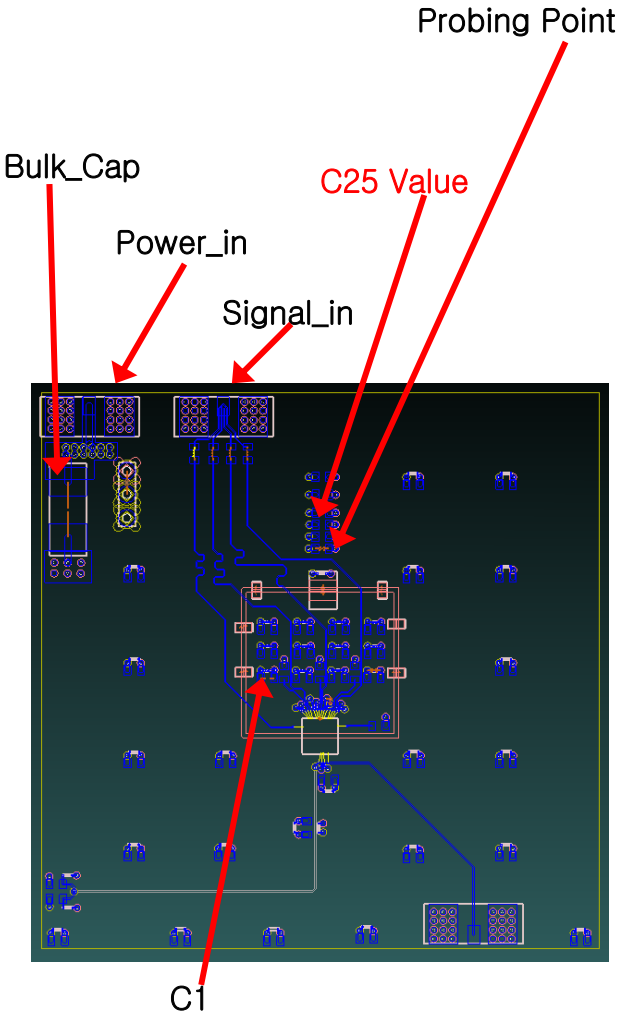




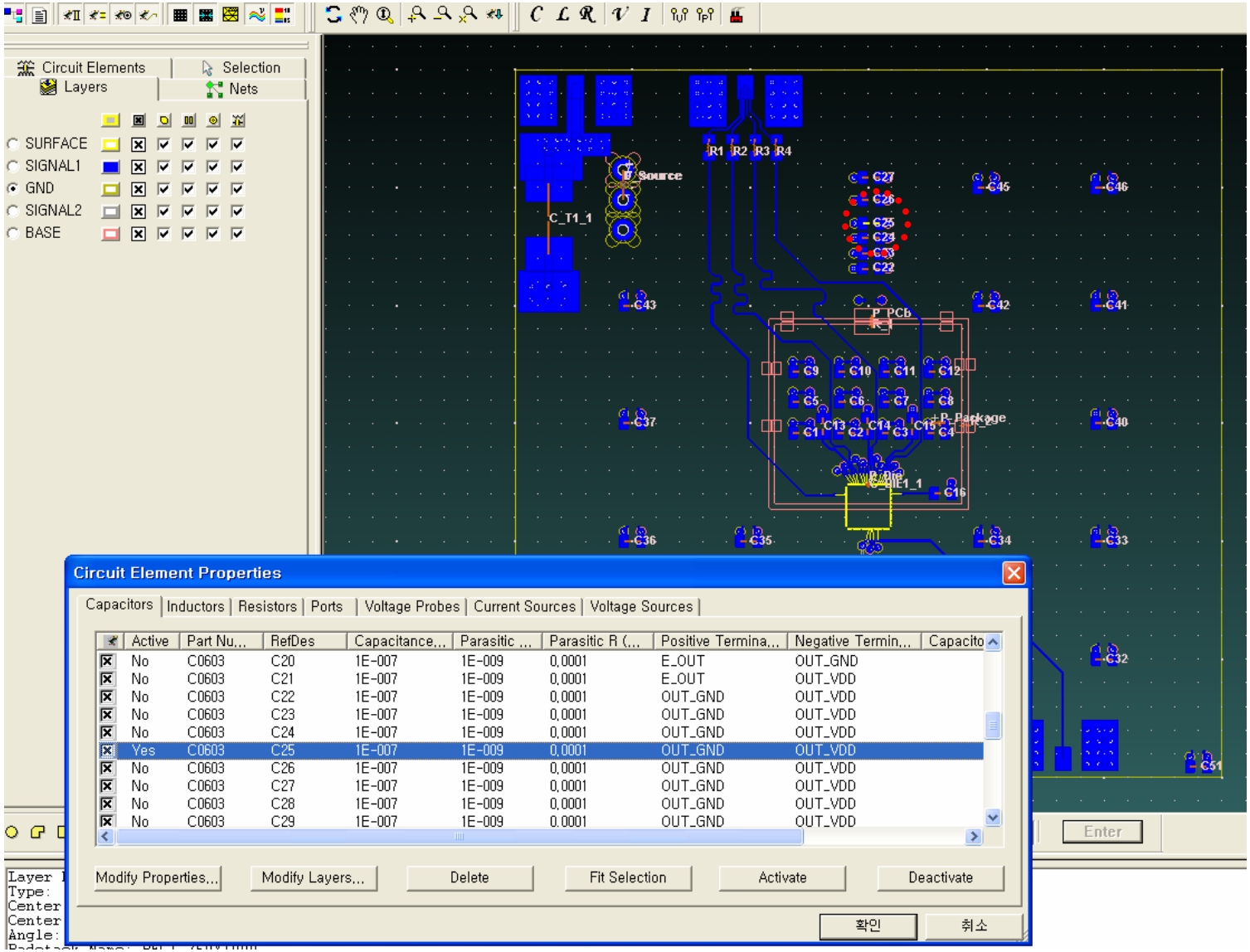


PI analysis related to De-cap Value

- Test Condition
  - Test Board A
    - ✓ C25; 100pF, 1nF, 10nF, 100nF
    - ✓ C1;1nF
    - ✓ Bulk Cap;330uF
    - ✓ DC: 3.3V
    - ✓ Signal; 1 V, Tr 2.5nS, 50MHz Square Wave
  - Probing Point (C22); Z plot

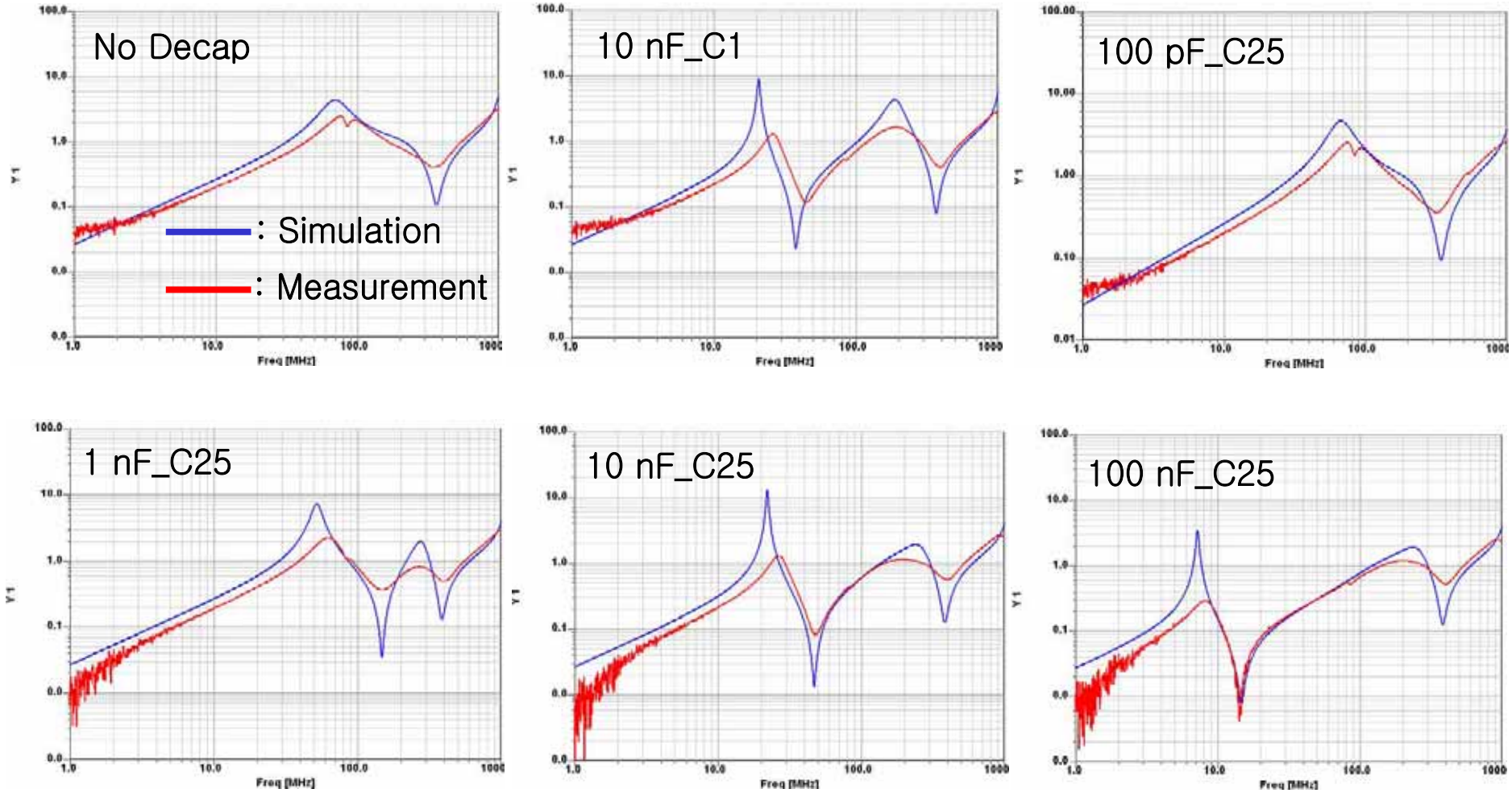


PI analysis related to De-cap Value



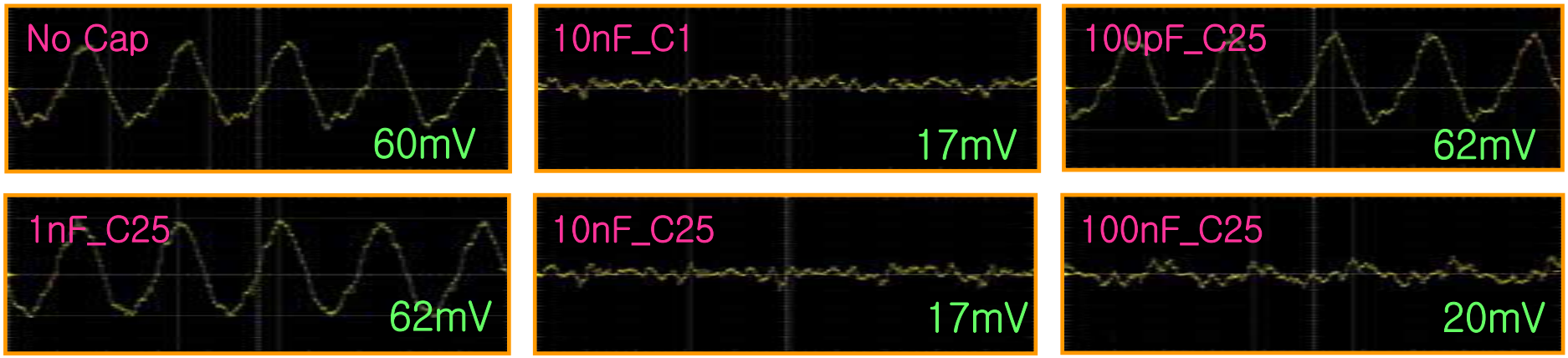
Simulation & Measurement Result

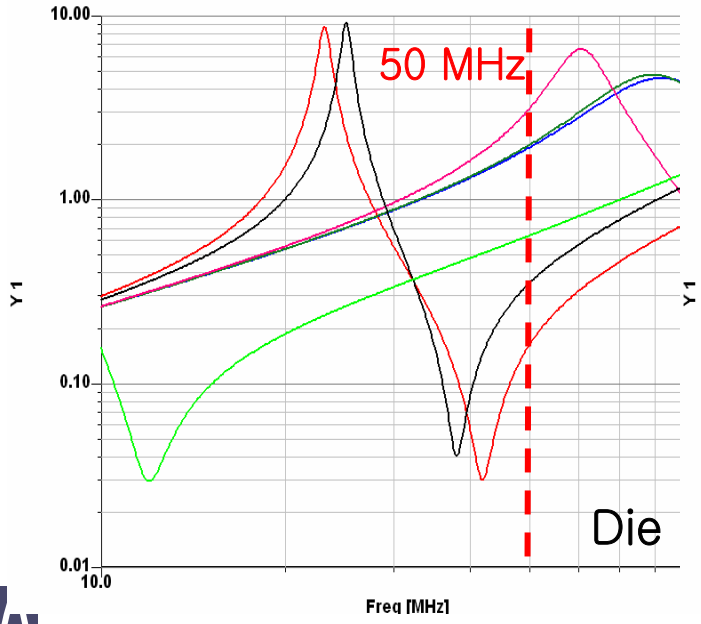
◆ Probing Point(C22); Z_{11} measurement vs Slwave simulation

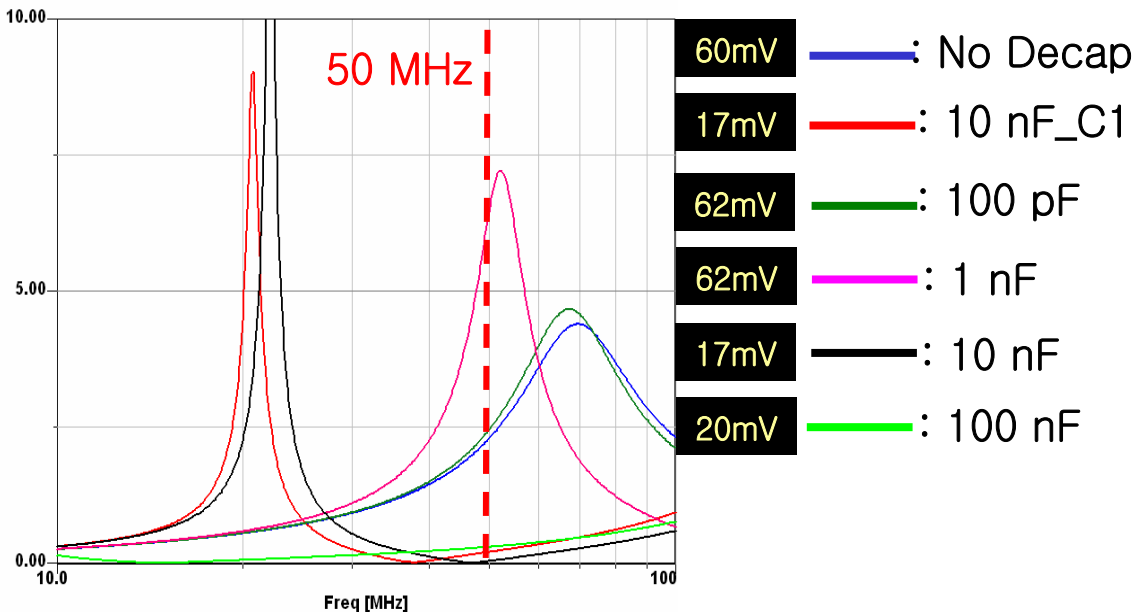


Time Domain Measurement vs Simulation

◆ Probing Point(C22)

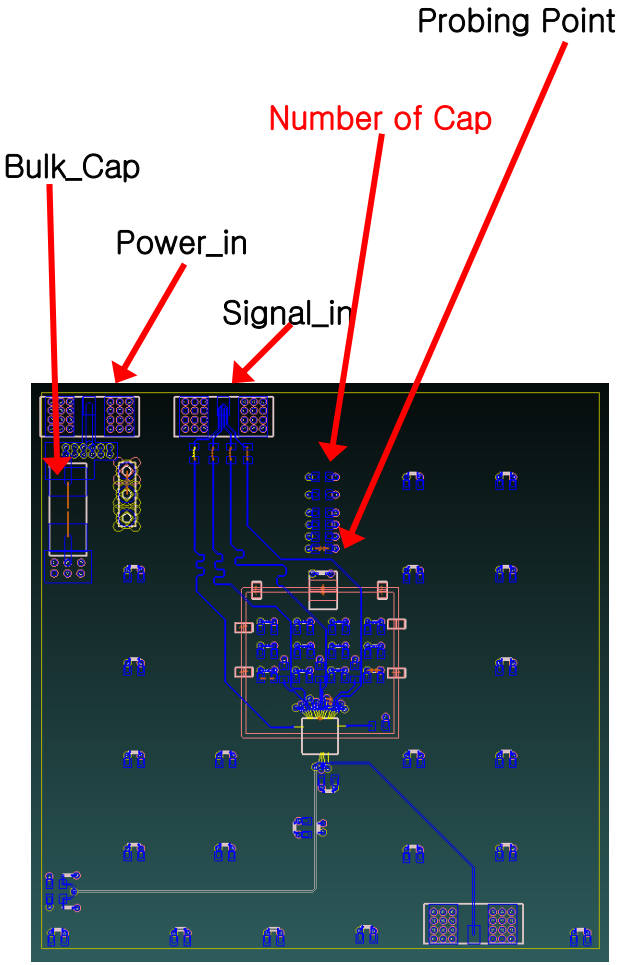




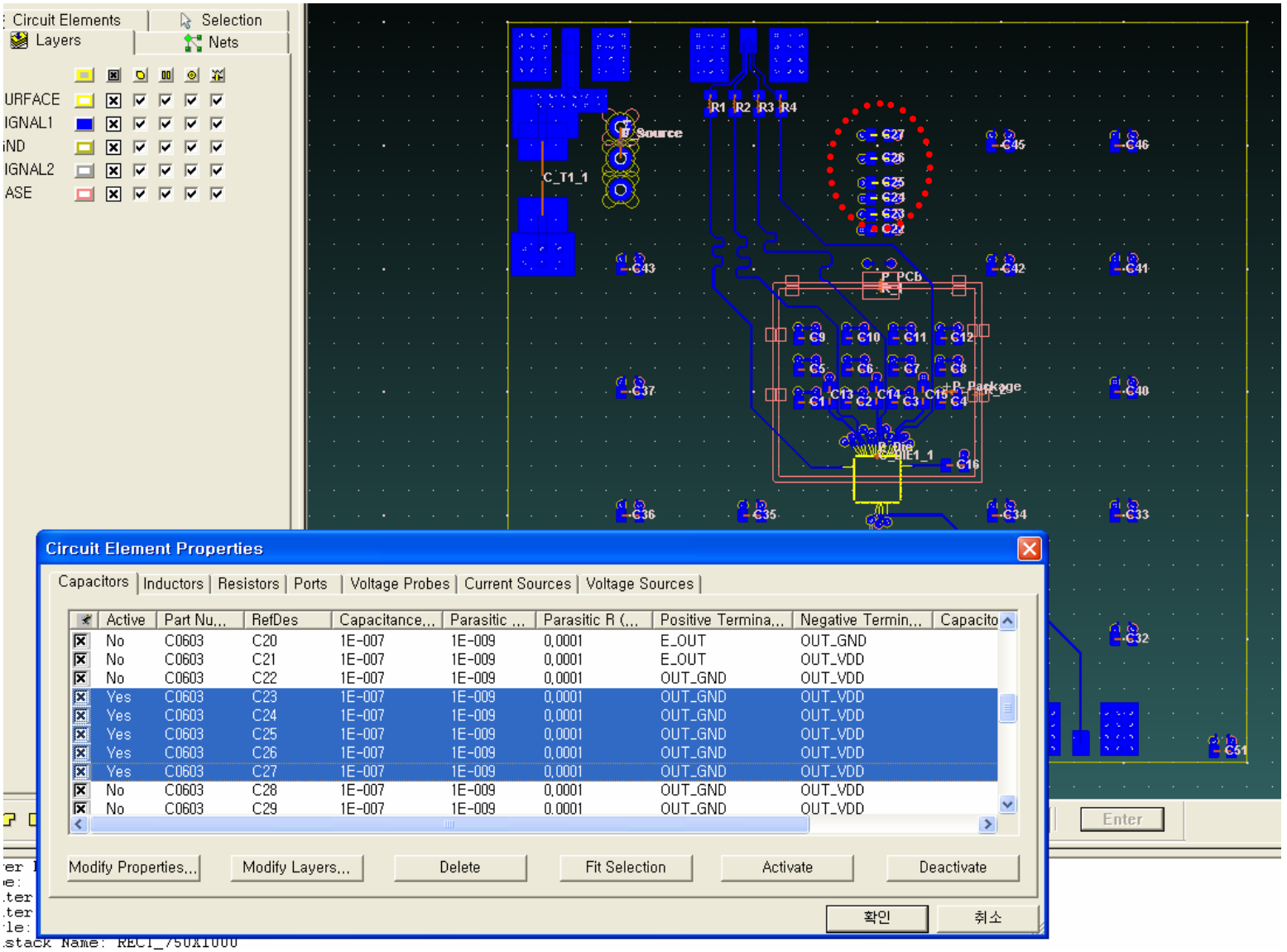


PI analysis related to Number of Capacitor

- Test Condition
  - Test Board A
    - ✓ 10nF Cap; added to C23/C24/C25/C26/C27
    - ✓ Bulk Cap;330uF
    - ✓ DC: 3.3V
    - ✓ Signal; 1 V, Tr 2.5nS, 50MHz Square Wave
  - Probing Point (C22); Z plot

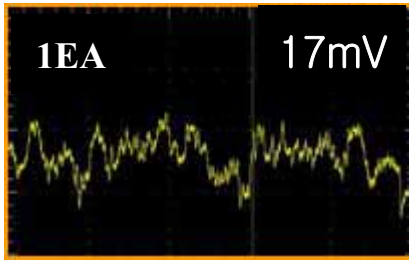


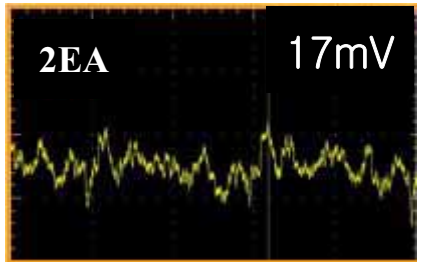
PI analysis related to Number of Capacitor

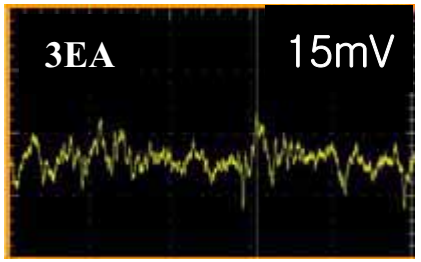


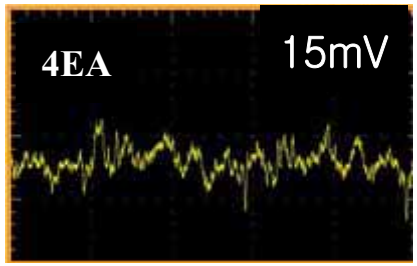
Time Domain Measurement vs Simulation; at 50MHz

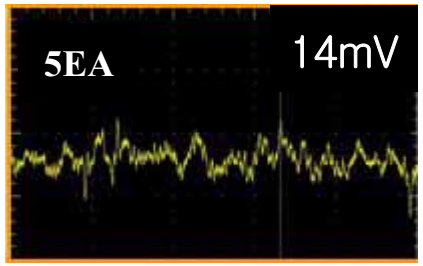
◆ C22 Probing Point

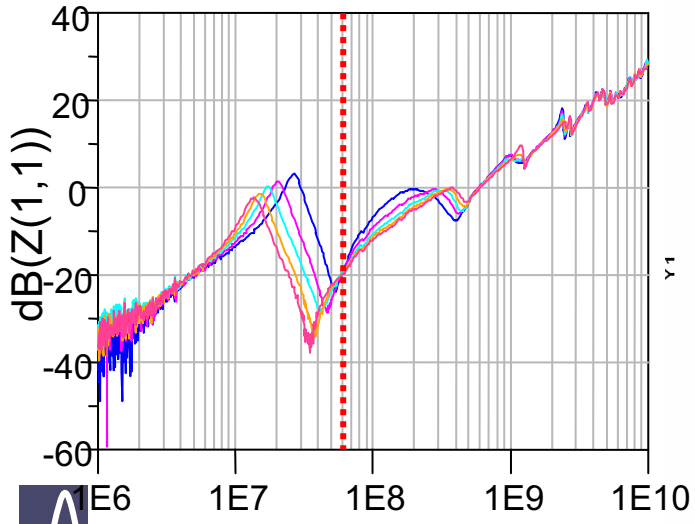


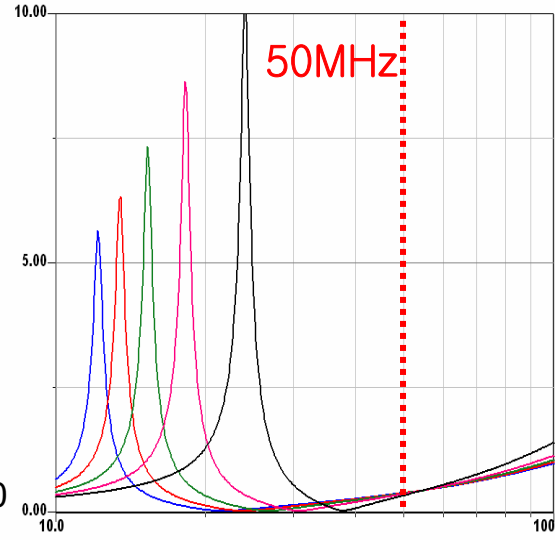


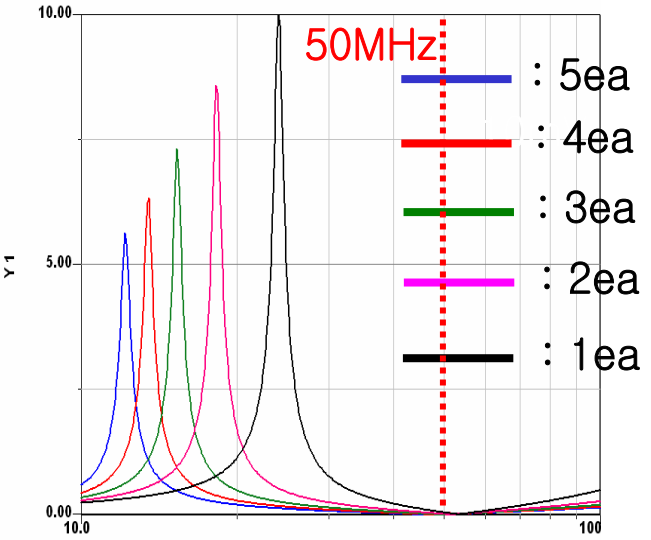












Time Domain Measurement vs Simulation; at 30MHz

◆ C22 Probing Point