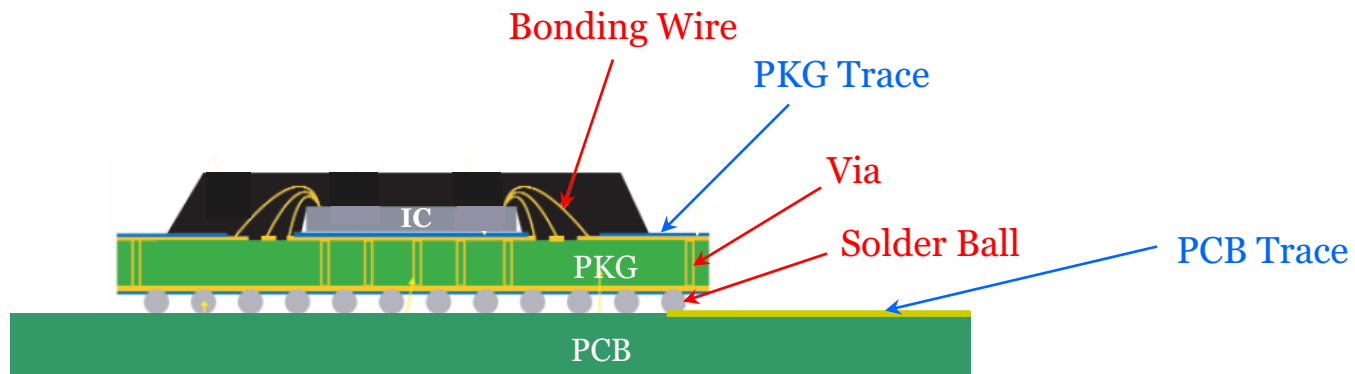


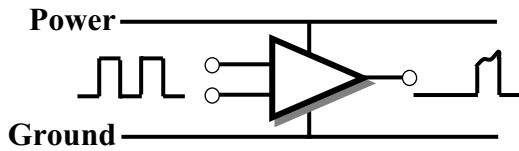
# Discontinuity Regions in Package

- Channel: **bonding wire** → **PKG trace** → **via** → **solder ball** → **PCB trace**
- PKG traces & PCB traces: **uniform transmission lines**
- Bonding wires, vias & solder balls: **discontinuity regions** - bandwidths depend on the 3-D structure's design.

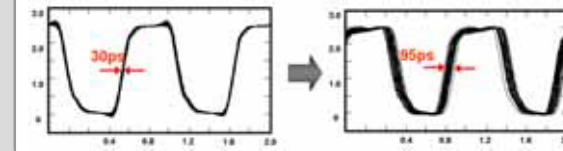


# Problems by Power/Ground Noise

## Logic Failure



## Timing Delay, Skew



Active Device (IC)

IR drop

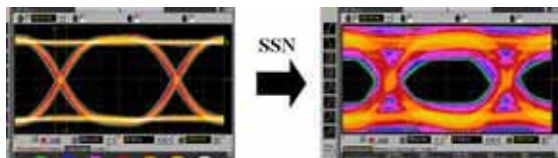
Package

SSN

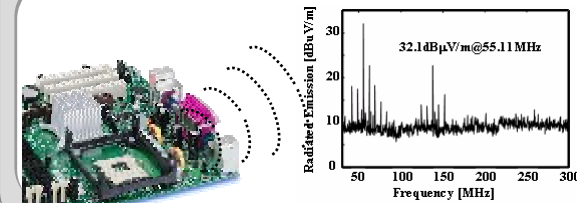
Signal Traces

PCB or Module

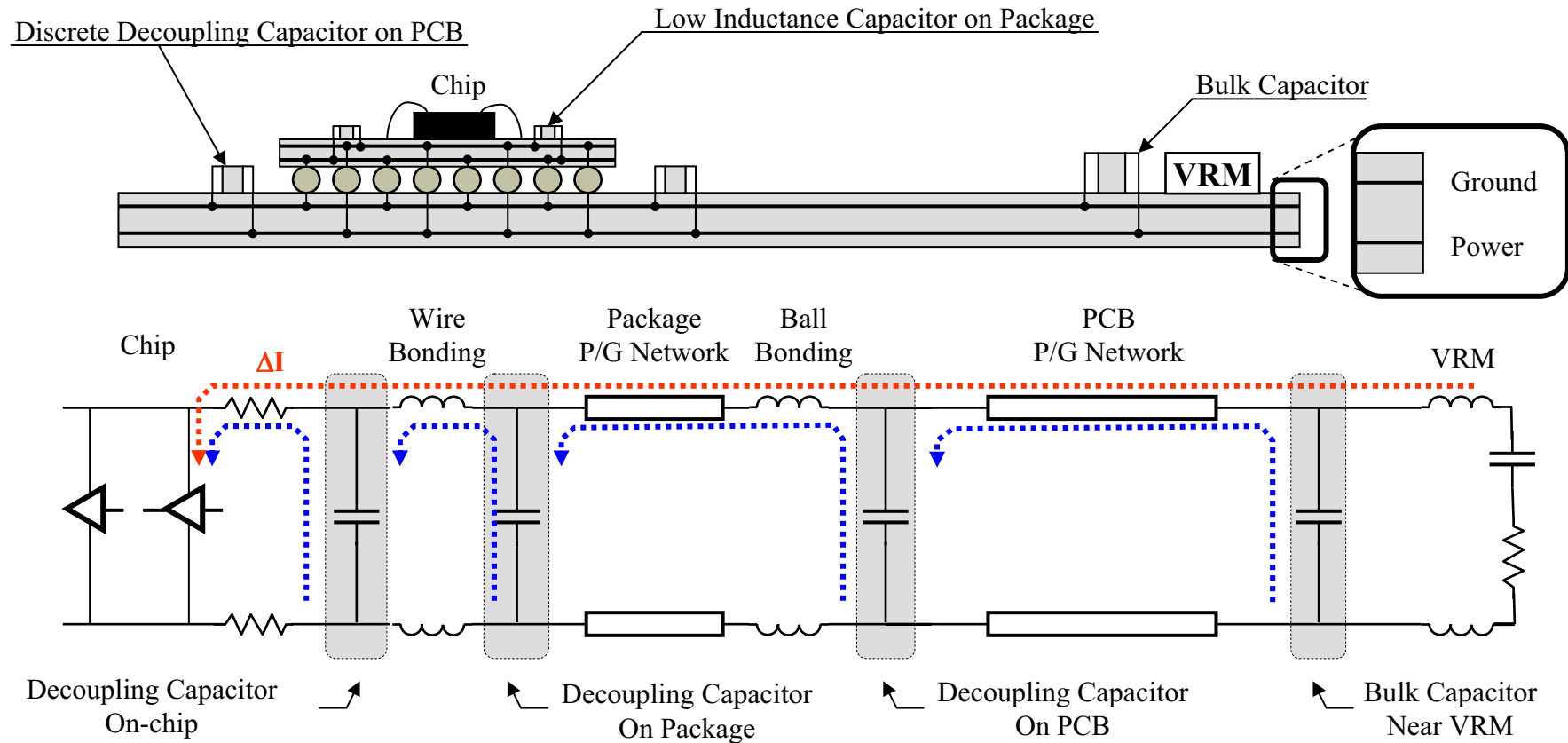
## Coupling to Signal Line



## EMI



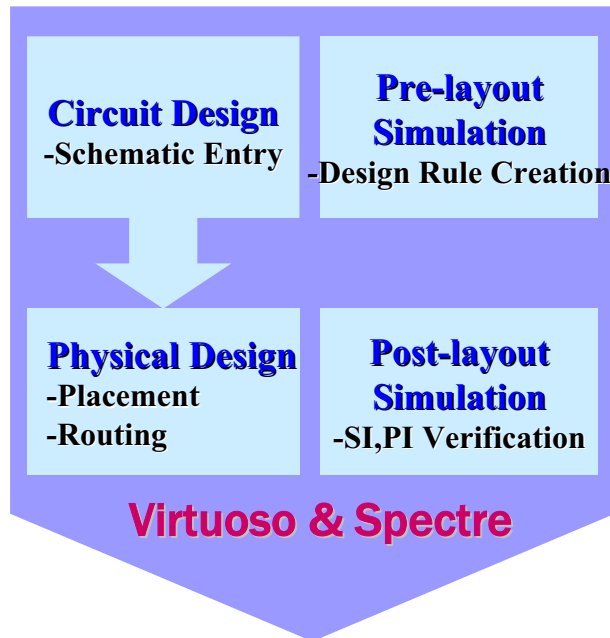
# Power/Ground Noise Reduction Method



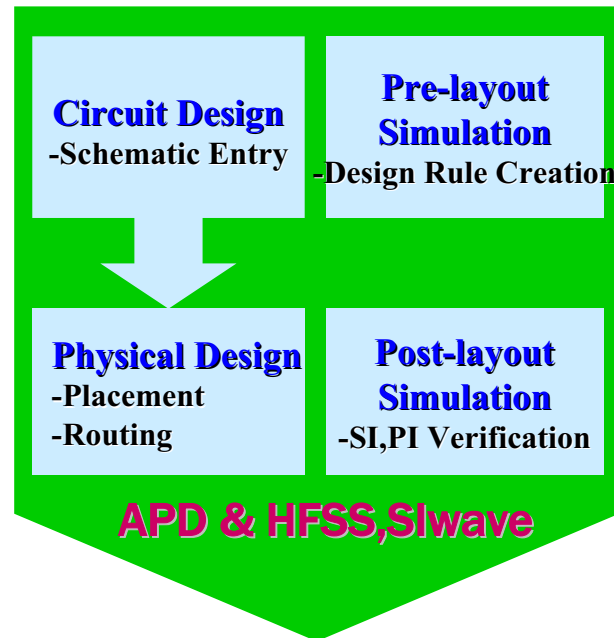
• Decoupling Capacitors → Low Impedance Current Path

# IC-Package-PCB Design and Verification Flow

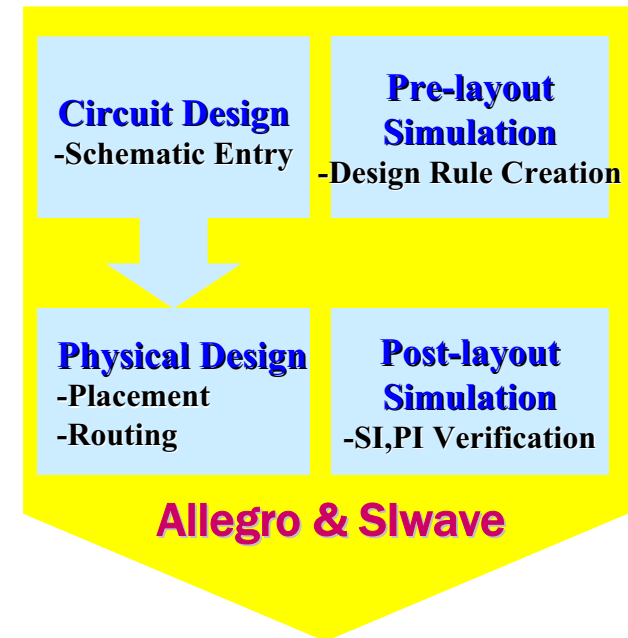
## IC Design/Verification



## Package Design/Verification



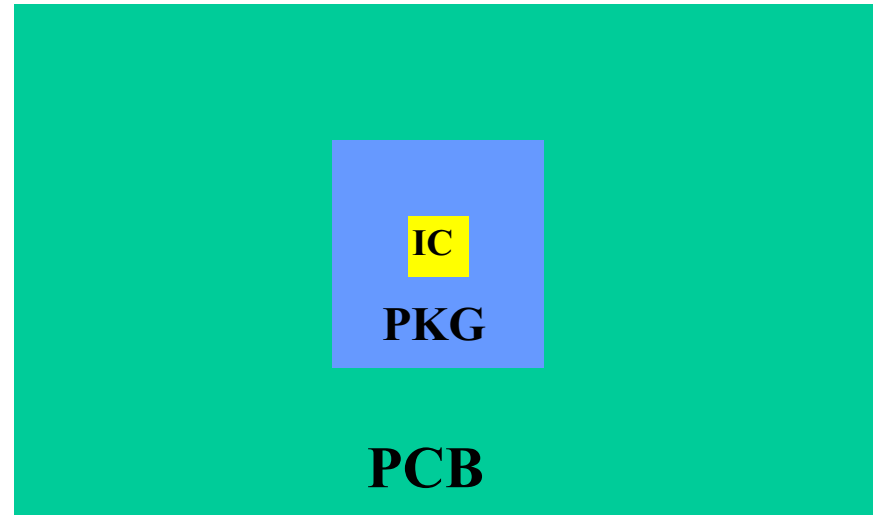
## PCB Design/Verification



## System Level IC-Package-PCB Co-simulation

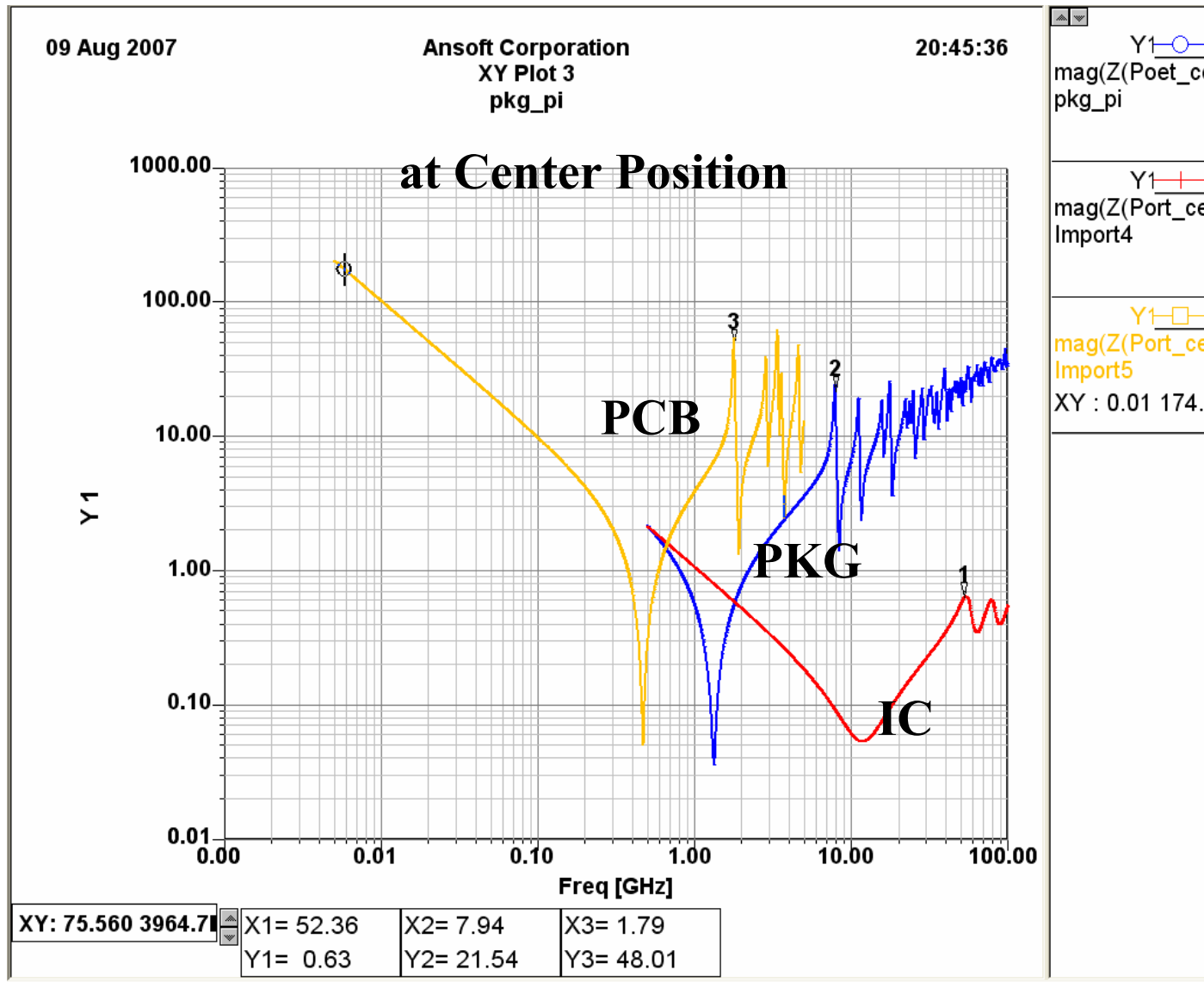
Ansoft Designer

# What is different between IC, PKG, and PCB

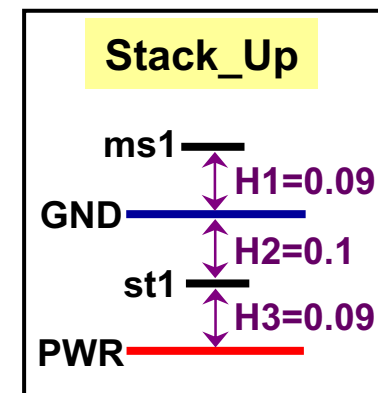
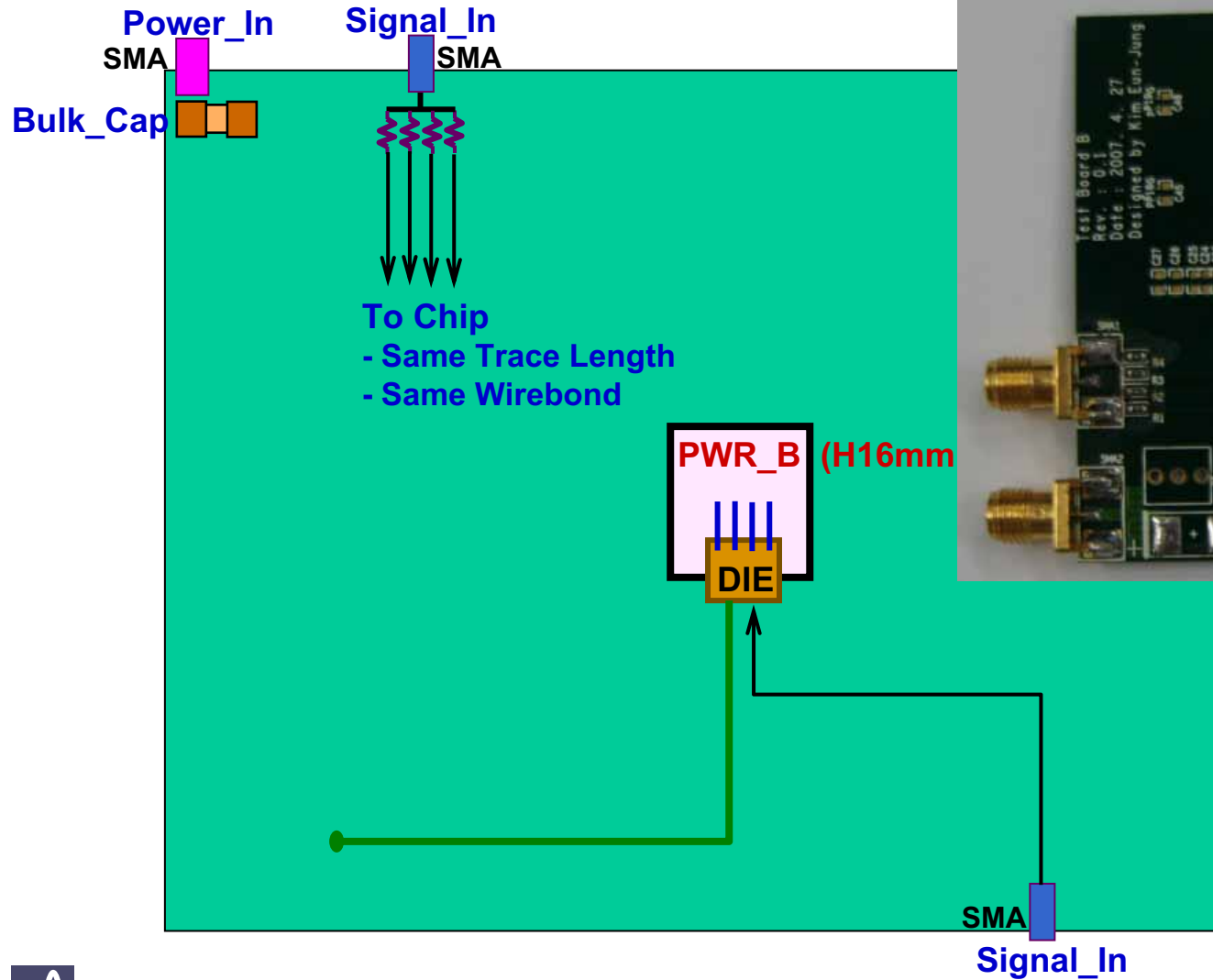


TYPE	H x V (mm)	P/G Height (mm)	Dielectric	Plane Capacitance
IC	2.4 x 2.4	0.00137	SiO2 (Er:4.0)	≐ 149pF
PKG	18 x 18	0.1	FR4 (Er:4.0)	≐ 115pF
PCB	80 x 50	1.0	FR4 (Er:4.0)	≐ 142pF

# SIwave Simulation for Plane Capacitance



# Test Board Design for Co-simulation



# IC Design for On-chip De-cap Test

## Chip layout for Verification

Hynix 0.25  $\mu\text{m}$  process

I/O voltage ( $V_G$ ) : 3.3V

Gate length : 0.34 $\mu\text{m}$  (for I/O)

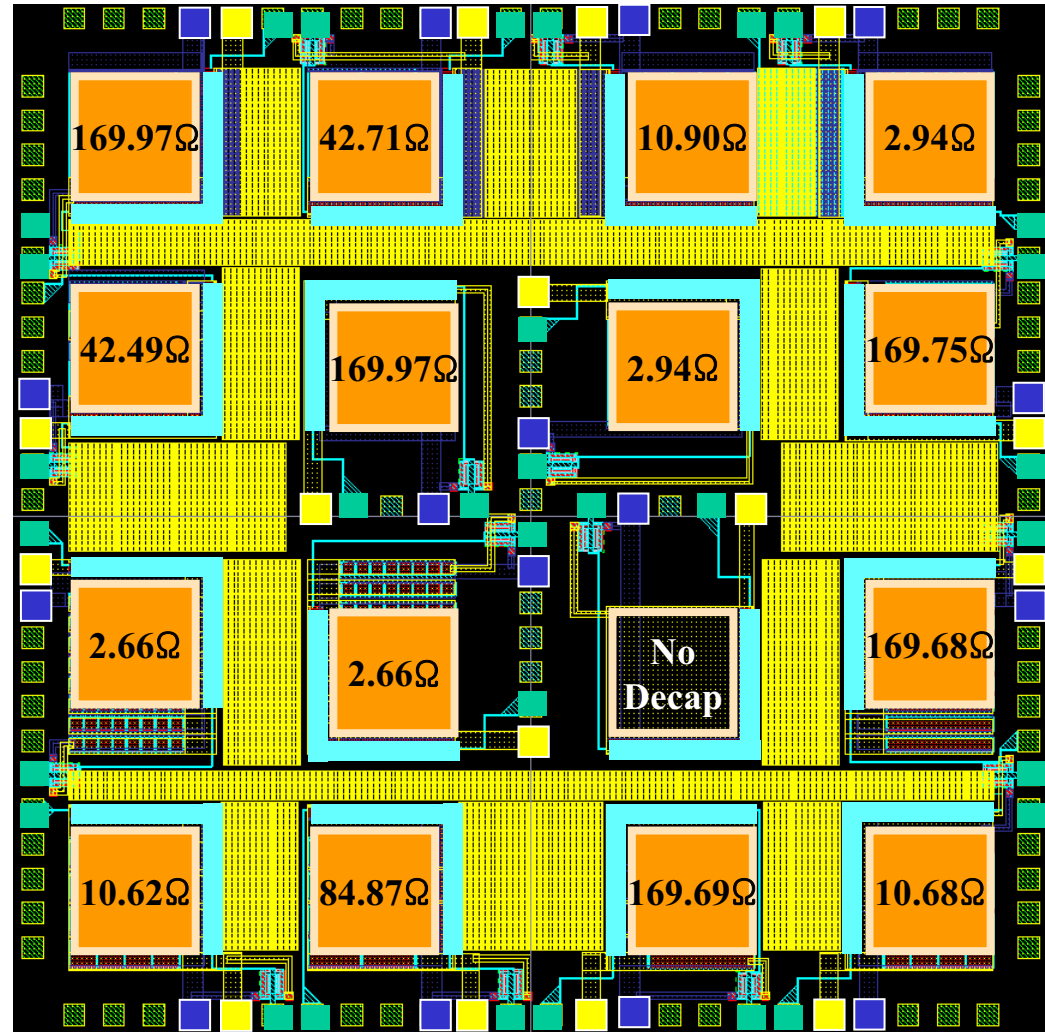
Gate Oxide ( $t_{\text{ox}}$ ) : 71 $\text{\AA}$

$V_T$  : 0.74V

$R_{\text{sheet}}$  : 3.5 $\Omega/\square$

Die Size : 2.4mm x 2.4mm

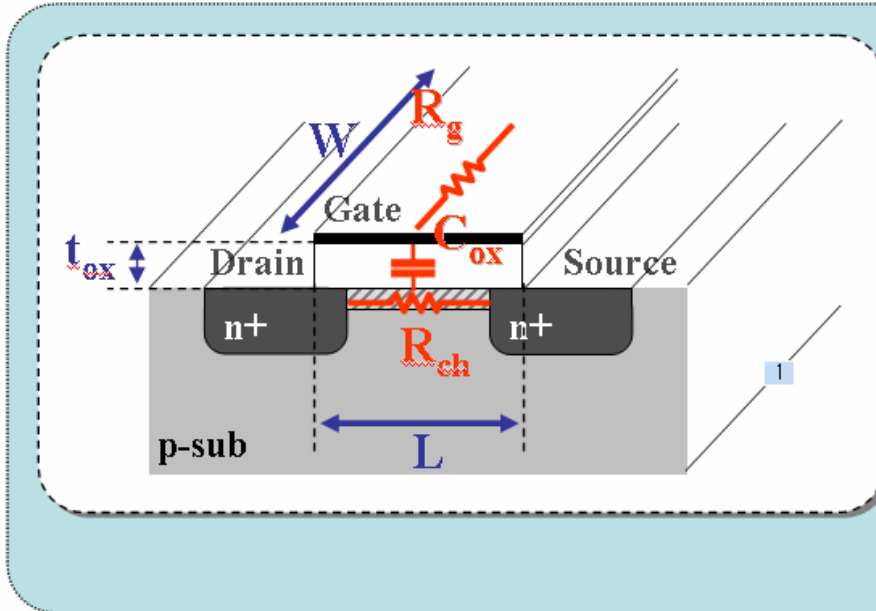
$$C_{\text{total}} = 778.14\text{pF}$$





# Cell Define

## Capacitor design Review



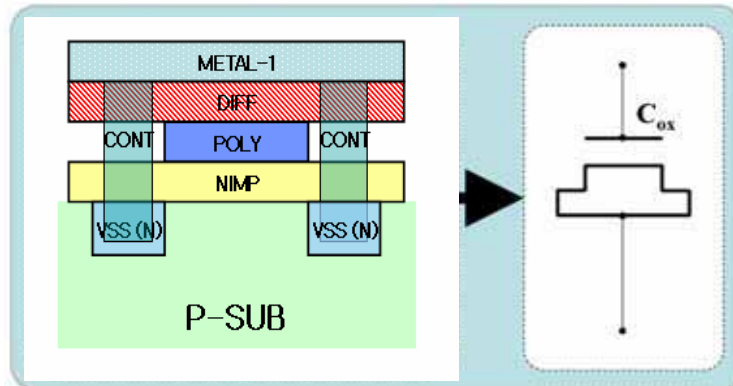
$$C_{ox} = \frac{\epsilon_{SiO_2} \epsilon_0}{t_{ox}} \times WL$$

$$R_g = R_{Sheet} \times \frac{W}{L}$$

$$R_{ch} = \frac{1}{\mu_n C_{ox,unit\ area} (V_G - V_T)} \times \frac{L}{W}$$

$\sim K\Omega/\square$

$R_{ch}$  will be dominant unless  $W/L$  is big.

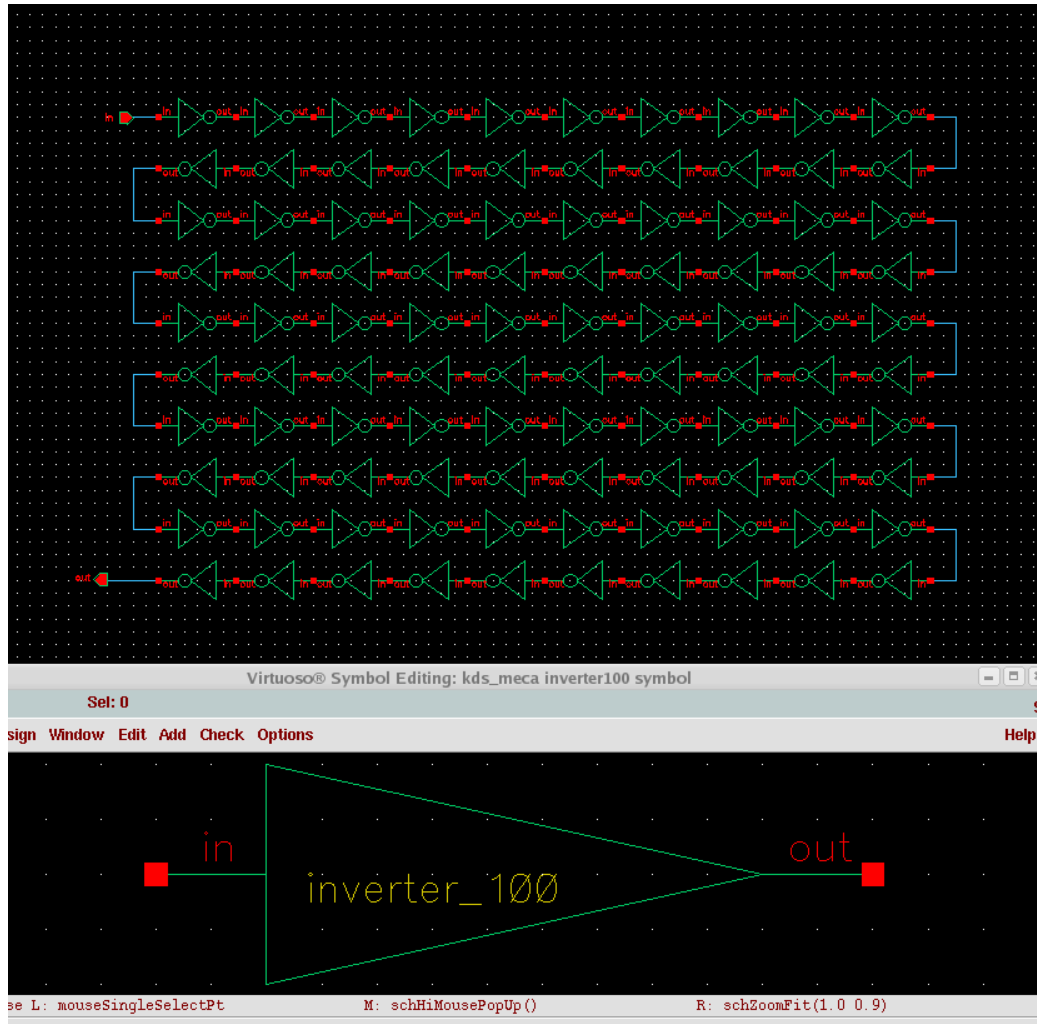


$R_{sheet}$  : gate (ex. poly) sheet resistance  
 $\mu_n$  : electron mobility ( $\sim 300\text{cm}^2/\text{V}\cdot\text{s}$ )  
 $V_G$  : gate bias voltage  
 $V_T$  : threshold voltage

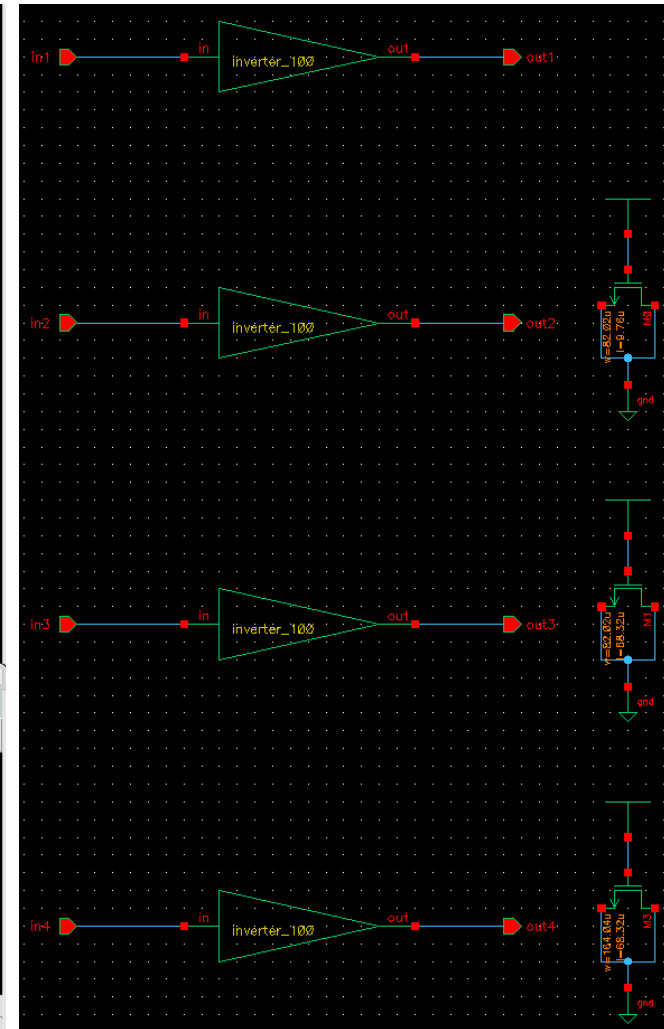
참조 : 박현정 학생 석사 논문

# Schematic with Virtuoso of Cadence

## Inverter 100EA & Symbol



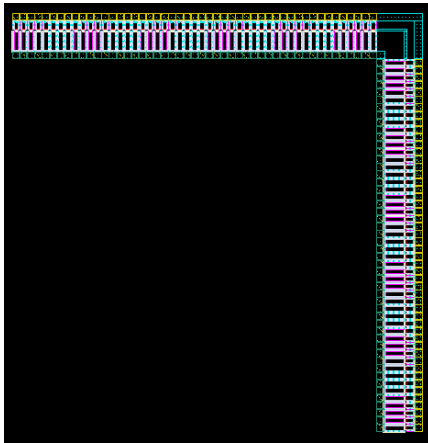
## All Block Schematic



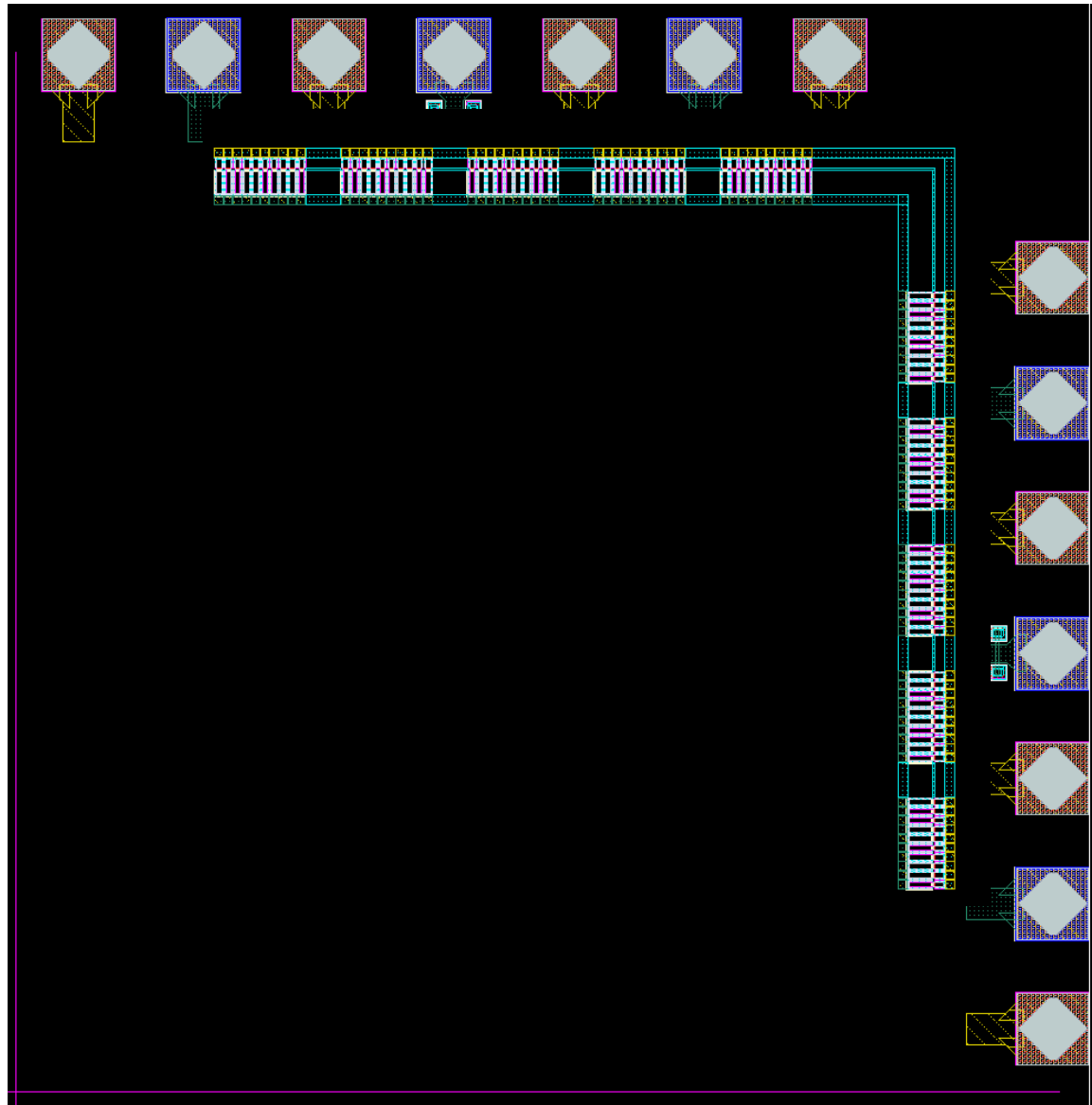
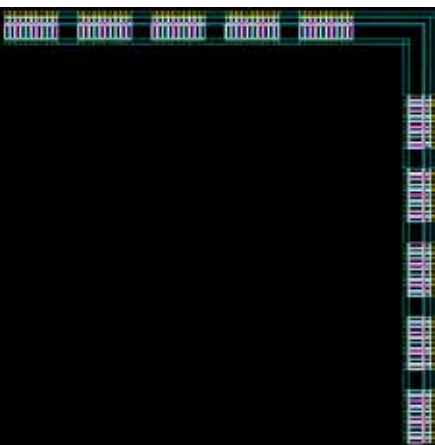
# Layout with Virtuoso of Cadence

## Inverter 100EA

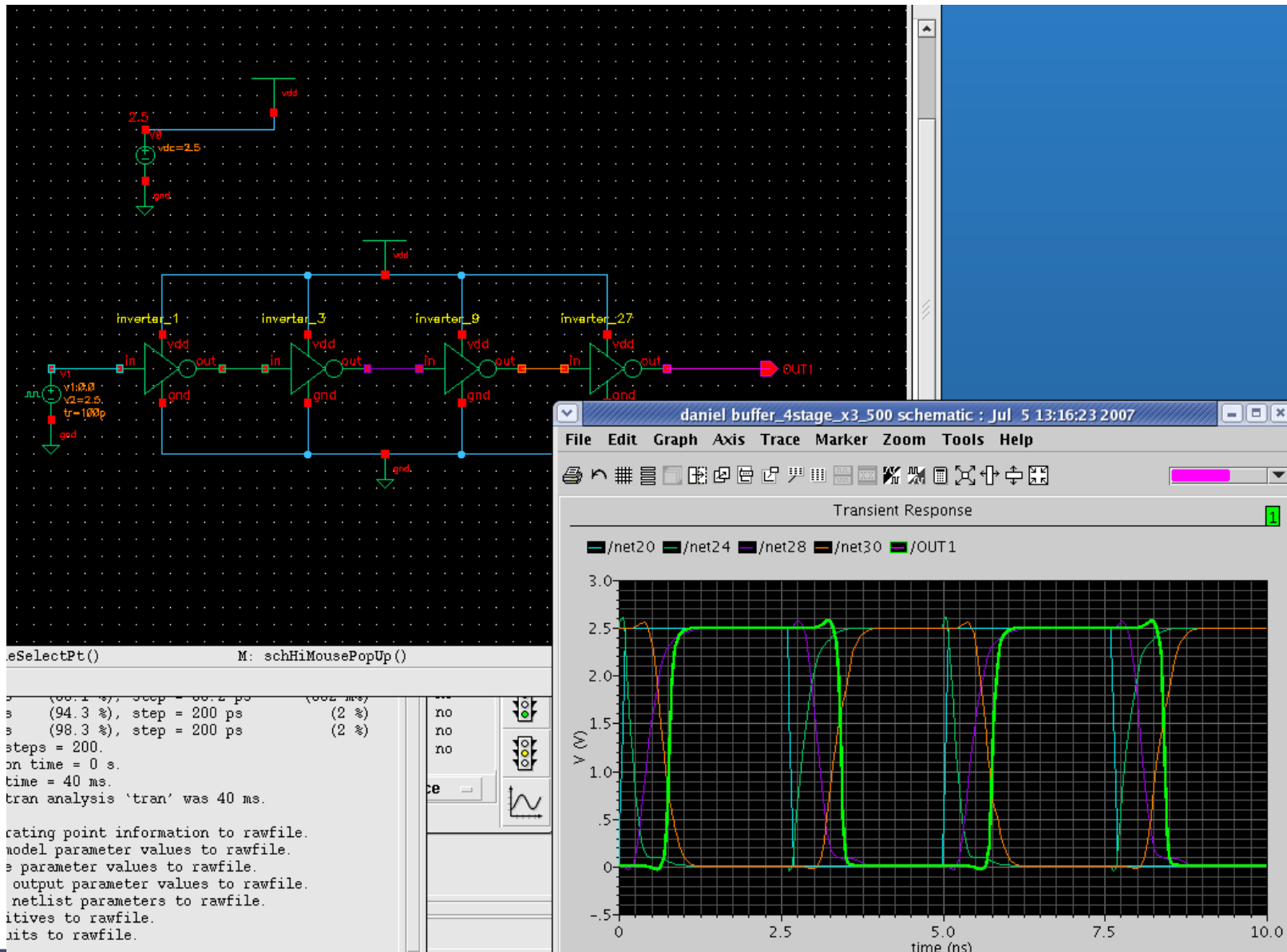
### 1st Inverter 100EA



### 2nd Inverter 100EA

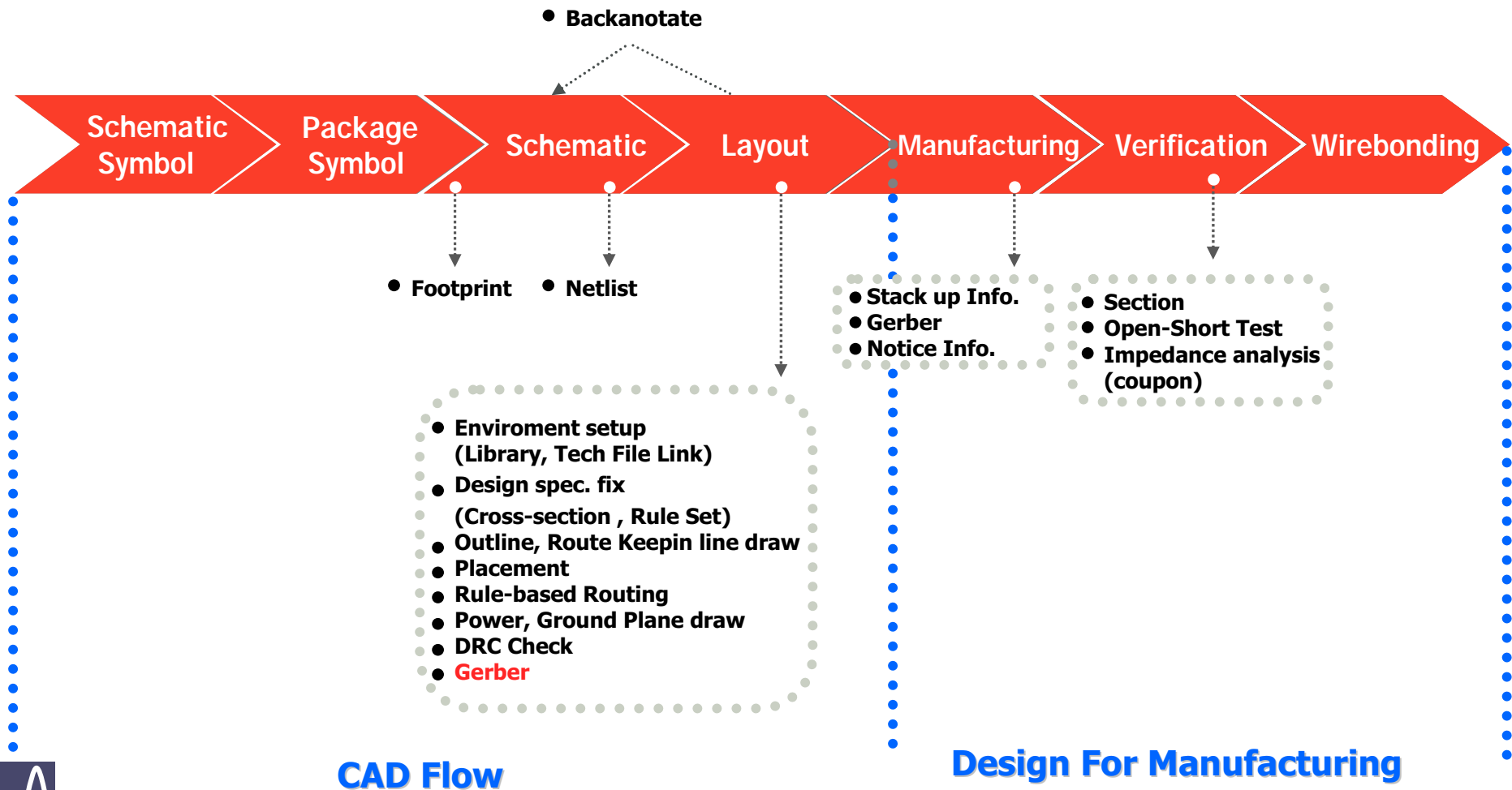


# 2.5V CMOS Inverter with 4 stage of 0.5u, 3x @200M

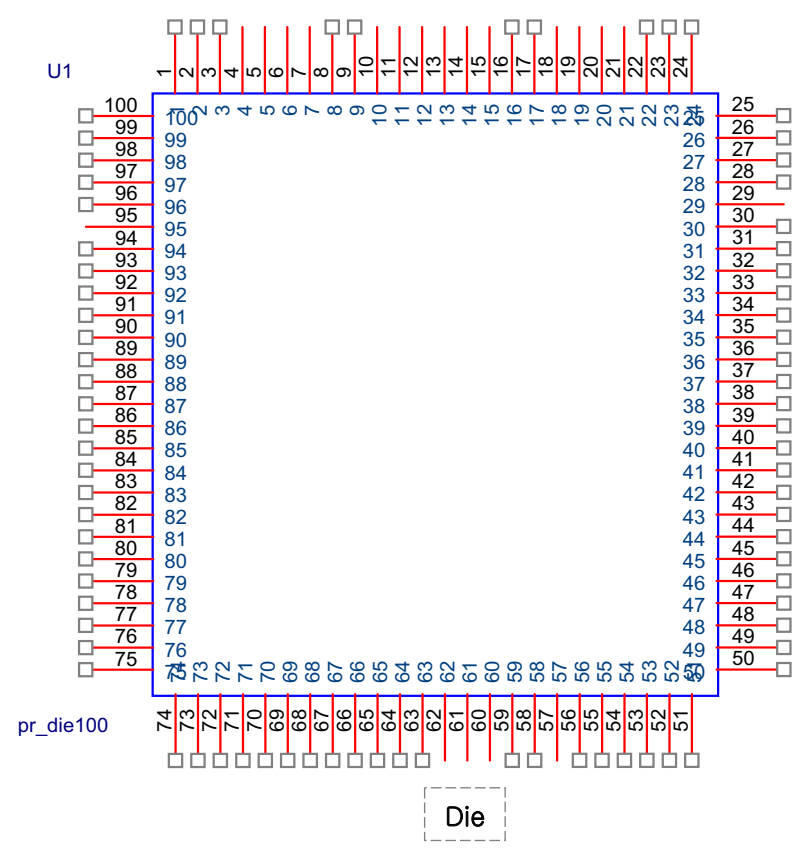
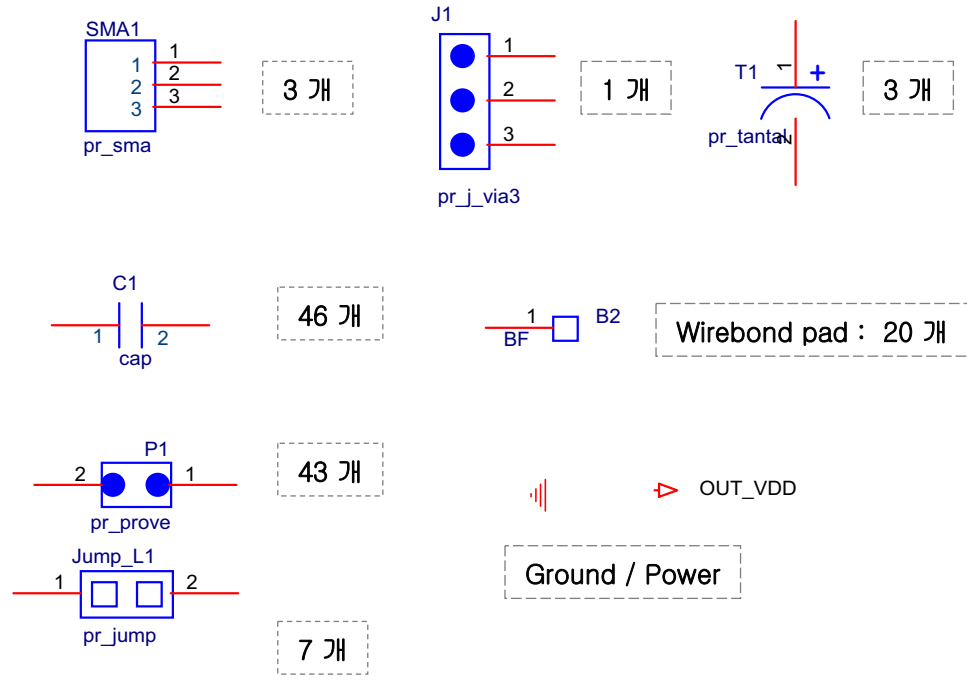


# Package Design Process with Cadence Tool

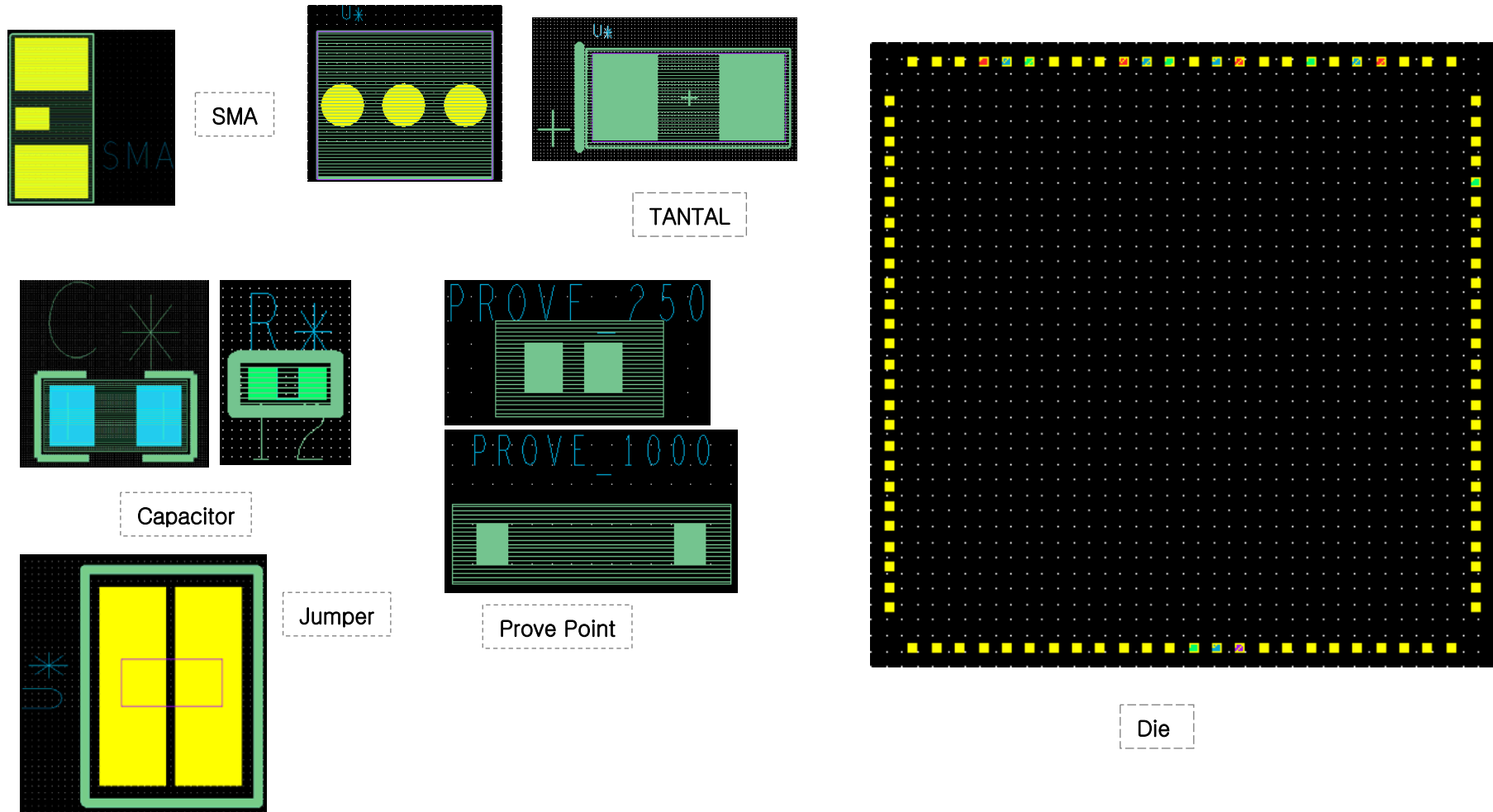
- Allegro Design Entry CIS (schematic)
- Allegro PCB Editor (layout)



# Schematic Symbol

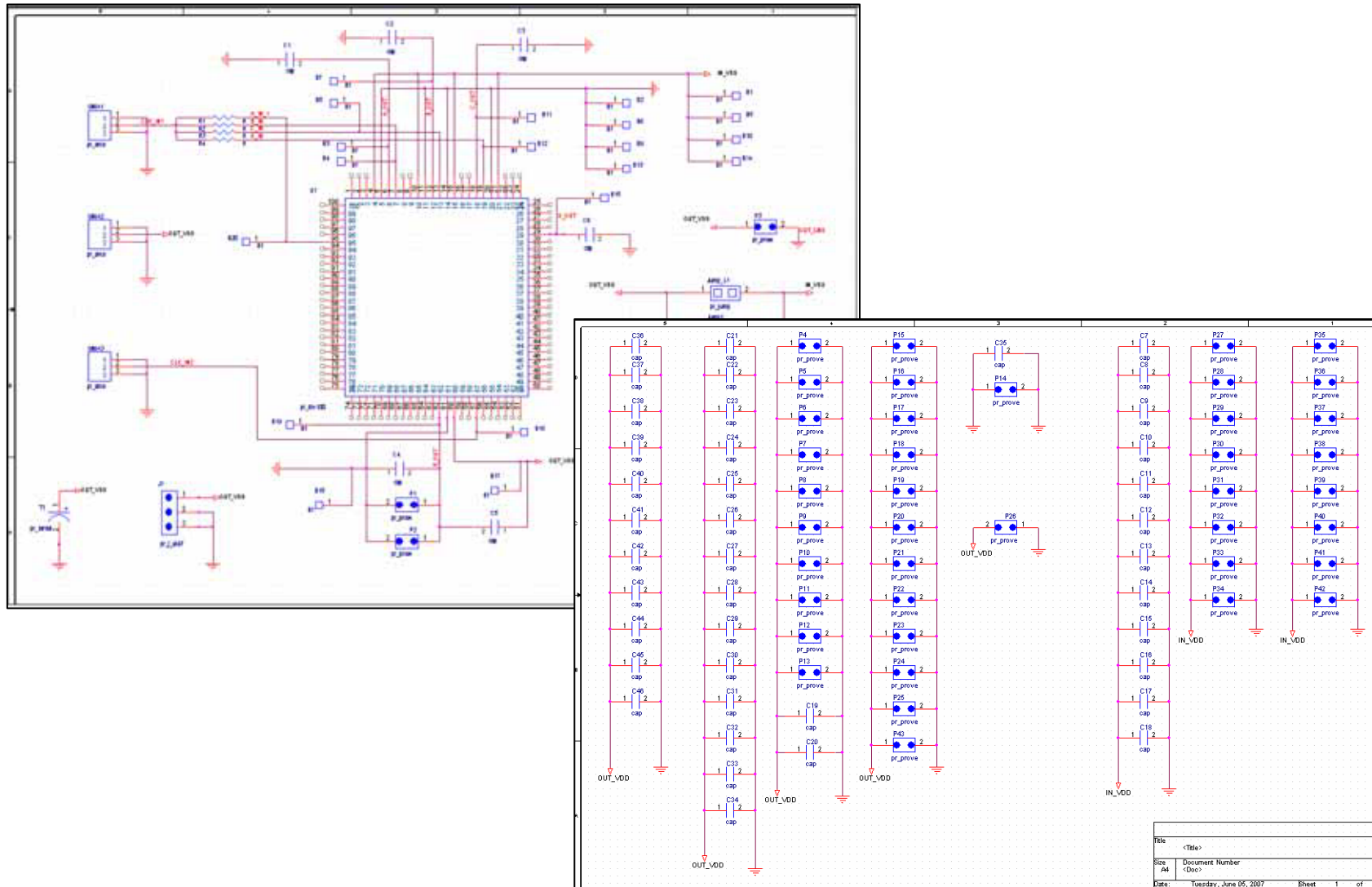


# Package Symbol



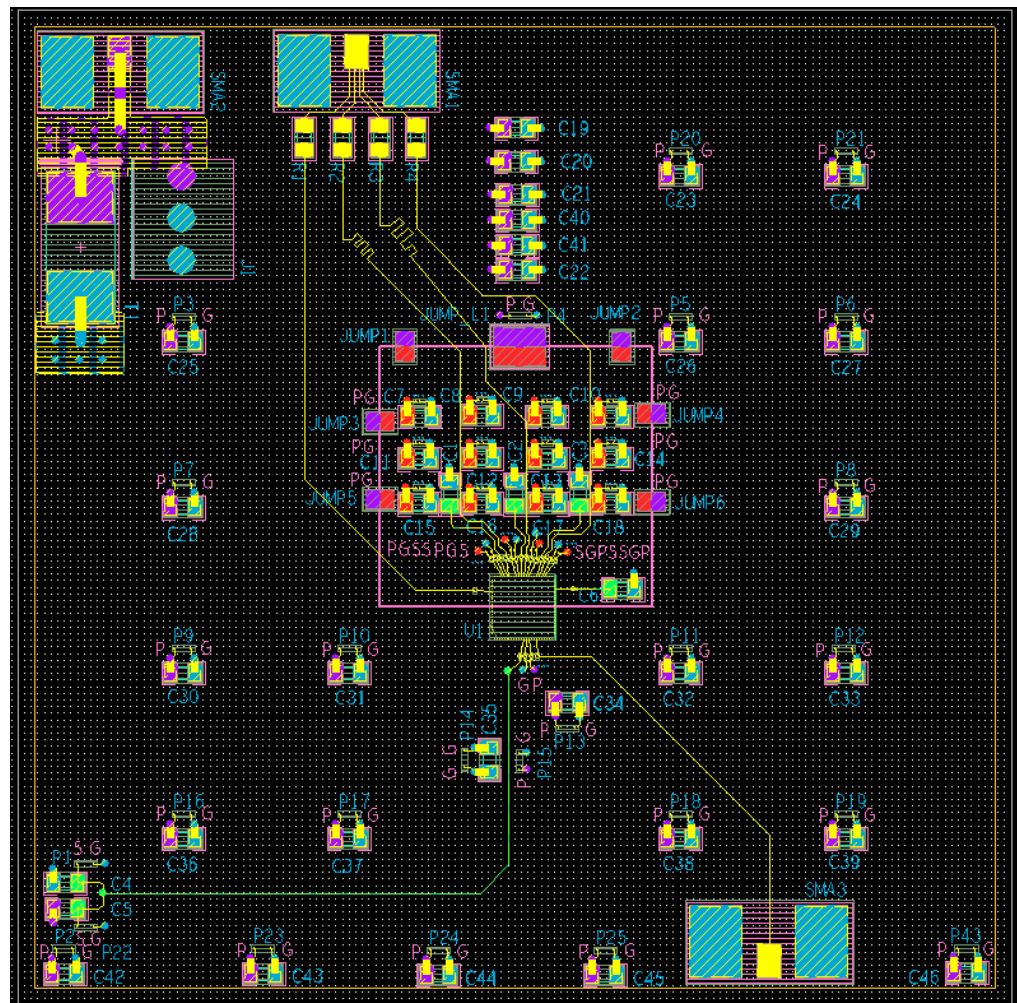
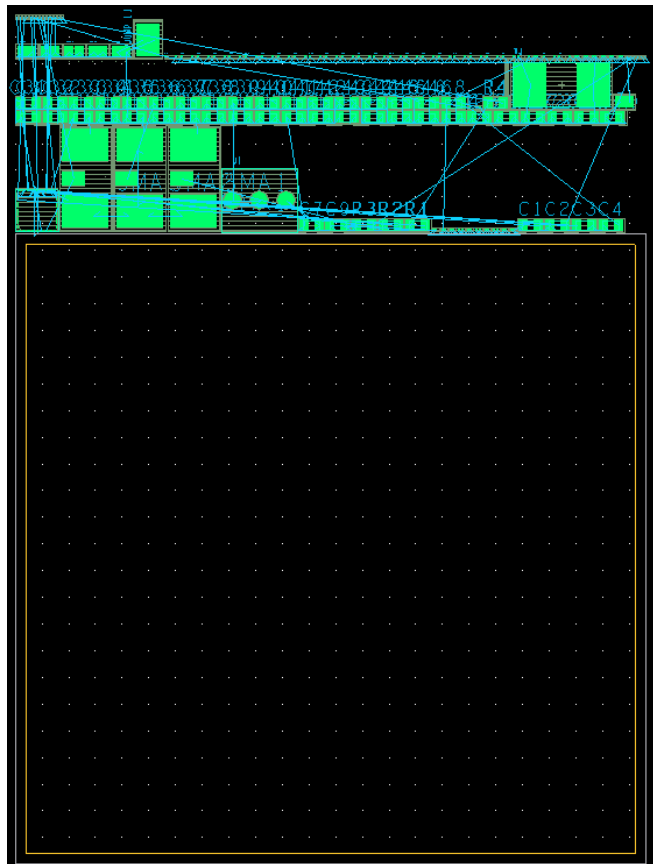
# Schematic

Schematic Symbol    Package Symbol    **Schematic**    Layout    Manufacturing    Verification    Wirebonding





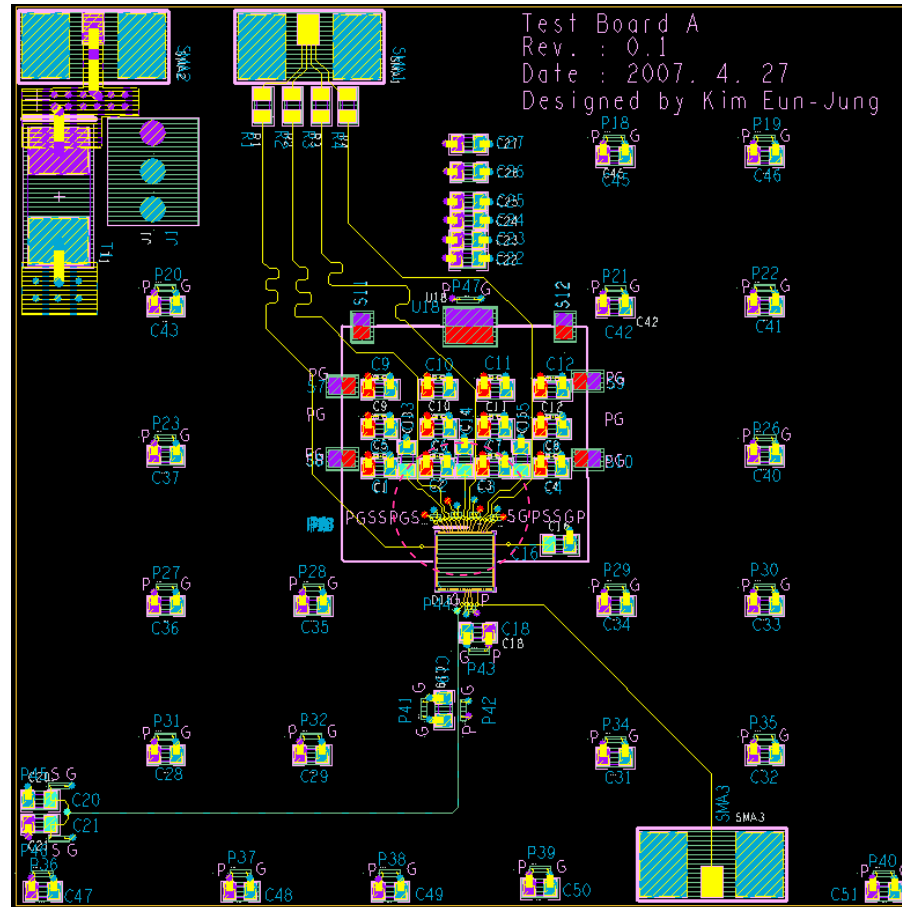
# Layout



# Layout (Test Board-A)

Schematic Symbol Package Symbol Schematic Layout Manufacturing Verification Wirebonding

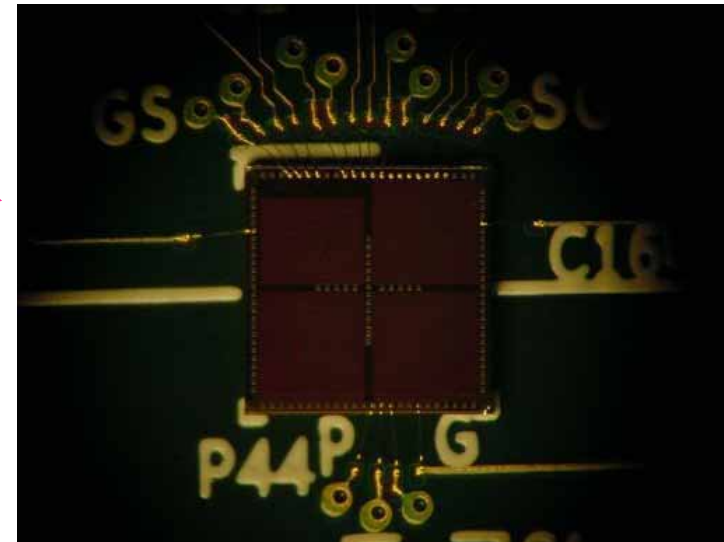
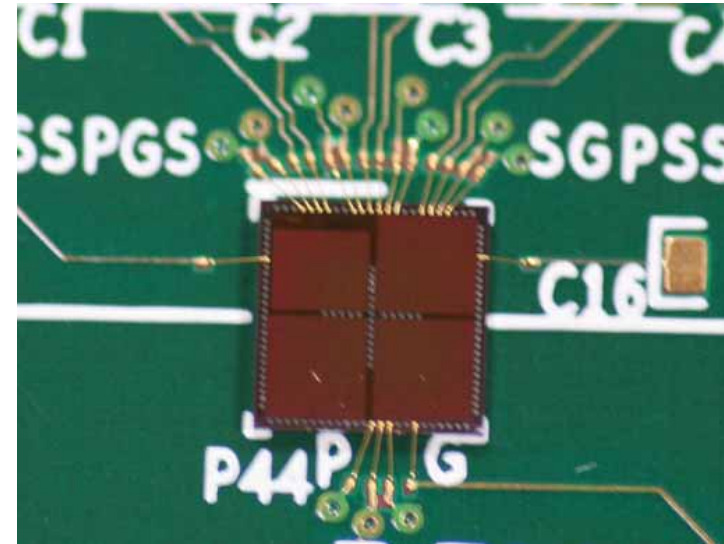
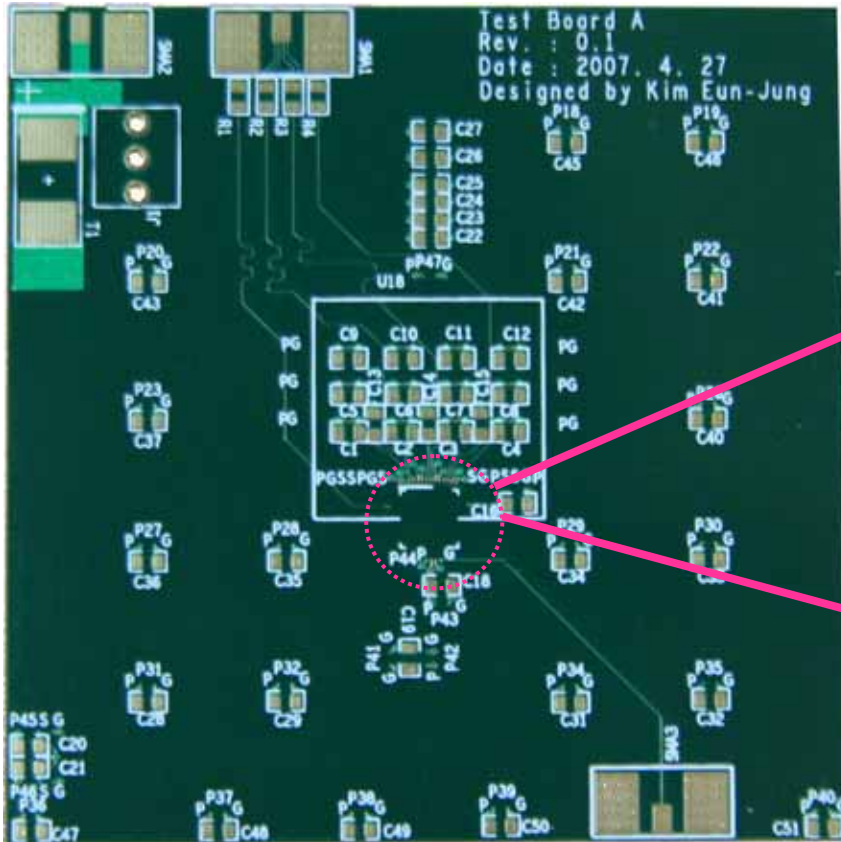
## Test board A



# Test Board and Wire Bond

## Test board A

Wire length = 1.0 mm



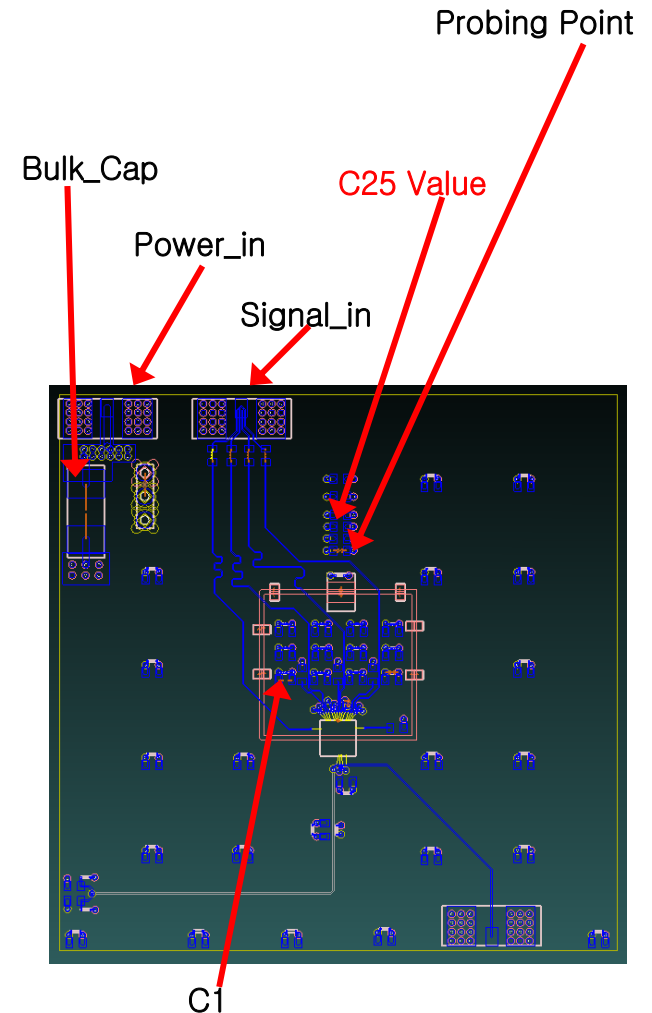
# PI analysis related to De-cap Value

## ◆ Test Condition

### ➤ Test Board A

- ✓ C25; 100pF, 1nF, 10nF, 100nF
- ✓ C1; 1nF
- ✓ Bulk Cap; 330uF
- ✓ DC: 3.3V
- ✓ Signal; 1 V, Tr 2.5nS, 50MHz Square Wave

### ➤ Probing Point (C22); Z plot



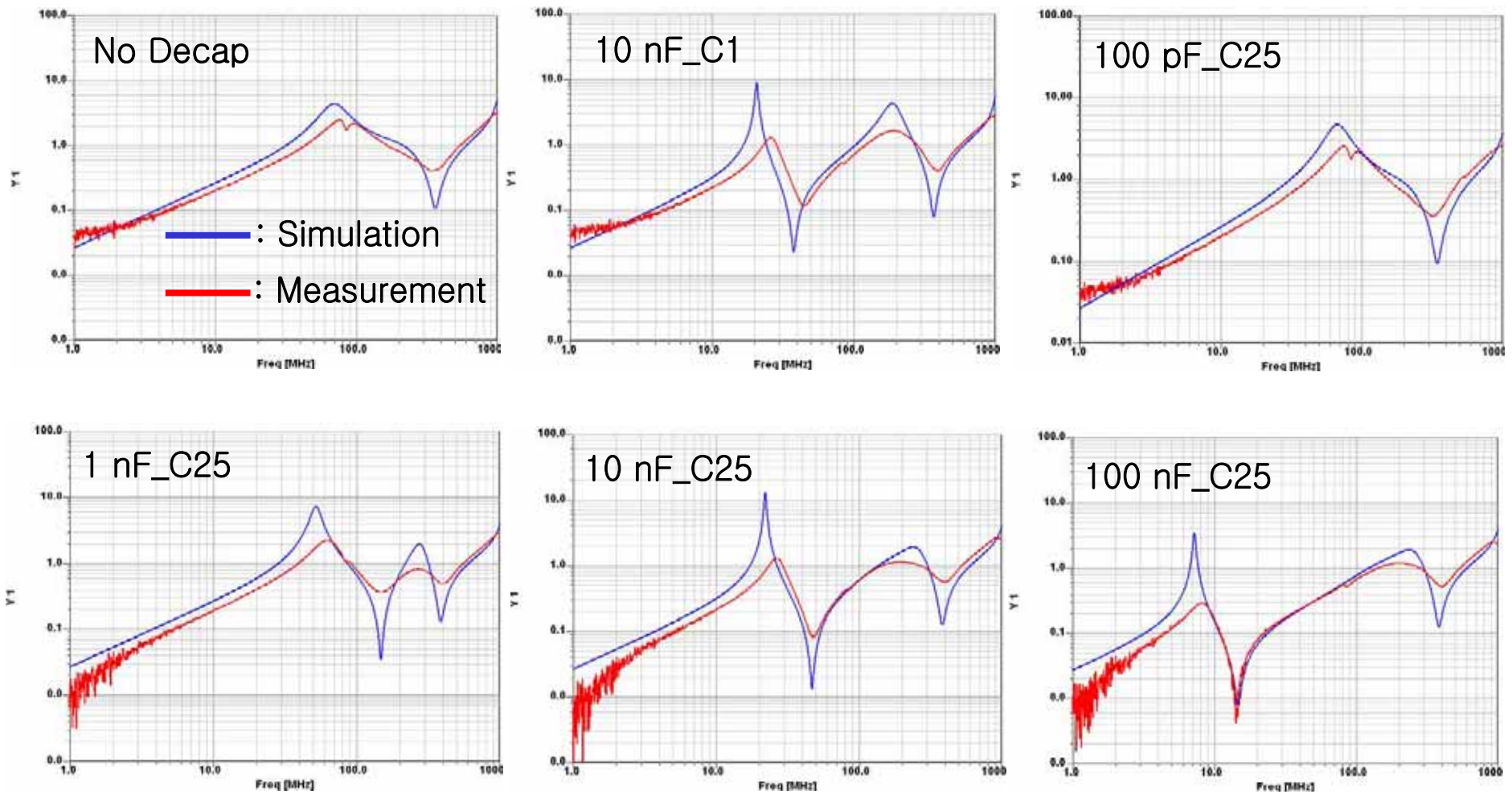
# PI analysis related to De-cap Value

The screenshot shows a circuit simulation software interface. The main window displays a PCB layout with various components including resistors (R1, R2, R3, R4), capacitors (C1 through C29), and a die. A 'Circuit Element Properties' dialog box is open, showing a table of capacitor properties. The table has columns for Active, Part Number, Reference Designator, Capacitance, Parasitic Inductance, Parasitic Resistance, Positive Terminal, Negative Terminal, and Capacitance. The row for capacitor C25 is highlighted, indicating it is selected.

Active	Part Nu...	RefDes	Capacitance...	Parasitic ...	Parasitic R (...)	Positive Termina...	Negative Termin...	Capacito
<input checked="" type="checkbox"/>	No	C0603	C20	1E-007	1E-009	0.0001	E_OUT	OUT_GND
<input checked="" type="checkbox"/>	No	C0603	C21	1E-007	1E-009	0.0001	E_OUT	OUT_VDD
<input checked="" type="checkbox"/>	No	C0603	C22	1E-007	1E-009	0.0001	OUT_GND	OUT_VDD
<input checked="" type="checkbox"/>	No	C0603	C23	1E-007	1E-009	0.0001	OUT_GND	OUT_VDD
<input checked="" type="checkbox"/>	No	C0603	C24	1E-007	1E-009	0.0001	OUT_GND	OUT_VDD
<input checked="" type="checkbox"/>	Yes	C0603	C25	1E-007	1E-009	0.0001	OUT_GND	OUT_VDD
<input checked="" type="checkbox"/>	No	C0603	C26	1E-007	1E-009	0.0001	OUT_GND	OUT_VDD
<input checked="" type="checkbox"/>	No	C0603	C27	1E-007	1E-009	0.0001	OUT_GND	OUT_VDD
<input checked="" type="checkbox"/>	No	C0603	C28	1E-007	1E-009	0.0001	OUT_GND	OUT_VDD
<input checked="" type="checkbox"/>	No	C0603	C29	1E-007	1E-009	0.0001	OUT_GND	OUT_VDD

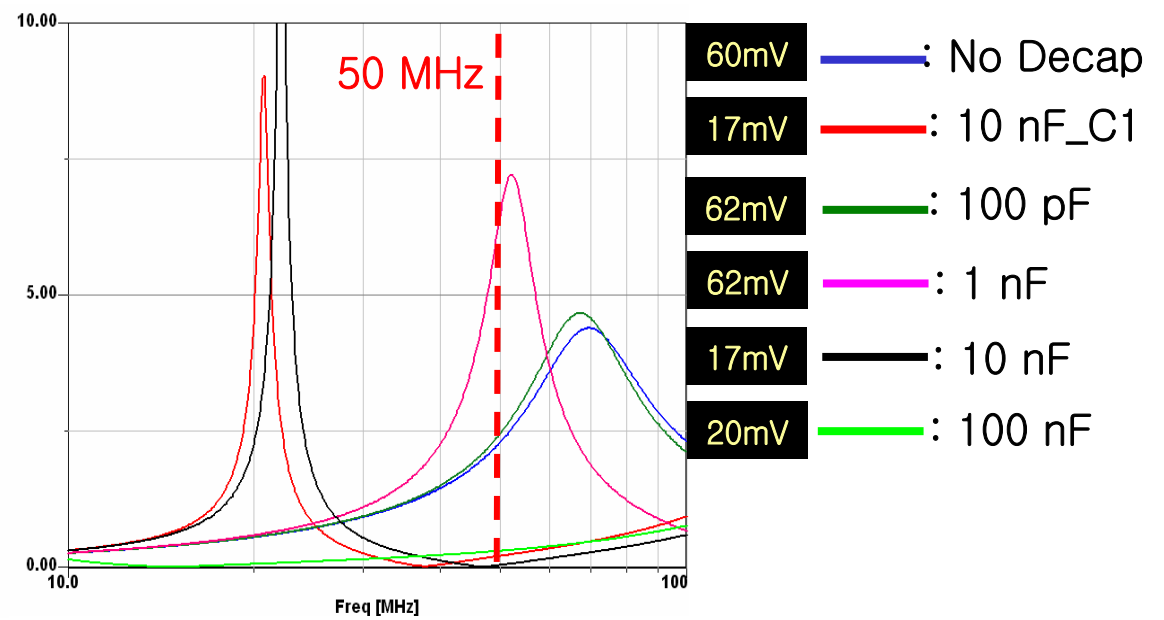
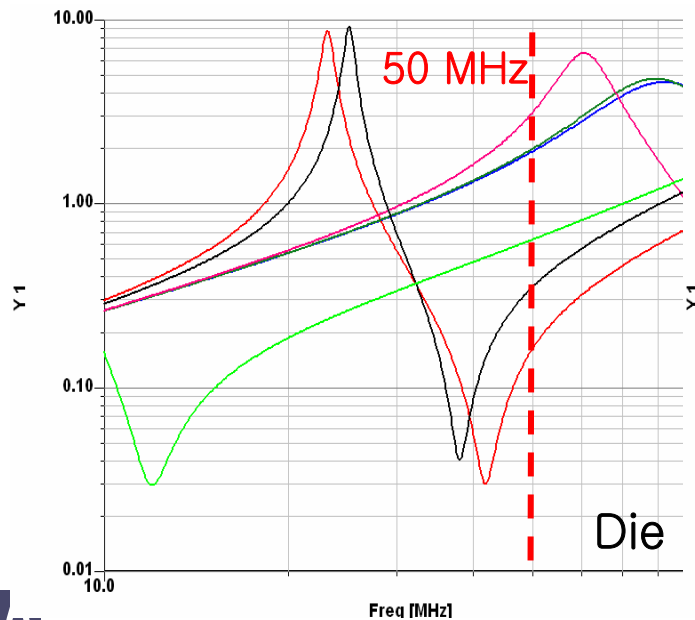
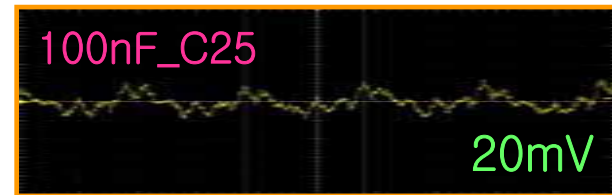
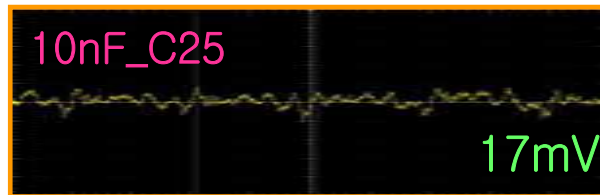
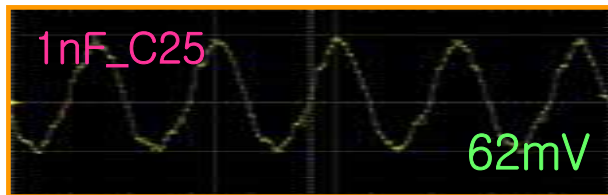
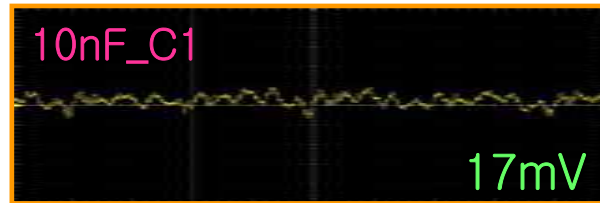
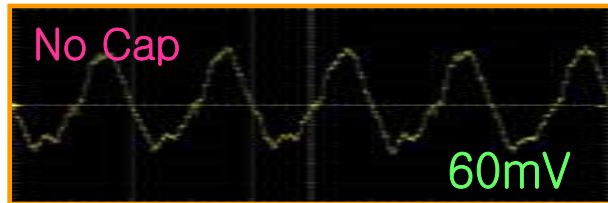
# Simulation & Measurement Result

## ◆ Probing Point(C22); $Z_{11}$ measurement vs Slwave simulation



# Time Domain Measurement vs Simulation

## ◆ Probing Point(C22)



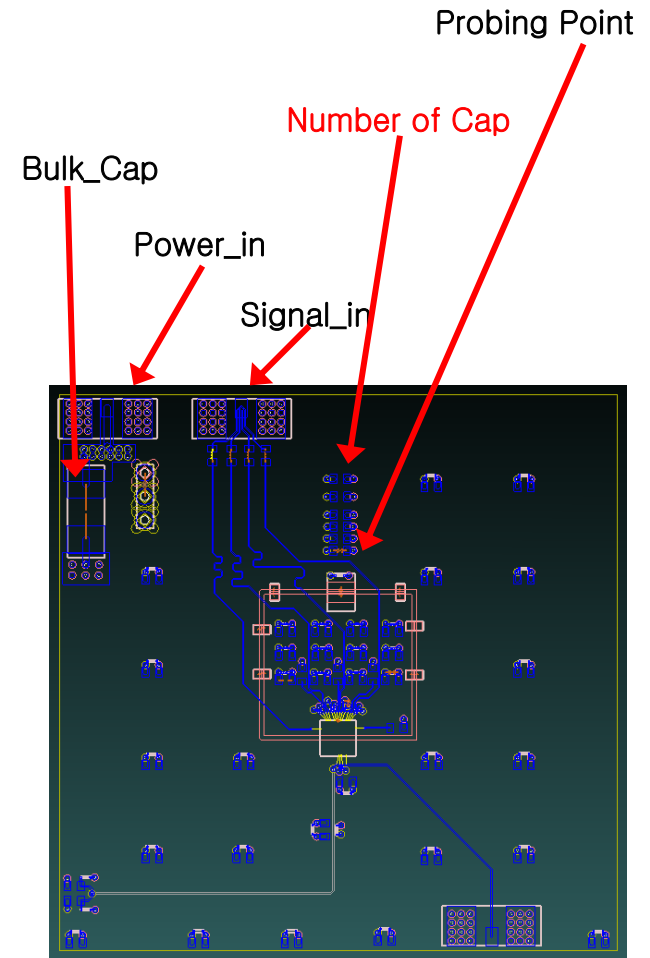
# PI analysis related to Number of Capacitor

## ◆ Test Condition

### ➤ Test Board A

- ✓ 10nF Cap; added to C23/C24/C25/C26/C27
- ✓ Bulk Cap; 330uF
- ✓ DC: 3.3V
- ✓ Signal: 1 V, Tr 2.5nS, 50MHz Square Wave

### ➤ Probing Point (C22); Z plot





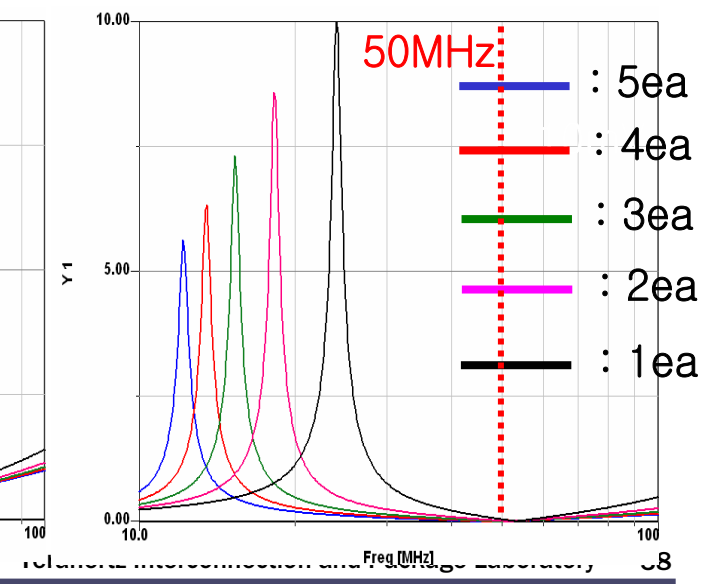
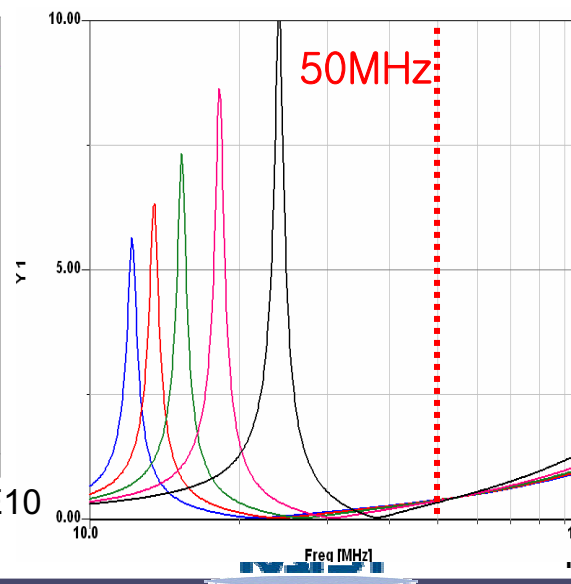
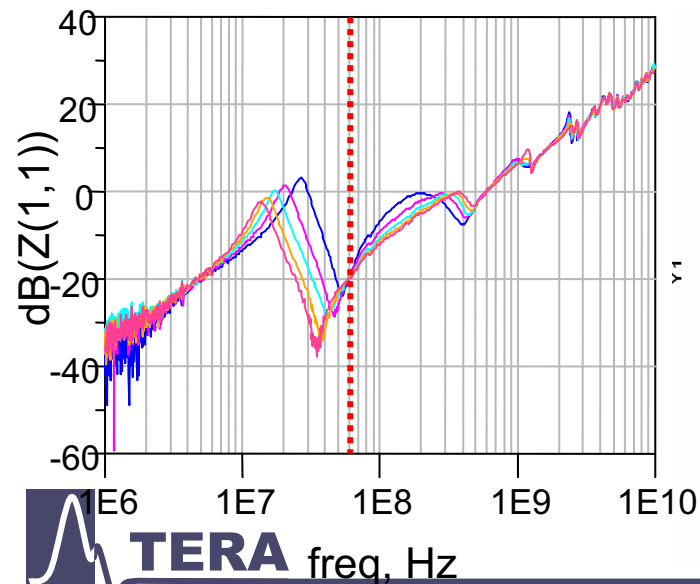
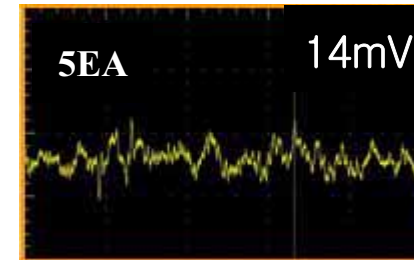
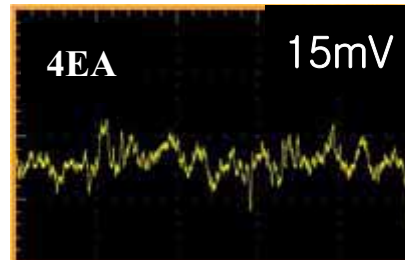
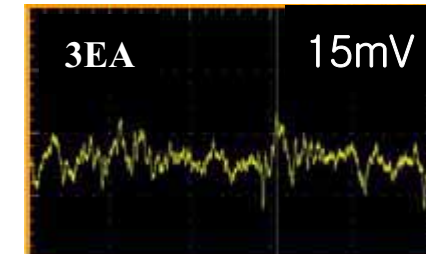
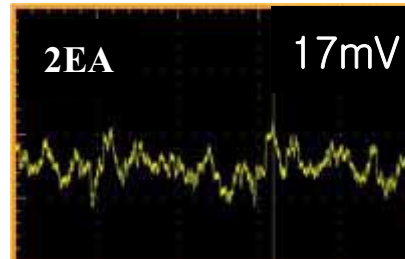
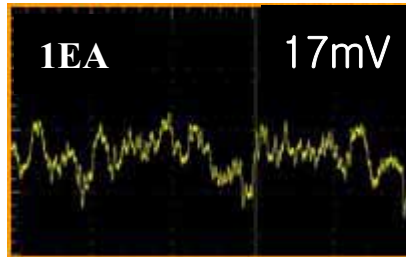
# PI analysis related to Number of Capacitor

The screenshot shows a PCB layout with various components. A dialog box titled 'Circuit Element Properties' is open, showing a table of capacitor properties. The table has columns for Active, Part Number, Reference Designator, Capacitance, Parasitic Inductance, Parasitic Resistance, Positive Terminal, and Negative Terminal. The table lists 11 capacitors, with C20 through C29 highlighted in blue.

Active	Part Nu...	RefDes	Capacitance...	Parasitic ...	Parasitic R (...)	Positive Termina...	Negative Termin...	Capacito
<input checked="" type="checkbox"/>	No	C0603	C20	1E-007	1E-009	0,0001	E_OUT	OUT_GND
<input checked="" type="checkbox"/>	No	C0603	C21	1E-007	1E-009	0,0001	E_OUT	OUT_VDD
<input checked="" type="checkbox"/>	No	C0603	C22	1E-007	1E-009	0,0001	OUT_GND	OUT_VDD
<input checked="" type="checkbox"/>	Yes	C0603	C23	1E-007	1E-009	0,0001	OUT_GND	OUT_VDD
<input checked="" type="checkbox"/>	Yes	C0603	C24	1E-007	1E-009	0,0001	OUT_GND	OUT_VDD
<input checked="" type="checkbox"/>	Yes	C0603	C25	1E-007	1E-009	0,0001	OUT_GND	OUT_VDD
<input checked="" type="checkbox"/>	Yes	C0603	C26	1E-007	1E-009	0,0001	OUT_GND	OUT_VDD
<input checked="" type="checkbox"/>	Yes	C0603	C27	1E-007	1E-009	0,0001	OUT_GND	OUT_VDD
<input checked="" type="checkbox"/>	No	C0603	C28	1E-007	1E-009	0,0001	OUT_GND	OUT_VDD
<input checked="" type="checkbox"/>	No	C0603	C29	1E-007	1E-009	0,0001	OUT_GND	OUT_VDD

# Time Domain Measurement vs Simulation; at 50MHz

## ◆ C22 Probing Point



# Time Domain Measurement vs Simulation; at 30MHz

## ◆ C22 Probing Point

