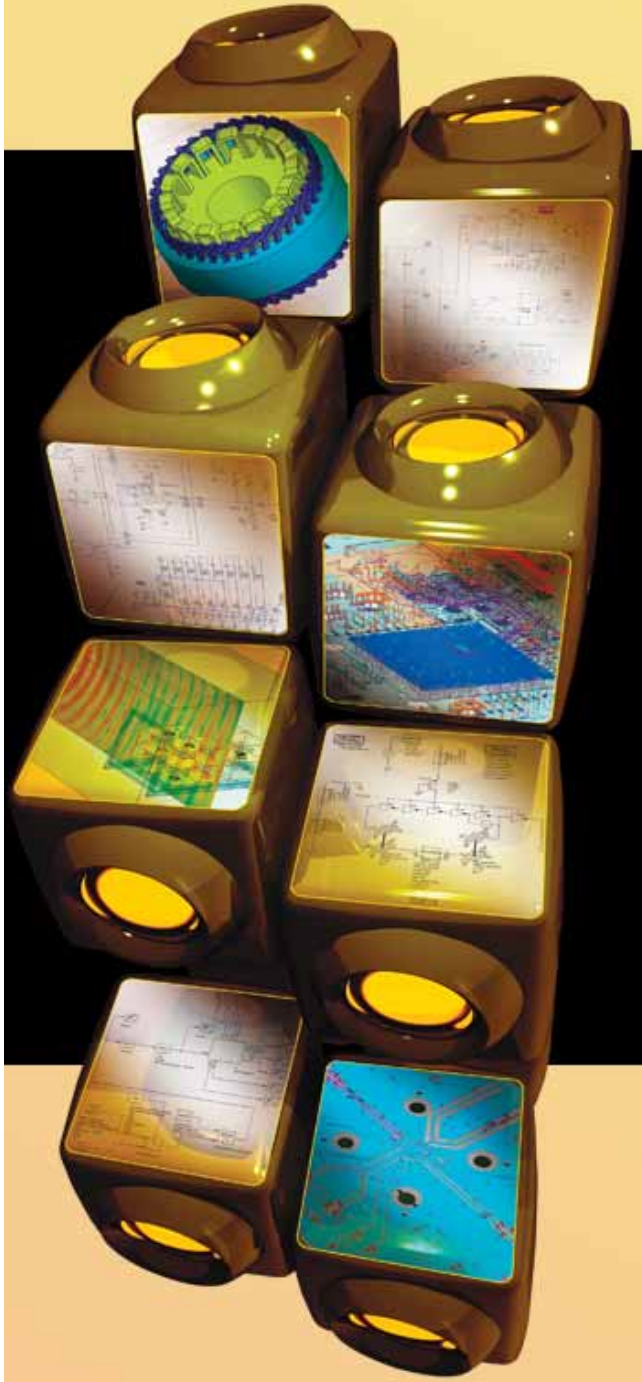

Inspiring Engineering

EMI Driven by PI

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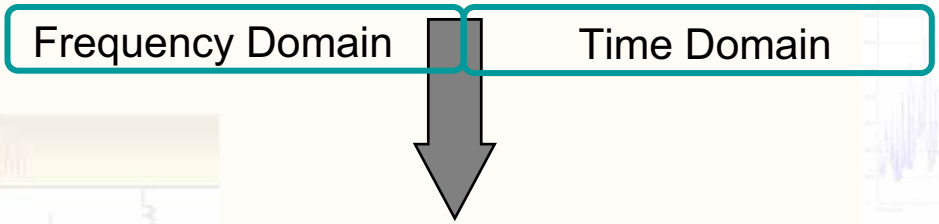
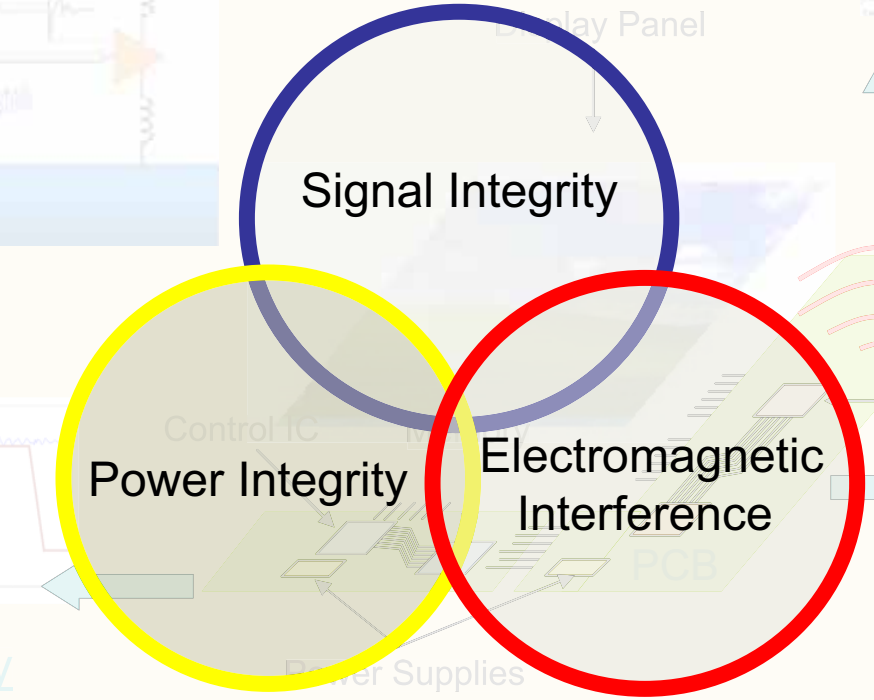
Outline

- SI + PI = EMI
  - These disciplines are no longer independent of each other
- Fundamentals of EMI
  - Where does it come from and how is it minimized
  - Five Step EMC Design Flow
- Power Integrity design methodology to reduce EMI
  - Fundamentals of Power Integrity
  - Design Process to meet design specs in the Time and Frequency domain
- 2nd Presentation on EMI Driven by SI
  - Fundamentals of Signal Integrity
    - Crosstalk is the main contributor to EMI
  - Case studies that show perils of crosstalk in real world designs

SI/PI/EMI Design Overview





Power Integrity
- Switching Noise
- Impedance Profile
- Power/Gnd Plane Resonance
- Decoupling Capacitors

EMI/EMC
- Common mode radiation
- Differential mode radiation

Signal Integrity
- Impedance
- Crosstalk
- Reflection
- Termination
- Dielectric Losses

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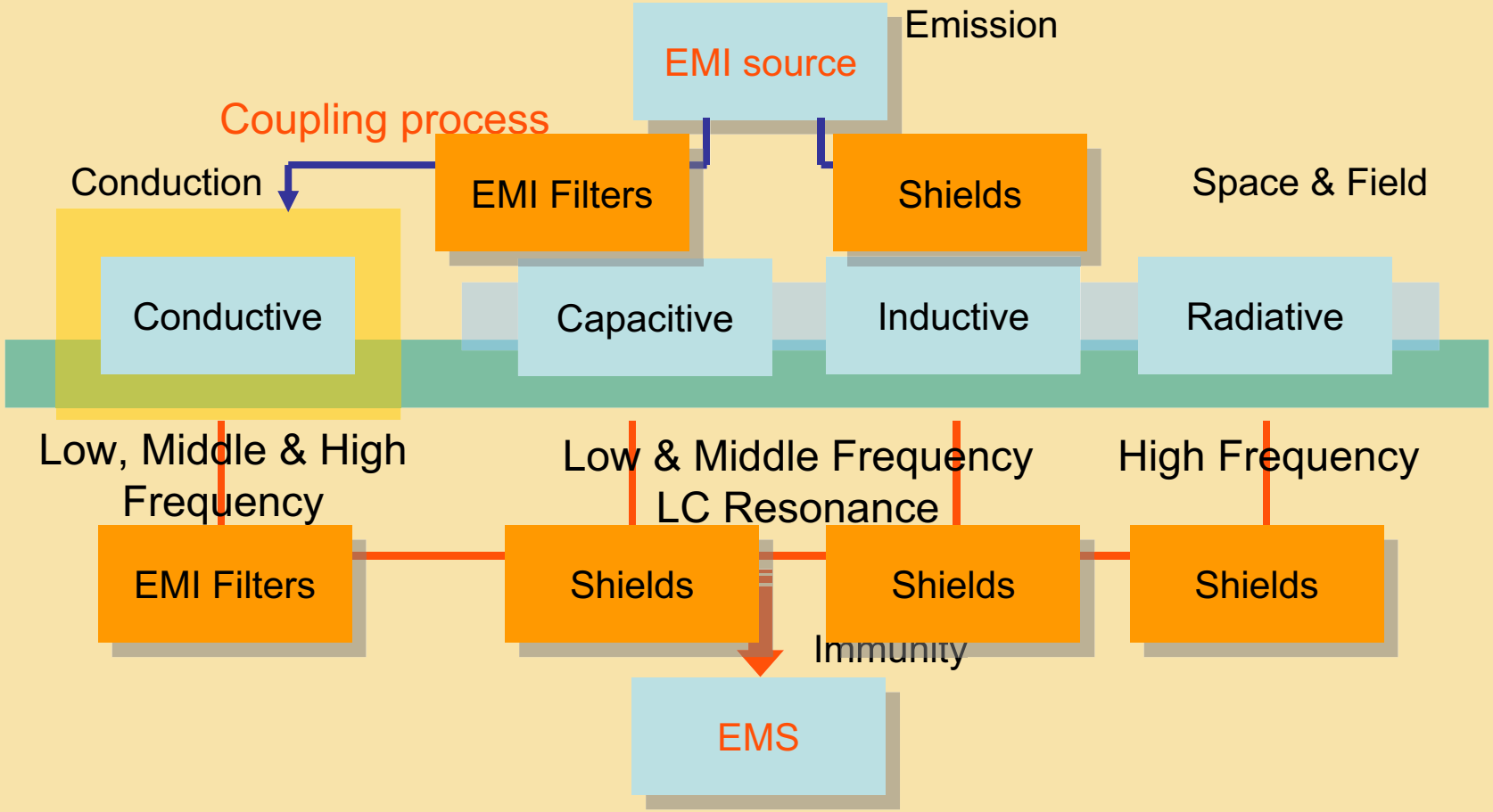
Three Basic Elements of EMC



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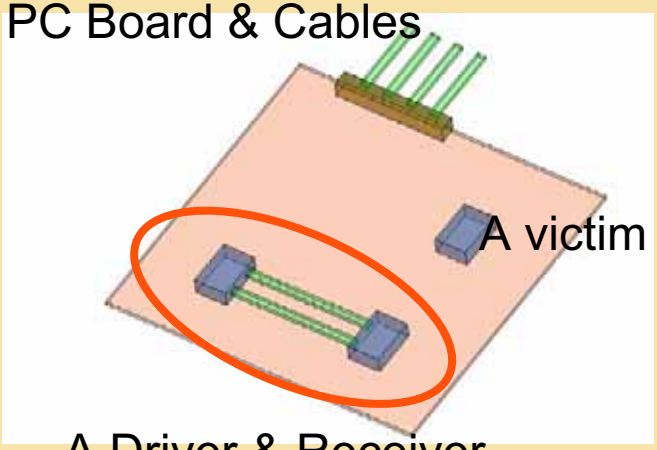
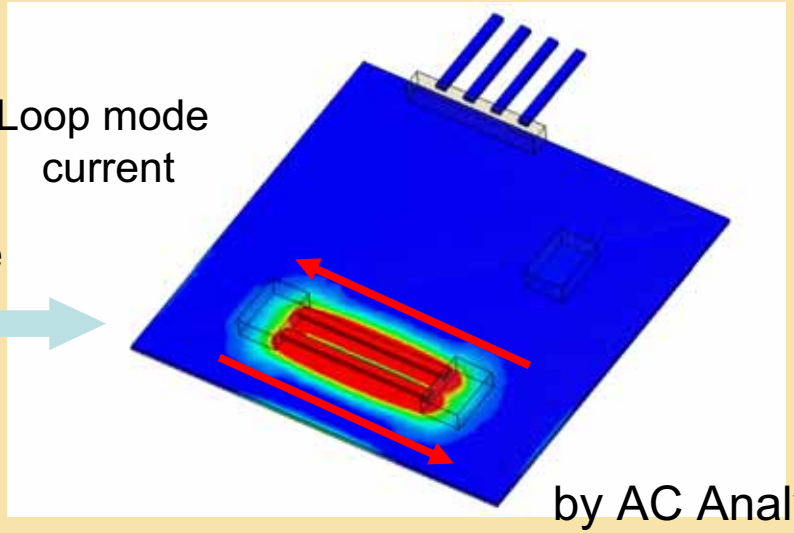
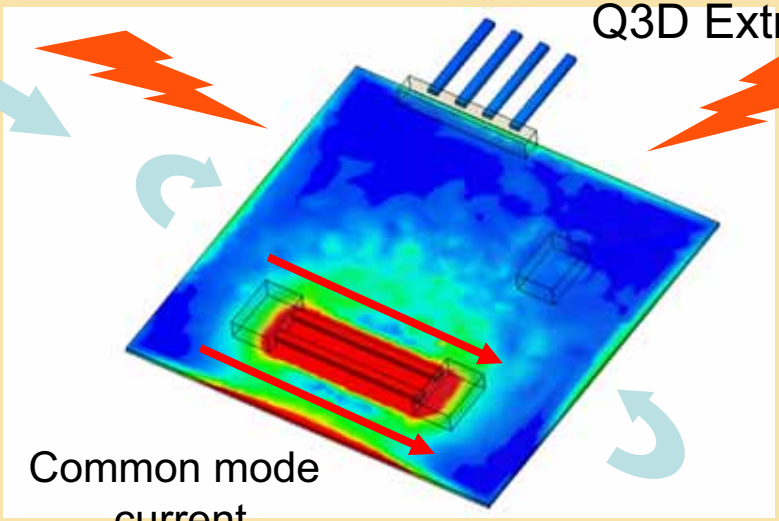
Loop Mode & Common Mode Noise

A PC Board & Cables





by AC Analysis of
Q3D Extractor



Differential mode current flows --- Loop
Common mode current flows --- Open

We can see Common mode current is more serious than Normal mode.

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Antenna theory

-A Differential mode current flow → Loop antenna theory
-A Common mode current flow → Dipole antenna theory

$$E = \frac{131.6 \times 10^{-16} (f^2 AI) \sin\theta}{r}$$

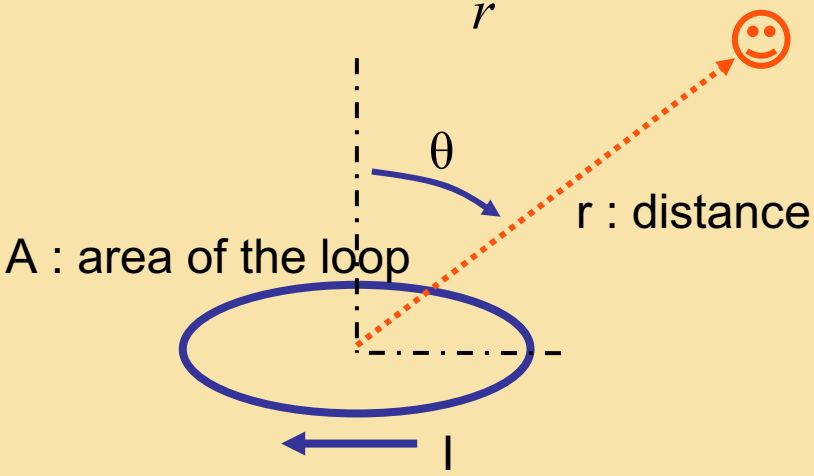

Illustration of a loop antenna

$$E = \frac{4\pi \times 10^{-7} (fIl) \sin\theta}{r}$$

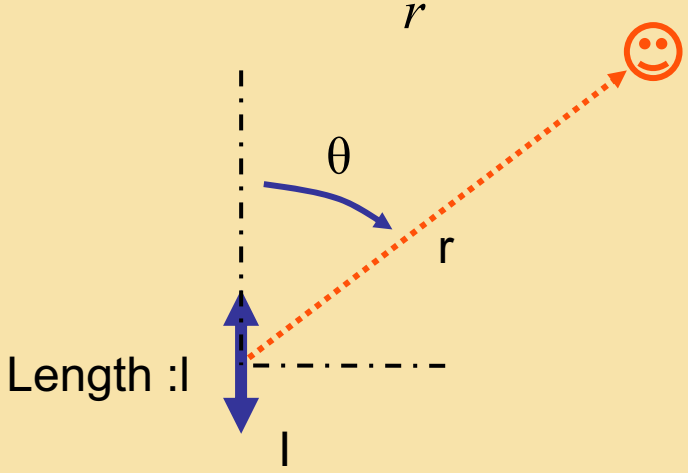

Illustration of a dipole antenna

FCC B level Mag. E limit :40dBuV/m @ 3m
Mag. E(Loop antenna) : 20mA
Mag. E(Dipole antenna) : 8uA

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EMC Design Flow

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Impedance Analysis

Resonance Analysis

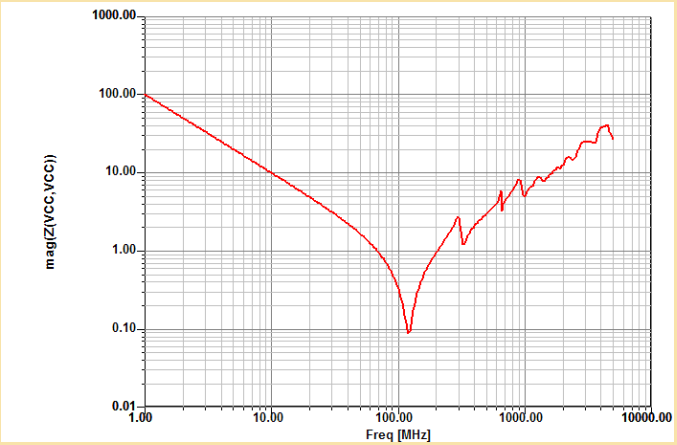
Signal Extraction

Emissions Analysis

Enclosure Simulation

Planes deliver power to ICs and return path for signal

Ensure that Plane impedance is smooth and low over broad frequency range



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EMC Design Flow

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Impedance Analysis

Resonance Analysis

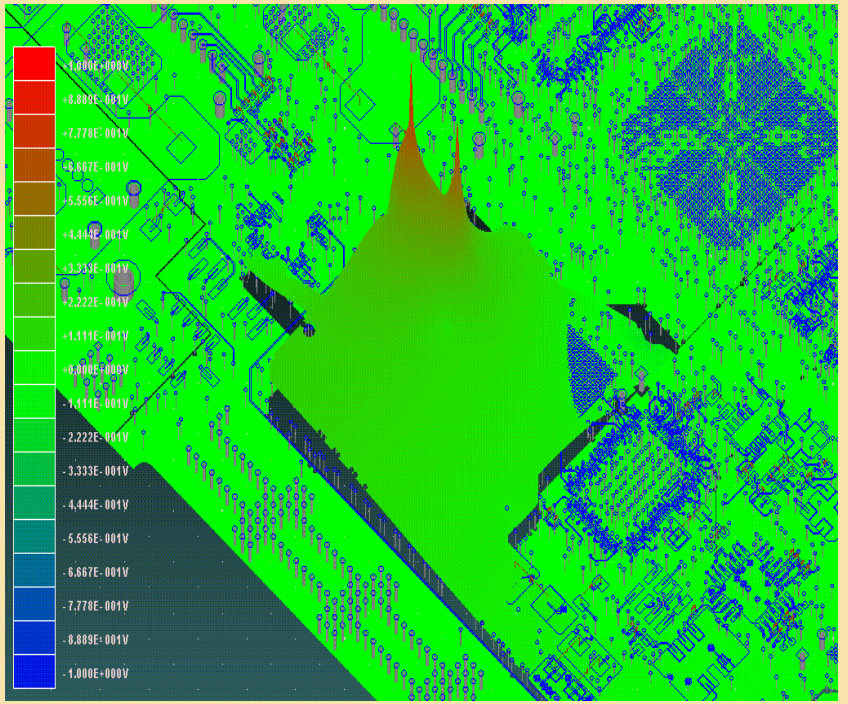
Signal Extraction

Emissions Analysis

Enclosure Simulation

Resonances indicate areas of high impedance and EMI potential

Ensure power planes do not resonant in critical locations



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EMC Design Flow

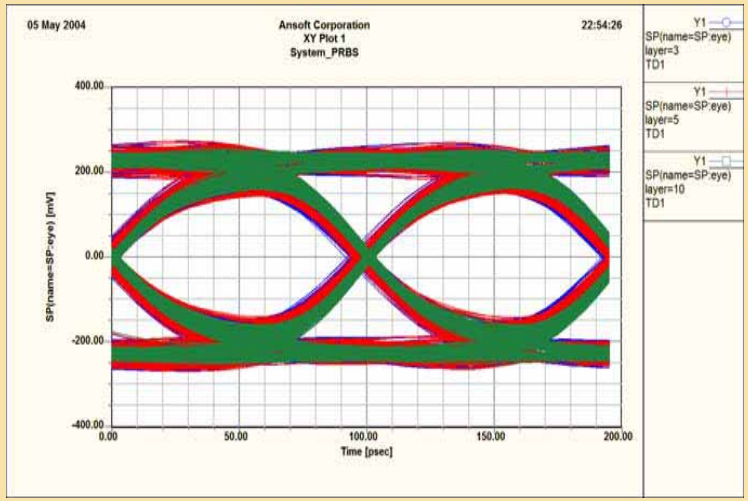
Impedance Analysis

Resonance Analysis

Signal Extraction

Emissions Analysis

Enclosure Simulation



If signal is not at the receiver, it went somewhere else

Ensure clean signal transmission and good return path for critical nets

Inspiring Engineering

EMC Design Flow

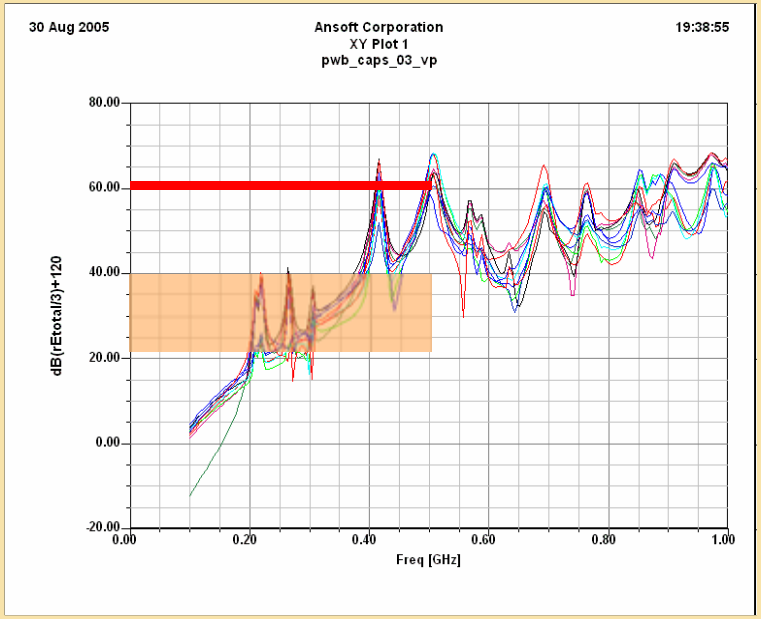
Impedance Analysis

Resonance Analysis

Signal Extraction

Emissions Analysis

Enclosure Simulation



Non-ideal planes and tight routing can lead to unintentional signals

Ensure there are no unintentional radiators

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EMC Design Flow

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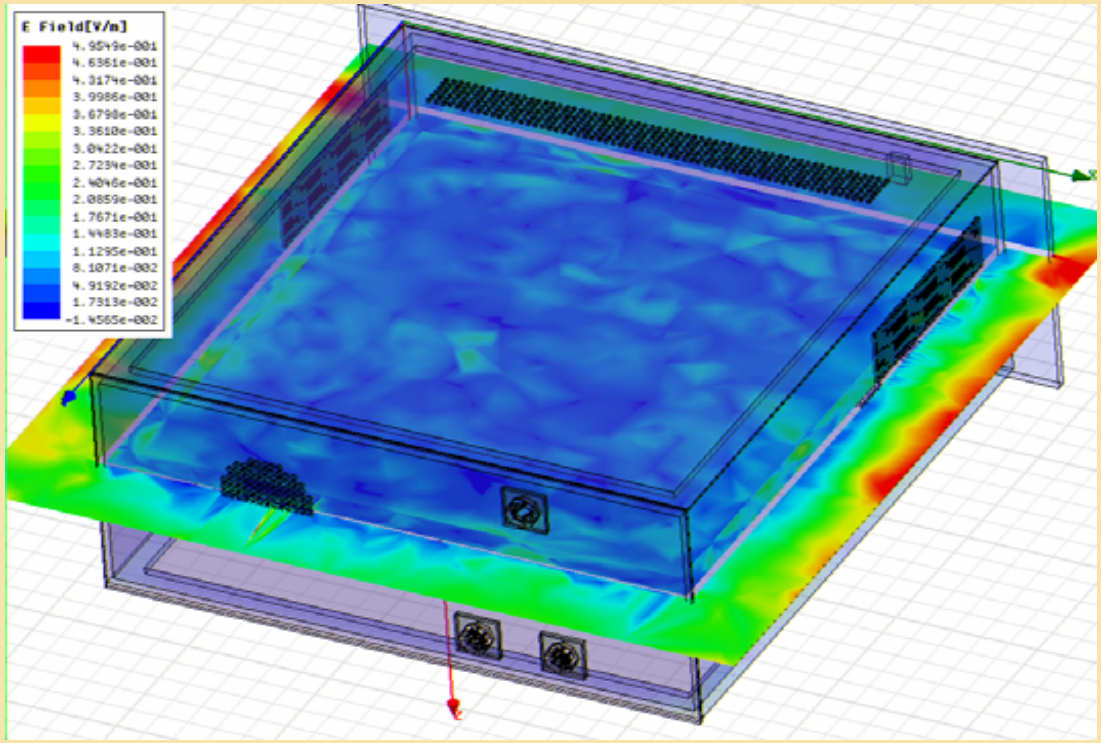
Impedance Analysis

Resonance Analysis

Signal Extraction

Emissions Analysis

Enclosure Simulation



Real enclosures are non-ideal and can pass radiation

Ensure minimal radiation from PCB escapes the chassis holes

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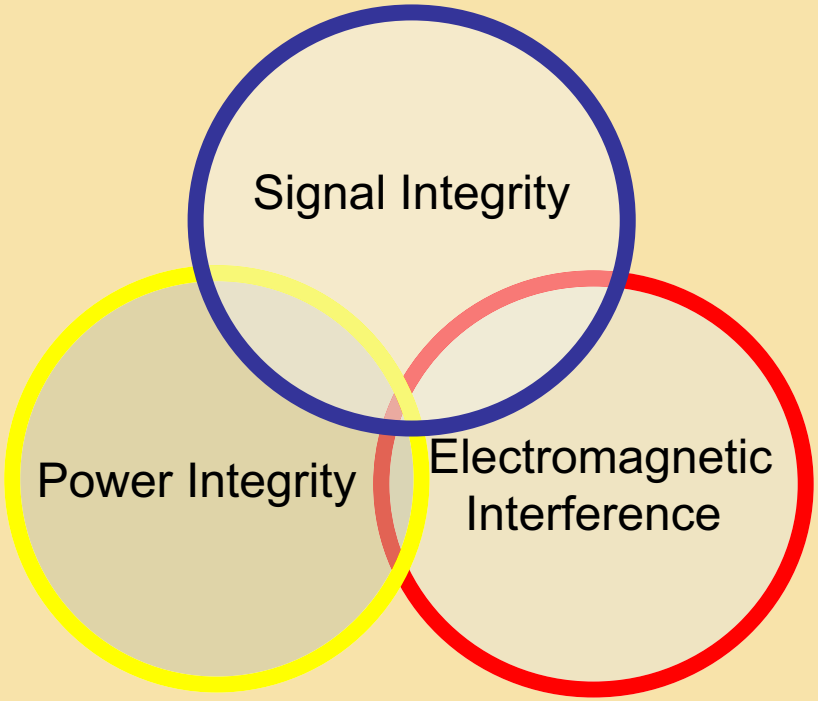
PI Methodology



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Power Integrity – A Case Study

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- Active devices require clean power to operate correctly
- Power distribution system (PDS) design engineers must ensure that all parts receive voltage between certain limits and that noise is kept sufficiently low
- Today's designs with many separate power domains of high current and low voltage devices complicate power integrity analysis

Board Imported from Layout

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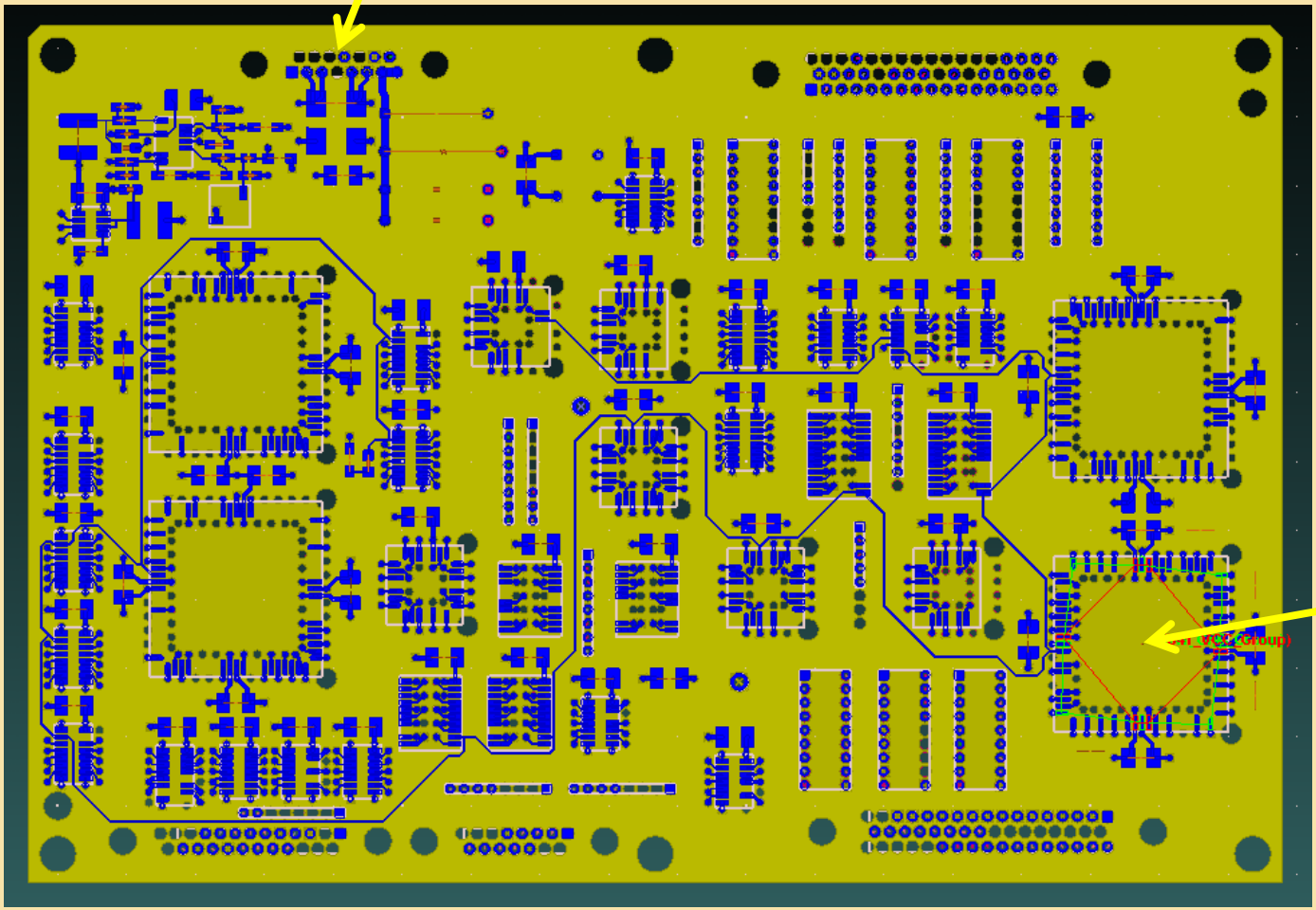

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PDS Design Flow

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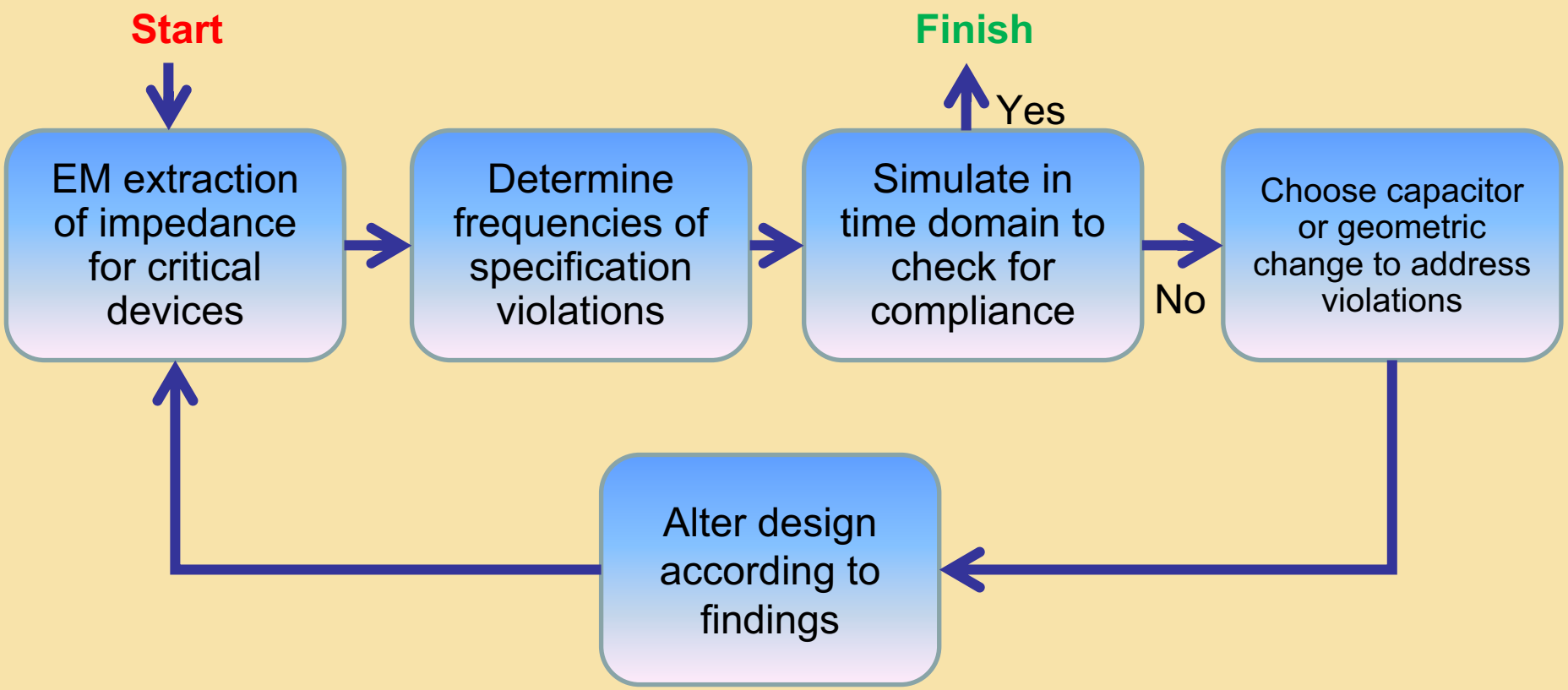

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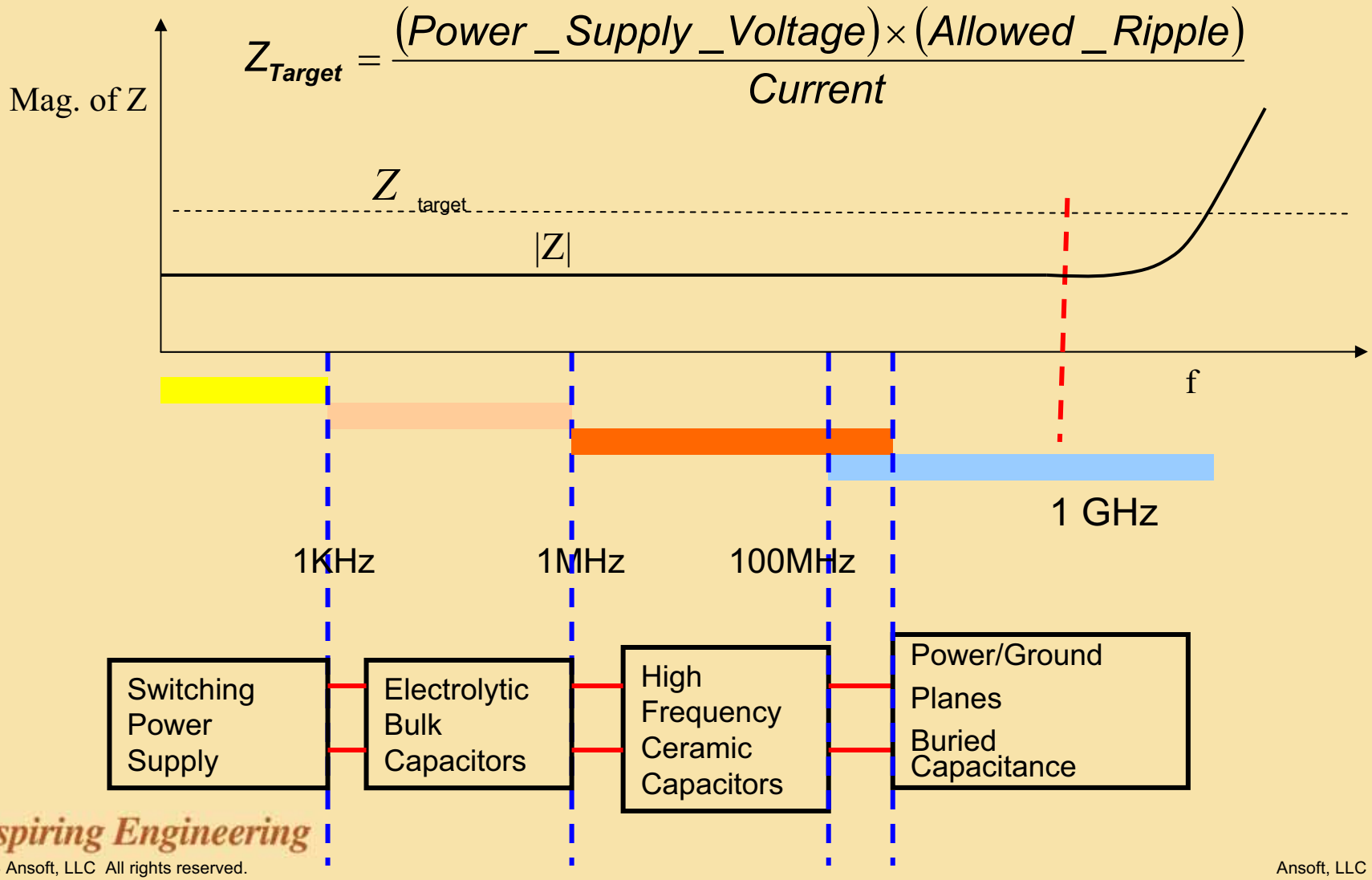
Frequency Domain PDS Targets



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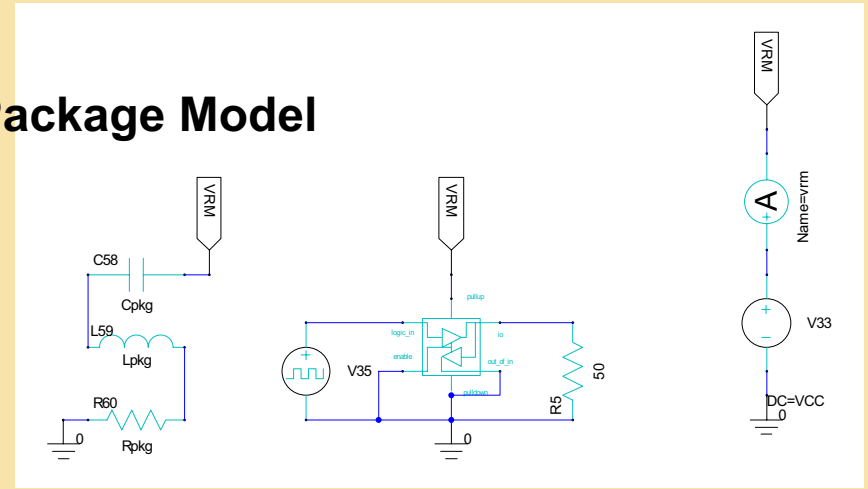
Defining the Target Impedance

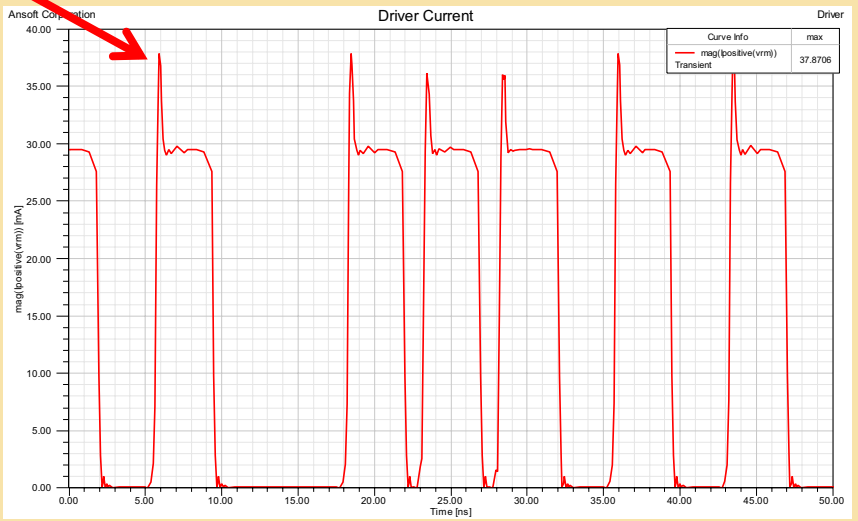


- To define the target impedance we need to consider two factors:
  - Peak current
    - Determines maximum impedance
  - Spectral power
    - Determines cutoff frequency

Inspiring Engineering

Peak Current

- Peak driver current 37.87 mA
- Example:
  - Six drivers and 0.18 V maximum voltage swing:



$$\frac{0.18\ \text{V}}{6(37.87\ \text{mA})} = 800\ \text{m}\Omega$$

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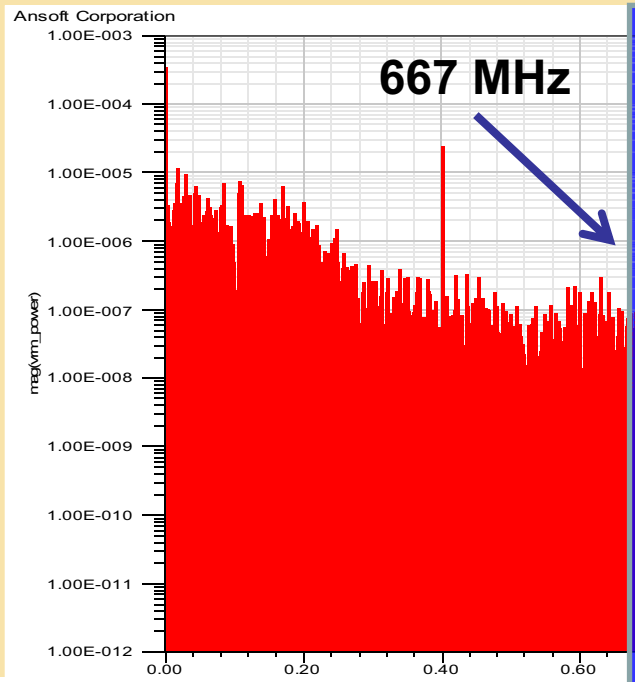
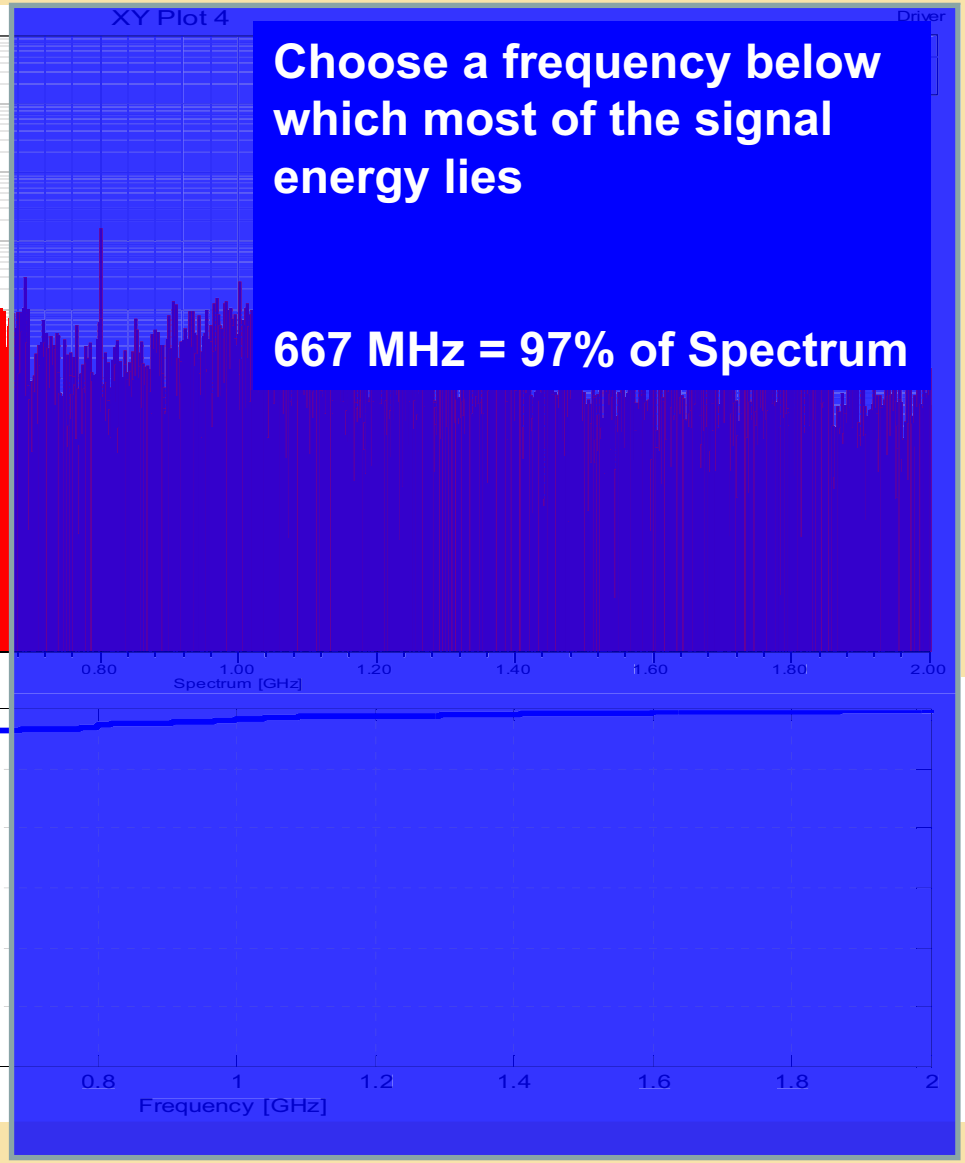
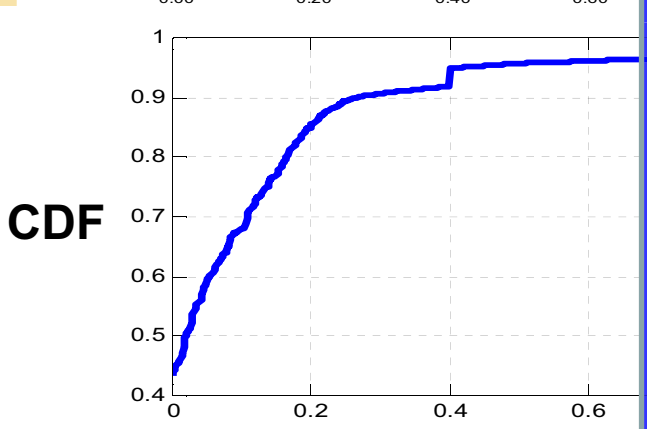
Driver Spectrum







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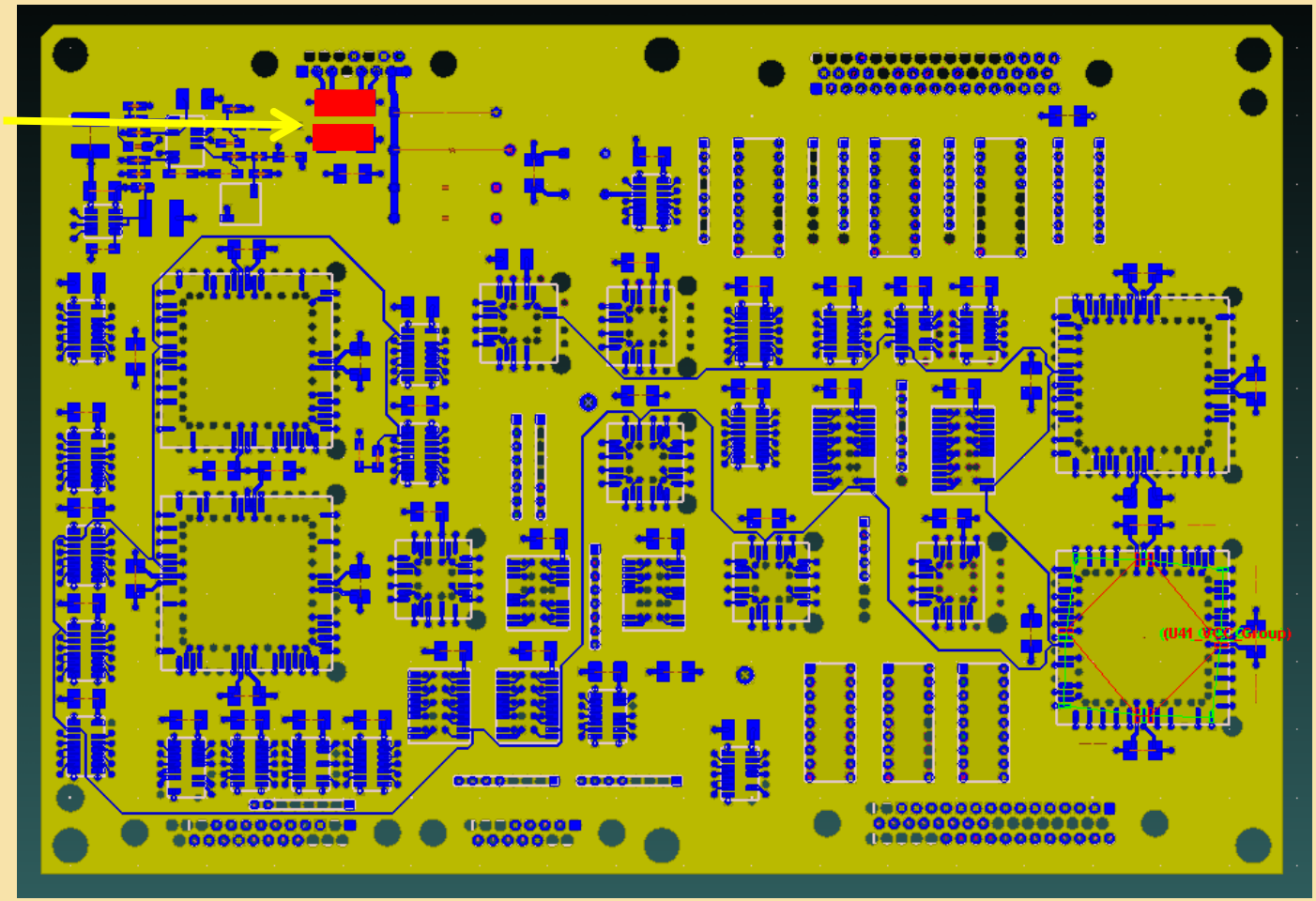
Power Integrity Investigation

Added two bulk 47 uF capacitors as specified by VRM manufacturer



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Bare Board vs. Bulk Capacitors

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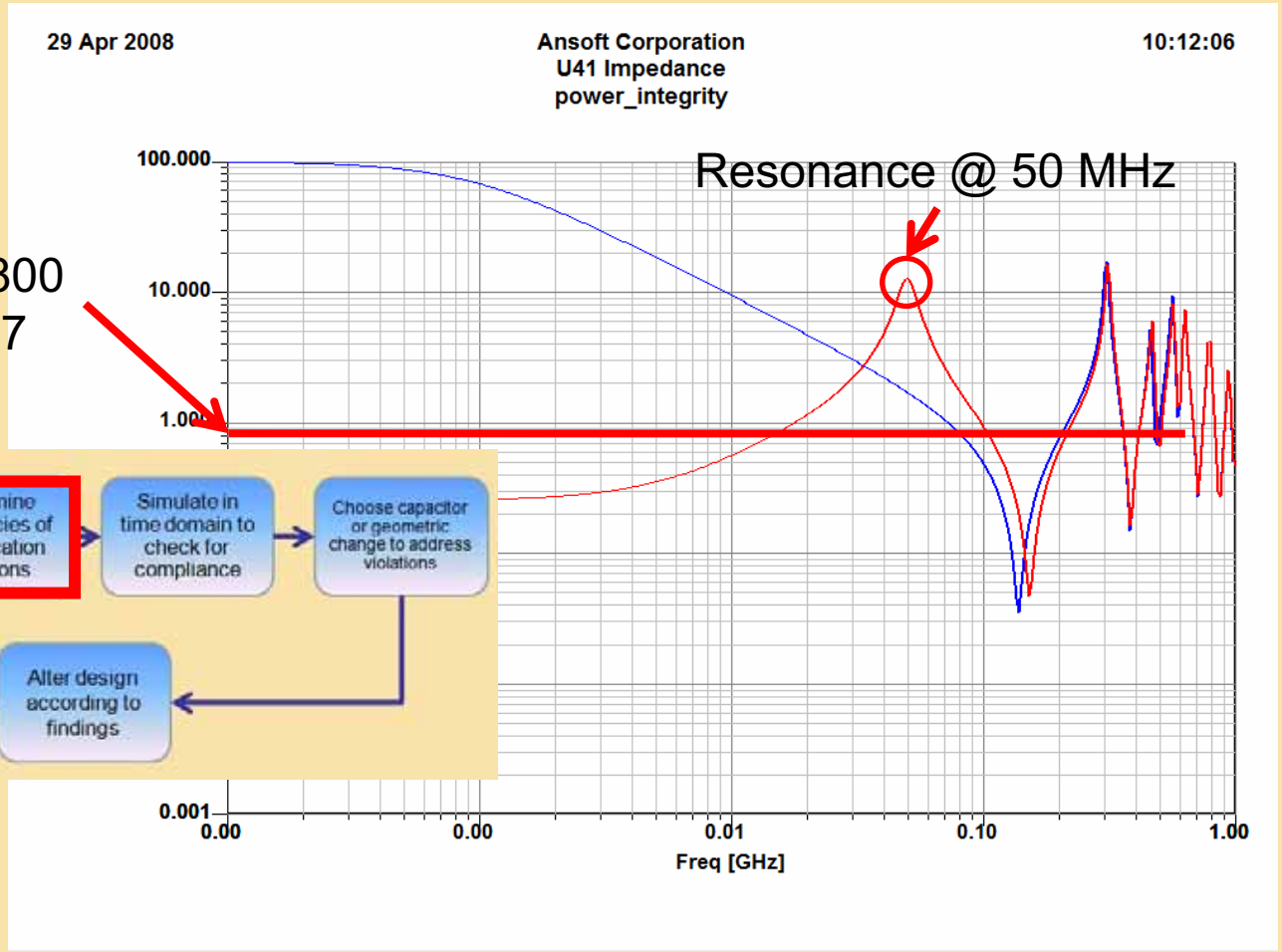
Target impedance 800 mOhm to 667 MHz



Bare Board
Board w/ Bulk Caps

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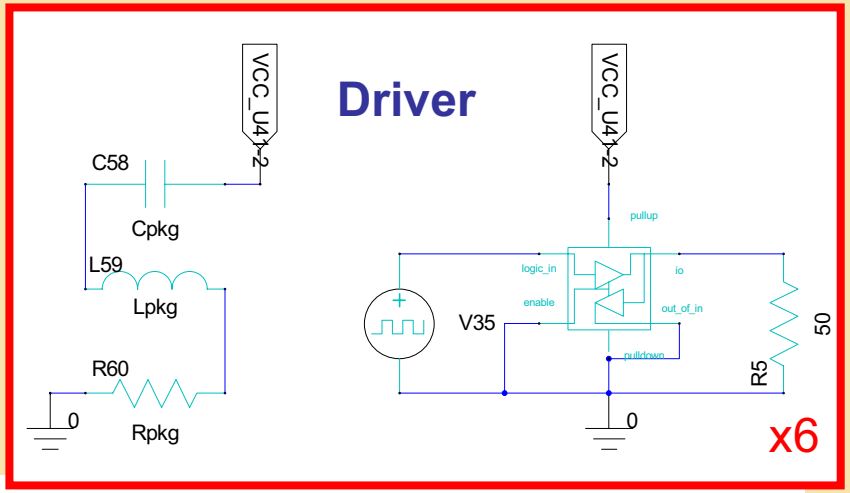
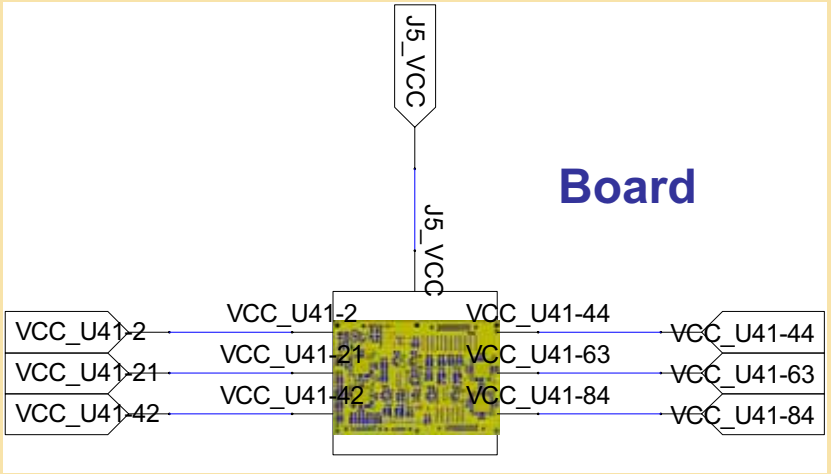
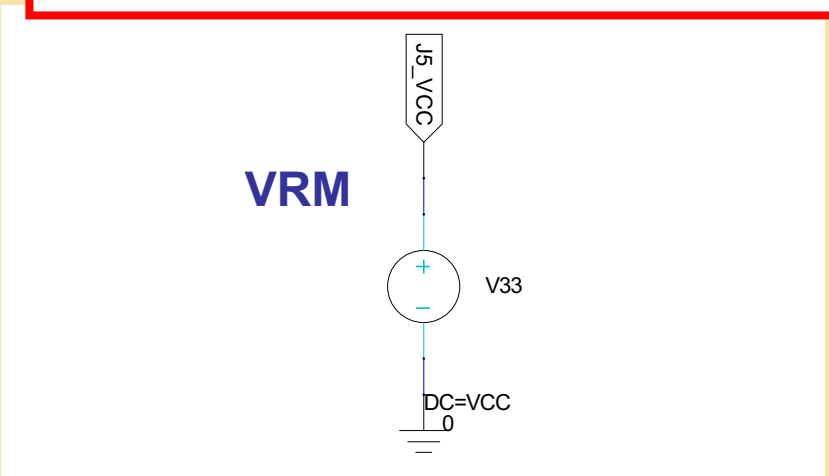
Time Domain Schematic







800 Mbps data rate

DDR2 IBIS driver into ideal termination used as load for PDS

Package decoupling modeled using a capacitor w/ ESR, ESL

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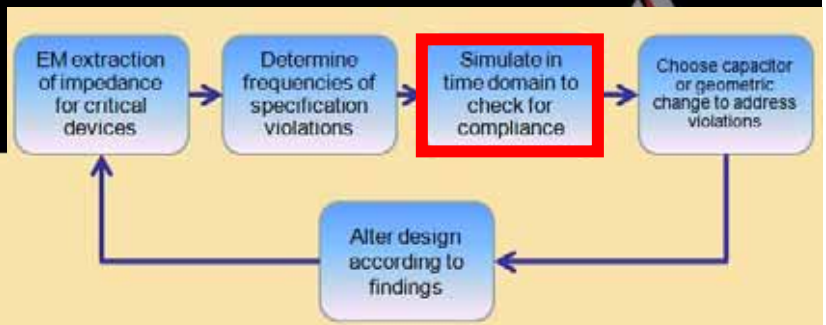
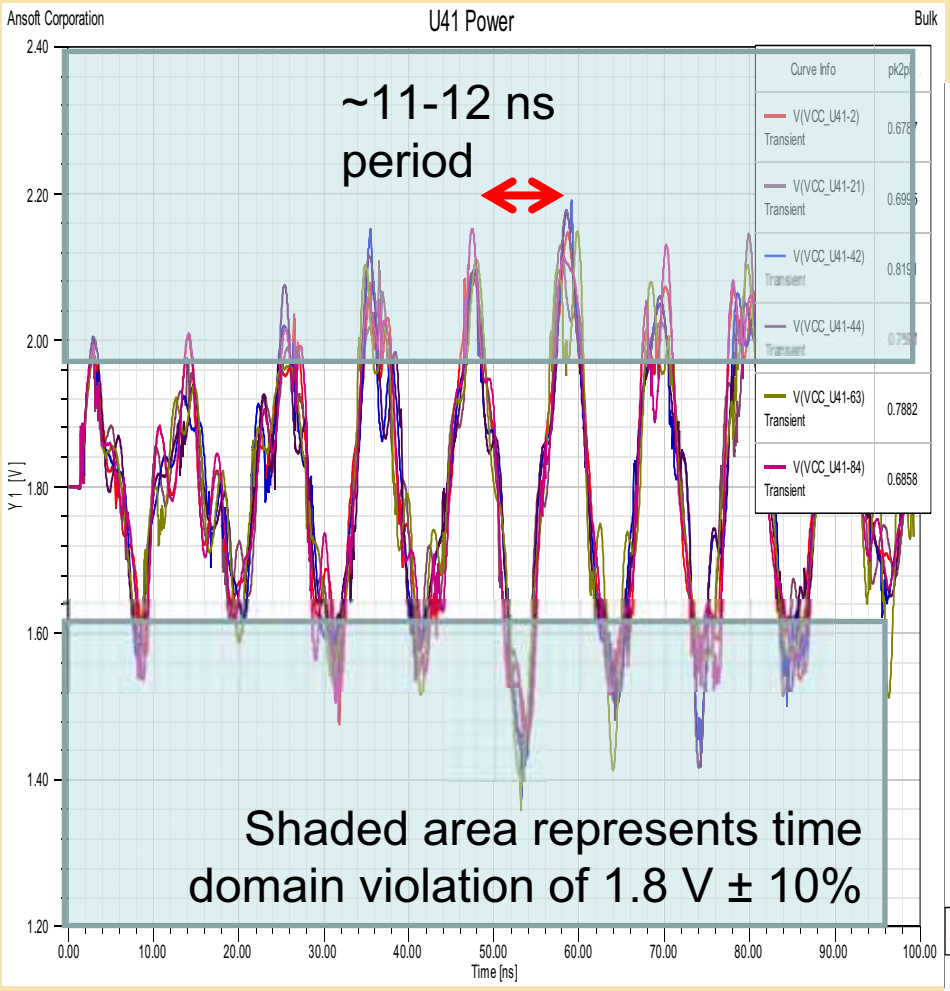
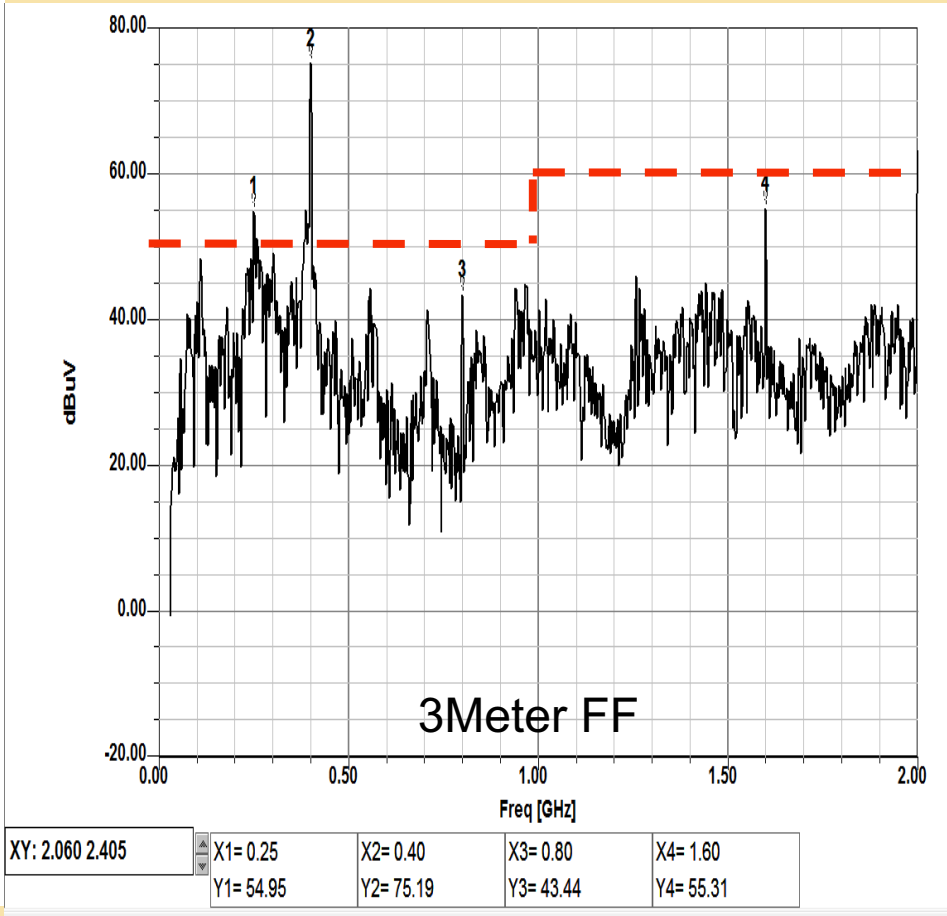
Switching Power Noise







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Choosing a Decoupling Capacitor

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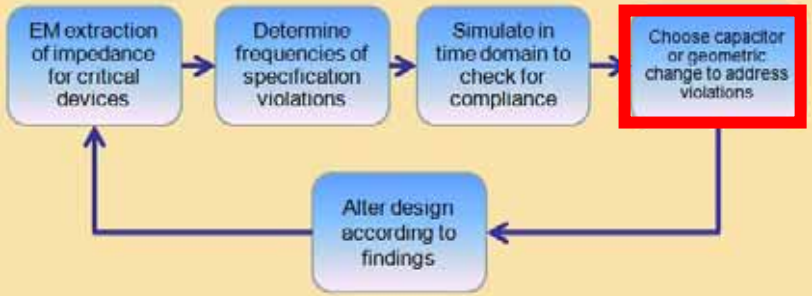
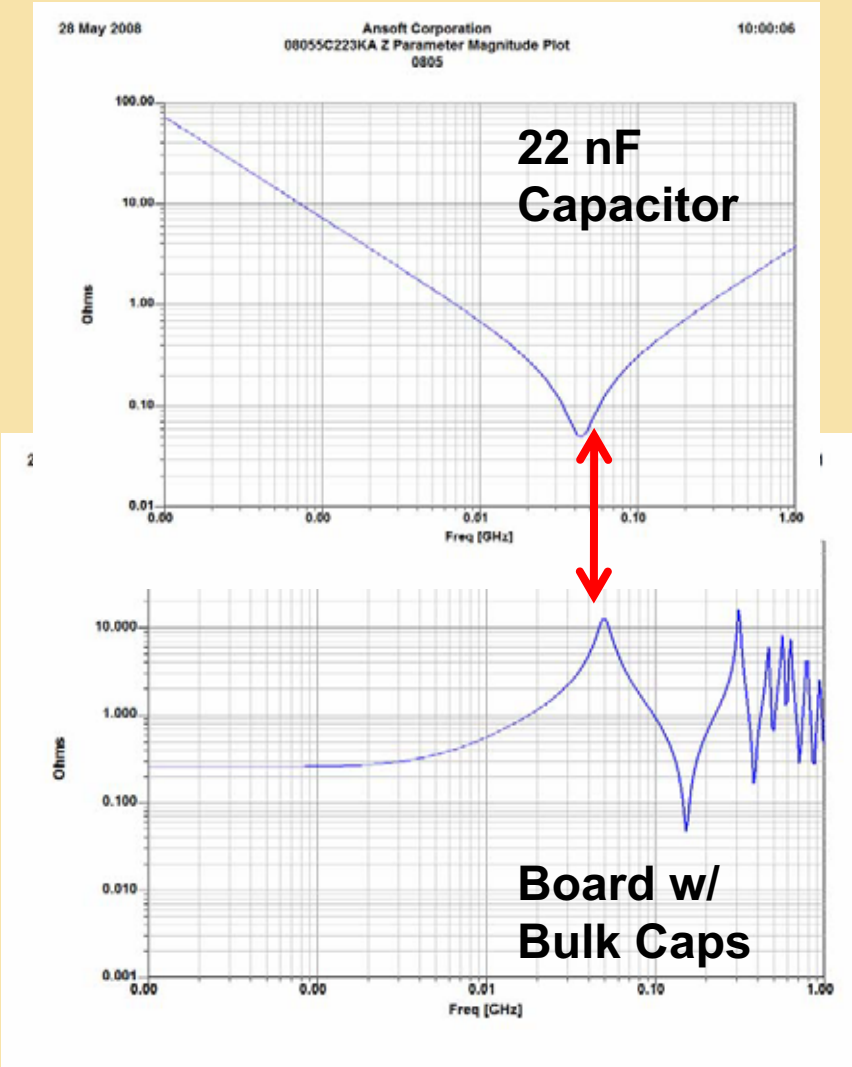
- To reduce the effect of a resonance, choose a capacitor with a low impedance at the resonant frequency





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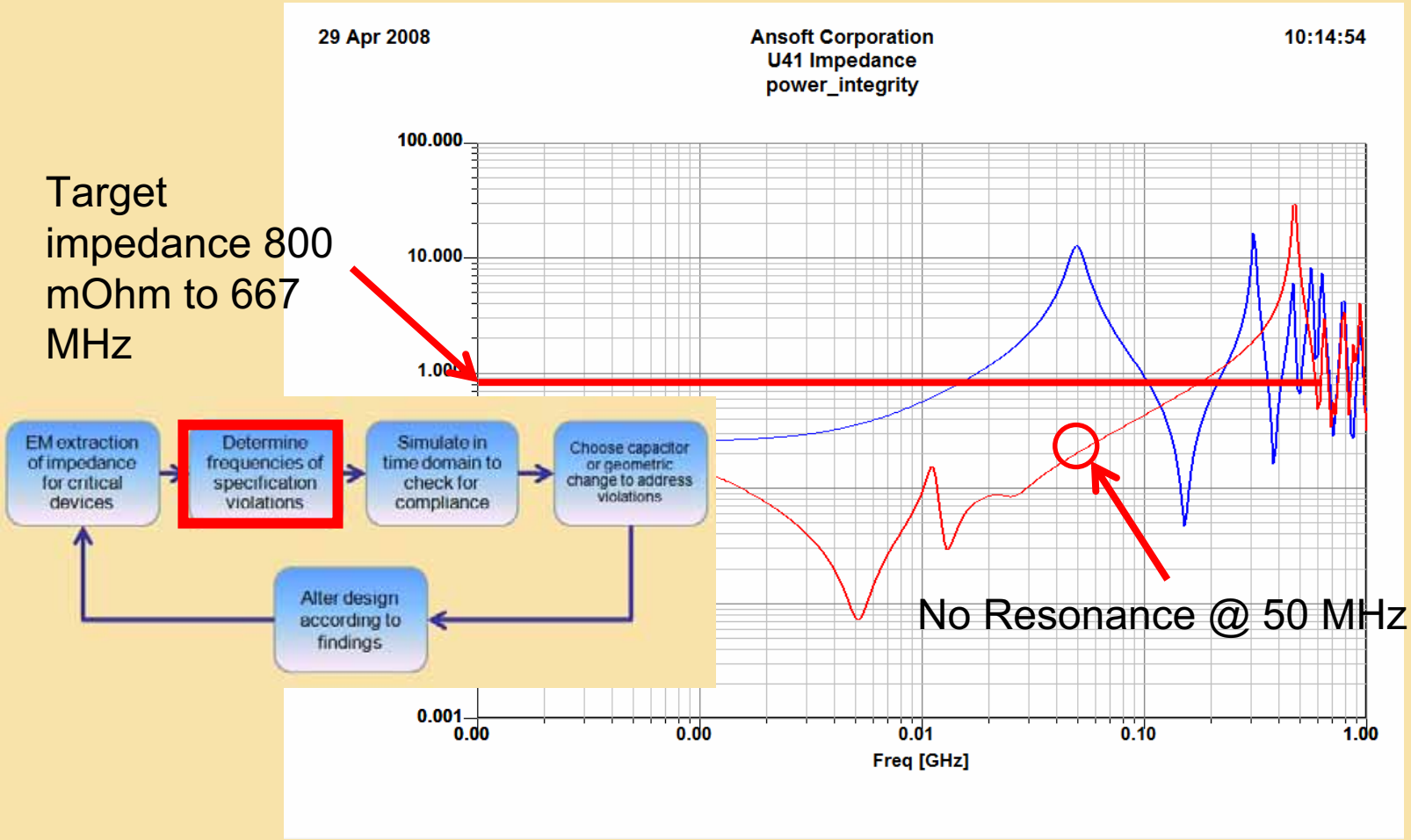
Bulk vs. HF Capacitors 1



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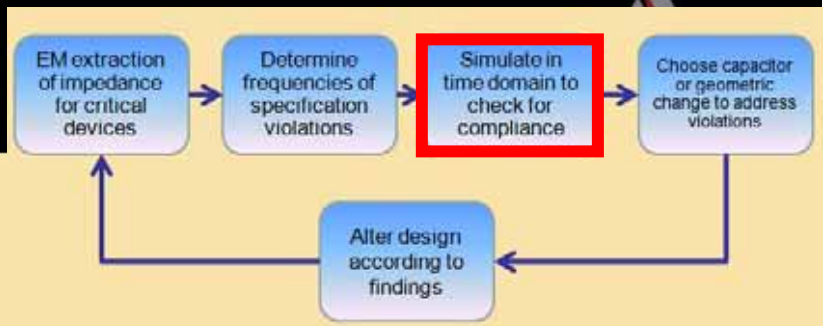
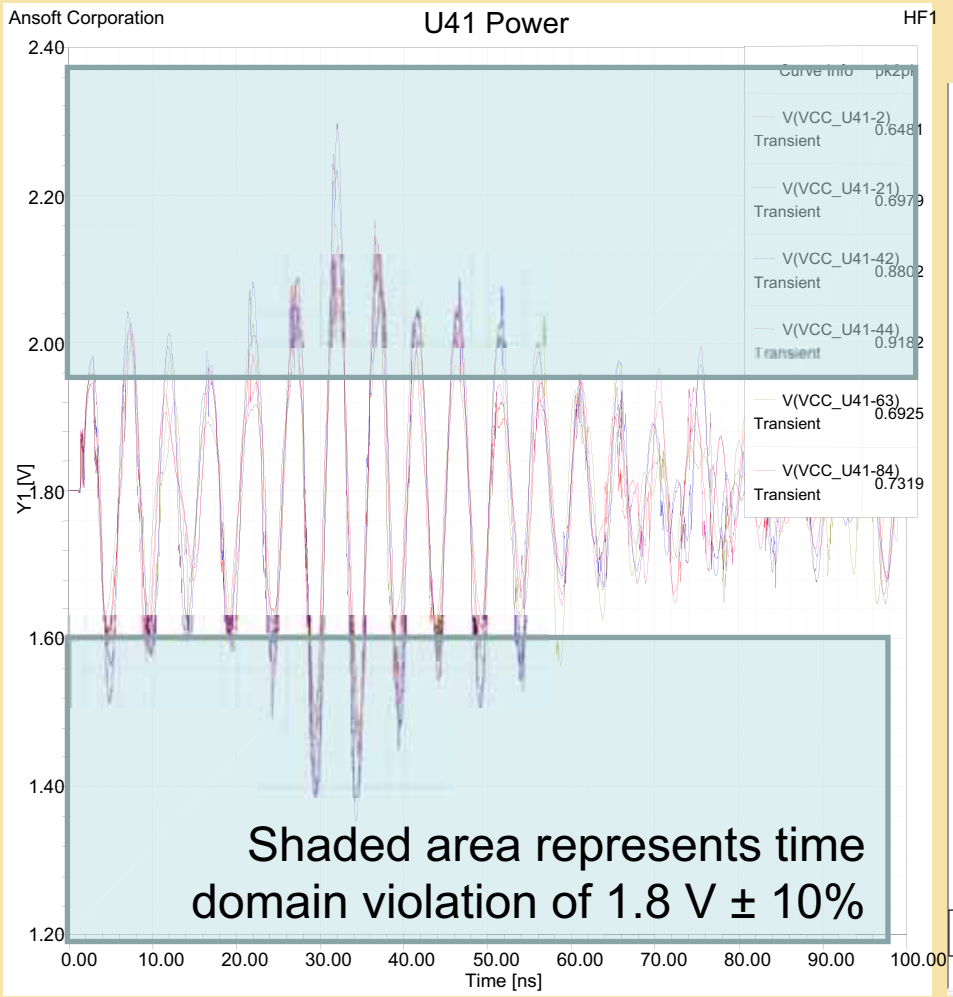
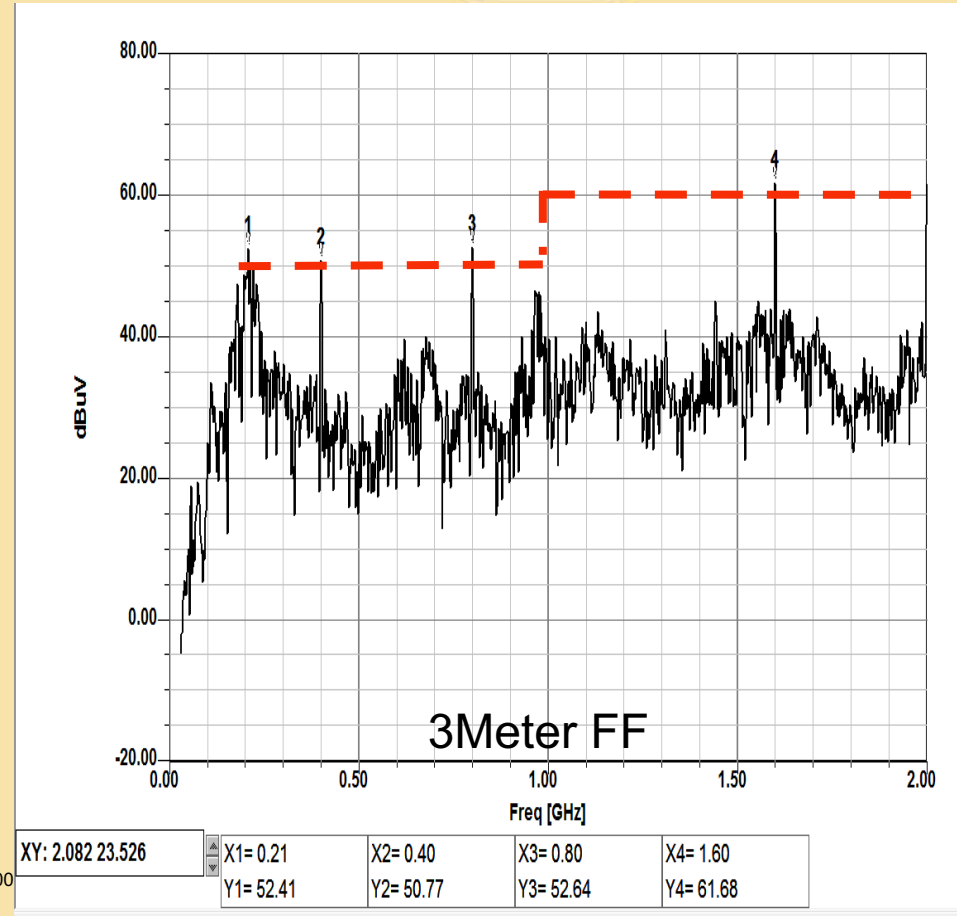
Switching Power Noise



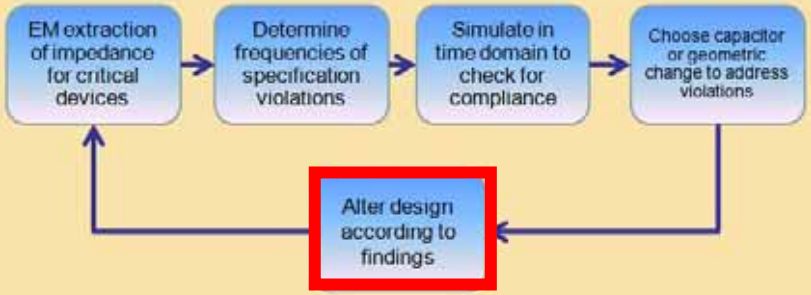


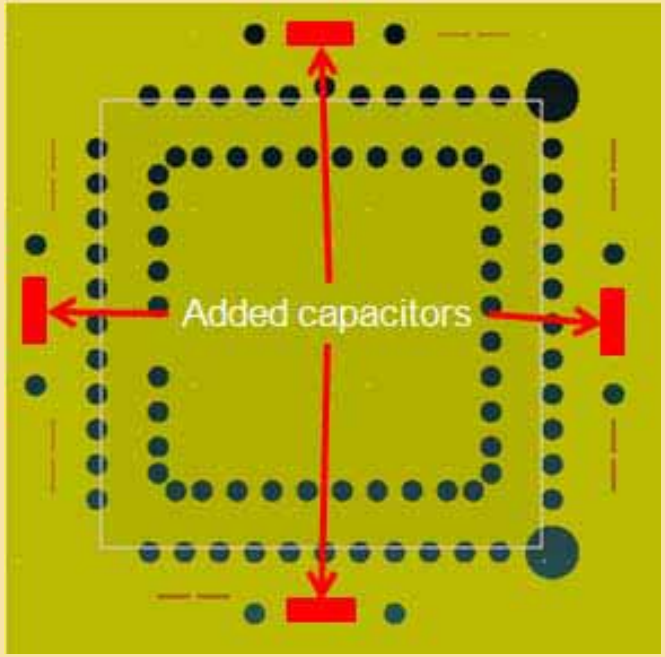


Inspiring Engineering

Extending Low Impedance

- 10 1.2 nF capacitors were added across the board to extend minimum high-frequency impedance
- 1.2 nF capacitor was chosen due to low impedance at 200 MHz
- 4 of these were located near U41





HF 1 vs. HF 2

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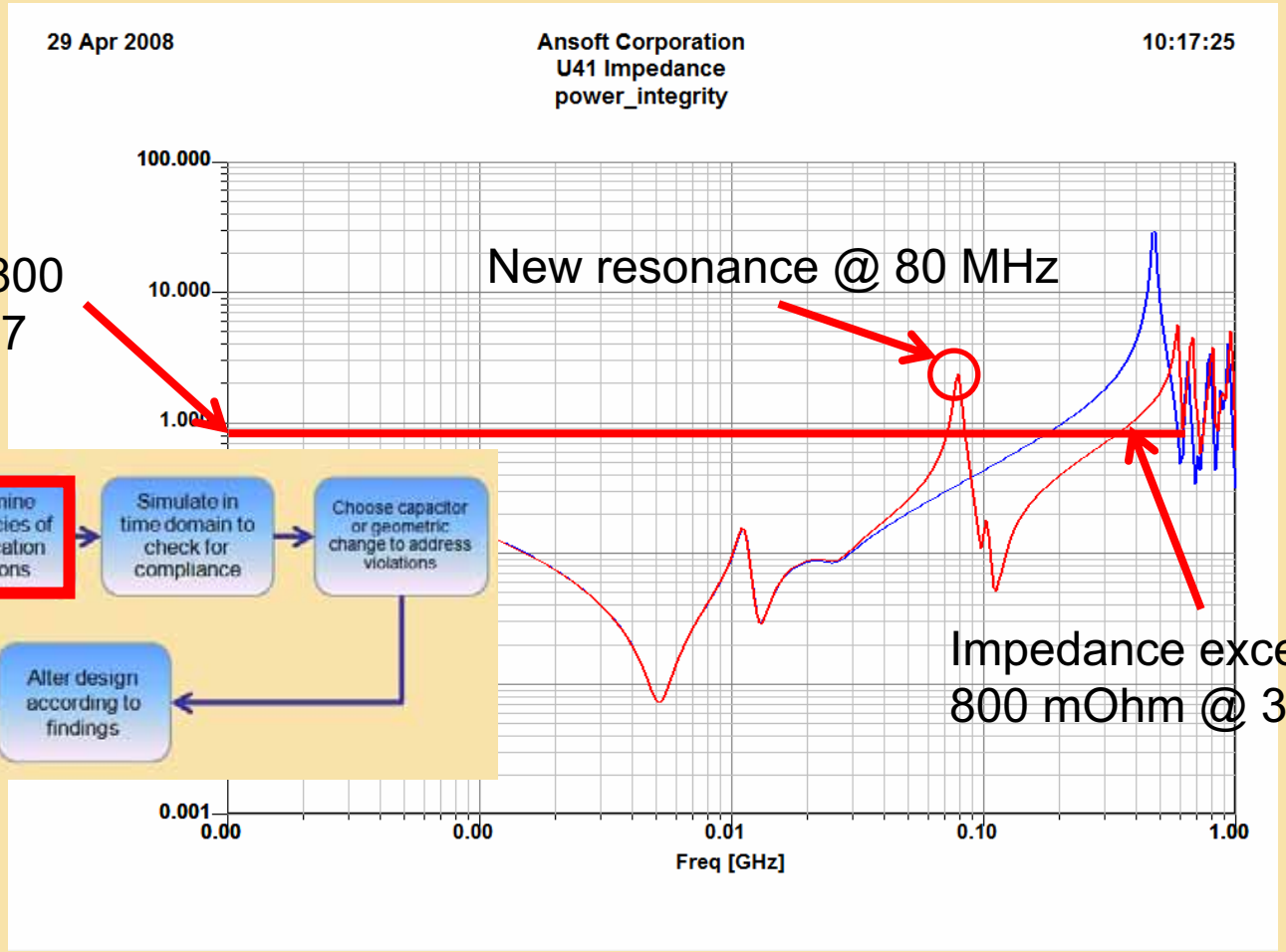
Target impedance 800 mOhm to 667 MHz



Board w/ HF Caps 1

Board w/ HF Caps 2

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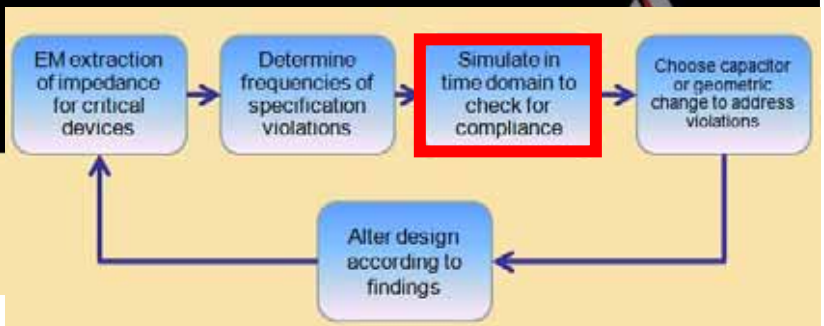
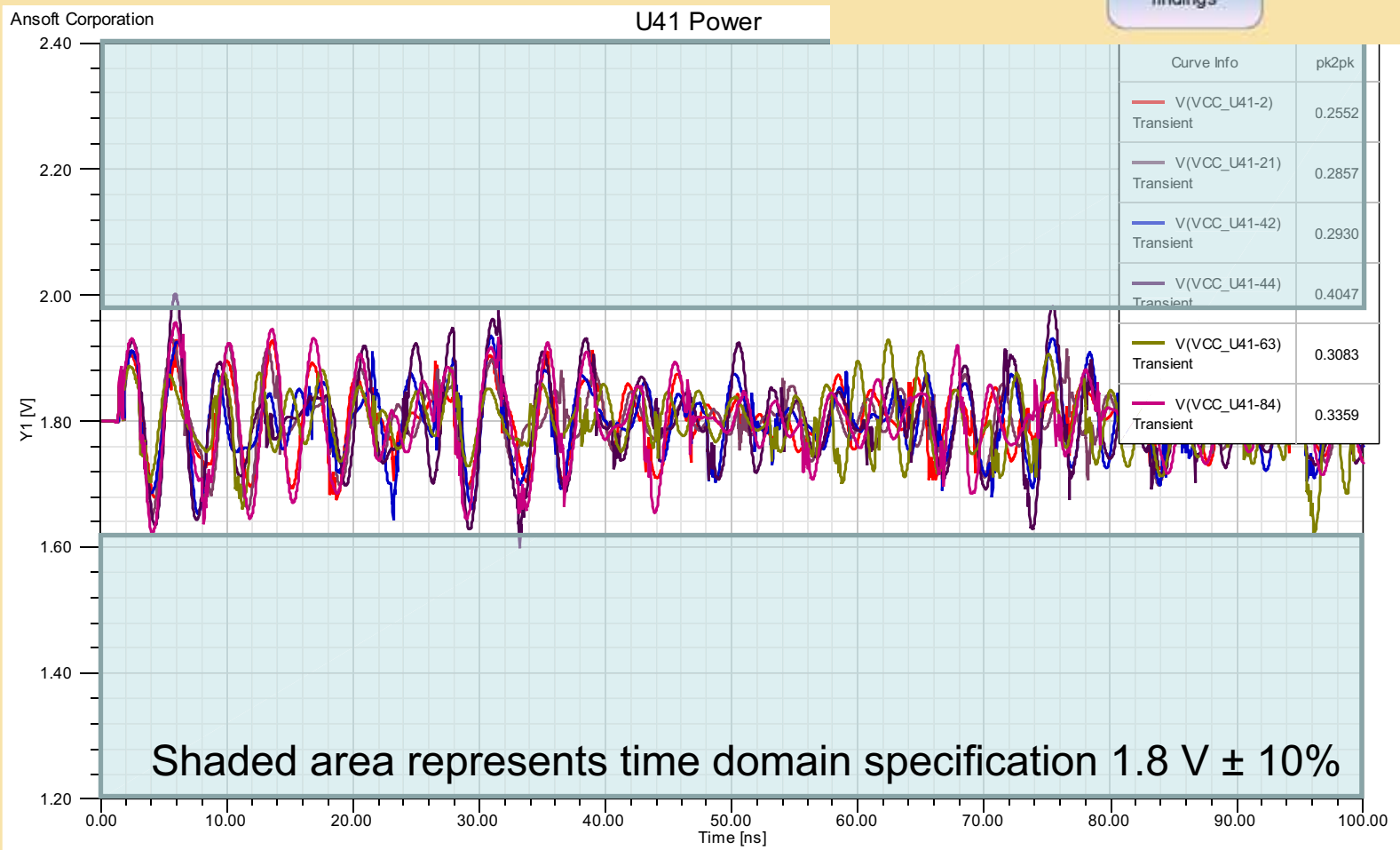
Switching Power Noise





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Removing a Resonance

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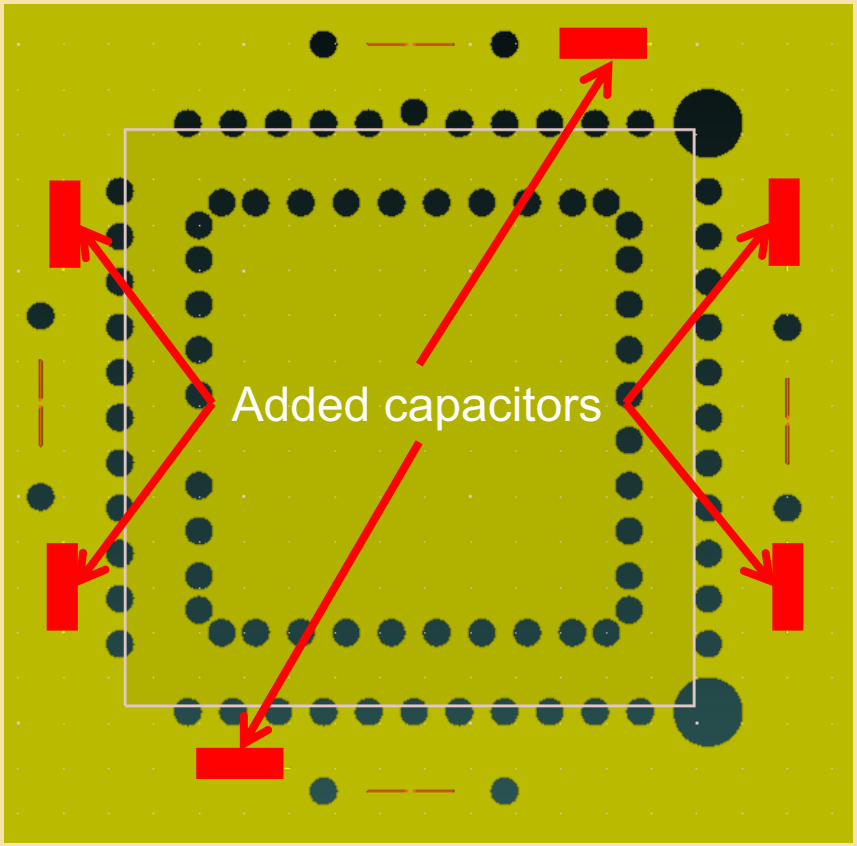
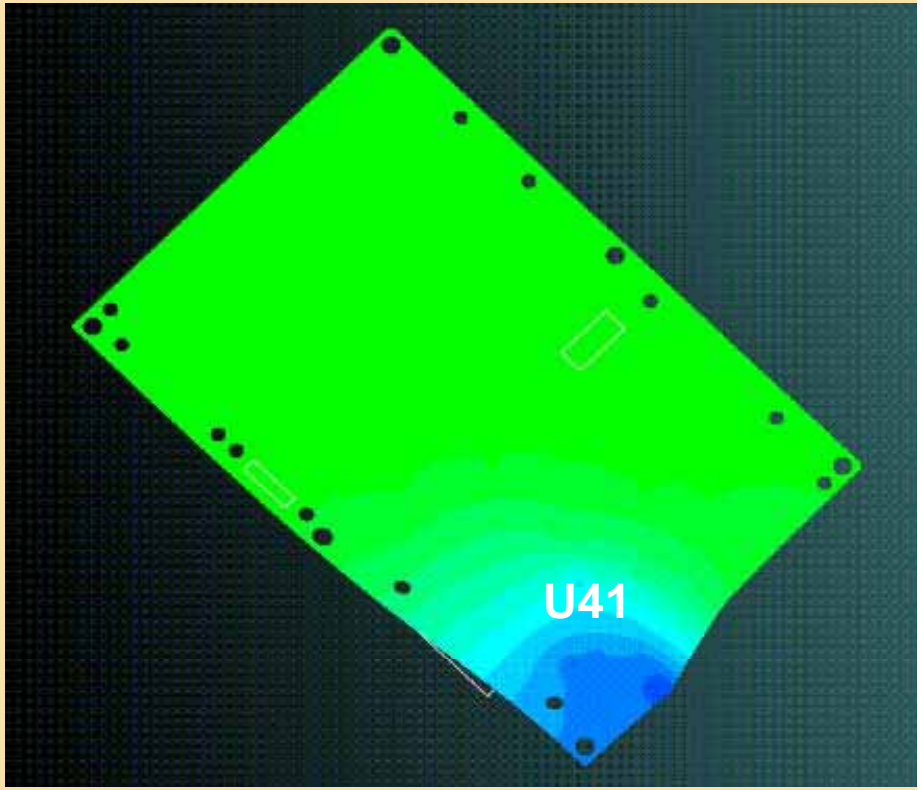


- Six 8 nF capacitors were added near U41 to cancel resonance at 80 MHz



Inspiring Engineering

HF 2 vs. HF 3

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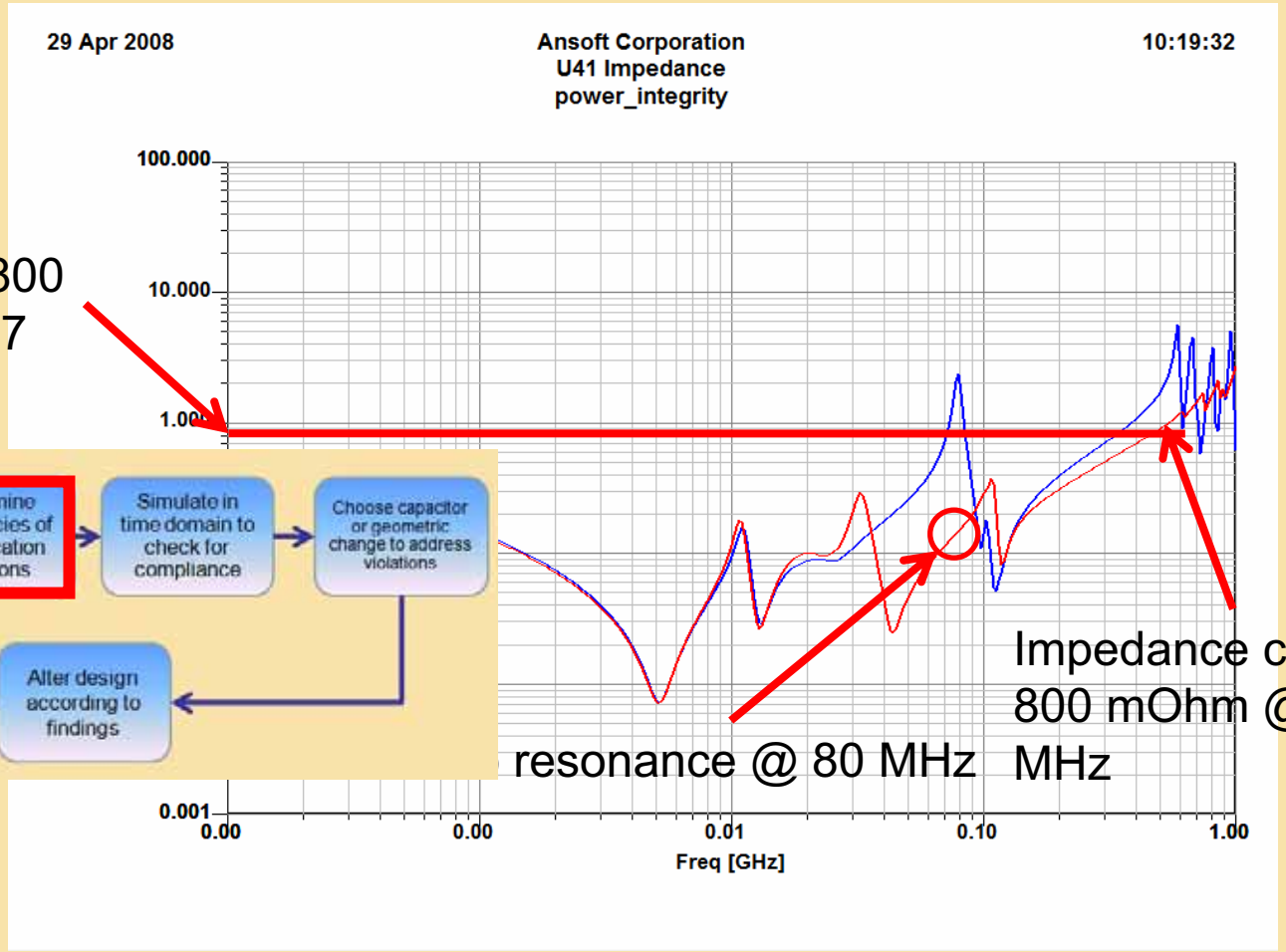
Target impedance 800 mOhm to 667 MHz

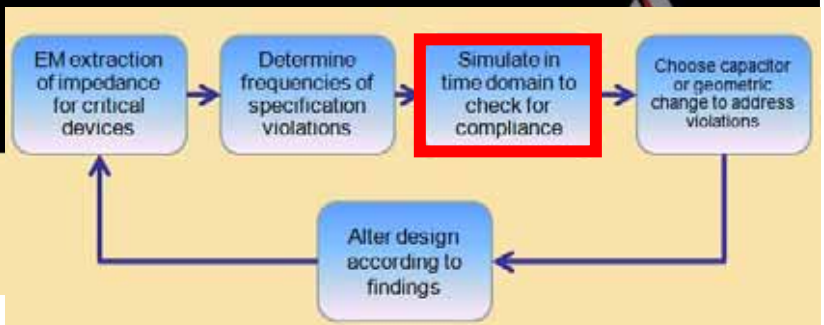


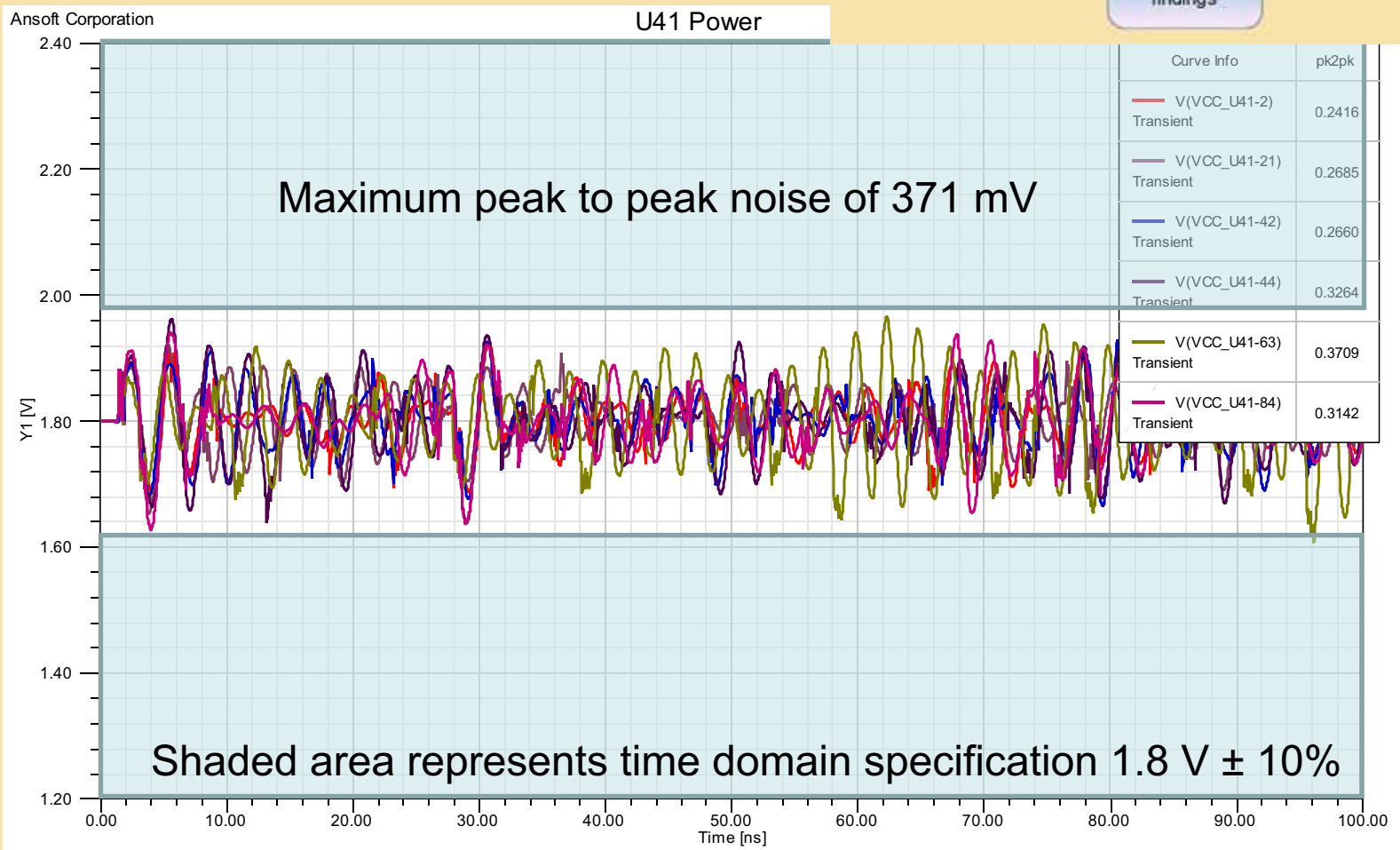
Board w/ HF Caps 2

Board w/ HF Caps 3

Inspiring Engineering

Switching Power Noise

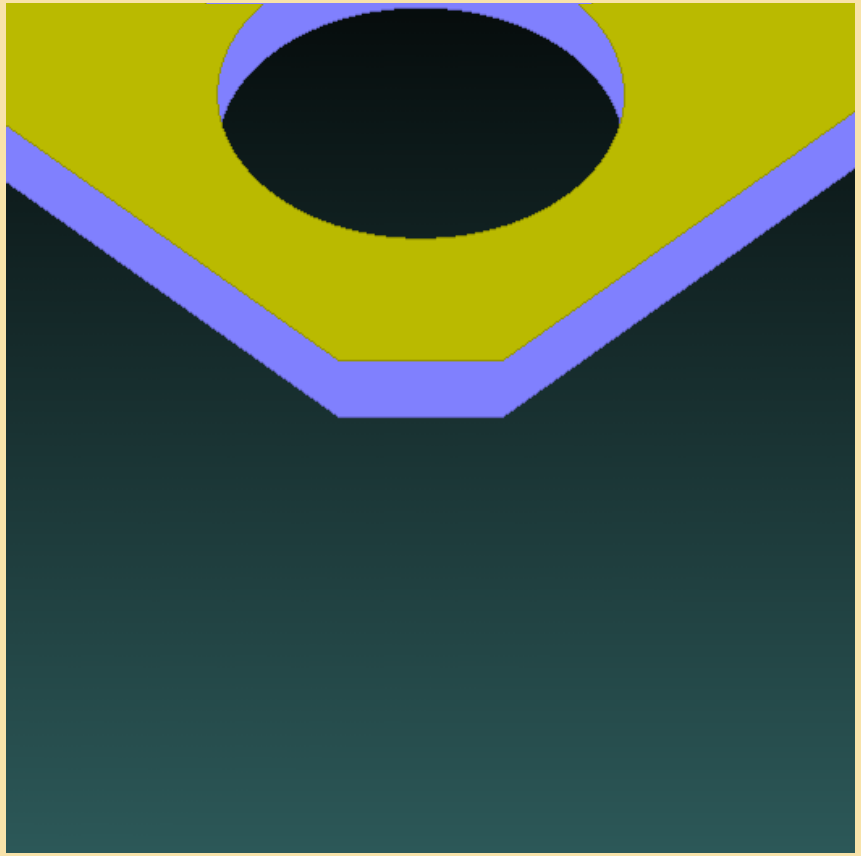




Inspiring Engineering

Buried Capacitance

- Due to parasitic inductance it is impossible to decouple the board with capacitors at frequencies greater than a few hundred MHz
- Using a thinner dielectric layer between power and ground planes introduces additional capacitance and reduces high frequency impedance



Capacitance of parallel plates: $C = \varepsilon \frac{A}{d}$

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HF 3 vs. Buried Capacitance

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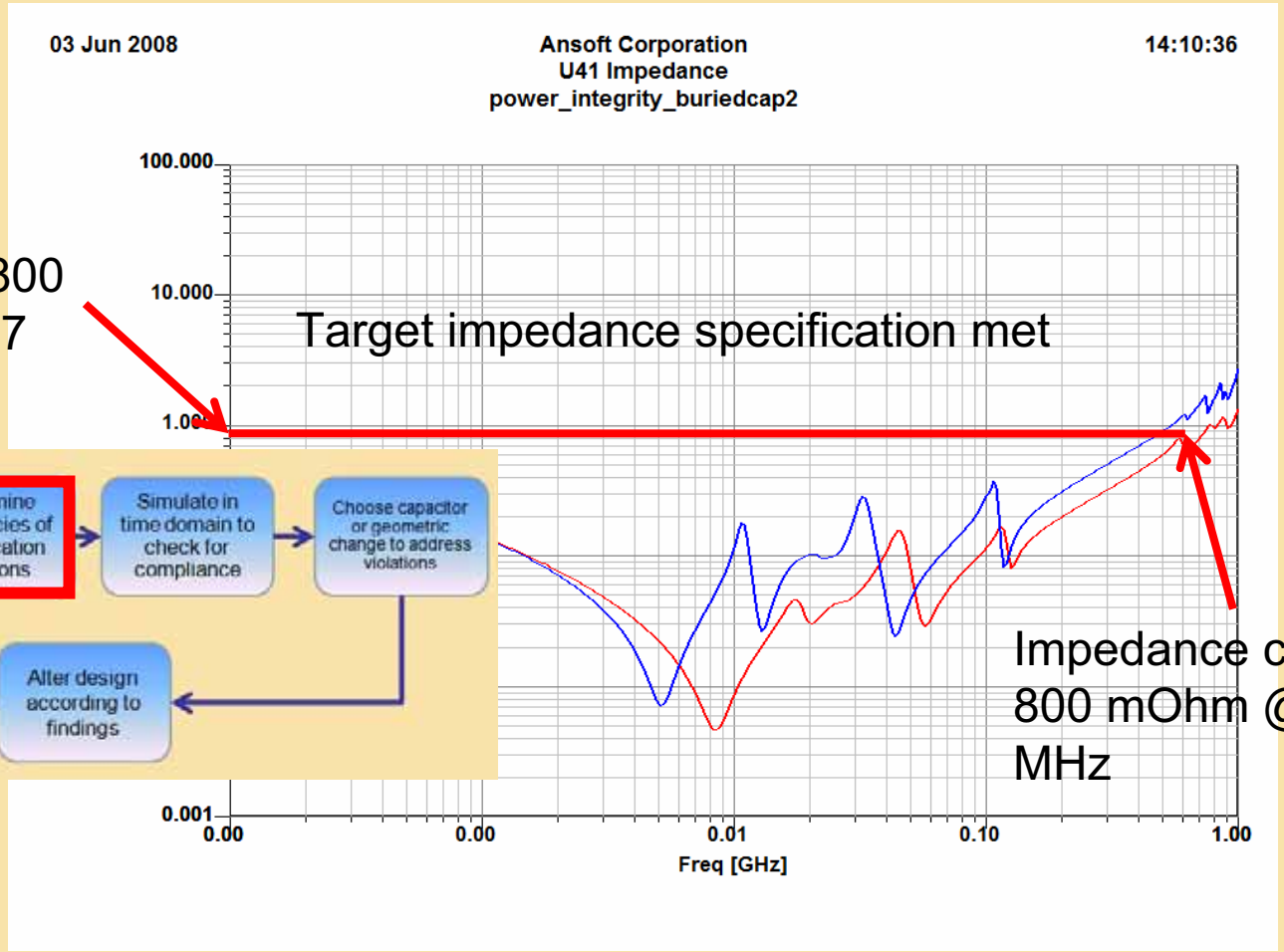
Target impedance 800 mOhm to 667 MHz



Board w/ HF Caps 3

Board w/ Buried Capacitance

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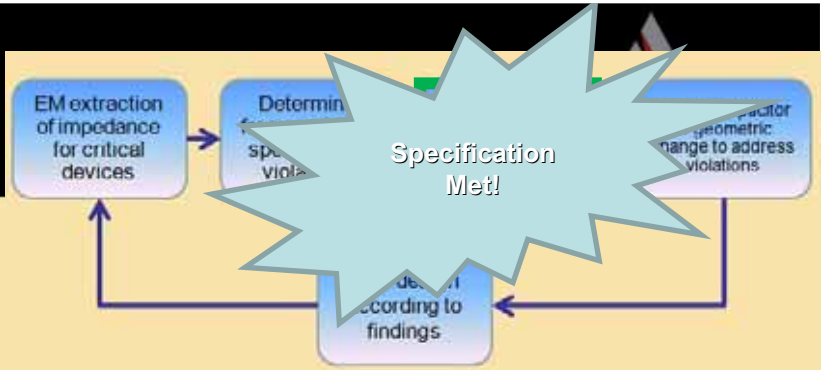
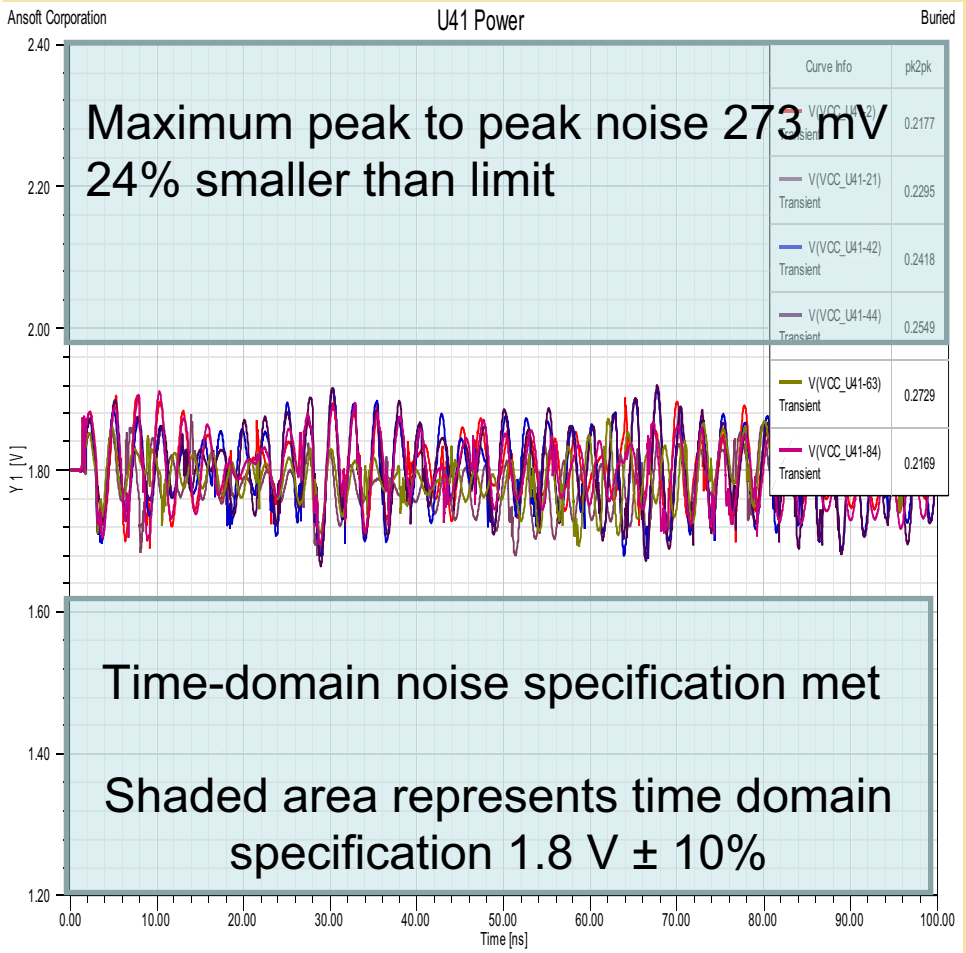
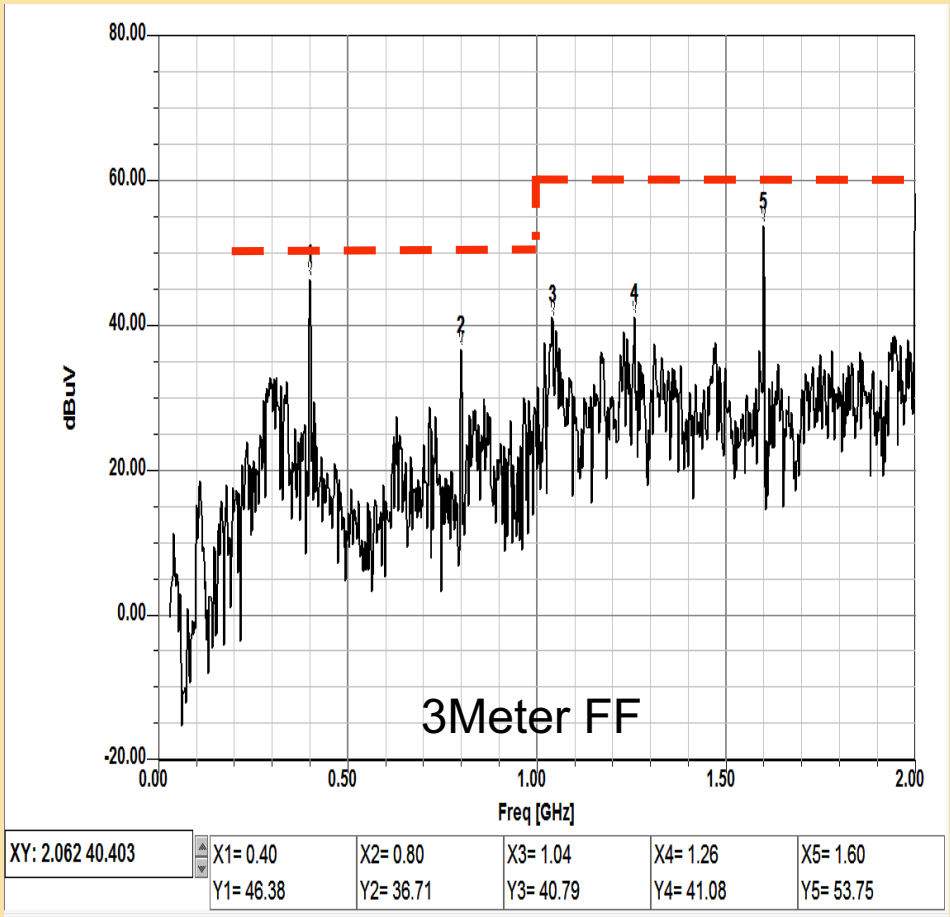
Switching Power Noise







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Conclusions

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- SI / PI / EMI are all based on the same electromagnetic fundamentals and cannot be separated
- Impedance and resonant mode simulations connect the frequency domain to the spatial domain and allow selection of capacitor value and placement
- *Frequency domain* extractions are useful for quickly optimizing PDS designs, but *time domain* simulations are necessary to ensure compliance with device specs
- Using a single design environment can help reuse the same models for SI/PI/EMI simulations

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Questions

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Any Questions?

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