Thermal Effects on Through-Silicon Via (TSV) Signal Integrity

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Abstract

The thermal effect on through-silicon via (TSV) noise coupling and S_{21} of TSV channel were measured in both frequency and time domain from corresponding TSV based passive chips. These measurement results are analyzed using the temperature-dependent TSV lumped model to TSV channel and shows good correlation with measurement. Under the hundreds-of-MHz frequency range, increasing temperature decreases the S_{21} of TSV channel, but over that frequency range, increasing temperature increases the S_{21}. These phenomena are explained from the model which thermal dependence of the materials is applied.

Introduction

As semiconductor industry needs denser system integration, diverse methods like System-in-Package (SiP), System-on-Chip (SoC), and etc. have been presented. In recent years, 3-dimensional integration circuits (3D ICs) with TSV has become one of the most promising technologies among them. The TSV inside of 3D ICs provides reduced interconnection in a vertical direction so that may reduce the time delay of signals, and due to the TSV's structure itself, this provides the shortest electrical path between stacked chips and allows low power packaging scheme compared to conventional wire bonding and flip chip technologies. Therefore, 3D ICs technology has important potentials in a view point of not only an area of chip (density, # of transistors/Area) but also a performance compared to conventional methods.

However, these 3D ICs generally have a structure which heterogeneous or homogeneous sub-chips are vertically and laterally stacked in a fixed area so that some of the fundamental problems like thermal or mechanical problems are occurred. Thus, it is necessary to consider these issues in advance to signal integrity or power integrity. The research trend of 3D ICs nowadays mainly targets on both these fundamental problems and signal/power integrity. Some researchers only focus on thermal or mechanical result itself. By changing temperature through the simulation, temperature gradient or the mechanical stresses are described [1]. Although some other researchers obtained signal integrity models for TSVs in 3D ICs [2], Most of signal integrity researches do not consider actual temperature range, but they mostly assume ideal situation which every material of TSV-based structure has fixed electrical properties as temperature varies. To make a connection between thermal and signal integrity, it is necessary to measure and analyze the thermal effect on signal integrity, and especially temperature dependence analysis of TSV in 3D ICs should be investigated.
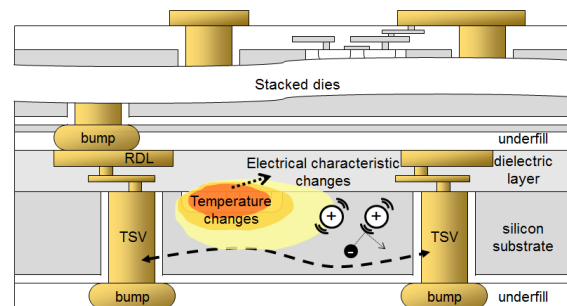

Figure 1. Conceptual figure of thermal effect on TSV signal integrity in 3D ICs

In 3D ICs, temperature effect should be considered in a view point of signal integrity. When dies are stacked, heat from the local hot spot might be isolated due to the insulation layer between each dies as Figure 1. Compared to 2D ICs, there are more possibilities which thermal issues is serious due to these vertical insulations between dies. These block electrical short between dies, but also blocks the heat dissipations path from the hot spot inside of the chip to a heat sink outside of the chip. Therefore, the effect of temperature on the materials in a stacked chip becomes very important and should be investigated when manufacturing 3D ICs.

When the temperature of silicon die varies, positive charges in it generally vibrate, and this phenomena cause the disturbing of the motion of free electrons. As a result, the material resistivity may increase and some electrical polarization characteristic may vary as depicted in Figure 1. Therefore, the noise coupling between signal TSVs and S_{21} of TSV channel may vary as well. These may change with frequency, and the trend of it changes depending on the materials property. Measuring and analyzing the effects of temperature variation are important to understand the signal integrity of the total system of 3D ICs.

In this paper, two types of TSV based passive test vehicles are used to measure temperature effects on signal integrity. The first test vehicle is for noise coupling between signal TSVs, and the second test vehicle is for S_{21} of TSV channel. Temperature is varied from 25°C to 100°C which is general range for proper chip operation. In measurement, the temperature was increased with the heat convection method to minimize the electrical effect and the approximated

temperature profile was obtained using a thermal imaging camera. The measurement result is analyzed with a simplified temperature-dependent TSV lumped model for TSV channel.

Measurement of thermal effect on TSV

To observe the actual thermal effect on TSVs, two types of test vehicle were fabricated from different designs. One was a test vehicle fabricated from Hynix Semiconductor inc. for observing noise coupling between signal TSVs, and the other was fabricated from KETI for observing S_{21} of TSV channel. For both frequency and time domain measurement, temperature was changed from 25°C to 100°C, which is generally considered as the region the chips conduct properly.

A. Thermal effect on noise coupling between signal TSVs
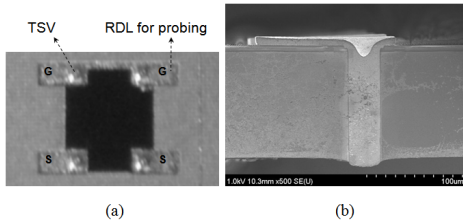

(a)   (b)

Figure 2. (a) The top view of the test vehicle for TSV noise coupling (b) The side view of the test vehicle SEM image.

For the measurement of noise coupling between signal TSVs, test vehicle was designed as coupled-TSV form as shown Figure 2a. A test vehicle was fabricated with via-last Hynix TSV process. Ground pads are connected each other through RDL metal, and the opened-ended TSVs have no interconnection at the bottom side. The TSVs made of copper (Cu) are separated from silicon substrate by surrounding thin silicon dioxide (SiO$_2$) layer around TSVs. Figure 2b shows the SEM image of one signal TSV cross section.

The test vehicle has 160μm pitch between signal TSVs, has 250μm pitch between signal and ground TSV, and has 100μm height of silicon substrate. The diameter of TSV is 33μm, and the thickness of silicon dioxide is about 0.52μm. Moreover, p-type silicon is used as a substrate and has 10S/m resistivity in room temperature. With these dimensions and electrical parameters, the result was obtained both from frequency domain and time domain.

A-1. Noise coupling in frequency domain

Basically, frequency response of noise coupling between signal TSVs is obtained by taking S-parameter. To measure S-parameter, the bottom ends of coupled TSVs are open-terminated and 2-port measurement is performed using Vector Network Analyzer (VNA), Agilent N2530A, and on-chip Cascade micro probes.

Because it is not common to make setup for temperature measurement especially in TSV based passive structure, measurement method was originally made. To increase the temperature of test vehicle, temperature adjustable metal with thin tip was used as heat source. This metal can have fixed position with arm, and not directly contacted with test vehicle to prevent electrical leakage through metal itself. Because the temperature of it is adjustable between approximately 150°C

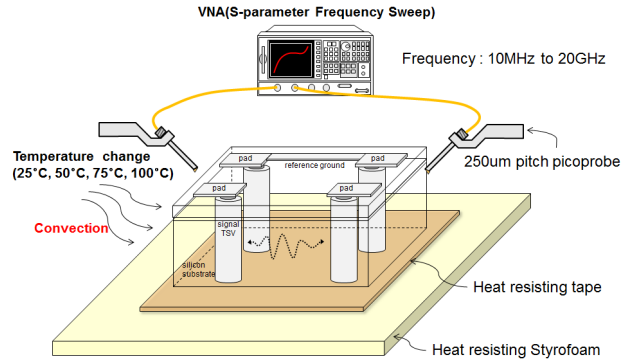to 450°C, a heat from metal can be transferred as a way of convection.

Figure 3. Pre-measurement setup for temperature-dependent TSV noise coupling in frequency domain

Figure 3 shows the pre-measurement setup for observing thermal effect on TSV noise coupling in frequency domain. To prevent electrical leakage from contact between open-ended TSV and metal jig, insulation is necessary. In addition, that insulation should endure from heat. Therefore, heat resisting dielectric material and heat resisting double-sided tape are attached under test vehicle. From this device setup, S-parameters can be obtained when the temperature of the die is changed.
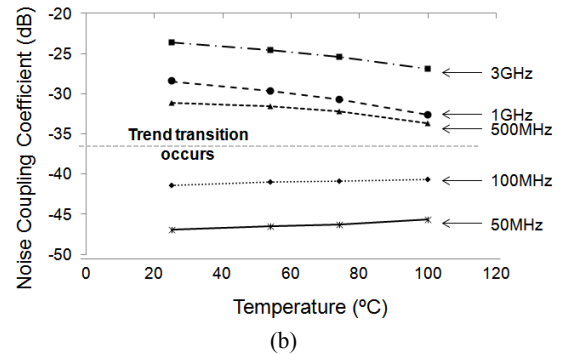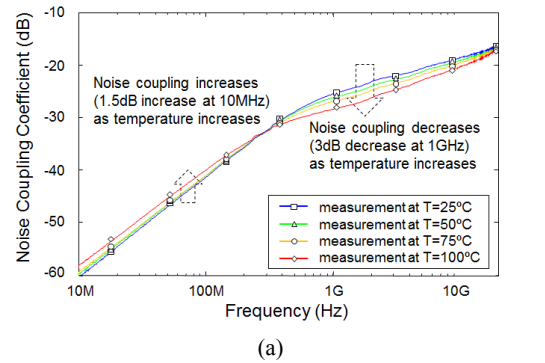

(a)

(b)

Figure 4. (a) The measurement result of noise coupling with temperature variation in frequency domain (b) Noise coupling at some frequencies in temperature domain

Figure 4a shows the result of temperature-dependent noise coupling coefficient in frequency domain. Noise coupling was measured from 10MHz up to 20GHz in frequency range and from 25°C to 100°C in temperature range. The result shows

different aspect in low frequency region and high frequency region. At high frequency region above hundreds of MHz, noise coupling decreases as temperature increases, however at low frequency region under it, noise coupling slightly increases as temperature increases. Over 10GHz range, the trend of noise coupling becomes same as frequency increases. At 1GHz, noise coupling decreases about 3dB, and at 10MHz, noise coupling increases about 1.5dB. About 400MHz range, the trend is reversed. An equivalent result of frequency response in temperature domain is depicted in Figure 4b.

A-2. Noise coupling in time domain

To confirm the frequency domain response of noise coupling shown in Figure 4a, time domain measurement was also performed. In time domain measurement setup, one probe is connected to the pulse pattern generator (PPG), Anritz MP-1763C, instead of VNA, and the other probe is connected to a digital sampling oscilloscope, Tektronix/TDS8000B, to monitor output waveforms. The injected voltage in TSV was 1.0 volt peak-to-peak rectangular clock with 1GHz frequency. Other setup was same as frequency domain measurement. Because the rising time of PPG is about tens of pico seconds, the results may include some high frequency component.
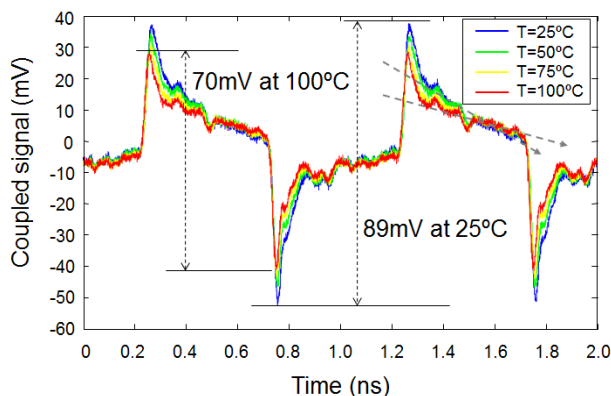

Figure 5. Noise coupling between signal TSVs measurement result with temperature variation in time domain

The time domain measurement result with the variation of temperature from 25°C to 100°C is shown in Figure 5. As the temperature rises until 100°C, the peak-to-peak value decreased from 89mV to 70mV. A peak value of coupled signal can be varied by signal's rising time or falling time, and it is the device's property. Although the peak values are determined by the device's property, the temperature dependence of coupled signal is clearly shown. Rectangular clock signal used as an input signal basically has three frequency components; 1GHz as an operating frequency, about tens of GHz from both rising and falling, and DC component during maintaining constant value of the clock signal. After signal is rising, signal suddenly goes from AC to DC component to maintain voltage until falling starts. This means, the trend reversion from temperature variation shown in frequency domain should be presented in time domain measurement. The slope of the graph gradually becomes flat,

so all of these phenomena shown in Figure 4 are roughly presented in Figure 5.
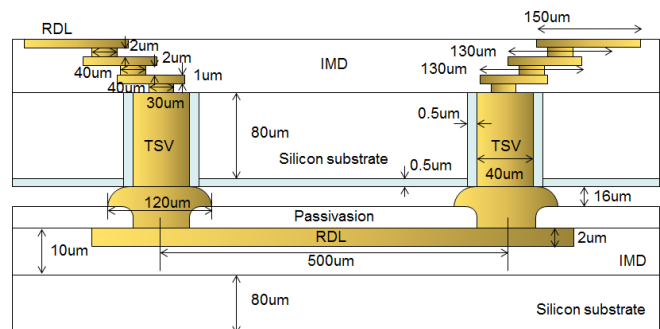
B. Thermal effect on TSV Channel

Figure 6. The dimension parameters of test vehicle for measuring TSV channel

The cross section of stacked die with RDL channel between TSVs is represented in Figure 6, and designed parameters are written in it. This through-pattern for measuring S_{21} of TSV channel was fabricated with the help of KETI. For RDL channel, the length is 500um, the width is 100um, the thickness is 2um, and the pitch is 250um. For TSV, radius is 20um, height is 80um, and oxide thickness is about 0.5um. For bumps between TSV and RDL, the radius is 120um, the height is about 34.6um. The whole length of metal RDL on the TSV is about 200um, and the thickness is between 1um to 2um. (1st stack : 1um, 2nd and 3rd stack :2um)
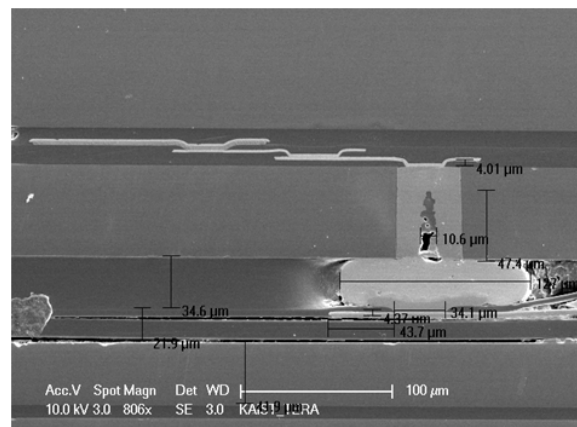

Figure 7. The side view of the test vehicle for TSV channel SEM image.

Although the test vehicle was designed using the values shown in Figure 6, there can be some manufacturing issues and it may include some defects and voids. These variations were carefully considered when the result was analyzed by comparing with temperature dependent model. Some of actual parameters are shown in Figure 7.

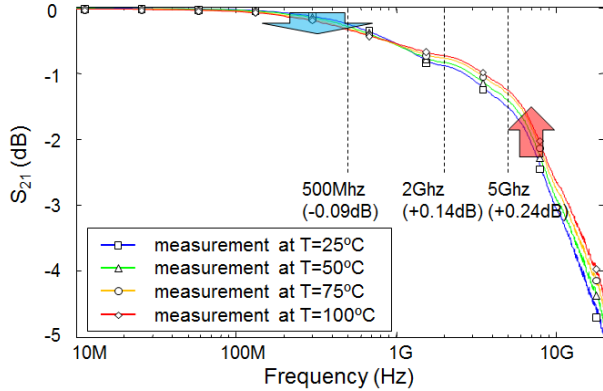*B-1. S_{21} of TSV channel in frequency domain*

Figure 8. S_{21} of TSV channel measurement result with temperature variation in frequency domain

TSV channel has basically similar structure with test vehicle for noise coupling except the RDLs below the TSVs, bumps between RDLs and TSVs, and the bottom silicon die under the RDLs. Therefore, it can be anticipated the S_{21} characteristic will be similarly presented with TSV noise coupling case. S_{21} measurement in frequency domain with temperature variation from 25°C to 100°C is shown in Figure 8. Under GHz range, S_{21} slightly decreases as temperature increases, but over GHz range, S_{21} increases as temperature increases. This means that in low frequency under GHz range, the loss increases as temperature rises, and in high frequency over GHz range, the loss decreases as temperature rises. Thus, this measurement is correspondent with noise coupling result.

B-2. Eye diagram of TSV channel

To confirm the result in frequency domain, eye diagram measurement, which is basically from time domain measurement, at 1Gb/s, 4Gb/s and 10GB/s were conducted. The input signal was 2^{11}-1 pseudo random bit sequence with amplitude of 500mV$_{p-p}$ and the output eye diagram was monitored in oscilloscope.

The eye diagrams from the signal of 1Gb/s, 4Gb/s and 10Gb/s transmitting through the fabricated TSV channel are shown in Figure 9a to Figure 9f. Eye height and jitter were compared between 25°C and 100°C at each bit rate. Each eye diagram was obtained after 5000 cycles. At 1Gb/s, eye height decreases about 1% and jitter is almost same. As shown in Figure 9b, there exists slight signal loss when temperature increases. For 4Gb/s, eye height increases about 2% and jitter is almost same. As shown in Figure 9d, signal loss is decreased when temperature increases. For 10Gb/s, eye height increases about 2.5% and jitter is decreased about 0.4%. As shown in Figure 9f, signal loss is also decreased as the case of 4Gb/s when temperature increases. These eye measurements showed correlation with frequency domain measurement result that the temperature variation affects on the S_{21} of TSV channel and the magnitude of difference varies depending on the input signal's frequency.
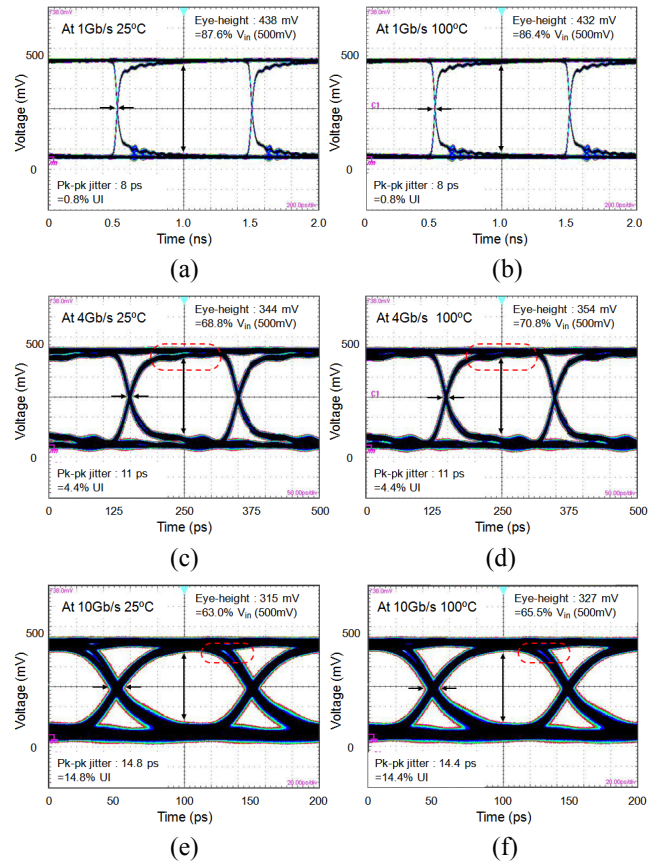

Figure 9. TSV channel eye measurement of (a) 1Gb/s at 25°C (b) 1Gb/s at 100°C (c) 4Gb/s at 25°C (d) 4Gb/s at 100°C (e) 10Gb/s at 25°C (f) 10Gb/s at 100°C

Analysis of thermal effect on TSV noise coupling and TSV channel

In this section, we analyze a thermal effect on signal integrity especially for S_{21} of TSV channel because the structure of TSV channel basically includes the structure for noise coupling. When the temperature of metal increases, lattice scattering, which the vibration of positive charges in the metals disturb the free electrons, is occurred. It causes the increasing of resistance in macro aspect. The test vehicle has four major materials; copper for TSV and RDL pads, silicon for die substrate, silicon dioxide for thin insulation layers covering the TSV, and passivation materials. To analyze the thermal effect of TSV channel, temperature-dependent TSV model should be used. To investigate temperature-dependent TSV channel, same approach with noise coupling was conducted [3]. For TSV channel model, we need some more parts to be modeled. RDLs have significant larger length than TSV height and it should be considered. They can affect not only to the increase of resistance itself but also to the increase of substrate resistance.

All the dimension parameters and material parameters are based on the actual test vehicle's SEM image and known material information.
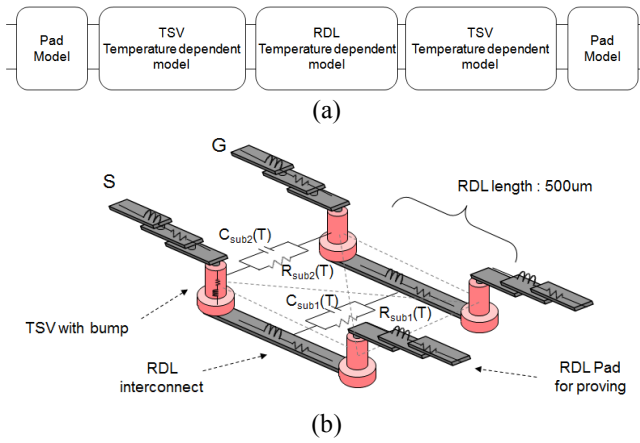
(a)

(b)

Figure 10. (a) A sectional view of temperature-dependent TSV channel (b) simplified modeling of TSV channel.

To establish entire TSV channel model, each section in Figure 10a is modeled separately and connected each other. The parameters related to thermal dependence were shared from top die and bottom die. From Figure 10b, the model of test vehicle is mainly composed of three parts. The first is the RDL extensions on the TSVs for probing, the second is the TSVs in the upper die, and the last is RDLs on the bottom die.

The RDLs and TSVs are composed of copper and modeled as the series of a resistance and inductance. TSVs are covered by thin silicon dioxide layer and these are modeled as a capacitor. For silicon substrate, it is modeled as the parallel of a resistance and capacitance [4]. For the exact model of silicon, every single TSV pair is connected with parallel RC model (dashed line between TSVs, and 'sub2' means the 2nd stack's substrate). The RDL is a metal interconnect which provides horizontal interconnections between stacked dies and parallel RC silicon model through bottom die (sub1, which means the 1st stack's substrate) is also used. Like TSVs, analytic RLGC equations for the equivalent circuit model of single-ended RDL can be modeled [2].
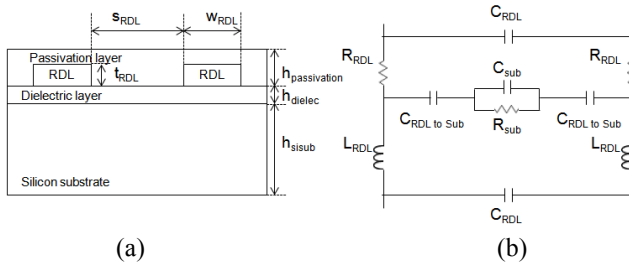

(a)   (b)

Figure 11. (a) Dimension parameters of RDLs (b) equivalent model of RDL

The resistance of RDL (R_{RDL}) is the function of frequency because the current flows along the surface of the RDL as frequency increases as in equations (1) and (2). The thermal effect is considered through resistivity, $\rho_{TSV}(T)$, in equation (1) [5]. A temperature effect to the inductance of RDL (L_{RDL}) is ignored with the assumption of little temperature effect on metal permeability.

$$R_{RDL} = \rho_{TSV}(T)\sqrt{\left(\frac{1}{w_{RDL} \times \delta_{skindepth}}\right)^2 + \left(\frac{1}{w_{RDL} \times t_{RDL}}\right)^2} \quad [\Omega/m] \quad (1)$$

$$\delta_{skin\,depth} = \frac{1}{\sqrt{\pi\mu\sigma \times freq}} \quad [m] \quad (2)$$

The capacitance between two RDL lines, in other words fringe capacitance, is the sum of the capacitance through air gap (C_{air}), passivation ($C_{passivation}$), and dielectric ($C_{dielectric}$), and these values are calculated conformal mapping methods [6]. In addition, there exists another capacitance between RDL and the bottom silicon die, namely 'RDL to substrate' capacitance which is also calculated using conformal mapping method in [7]. The resistance and capacitance of substrate, C_{sub1} and R_{sub1}, are calculated using the concept of effective penetration depth of the electric field into the silicon substrate [8].

In this analysis, the thermal dependence on the resistivity of silicon and the permittivity of silicon dioxide are considered. The test vehicle for TSV channel is made of p-type silicon with $10\Omega\cdot cm$ in room temperature and the temperature dependence of it is applied from [9] [10]. The dimensionless experimental equations of these are obtained from [3] and applied to this TSV channel model as same. For the silicon dielectric constant, a temperature-dependent equation is not determined because the noise coupling difference due to temperature variation over 10GHz is negligible.
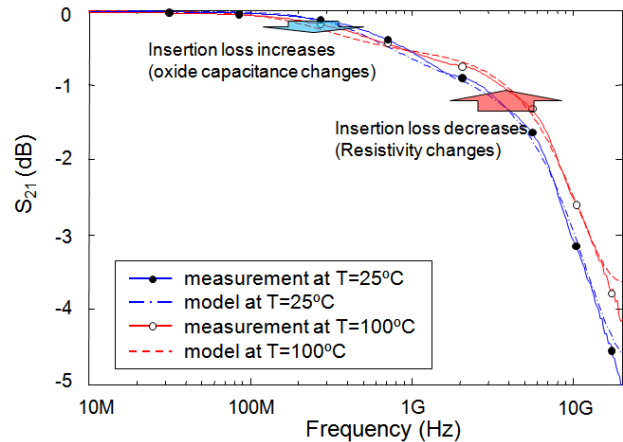

Figure 12. The comparison of temperature-dependent TSV channel model and measurement at 25°C and 100°C

When the temperature-dependent parameters are applied to the model of test vehicle, the result shows good correlation as shown in Figure 12. A low frequency region is dominant region of TSV oxidation and a high frequency region is dominant region of silicon resistance [3]. Because RDLs under the TSVs mainly see silicon substrate of 1st stack, they are modeled similarly as TSVs and explained in a similar way. This result is correspondent to the result shown in temperature dependent noise coupling model [3] and well explains the thermal effect on signal integrity.

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Conclusions

This paper presents the thermal effect on TSV based 3D ICs; in particular the thermal effect on TSV signal integrity is presented. TSV noise coupling and S_{21} of TSV channel were measured in both frequency and time domain within 25°C to 100°C temperature range, and TSV channel was simply analyzed using the corresponding temperature-dependent TSV model. For p-type 10Ω·cm silicon substrate, increasing temperature decreases the S_{21} of TSV channel under the hundreds-of-MHz frequency range, but over that frequency range, increasing temperature increases the S_{21}. Therefore, it can be anticipated that the signal transmission will show different aspect depending on both frequency and temperature.

Acknowledgments

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