Thermal Impact on High Speed PCB Interconnects

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Abstract—As signal speeds increase, small imperfections start to dictate the performance of interconnects. Thermal effects are an inseparable aspect of interconnects due to self-heating caused by the flow of current, and due to environmental heating in high speed designs. This paper presents in detail, thermal effects and their impact on insertion loss, crosstalk and phase of high-speed signals. The paper also describes the thermal sensitivity on various aspects of interconnect design such as inter pair spacing, trace height, and dielectric thickness. For our analysis, simulations were performed using field solvers for temperatures ranging from 20°C to 100°C. Finally, results are analyzed with percentage variation in copper loss versus dielectric losses.

Keywords—Thermal sensitivity, high speed design, crosstalk, insertion loss.

I. Introduction

The demand for speed is constantly increasing with every technology upgradation. While PCIe speeds have doubled every generation from 8 Gbps (@ Gen 3.0) to 16 Gbps (@ Gen 4.0) to 32 Gbps (@ Gen 5.0), the channel loss budgets have not doubled [1]. This has in-turn reduced the margin of error in high speed designs, thereby putting a lot of pressure to consider all possible impairments that would impact high speed printed circuit boards (PCBs). Thermal effect is an inseparable aspect of interconnects due to self-heating (Joule heating) and environmental heating. In the past, thermal impacts have been studied for submicron VLSI interconnects that limit the current density [2]. This paper focuses on thermal impacts on high speed PCB interconnects.

In this paper, section II explains the sources of heat in PCBs. Thermal impact on PCB traces is discussed in Section III. Thermal sensitivity on various aspects of interconnect design is studied in Section IV and section V summarizes the paper.

II. Heat Sources

There are two kinds of heat sources, one due to Joule heating and the other due to environmental heating [4][5]. Joule heating takes place due to current flow in the conductor, while environmental heating is due to the ambient temperature. Resistivity of Cu interconnects increases with increase in temperature. As temperature increases, the random motion of electrons increases, which causes an increase in the resistivity as given in (1).

$$\rho(T) = \rho(T_0)[1 + \beta(T - T_0)] \quad (1)$$

where, ρ represents resistivity, β represents temperature coefficient of resistivity, T_0 is the room temperature (25°C) and T is the interconnect temperature during operation [6][7]. Similarly, the dielectric constant of material also increases with increase in temperature. Table I shows the measured values of dielectric constant and loss tangent with respect to temperature [8] for a mid-loss material.

III. Thermal Impact on PCB Traces

In this section, insertion loss, phase and crosstalk effects are modeled with respect to change in temperature. Differential microstrip and stripline traces of 1-inch length are considered in our analysis. Electromagnetic field solvers are used for simulation. Table II shows dimensions for microstrip and stripline configurations, where t_w, t_s, d, h_1, t_h and h_2 represent trace width, intra-pair spacing, inter-pair spacing, core thickness, trace height and prepreg thickness, respectively. For analyzing the thermal impact, temperatures of 20°C, 60°C and 100°C are considered. Figs. 1 (a) and 1(b) show the insertion loss variation due to temperature for microstrip and stripline, respectively. It shows that insertion loss increases with frequency. For this particular material, stripline and microstrip loss increase is 23% and 15% respectively at 25 GHz as temperature increases from 20°C to 100°C.

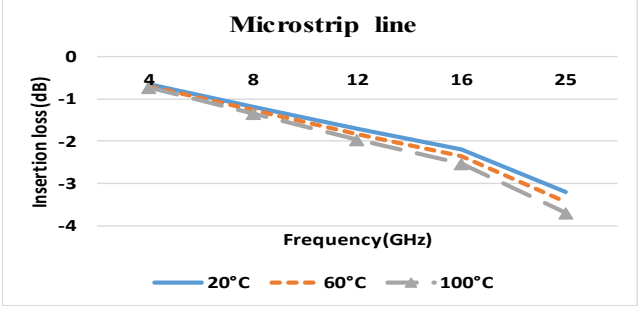
Fig. 2 shows the phase delay with respect to temperature at 25GHz frequency. As temperature increases, the magnitude of phase delay increases. As the temperature rises, the interconnect dielectric constant and resistivity increase which increase the phase delay. Fig. 3 shows the far-end crosstalk (FEXT) effects with respect to temperature for microstrip. As temperature increases, insertion loss increases, which dampens the FEXT. At 25 GHz FEXT is reduced by 1.5 %. Stripline traces exhibit little to no FEXT due to the homogenous nature of the dielectric on both sides.

TABLE 1: Material properties with respect to temperature[8]

Temperature (°C)	Dk (Dielectric constant)	Df (Loss tangent)	Resistivity (Ohm-m)
20	4.23	0.0124	1.72E-08
60	4.26	0.0146	2.00E-08
100	4.3	0.0173	2.27E-08

TABLE II: Dimensions for differential line (mil)

	t_w	t_s	d	h_1	t_h	h_2
Microstrip	4.75	7.8	14.25	2.85	1.3	---
Stripline	3	5.25	15.5	3	1.3	4.55



(a)

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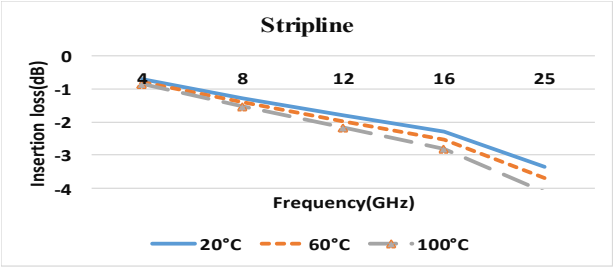

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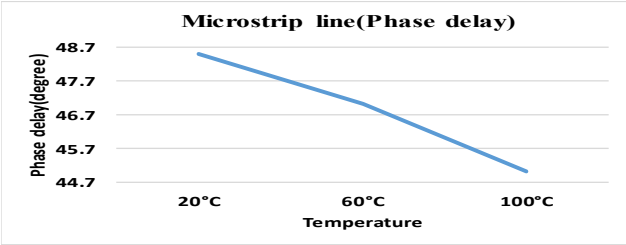
Fig. 1: Insertion loss variation with temperature (a) Microstrip (b) Stripline



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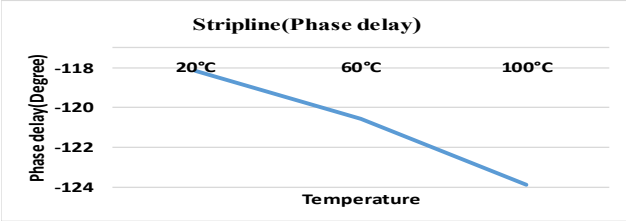


(b)

Fig. 2: Phase angle variation with respect to temperature @25GHz (a) Microstrip (b) Stripline

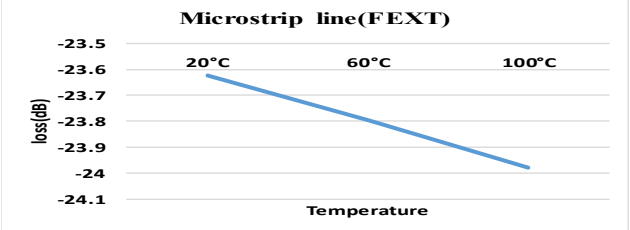


Fig. 3: FEXT effects with temperature on microstrip @25GHz

IV. Thermal Sensitivity To Interconnect Design

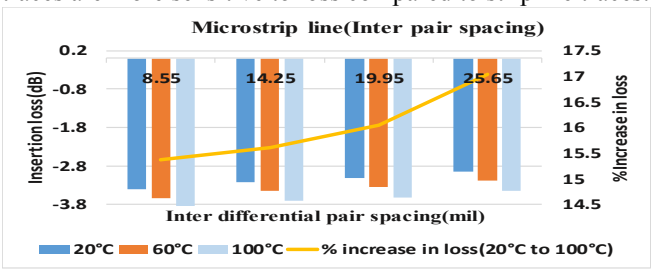
In this section, thermal sensitivity to various aspects of interconnect design such as inter-pair spacing, trace height and dielectric thickness are analyzed. The analysis is performed for an 85 ohms impedance at 25 GHz. Trace dimensions are taken from Table II for a 1-inch differential line. Percentage loss from copper and dielectric medium is analyzed for microstrip and stripline structures. Thermal impact of via is also analyzed with and without planes.

In the below sub-section, the term 'percentage increase in loss' is used and is defined as per (2). This term is helpful to analyze the thermal impact on microstrip and stripline.

$$Percentage\ increase\ in\ loss = \frac{\text{loss}(100°\text{C}) - \text{loss}(20°\text{C})}{\text{loss}(20°\text{C})} * 100 \quad (2)$$

A. Inter-pair spacing

The thermal effects are analyzed with respect to inter-pair spacing for both microstrip and stripline. Fig. 4 shows that as inter-pair spacing increases, the loss variation due to temperature also increases. Temperature variation has more impact on microstrip trace loss when inter-pair spacing is increased as compared to stripline. The percentage increase in loss is about 2% on microstrip compared to 0.5% on striplines. Capacitive coupling between traces is the reason behind this trend. As the inter-pair spacing increases the capacitive coupling decreases, increasing the loss. Coupling plays more significant role in microstrip traces compared to stripline. Hence, with change in inter-pair spacing, microstrip traces are more sensitive to loss compared to stripline traces.



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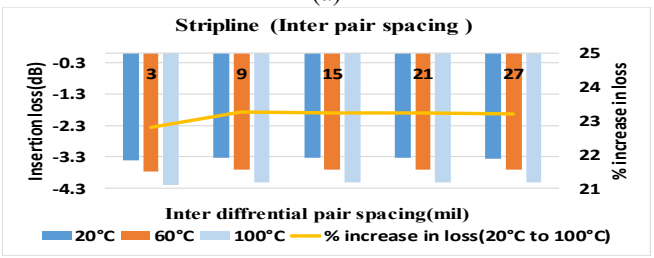
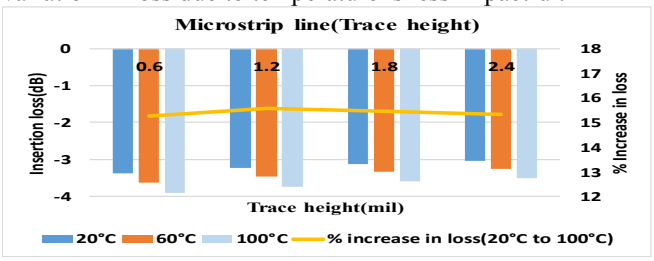


(b)

Fig. 4: Insertion loss with respect to inter pair spacing at various temperatures (a) Microstrip (b) Stripline

B. Trace height

In this section, thermal effects are analyzed with respect to trace height variation. Trace heights of 0.6mils, 1.2mils, 1.8mils and 2.4mils are considered. For microstrip, percentage increase in loss due to trace height is negligible as shown in Fig. 5a. Fig. 5b shows that for striplines, percentage increase in loss increases by about 3%. As the trace loss decreases, the percentage variation in loss due to temperature increases. In striplines, as the trace height increases, the trace loss decreases, increasing the loss percentage variation due to temperature. In microstrip traces, the trace loss is not decreased significantly as the trace height increases due to the thin dielectric thickness assumed. Hence, the percentage variation in loss due to temperature is less impactful.



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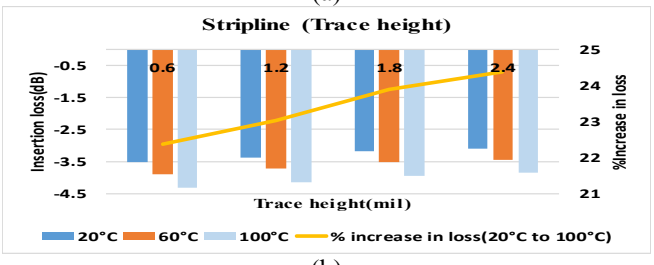

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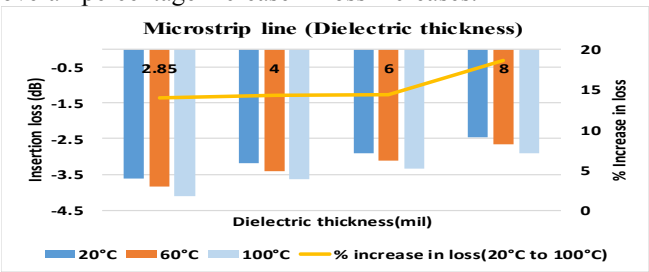
Fig. 5: Insertion loss with respect to trace height at various temperatures (a) Microstrip line (b) Stripline

C. Dielectric thickness

In this section, temperature effects are analyzed with respect to dielectric thickness variation for microstrip and stripline traces. For microstrip, dielectric heights of 2.85mils, 4mils, 6mils and 8mils are considered. Fig. 6a show that as dielectric thickness increases, percentage increase in loss also increases. Percentage increase in loss is 5% for microstrip due to dielectric thickness variation.

In case of stripline, dielectric height is varied for various core/prepreg combinations like 3/3 mils, 3/4 mils, 5/8 mils and 8/10 mils. Fig. 6b shows that the percentage increase in loss increases as dielectric thickness increases. Percentage increase in loss is 5% for stripline. As the dielectric thickness increases, the traces become less capacitive and therefore the overall percentage increase in loss increases.



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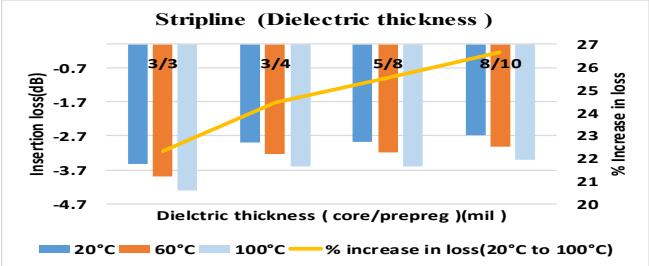

(b)

Fig. 6: Insertion loss with respect to trace height at various temperature (a) Microstrip line (b) Stripline

D. Copper and dielectric loss

When a signal propagates through an interconnect, there will always be some loss. There are two kinds of losses, copper/conductor loss and dielectric loss. These losses increase as temperature of the interconnect increases. In this section, the percentage increase in loss due to Copper and dielectric medium of an interconnect with respect to temperature is studied. Fig. 7 shows that 19% and 24% increase in loss due to temperature is from copper and 76% and 81% increase in loss due to temperature is from dielectric medium for stripline and microstrip, respectively.

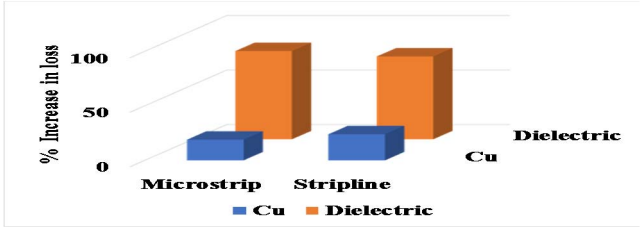

Fig. 7: Dielectric and copper loss percentage from temperature increase (20°C to 100°C)

E. Impact on via

Temperature impact on vias has a different trend as compared to transmission lines. As the frequency increases, the thermal impact on vias becomes negligible. This is due to the capacitive coupling between vias and planes. A plane less via model was created to show that vias would behave like transmission lines in the absence of planes. When the via insertion loss is dominated by the via-planar capacitance, percentage increase in loss reduces.

TABLE III: INSERTION LOSS COMPARISON OF VIAS WITH 0 AND 8-PLANES

Frequency(GHz)	0-Planes	8-Planes
4	15%	42%
8	18%	35%
12	37%	20%
16	38%	13%
20	19%	12%

V. CONCLUSION

In this paper, thermal impact is studied on microstrip and stripline traces along with PCB vias. It is found that ~18% of loss variation can be due to temperature variation. If a PCB stack-up is carefully designed, the sensitivity of transmission lines with respect to temperature can be reduced. Temperature variations considered range from 20°C to 100°C for PCB stack-up. As a result, insertion loss and phase delay of traces increase and FEXT reduces.

In this paper, temperature variation effects are studied with respect to stack-up parameters like inter pair spacing, trace height and dielectric thickness. It is seen that loss increases when inter pair spacing, trace height or dielectric thickness of transmission lines increase. However, in microstrip traces, the loss reduces marginally as the trace height increases. For vias, the percentage increase in loss is very minimal due to thermal impact since most of losses are dominant due to interplanar capacitance.

VI. ACKNOWLEDGEMENTS

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