Gen 4 PCIe Connector & Channel Design and Optimization: 16GT/s for Free

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Tim owns passive channel interconnect pathfinding for the I/O technology and standards group within Intel's data center organization.

Tim’s duties include design, simulation and measurement at the component and full-channel level. He supports Intel’s fastest data paths, which include PCI Express, fabric, on-package memory, and CPU coherency buses. He has 14 years of experience in client and server SIE.

He was also awarded a PhD in Engineering Science by Washington State University, and also holds BS and MS degrees in Electrical Engineering and a BS in Engineering Physics from the University of North Dakota.
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Steve is PCIe SI Technical Lead in Intel’s data center group.

He has 12 years of experience in server SIE, and is co-author of *High Speed Digital Design: Design of High Speed Interconnects and Signaling*.

He served a central role in delivering the industry's first PCI Express Gen3 product, and has been a pivotal contributor in the design and analysis of several other high speed channels.

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Marc serves as a member of the I/O standards and enabling organization within the datacenter group.

He began his electronics career in 1974 at Tektronix, first as a technician and later as a manufacturing engineer and researcher in Tek Labs. Marc joined Intel in 2005 where he works to develop next generation, high-speed serial communications systems such as PCI Express and USB.

Marc holds a Bachelor of Arts degree in Mathematics and Physics from Whitman College.
Why We Are Here

- We have a vested interest in ensuring PCIe interoperability, whether we are working on the baseboards mounting PCIe connectors or on add-in cards plugging into PCIe connectors.

- Intel sells both:
  - Baseboards
    - Multi-socket server boards
  - Add in cards
    - Network interface cards
    - Xeon Phi® supercomputing cards
    - Solid state storage solutions
Disclaimers

- We are here on behalf of Intel, and do not represent the PCI-SIG®
  - Though we are active contributors to the SIG
  - The PCI-SIG owns all PCIe specifications, and oversees all the workgroups

- We cannot comment on specific Intel products, roadmaps, or IP

- Any techniques we introduce should be verified in simulation and measurement before applying them to your products
  - The spec, not this presentation, will be the ultimate authority
Scope

- Our focus will be the Gen4 passive channel
  - With special emphasis on connector interface
    - PCIe connector
    - Baseboard pinfield
    - Add-in card

- Little attention will be paid to the silicon
  - Equalization, Protocol, etc.
Mission

- Identify and characterize the impact of any PCIe channel impairments
  - e.g. stubs, dielectric loss, or impedance mismatches

- Evaluate the suitability of existing PCIe Gen 1-2-3 style connectors, particularly the thru-hole mount version, at 16GT/s Gen 4 speeds

- Develop, optimize, and evaluate suitable remediation methods
  - e.g. material or geometry changes

- Prioritize any enablers and propose them for inclusion in the Gen 4.0 PCIe Card Electromechanical spec
The methods we propose may, when combined, allow us to continue using the existing PCIe Gen 3.0 thru-hole mount connector at 16GT/s Gen 4.0 speeds.

- This could result in significant cost savings

- This is achieved without requiring significant cost adders with respect to the connector interface such as new connector materials, backdrilling, new connector designs, tighter PCB artwork tolerances, etc.
Updates To Other Channel Elements Won’t Be Free!

- Of course, channel factors other than the connector will require significant scrutiny as speeds double.

For example:
- Package and PCB loss may require lower loss materials
- Package pinfield crosstalk may require reshuffling of pinouts, or additional pins

- These will come at a cost
Overview

- Background on signaling and bandwidth
- Add in cards, connectors, mounting styles
- Edge finger length and plating
- Via stub mitigation
- Full channel considerations and budgeting
- Ground conductor resonance 8GHz & adjacent ground via method
- Sideband conductor resonance 4.5 GHz & AC sideband termination
- Via dimensions and baseboard pinfield discussion
- Baseboard broadband crosstalk suppression using sentry vias
Signaling, Bandwidth, and Performance

- Before we discuss the channel and components we should review the traffic that flows through them
  - Provides insight into the bandwidth demands
Data Rate and Bandwidth Requirements

- Line encoding schemes such as 8-bit/10-bit (8B/10B) are used to ensure transition density, but they incur overhead that reduces the effective throughput.

- PCIe Gen 1 & 2 used 8B/10B encoding
  - Effective data payload is $8 \div 10 = 80\%$ of the raw data rate.

- PCIe Gen 3 & 4 use 128B/130B encoding
  - Effective data payload is $128 \div 130 = 98.5\%$ of the raw data rate.
Data Rate and Bandwidth Requirements

- When we account for the line encoding scheme, the effective data rate doubles (or nearly doubles) with each PCIe generation.

- The frequency spectral bandwidth doubles as well, with some dependence on edge rate.

<table>
<thead>
<tr>
<th>PCIe Gen.</th>
<th>Raw Data Rate</th>
<th>Line Encoding</th>
<th>Effective Throughput</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>2.5 GT/s</td>
<td>8B/10B</td>
<td>2 Gbit/s</td>
</tr>
<tr>
<td>2</td>
<td>5 GT/s</td>
<td>8B/10B</td>
<td>4 Gbit/s</td>
</tr>
<tr>
<td>3</td>
<td>8 GT/s</td>
<td>128B/130B</td>
<td>7.877 Gbit/s</td>
</tr>
<tr>
<td>4</td>
<td>16 GT/s</td>
<td>128B/130B</td>
<td>15.754 Gbit/s</td>
</tr>
</tbody>
</table>
Data Rate and Bandwidth Requirements

- We would like a frequency bandwidth target for this effort

- We find most of the signal power lies far below the 16GHz harmonic limit we may use as a rule of thumb
  
  - The **sinc function** is used to obtain the spectrum of square edged functions
  
  - Factoring in the **power weighting function** to account for risetime lowers the bandwidth further
Regardless of how we compute the power spectral content of a signal, perhaps we can agree that the bandwidth roughly doubles with data rate.

We could start with the \( \text{sinc}^2 \) function \( \left( \frac{\text{Sin}(x)}{x} \right)^2 \) to approximate the power spectrum of a square wave.

- There is probably faint hope of energy at the 3\(^{rd}\) harmonic or above.

But if we consider the risetime and perhaps the bandwidth of the receiver, we find that the bandwidth required for the connector is even lower.

- For a 16 GHz signal with a 25% Unit Interval (UI) → 16.625 ps risetime
- After we do the math, we find that perhaps 86% of the energy lies below 8GHz, and 91% of the energy lies below 9GHz.

- Power content drops off steeply, so if we push crosstalk into higher frequencies, for example, the net crosstalk power in the frequency of interest is reduced.
- ~86% of the power lies below 8GHz
- ~91% of the power lies below 9GHz
- If we optimize for this range, it's a good start
The PCI Express connector is a card edge connector

- Gold plated edge fingers on the mating add in card (AIC) engage the connector contacts

- The connector is available in four different lengths:
  - x1, x4, x8, x16
    - the number of Tx/Rx pairs
  - Pronounced “by one”, “by four”...

- Typically referred to as the “CEM Connector”

- Very inexpensive – Cost less than $1
Do I Have to Use the CEM Connector for PCIe?

- It’s OK to route PCIe signals using a different kind of connector, through a cable, or with no connector
  - But if you want to interface with other companies’ hardware, you must comply with a common spec
We can subdivide the connector interface into three regions:

1. The add-in card (AIC) including the gold plated card edge fingers

2. The connector body

3. The baseboard [= motherboard or host] including the pinfield pads and vias
The pinfield can be broadly divided into two sections (x16 connector shown):

- Pins 1 through 11 are not important to us
  - DC power, JTAG, SMBUS, Wake, Reset, etc.

- Pins 12 to 82
  Our interest lies with these pins
  - High speed differential pairs
  - Grounds
  - Differential 100MHz Ref Clock
  - Low speed sideband signals
Add-in Card Pin Assignment

- The **A** side of the add in card is also called the **solder** side
  - Typically mounts only low profile components
  - The **A**-side pins, labeled A1-A82, include all of the high speed **Rx** pairs

- The **B** side of the add in card is also called the **component** side of the board.
  - Typically mounts the main integrated circuits, heatsink, connectors, and thick components
  - The **B**-side pins, labeled B1-B82, mount all of the high speed **Tx** pairs

- **Note that the terms **Tx** and **Rx** are with respect to the host**
  - **Tx** = driven from the motherboard
  - **Rx** = driven from the add in card

- The pinfield is **geometrically symmetric** front-to-back for both the add-in card edge fingers and the connector footprint

- The pins’ signal assignments are very irregular, however
Connector Mounting Styles

Thru-Hole Mount (THM) connectors

- Straight mounting pins extend through the host baseboard
- Pins protrude beyond PCB bottom to permit a solder fillet on the backside pad.
Press fit (PF) connectors

- Conformal eye-of-the-needle pins provide a tight mechanical fit against the via walls.
- This eliminates the need for a subsequent solder operation following PCB component placement (stuffing).
- These permit back-drilling (stub removal) in thick boards.
Connector Mounting Styles

Surface mount (SMT) connectors

- Generally allow less congested routing in lower baseboard layers, since smaller vias may be used
- May increase complexity or cost of assembly
- Mechanical risks are low
In terms of baseboard PCB layout and electrical performance, the Thru-Hole Mount and Press Fit styles will be considered to be functionally equivalent.

- Same PCB geometry
- Perhaps some slight performance difference

Historically, the soldered thru-hole mount version has been used far more than the press-fit connector, due to its ease of assembly.
There is significant industry pressure to find a workable signal integrity solution for Gen 4 using the thru-hole & press-fit connector

- Presumably important for cost sensitive applications
- That is where we focus most of our effort
- We will revisit surface mount connectors later in the presentation
Problem Statement

- Above 4GHz, the PCIe thru-hole connector interface has multiple channel impediments that severely affect channel signal integrity
  - If commonly applied PCIe Gen 1-2-3 PCB design methods are used.
What is Wrong With the Current PCIe Connector at 16GT/S?

The short answer is:

Nothing is wrong with the connector itself

(nothing major, at least)

At 16GT/s Gen4 speeds, most of the problems with using Gen3 connectors lie in the mating circuit boards
Gen 1-2-3 Performance vs. Gen 4

- For Gen 1-2-3 designs, channel degradation due to the connector interface was not very pronounced.

- Here we consider the connector interface to comprise:
  - The connector itself
  - The baseboard pinfield
  - The gold-plated edge finger region of add-in card

- At Gen 4 speeds, not only does performance plummet, but three different frequency responses are observed among different lanes in the same connector.
Constraints

- Any solution should preserve forward & backward compatibility among PCIe Gen 1-2-3-4 cards and connectors
  - Run at the lowest common speed
    - A Gen 4 add in card plugged into a Gen 2 capable board will be limited to Gen 2 speeds
  - No change in the pin assignments or connector/pinfield geometry allowed
- Use only common materials for the connector and PCB, with no exotic manufacturing or assembly techniques
  - We cannot mandate laser microvias, for example
We will focus on pins B12 to B26

- Add-in card shown engaged with connector pins
  - Plastic connector body not shown

- Three high speed differential pairs
  - Tx0 (Red)
  - Tx1 (Green)
  - Tx2 (Blue)

- Seven **Ground** pins (Black)

- Two sideband pins - single ended
  - **Reserved** (Aqua)
  - **Present** (Grey)
Edge Finger Length

- The length of the add in card edge finger was shortened from 4.30 mm to 3.91 mm for the CEM spec
  - Reduces the risk that metal burrs will form during the chamfer operation to cause shorts, etc.
  - This is not new
    - Approved by the CEM in the Gen 3.0 timeframe
Edge Finger Dimensions

- Original edge finger dimensions: \(0.7 \text{ mm} \times 4.3 \text{ mm}\)

Lower PCB edge engages the connector
Edge Finger Dimensions & Chamfer

- A 20° chamfer is present at the edge of the add in card to help it smoothly engage the connector pins.

- There is a chance that burrs could be created at the tips of the edge fingers when this bevel is machined.

- Chamfering is not completely precise.
Edge Finger Plating Tie Bar Detail - Original Finger Length

PRESENT pin is connected indirectly for plating

Chamfer grinds fingers back to this line

Final board edge

Risk of metal burrs forming

Plating tie bar

RESERVED
GROUND
TX0P
TX0N
PRESENT
GROUND
TX1P
TX1N
GROUND
TX2P
TX2N
GROUND
GROUND
Edge Finger Dimensions – Revised length

- We can shorten the edge fingers’ length from 4.3 mm to 3.91 mm to reduce the risk of burrs
Plating tie bars are still required, but the narrower widths of chamfered metal reduce the risk of burrs & shorts.
In accordance with this ECO to the spec the edge fingers must:

- Must have a length of 3.91 mm
- Use plating tie bar widths in the range
  - 0.20 mm to 0.51 mm
  - = 8 mils to 20 mils

There is a slight, but definite signal integrity benefit in keeping the plating tie bar narrow.
The Gen 3.0 CEM spec requires that, in the edge finger region of the add in card, all inner metal layers are voided
   – Only surface metal is present – just the edge fingers

This has been violated in many cases in the past
   – Perhaps an oversight
   – Or an ill-advised attempt to provide “shielding” from crosstalk
Add-in Card Pinfield Ground Plane Voiding

- Remove all inner layer metals beneath the edge fingers, and in the chamfer region

Planets voided (no inner layer metals) within the edge finger region of the add-in card
Examples of Plane Voiding

- Correct add in card plane voiding is easily verified
  - Hold the card up to the light
  - Spec compliant voiding is evident from the light visible between the edge fingers, and below

Glow is from backside lighting
We have found several cases of incomplete ground voiding.

Some have complete ground floods, while others are partially flooded.
- The presence of inner layer ground planes beneath the relatively wide edge fingers creates high parasitic capacitance.

- The capacitive loading between the edge fingers ground planes is fatal at Gen4.

- At 8 GHz, 68% of the incident energy is lost due to reflection.
  - Even at 4 GHz, 36% of the incident energy is reflected.
  - Only 5% reflection at 8 GHz if the planes are properly voided.

### AIC Finger Region Plane Voiding

**Return Loss with/without ground plane voiding**

![Graph showing return loss with and without ground plane voiding.](image-url)
This causes noticeable signal loss, even at Gen 1.0 data rates

At 8 GHz, roughly 27% of the transmitted energy survives
  - vs. 86% for the baseline case
Note that the ground pins (Black) flanking the differential pairs are Single or Double.

Three combinations are possible for Tx pairs:
- **Tx0**: Two adjacent Single grounds
- **Tx1**: One adjacent Single ground and one Double ground
- **Tx2**: Two adjacent Double grounds

These represent all combinations across the pinfield, for both Tx and Rx.
Simulated insertion loss (thru) for
- Baseboard
- Thru-Hole connector
- AIC fingers

Typical Gen 1-2-3 construction
Relatively benign
- Baseboard 1.57mm [62 mil] thick
- No connector pin via stub
- Add in card has relatively short 2.2 mm long ground feeds

PCle Gen 1-2-3-4 frequency bandwidth requirements are indicated
Typical Frequency Response vs. Gen 1-2-3-4 Bandwidth

Three distinct XTalk frequency responses

Lane 0 ↔ 1
Lane 1 ↔ 2
Lane 0 ↔ 2

Differential Return Loss (Reflect) for a typical Gen 1-2-3 layout

Differential Crosstalk (FEXT) for a typical Gen1-2-3 layout

Tx0: 2x Single Grounds
Tx1: 1x Double Ground
1x Single Ground
Tx2: 2x Double Grounds
At 7-8 GHz, strong resonances emerge in the ground conductors. A length of wide trace connects the AIC ground edge finger and ground via. High field intensity on the ground conductor. Add in card ground Via. Connector Contact.
The resonant frequency is related to the distance between:

- The bottom of the connector ground contact (motherboard surface)
- The AIC ground via (end of the hockey stick)

We cannot shorten the connector, but we can shorten the distance between the ground finger and its ground via.
Prior to Gen 4, *most*, but not all dimensions in the edge finger region were fully constrained

- The ground finger connection *was not* addressed by the Gen 1-2-3 CEM spec

In practice, ground fingers have commonly been connected to the ground plane with a length of wide trace leading to a via, as shown

- Minimize the conductor length in order to increase the resonant frequency to beyond 8-9 GHz

- **Lower the ground vias to shorten the resonating ground conductor**
Place the ground vias as close as possible to the ground finger

- Since each **ground** finger opposes a **signal** finger on the back side of the card, the vias are center-aligned with the gaps between fingers.

- Shown here with 10/20/30 mil vias (drill/pad/clearance)
Joining Adjacent Single Ground Vias

We can also unite the ground vias of adjacent double ground pads

- Reduces crosstalk by raising the resonant frequency of the double grounds
- Without this, the double grounds can actually perform worse than the single grounds
Some (slight) additional reduction in crosstalk is obtained if the vias are doubled

- But this may restrict the clearance for escaping signal traces (not shown)
- We suggest that double ground vias are **OPTIONAL**
- Observe that some seemingly unconnected vias are present for backside grounds
Performance Improvement - FEXT

- Compare a relatively benign Gen3 style board (2.2 mm ground via trace) with an identical board implementing both *Double Adjacent Vias* and *Joined Ground Vias*

Lane 0 - Lane 1 FEXT spike is suppressed, moved to the right

Baseline: Dashed  
Improved: Solid

Lane 1 - Lane 2 FEXT spike is suppressed, moved to the right

Baseline: Dashed  
Improved: Solid
Performance Improvement – Insertion Loss

- Compare a relatively benign Gen3 style board (2.2mm ground via trace) with an identical board implementing both *Double Adjacent Vias* and *Merged Ground Fingers*

Lane 0 insertion loss spike is moved beyond 8 GHz

Lane Tx1 insertion loss spike is moved beyond 8 GHz
Poor Practice – Long Ground Traces

- Legacy board with long ground traces and no shared ground vias
Poor Practice – Long Ground Traces

- Legacy edge finger design with ground fingers connected to separate ground vias through long traces
- Both front and back surface edge fingers and routing are shown
- Separate ground vias, shown here, are not necessary
- Sharing ground vias fingers between front and back of the card would allow very short connections from the ground fingers
- The increased ground trace length increases the negative effects of ground finger stub resonance

This ground trace is 6.3 mm long, \( \approx 50\% \) longer than the ground finger itself
Worst-case Example

- Instead of the baseline 2.2 mm long ground trace, compare to the crosstalk of a 6.4mm test case

FEXT - Simulated

FEXT spikes fall in the middle of our Gen4 frequency band

FEXT - Measured

Measurement largely confirms simulation

Lane 0 ↔ 1
Lane 1 ↔ 2
Lane 0 ↔ 2
Worst-case Example

- This case is actually Gen 3 compliant
  - Its only “crime” is a long ground connection

Insertion Loss - Simulated

Return Loss - Simulated

Thru performance drops out in the middle of the critical 0-8GHz band

Insertion loss is very high for half of the 0-8GHz frequency band
Recommendations: AIC Adjacent Ground Vias

- Place one ground via adjacent to every edge finger ground
  - The ground vias should be center aligned with the gap between edge fingers
  - Ground vias should be placed as close as the PCB fab pad-to-trace or pad-to-shape clearance rules permit
  - Join adjacent double ground fingers with surface etch

- The minimum via drill size is likely sufficient
  - 8 or 10 mil, for example

- Share ground vias between front-side and back-side ground fingers
Recommendations: AIC Adjacent Ground Vias

- Double Adjacent AIC Ground Via approach **OPTIONAL**
  - Place a ground via in every gap between edge fingers
  - This will connect **two** adjacent vias to each “single ground” edge finger
  - This will unite **three** adjacent vias for each adjacent “double ground” edge finger pair
Cost

- This could be a low-cost or no-cost solution, since thru hole vias are inexpensive, and would be required anyway

  - If this replaces a “one ground via per finger” layout, it is possible that fewer ground vias will be used
A slight cost increment will be incurred if there is an increase in the surface that is gold plated

- The adjacent ground vias may be difficult to mask for plating and may simply need to be gold plated

This would be a consequence of shifting the hard gold plating boundary slightly beyond the edge fingers, across the ground vias

Extra gold required to plate this area, which is normally covered with soldermask
Decoupling capacitors are required for the baseboard Tx lanes

- It is often cost effective to place these discrete components on the topside of the baseboard, to permit use of more routing layers

- In Gen 3, an 062 mil pinfield via stub could be risky

- In Gen 4 an 062 via stub could be very serious

- But it is hard to avoid a stub if we have to route into the connector from a topside capacitor
One possibility is to use *Boomerang Vias* to transit the board twice, to avoid the via stub.
The boomerang via removes the stub effect, which starts at about 4GHz.

- **Color code for insertion loss plots**
  - 62 mil stub
  - Boomerang via
  - Zero stub, backside fed

**Differential Deembedded THRU 85 Ohm**

[Graph showing measurement data]
Boomerang Via

- Boomerang vias reduce or eliminate the stub effect
  - When used to connect upper layer signals to a signal pin, they reduce the stub length by 50-100%
  - The extra vias can have the minimum drill diameter; they don’t need to be 27 mil finished holes (like the pins)
  - Simulation and measurement show insertion loss performance that equals to the conventional no-stub backside fed pin
    - Pinfield crosstalk is actually a little lower
Similar between Gen3 and Gen4, the electrical budget could be considered approximately 60% Silicon and 40% Interconnect.

- Considering 0.2 UI Tx jitter, 0.3UI* receiver margin, and 0.7ps RMS ref clock.
- Largest consumer of interconnect budget is insertion loss.

*RX eye of 0.3UI includes some non-silicon noise sources.
Loss Budget: Role of Connector+PTH and Packages

- 30% Loss Budget Increase at 16GT/s vs 8GT/s of 23.5dB
- Expectation of 12-14” reach
- 28dB budget is constrained with Gen3 assumptions
  - 2.5dB for connector + PTH\pin
  - ~7dB for Gen3 reference package at 8GHz
- Only 7” remains for PCB route (MB + Card) or 10.8dB
- Channel Enablers
  - Mid-loss PCB (loss tangents nominally ~0.015)
  - Connector boomerang via and edge finger improvement
  - Asymmetric reference packages (3dB and 5dB)
  - Reduced AIC budget (MB benefit)
- 13” available for PCB route (MB + Card)
Enablers for PCB Loss Reduction

- Material with lower loss tangent
- Thicker core or prepreg
- Smoother copper surface
- Wider conductor trace
- Material with low dielectric constant

Differential Insertion for 10” trace on Various Stack Ups
# Microstrip Add In Card Loss Solutions for 8dB Budget

As an example – 4dB is allocated for PCB trace (3dB for package, and 1dB for via & crosstalk)

First Order Assessments – Not simulated against CEM standard

<table>
<thead>
<tr>
<th>Dielectric</th>
<th>Trace Width / Space / Height</th>
<th>Copper Roughness</th>
<th>8G Loss Rate @highT (dB/inch at 8GHz)</th>
<th>PCB Length</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standard dielectric</td>
<td>6 / 5 / 4</td>
<td>Standard</td>
<td>1.337</td>
<td>3.0”</td>
</tr>
<tr>
<td></td>
<td>8.5 / 5 / 6</td>
<td>Standard</td>
<td>1.187</td>
<td>3.4”</td>
</tr>
<tr>
<td>Mid-loss dielectric</td>
<td>6 / 5 / 4</td>
<td>Standard</td>
<td>1.212</td>
<td>3.3”</td>
</tr>
<tr>
<td></td>
<td>8.5 / 5 / 6</td>
<td>Standard</td>
<td>1.064</td>
<td>3.8”</td>
</tr>
<tr>
<td></td>
<td>8.5 / 5 / 6</td>
<td>VLP/other</td>
<td>0.980</td>
<td>4.1”</td>
</tr>
<tr>
<td>Low-Loss dielectric</td>
<td>6 / 5 / 4</td>
<td>VLP/other</td>
<td>0.786</td>
<td>5.1”</td>
</tr>
<tr>
<td></td>
<td>8.5 / 5 / 6</td>
<td>VLP/other</td>
<td>0.742</td>
<td>5.4”</td>
</tr>
</tbody>
</table>
**Stripline Add In Card Loss Solutions for 8dB Budget**

### TX traces

- 0.25 dB
- Height
- Via stub

### RX traces

- 1.25 dB
- Height
- Via stub

- **Optimized via to ~0.25dB @ 8GHz**

### 85 Ohm Stack Up Solutions

<table>
<thead>
<tr>
<th>Dielectric</th>
<th>Trace Width / Space / Height</th>
<th>Copper Roughness</th>
<th>8G Loss Rate @ highT (dB/inch at 8GHz)</th>
<th>PCB Length</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Standard dielectric</strong></td>
<td>5 / 6.5 / 4</td>
<td>Standard</td>
<td>1.415</td>
<td>2.8”</td>
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<tr>
<td></td>
<td>7 / 6.5 / 6</td>
<td>Standard</td>
<td>1.301</td>
<td>3.1”</td>
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<td>Standard</td>
<td>1.316</td>
<td>3.0”</td>
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<tr>
<td></td>
<td>7 / 6.5 / 6</td>
<td>Standard</td>
<td>1.201</td>
<td>3.3”</td>
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<tr>
<td></td>
<td>7 / 6.5 / 6</td>
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<td>1.139</td>
<td>3.5”</td>
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<td>VLP/other</td>
<td>0.824</td>
<td>4.8”</td>
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<tr>
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<td>7 / 6.5 / 6</td>
<td>VLP/other</td>
<td>0.719</td>
<td>5.5”</td>
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</tbody>
</table>

As an example – 4dB is allocated for PCB trace (3dB for package, and 0.5 to 1.5dB for vias)

First Order Assessments – Not simulated against CEM standard
Managing Reflection: Ground Plane Removal at Edge Finger

AIC Edge Finger
With Ground Plane Removed

Lab Measurement of Pulse at Motherboard RX
Anonymous AICs; TXLE = P7

Differential Voltage (V)

18mV reflection near DFE 4 and 5 positions
Managing Reflection: Boomerang via at PCIe Connector

Example Boomerang Via Layouts

Connector + Via TDR Response
16L .093” Stack Up

- L10 (30 mil stub)
- L10 (Boomerang)
- L3 (80 mil stub)
- L3 (Boomerang)

Over-optimization
Managing Reflection: Boomerang via at PCIe Connector

Simulated EH

Layer 10: Negligible change

Layer 3: Significant enabling

Simulated EW

Layer 3: Significant enabling

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<thead>
<tr>
<th>L10_30mil_Stub</th>
<th>L10_Boomerang</th>
<th>L3_80mil_Stub</th>
<th>L3_Boomerang</th>
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</thead>
<tbody>
<tr>
<td></td>
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</tr>
</tbody>
</table>

Eye Height (mV) vs. Distance

Eye Width (ps) vs. Distance

-designcon 2016

January 19-21, 2016

#DC16
Managing Crosstalk: Attention to Vertical Coupling

- Device S:G ratio is increasingly important
- Device pinmap determines vertical via coupling in the board
- Coupling is significant with insufficient ground pin isolation
- Shorter via stubs actually lead to MORE crosstalk
  - Coupled for a greater distance
  - Negates the benefit of short-stubs
- Further, thicker boards experience more crosstalk

![Diagram showing short and long coupled length](image)

- Short Coupled Length
- Long Coupled Length

- More Reflection, Less Crosstalk
- Less Reflection, More Crosstalk
Managing Crosstalk: Attention to Vertical Coupling

High TX-TX Crosstalk Ball Map

Far End Crosstalk Pulse Response
DUT: 1” – via – 1”

<table>
<thead>
<tr>
<th>Distance</th>
<th>Layer</th>
<th>Connection</th>
</tr>
</thead>
<tbody>
<tr>
<td>8L .062&quot;</td>
<td>L1 → L3</td>
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</tr>
<tr>
<td>8L .063&quot;</td>
<td>L1 → L8</td>
<td></td>
</tr>
<tr>
<td>14L .093&quot;</td>
<td>L1 → L14</td>
<td></td>
</tr>
</tbody>
</table>
Managing Crosstalk: Attention to Vertical Coupling Polarity

- Vertical to trace transition (breakout) can effect how crosstalk accumulates in the channel
  - Constructive or Destructive
- Blind connectivity can inadvertently lead to optimistic crosstalk levels – caution!
- Know the PCB layout – simulate appropriately
- Caution: Reliance on destructive crosstalk may not be realized – many factors at play
Managing Crosstalk: Attention to Vertical Coupling Polarity

Far End Crosstalk Response
8” Microstrip Trace with Via

Constructive
Destructive

Only difference is how via connects to PCB

Measured Far End Crosstalk Channel Response: Unrealized Crosstalk Reduction
Baseline Gen3 Server Board & Add-in Card

Gen 3 style construction

- **Add-in card**
  - 062 mil FR406
  - 2.2 mm AIC ground via connection
  - Nominal 0.7 mm wide fingers
  - Edge finger plating bar ECN applied

- **Motherboard**
  - 120 mil thick FR406
  - 10 planes
  - Via antipads are 53 mils
  - 30 mil via stub

- **No sideband termination**
In practice, most sideband signals designated as RESERVED are unconnected to the motherboard and AIC, in Gen 3.0 style boards.

The sideband via, connector pin, and add-in card edge finger are often floating nets.
- solid geometry in figure →
In some of the previous slides shown above (both simulation and measurement), the sideband signals were resistively terminated on both ends with 42.5Ω

This is not realistic

In practice, all sideband signals are poorly terminated or unused, i.e. open circuited, in Gen 1-2-3 boards

What happens if the sideband signals are terminated in worst case impedances?
  - Perhaps 1 Meg Ω? Or 0 Ω, perhaps at the end of a long trace?
Unterminated Crosstalk/Resonance

Far End Crosstalk (FEXT) - Simulated

Insertion Loss (Thru) - Simulated

Crosstalk spikes in the middle of the Gen4 band

Lane 0 ↔ 1
Lane 1 ↔ 2
Lane 0 ↔ 2

Corresponding dropout in insertion loss

Lane Tx0
Lane Tx1
Lane Tx2
Coupling and Resonance Mechanism

- Energy is coupled from high speed pairs and grounds into the sideband conductor
- Multiple reflections occur at the resonant frequency of the floating, or otherwise mismatched, sideband conductor
  - The resonant energy is coupled into another high speed pair

![Diagram showing coupling and resonance mechanism](chart)
Remedy: Sideband Signal Termination

- Simplified Options:
  - If the sideband conductors are connected to a matched resistance, the resistor will absorb the coupled energy, and no resonance will be possible (no multiple reflections)

1. Resistor on the motherboard alone, ~42Ω-50Ω, between sideband signal’s connector pin and ground plane

2. Resistor on add-in card alone, ~42Ω-50Ω, between sideband signal’s gold edge finger and ground plane

3. Resistors on both motherboard and add-in card
What benefit do we gain? FEXT

FEXT (Simulated)
Unterminated sidebands

Add 43Ω resistors on sidebands

FEXT (Simulated)
Sidebands terminated on both ends
What benefit do we gain? Thru

**Insertion Loss:**
- Unterminated sidebands
- Sidebands terminated on both ends

Add 43Ω resistors on sidebands
Compare Simulated FEXT to Measurement

- Fair correlation, measurement is a little lower
  - Note: These plots address a thinner 062 mil board
Measured with/without Termination

No termination resistors

Resistors on both ends

Resistors on one end (add-in card only)

Color code for crosstalk
Lane 0 ↔ Lane 1
Lane 1 ↔ Lane 2
Lane 0 ↔ Lane 2

Color code for crosstalk
Lane 0 ↔ Lane 1
Lane 1 ↔ Lane 2
Lane 0 ↔ Lane 2

Color code for crosstalk
Lane 0 ↔ Lane 1
Lane 1 ↔ Lane 2
Lane 0 ↔ Lane 2
Thru-hole vs. Surface Mount, Measured

No termination resistors

Thru Hole, 062 mil thick

Surface Mount

Color code for crosstalk
Lane 0 ↔ Lane 1
Lane 1 ↔ Lane 2
Lane 0 ↔ Lane 2

Color code for crosstalk
Lane 0 ↔ Lane 1
Lane 1 ↔ Lane 2
Lane 0 ↔ Lane 2
What are the functions of the sidebands?

- Sideband (auxiliary) pins
  - PRESENT2#
  - CLKREQ# - Clock Request (formerly RESERVED) Pin B12
  - PWRBRK# - Power Brake (formerly RESERVED) Pin B30
  - Five unassigned RESERVED pins

- Many PCIe sideband pins within the high speed region of the card are unused, and the edge finger pads have been depopulated in some Gen 3 cards
  - Depopulating them doesn’t help, and is actually counterproductive
PRESENT# Pins

- The motherboard connector PRESENT2# contact is connected to a DC net to detect card length and sense hot-plug extraction.

- In a x16 card, the PRESENT2# pins, such as the x1 x4 x8 PRESENT2# pins would be unconnected on the AIC
  - Similar for x4 and x8 length cards
  - On x1 length cards, only the x1 pad will be present, and it is used.

- Unused PRESENT AIC edge finger pads do not connect to any net on the AIC
  - i.e. unconnected to AIC graphics chip components, etc.
  - Spec says it’s OK to depopulate the pads (this needs to change)
  - The connector pin contact will always exist, though.
Reserved Pins

- RESERVED
  - These are typically left as unconnected edge finger pads on most AICs
  - Unlike PRESENT2#, RESERVED are also unconnected on the motherboard at the base of the connector pin
  - So the pin and pad typically float, electrically
  - Apart from these two former Reserved pins (CLOCK REQUEST# and POWER BRAKE#) there are five remaining RESERVED pins in a x16 card
Complications – DC Path

- We can’t just add a resistor to ground, since that may disrupt the assigned function of the pin
  - Sideband signals are very slow, so perhaps we can essentially terminate to a resistance at >1GHz
  - Series RC to DC decouple the noise

\[
X_c = \frac{1}{2\pi f \cdot C}
\]

- e.g. 1pF @ 4.4GHz → 36.2Ω

- What’s the highest frequency we need to leave untouched, and what impedance do we need to present?
  - i.e. 1.5 kΩ at 100 MHz?

<table>
<thead>
<tr>
<th>Cap pF</th>
<th>Xc @4.4GHz</th>
<th>Xc@100MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>36.2</td>
<td>1592</td>
</tr>
</tbody>
</table>
Channel Results – AC Termination

- For a 28dB full-channel simulation, Lane 0 is clearly the chief challenge for the baseline case
- Compare to the “No Connector” case

Remember we need to satisfy all three lanes, since all three are present on every x4, x8, and x16 card

As expected, adding termination greatly Improves Lane 0
- Somewhat improves Lane 1, little effect on Lane 2

<table>
<thead>
<tr>
<th>Eye Height (mV)</th>
<th>Higher is better</th>
<th>Eye Width (ps)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lane 0</td>
<td>Lane 1</td>
<td>Lane 2</td>
</tr>
<tr>
<td>17.36</td>
<td>21.75</td>
<td>23.28</td>
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<tr>
<td>19.55</td>
<td>22.28</td>
<td>23.50</td>
</tr>
<tr>
<td>19.28</td>
<td>22.22</td>
<td>23.54</td>
</tr>
</tbody>
</table>

|                      |                 |                |              |
| 30.14                | 30.52           | 30.12          | ← No Connector → | 25.15 | 25.65 | 25.10 |

**Eye Height (mV):** Higher is better

**Eye Width (ps):**
Compare 120 mil vs. 62 mil Motherboard

FEXT, 120 mil motherboard

Thicker board has higher FEXT & lower resonant frequency

Additional resonance at ~2x the frequency

FEXT, 062 mil motherboard

Additional resonance at ~2x the frequency
Representative Termination Scheme

- RC termination is shown on the add in card only
  - Motherboard is left un-terminated

No termination (open circuited)

Conductors on the baseboard

Conductors on the add in card

RC termination absorbs coupled energy & blocks DC
What if the pin is in use?

- Even with a tee connection, at one or both ends, with an imperfect termination, the damping will help
Possible Add-in Card Implementation

- DC Voltage Rail
- High impedance pullup resistor ≥10 kΩ
- Low speed and power signals Pins B1-B11
- Connection to CLKREQ# (Clock Request) logic circuits on add-in card.
- “Tee” connection
- Connection to PWRBRK# (Power Brake) logic circuits on add-in card.
- Connection to baseboard ground through PRESENT1# (Presence Detect) connector pin A1
- “Tee” connection
- Unused PRESENT2# Pin B31
- Unused PRESENT2# Pin B48
- Unused RESERVED Pin B82
PRESENT Signal In Use vs. Not In Use

- We expect the unused PRESENT pins on the add-in card can be terminated with no problem.

- The one PRESENT pin that is used on the AIC will have a T-connection, which will make termination imperfect.
  - Fortunately the active PRESENT pin will always be at the end of the card, so little or no crosstalk will result.
Motherboard Pinfield

- PCIe x4 pinfield is shown, for context
  - The area we have been modeling is indicated

Region modeled in plots & drawings
The baseboard plated-thru hole (PTH) finished hole diameters are tightly constrained

- 0.7 mm = 27.6 mil finished (plated) hole to accommodate the thru-hole connector pin
- Commonly drilled with a 0.75 mm or 29.5 mil drill
- The baseboard pin locations \((x,y)\) are completely constrained
- The pin pitch is regular, but the signal assignments are not
Via Drill and Pad Size

- The baseboard via dimensions can have an effect on signal integrity
  - Via pad (annular ring) diameter
  - This a parameter we can control

- For thru-hole and press-fit parts, the connector manufacturers typically specify a baseboard pad diameter of 1mm
  - 1mm = 39.37 mils, ≈ 39 or 40 mils
  - This satisfies the common PCB pad size requirement
    Pad = Drill + 10 mil = 29.5 + 10 = 39.5 mil

- In legacy designs we have found that larger pad sizes are common
  - 43 to 45 mil pads
There are two penalties from using a via pad size that is too large

1. Increased reflection and insertion loss
   - This is a consequence of increased capacitance

2. Decreased trace routing “alleys” between pins
   - This is especially important if our antipads grow larger
   - It would be valuable if we could recoup 5 or 6 mils of baseboard routing space between pins
Assuming via and trace dimensions of:

- 29.5 mil drill
- 45 mil pad
- 59 mil antipad

59 mil is probably the minimum antipad for high speed signals in Gen 4 PCIe. It could be bigger.

- 5 mil trace width
- 7 mil trace spacing
- \(5 + 7 + 5 = 17\) mils pair width

Depending on the antipad size we might route over voids if the layers are not aligned (mis-registered)
This section addresses a third crosstalk issue that is related to the motherboard.

This stems from an inconsistent \textit{Signal:Ground} distribution across the motherboard PCIe pinfield.

- High via-to-via crosstalk is present in the baseboard.
- This is a direct consequence of the CEM spec thru-hole pinfield pattern.
- The crosstalk is broadband – not just a resonant peak.
Sentry Vias

- Small ground vias adjacent to sideband pins
- Affects the motherboard alone, and not the add-in card
- Provides broadband crosstalk reduction
  - Also provides significant benefit for insertion loss at high frequencies
- Proposing as required
Recall that the pin assignments are not uniform.

Note that the ground pins (Black) adjacent to the differential pairs are Single or Double.

Three combinations are possible:

- Two adjacent Single grounds (Tx0)
- One adjacent Single ground and one Double Ground (Tx1)
- Two adjacent Double grounds (Tx2)
We showed that straightforward AIC layout changes can reduce crosstalk magnitude and push the resonant peaks beyond 8GHz.

When the baseboard is not considered, FEXT is better than 48dB in the 0-8 GHz range.

**Improved Add in Card Design**

- Baseboard vias/pins were NOT included in the simulation.
- Adjacent AIC vias and AC sideband termination are added.

-49 dB maximum (reduced from -21dB)

**Color code for crosstalk**
- Lane 0 ↔ Lane 1
- Lane 1 ↔ Lane 2
- Lane 0 ↔ Lane 2
The AIC improvement shown above reflects only the simulation connector & AIC with no via & motherboard included.

Now we turn our attention to the baseboard.
- How much crosstalk contribution stems from the baseboard via field?
Add the Via Pinfield

- Desktop stackup
  - 62mil, 4-layer, no stub
  - Likely a best case stackup for low FEXT/NEXT

Compare two cases:
- Improved AIC + AC Termination + Connector (Dashed)
- Improved AIC + AC Termination + Connector + Baseboard

Color code for crosstalk
- Lane 0 ↔ Lane 1
- Lane 1 ↔ Lane 2
- Lane 0 ↔ Lane 2
Observations

- The far end crosstalk of the connector body and add in card alone (ignoring the motherboard) is low
  
  - FEXT increases dramatically when even a relatively thin 062 mil motherboard is added to the connector model
  
  - We can presume that thicker motherboards would have even greater coupling among connector vias in the PCB

- The crosstalk between lanes 0↔1 is much higher than the crosstalk between lanes 1↔2
Now Consider The Baseboard Alone
Pinfield Studied

- Tx (B-side) pinfield
  - Three pairs
  - Two sideband signals
  - Seven grounds

- Sideband signals:
  - Reserved and Present
  - Are floating or undefined impedances, for the most part
  - They essentially take the place of a Ground via in the typical pattern Ground-Ground-Signal-Signal-Ground-Ground …
Pinfield Ground Via Insufficiency

- Signal: Ground differences
  - Blue differential pair has four ground vias (typical pattern)
Another perspective

- Blue differential pair has four ground vias (typical pattern)
- Green differential pair has three ground vias & one sideband via

Pinfield Ground Via Insufficiency
Pinfield Ground Via Insufficiency

- Another perspective
  - Blue differential pair has four ground vias (typical pattern)
  - Green differential pair has three ground vias & one sideband via
  - Red differential pair has two ground vias and two sideband vias
Pinfield Ground Via Insufficiency

- Blue differential pair has four ground vias (typical pattern)
- Green differential pair has three ground vias & one sideband via
- Red differential pair has two ground vias and two sideband vias

- High speed differential pairs adjacent to sideband signals don’t have as many ground pins.
Remedy: Add Baseboard Ground Vias

- Add small ground vias or “Sentry Vias” adjacent to the higher impedance sideband signal vias
  - Use minimum drill size – 8 mils shown here, 10-12 mils could work
  - Hopefully they will not obstruct routing lanes
  - Sideband signals are unused, low speed, or DC, so we shouldn’t perturb these signals by adding adjacent Ground vias
PCIe x4 pinfield shown, for context
- We want to add two sentry (ground) vias per sideband pin
  - Perhaps as many as four
Extend to Other Sideband Pins

- We can apply this approach to all the sideband pins
- It can also be used for the Ref Clock
Baseboard Vias Alone

- Note that while simulating vias by themselves can be quick and give insight into what the baseboard effects are, the connector + AIC + baseboard should be simulated together to confirm any findings.
Crosstalk between lanes 0 & 1 is **33dB** for the PCB alone (no connector).

**Dashed:** AIC + Connector + Baseboard Vias/Pins

**Solid:** Baseboard vias alone. 62 mil thick baseboard. The baseboard vias probably account for most FEXT.
Add 2 Baseboard Sentry Vias

- Baseboard only – no connector
- Adding two sentry vias per sideband pin improves the worst case FEXT
  - Lane 0 ↔ Lane 1 FEXT drops by about 4.5dB across much of the 0-8 GHz band
  - Lane 1 ↔ Lane 2 largely unaffected
If we look at the vias in the 062 baseboard as single ended conductors, the reason for the improvement looks clear – i.e. viewing +/- legs of differential pairs individually.

- These signal vias have ONE adjacent ground pin assigned, NO sentry vias
  - Tx0 P & N  Tx1 N

- These signal vias have ONE adjacent ground pin assigned, and three sentry vias per sideband pin

- These have TWO adjacent double ground vias assigned, NO sentry vias are needed
  - Tx1 P  Tx2 P & N

- These have TWO adjacent double ground vias assigned, NO sentry vias are needed
  - Tx1 N  Tx2 P & N
What about thicker boards?

- If we thicken the same board from thin 62 mils to server board thickness 120 mils, we’d expect more crosstalk
  - Caveat – it is still only 4 layers but is probably not a bad example
  - Return to differential S-parameters
Improved Thicker Baseboard FEXT – 120 mil

- Thicker 120 mil 4-layer baseboard pinfield
- No connector, PCB Only
- Two added ground vias for each sideband signal can dramatically reduce FEXT in the thicker board across the whole frequency band

![Graph showing improved FEXT with added ground vias](image-url)
For the thicker board (no connector), the DIFFERENTIAL via insertion loss is markedly improved with the addition of two sentry vias per sideband pin.

Baseline thick 120 mil baseboard suffers noticeable degradation in the Thru.

That’s actually worse than the connector alone: 0.67 vs. 0.43 dB.

Same config, plus two ground vias per sideband improves insertion loss by 0.4dB.
Now consider the FEXT with the combined baseboard and connector again, 120 mil thick

Baseline 120Mil board
- No extra ground vias
- 42.5Ω Sideband termination resistors

8GHz Lane 0-1 FEXT is improved by about 6dB

29.1 dB: Baseline 120mil baseboard

↓ ↓ ↓ ↓ ↓ ↓

34.9 dB: Baseline 120 mil baseboard + 2 ground vias

The improvement is across the whole band, which is very good
Now consider the FEXT with the combined baseboard and connector mil thick,

- Measured data showing the crosstalk benefit for **Tx Lane 0 ↔ Tx Lane 1**
- Note that these data show the improvement within one lane, not differences among lanes.

**Baseline 120Mil board**
- **No extra ground vias**
- 1pF 42.5Ω AC Sideband term

**Same 120Mil board configuration**
- **Two or Four** sentry vias per pin

<table>
<thead>
<tr>
<th>Via Qty</th>
<th>4 GHz</th>
<th>7.7 GHz</th>
<th>8 GHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>37.8</td>
<td>28.7</td>
<td>30.9</td>
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<tr>
<td>2</td>
<td>41.9</td>
<td>35.5</td>
<td>41.2</td>
</tr>
<tr>
<td>4</td>
<td>42.7</td>
<td>37.0</td>
<td>43.5</td>
</tr>
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</table>
CHANNEL RESULTS
Baseline Gen 3 Server Board

Gen 3 style construction

- **Add-in card**
  - 062 mil FR406
  - 2.2 mm AIC ground via connection
  - Nominal 0.7 mm wide fingers
  - Edge finger plating bar ECN applied

- **Motherboard**
  - 120 mil thick FR406
  - 10 planes
  - Via antipads are 53 mils
  - 30 mil via stub

- **No sideband termination**
Recall that for a 28dB full-channel simulation that included the connector, Lane 0 was the chief challenge for the Gen 3 baseline configuration.

Compare this to the No Connector case.
  - Try to achieve this as our goal.

Remember we need to satisfy all three lanes, since all three are present on every x4, x8, and x16 card.

### Channel Results – AC Termination

<table>
<thead>
<tr>
<th>Eye Height (higher is better)</th>
<th>Eye Width (higher is better)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lane 0</td>
<td>Lane 1</td>
</tr>
<tr>
<td>30.14</td>
<td>30.52</td>
</tr>
<tr>
<td>9.74</td>
<td>19.00</td>
</tr>
</tbody>
</table>
Channel Results – AC Termination

- We saw that merely adding AC sideband termination to the baseline case helped recoup about half of the lost Eye Height and Eye Width
  - Terminating only one end is a good start

<table>
<thead>
<tr>
<th>Eye Height (higher is better)</th>
<th>Gen 3 Baseline</th>
<th>Eye Width (higher is better)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lane 0</td>
<td>Lane 1</td>
<td>Lane 2</td>
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<td>30.14</td>
<td>30.52</td>
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<td>9.74</td>
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<td>21.54</td>
</tr>
<tr>
<td>19.70</td>
<td>20.99</td>
<td>20.88</td>
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</tbody>
</table>
Add Other Low Risk Improvements

Additional enablers
- Four sentry vias on each sideband pin
- Improved (larger) antipads
- Adjacent AIC ground finger vias
- Joined add-in card ground vias
Add Other Low Risk Improvements

- Getting much closer to the No Connector case when we add
  - Four sentry vias on each sideband pin
  - Improved (larger) antipads
  - Adjacent add-in card ground finger vias
  - Joined add-in card ground finger vias

<table>
<thead>
<tr>
<th>Eye Height (higher is better)</th>
<th>Sentry vias &amp; other enablers</th>
<th>Eye Width (higher is better)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lane 0</td>
<td>Lane 1</td>
<td>Lane 2</td>
</tr>
<tr>
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<td>30.52</td>
<td>30.12</td>
</tr>
<tr>
<td>23.27</td>
<td>24.93</td>
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<td>24.93</td>
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<tr>
<td>24.65</td>
<td>24.86</td>
<td>25.12</td>
</tr>
<tr>
<td>25.33</td>
<td>25.51</td>
<td>25.14</td>
</tr>
</tbody>
</table>
Summary – The Enablers

- We obtain the best performance if we combine all of our channel enablers
  1. Reduce high frequency crosstalk with adjacent AIC ground vias
  2. Dissipate mid-band resonant crosstalk with AC termination
  3. Suppress broadband crosstalk with sentry vias
  4. Use boomerang vias to avoid via stubs
Additional Takeaway Comments

- No single enabler will mitigate the potential problems
- Success with PCIe Gen4 will require a close interaction of the signal integrity engineer and the board layout staff
  - Ensure consistency by incorporating these changes into your layout symbol to reduce the chances of errors creeping into your design
  - Review the ODB++ artwork before going to fab
    - Check plane voiding & suppress non functional via pads, for example
- Even with the enablers applied, thru hole connectors may not be sufficient to enable Gen4 in some channels
  - Consider surface mount connectors instead
Thank you!

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QUESTIONS?