Significant Reduction of Common-Mode Noise in Weakly Coupled Differential Serpentine Delay Microstrip Lines Using Different-Layer-Routing-Turned Traces

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Abstract—This paper proposes a new structure to reduce the commonmode noise (CMN) of weakly coupled differential serpentine delay lines (DSDLs) in microstrip line structure. In the proposed CMN reductions structure, different-layer-routing-turned traces are used as substitutes for same-layer-routing-coupled turned traces (i.e., as in the conventional scheme). The proposed reduction schemes, which are based on different-layer-routing-turned traces, include the original reduction scheme, in which all traces are impedance matched, and the improved reduction scheme, in which all traces have a narrow width. In the time domain, the peak-to-peak amplitude of the CMN obtained by the proposed solution is more than 90% higher than that obtained by the conventional scheme. Implementing the reduction scheme in DSDLs reduces differential-to-common mode conversion ($|S_{cd21}|$) by at least 20 dB (range 0.8–16 GHz). The causes of the improved signal integrity are also investigated. Therefore, an improved CMN reduction scheme for DSDLs is proposed. Regarding the frequency domain, the asymmetry can limit the CMN reduction at low frequencies. Symmetry is an important requirement for DSDLs in the proposed CMN reduction scheme. Finally, a favorable comparison between the simulated and measured results confirms the substantial CMN reduction achieved by the proposed schemes.

Index Terms—Common-mode noise (CMN), differential reflection loss, differential serpentine delay lines (DSDL), differential-to-common mode conversion, signal integrity.

I. INTRODUCTION

A S CLOCK frequencies and data transmission rates in semiconductor systems begin to exceed the GHz range, the timing control of high-speed clocks and digital data propagated via trace signals on printed circuit boards (PCBs)

and packages is becoming a critical issue in high-speed digital circuit design [1]. Although several methods for minimizing clock or digital data signal skew have been presented, delay lines are generally used in the critical nets of a PCB or package. For example, conventional serpentine routing schemes are widely used in industrial PCB design. The use of differential signaling in modern high-speed digital circuits is increasing. Interference is not problematic in differential lines compared with single-ended transmission lines [2]. Notable applications include Serial Advanced Technology Attachment III (SATA III/6 Gb/s), High Definition Multimedia Interface (HDMI/5 Gb/s), PCI Express interconnect III (8 Gb/s), Thunderbolt (10 Gb/s), and USB 3.0 (5 Gb/s) devices. Because these high-speed digital systems rely on multiple differential line pairs, timing synchronization is an important design issue. A recently developed solution is the differential serpentine delay line (DSDL).

In high-speed data links, cables and connectors used to transmit differential signals among various electronic devices or PCBs can cause electromagnetic interference (EMI) because common-mode noise (CMN) is coupled to I/O cables or connectors, which act as antennas [3]. Hence, during the design of state-of-the-art electronic systems, reducing the CMN that is induced by differential interconnects, is critical. A recently developed solution is the use of common-mode filters (CMFs), which include defected ground structure (DGS) filters [4] and electromagnetic bandgap (EBG) filters [5]. Another recently developed CMF solution is use of the differential signals that cross a planar EBG [6], [7] to suppress the harmonic components of the portion of the CM signal generated by skewed differential signals. In a wideband CMF that uses several cascading quarter-wavelength resonators, implementation is greatly facilitated using a multilayer structure and multiple differential signaling pairs for high-speed digital systems [8].

In DSDLs, the CMN is dominated by the length mismatch of the coupled turned traces, the length of the parallel differential coupled traces, and the crosstalk between the parallel pairs of differential coupled lines [9]. Recent studies have proposed various methods of reducing the CMN produced by differential bends, including the use of capacitance [10], inductance [11] or slow-wave structures [12] to reduce discontinuity in the bend and the use of tightly coupled microstrips [13].
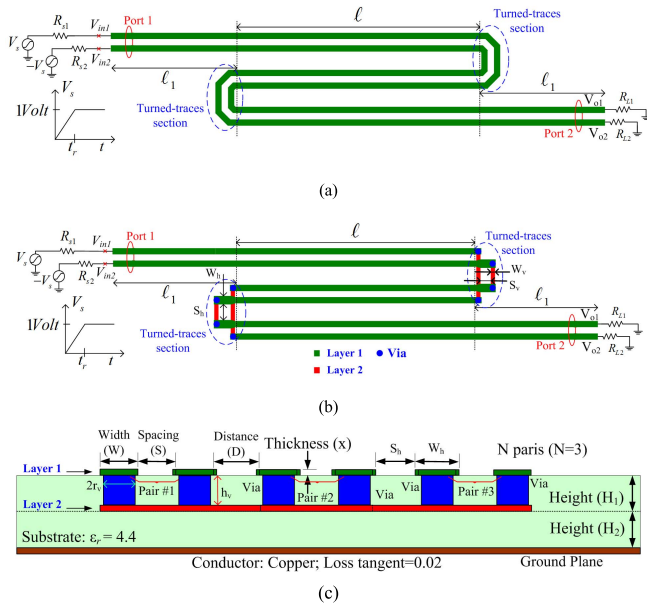
Fig. 1. (a) Conventional routing scheme in which all traces are in one layer and (b) proposed CMN reduction routing structure with different-layer-routing-turned traces for weakly coupled DSDLs. (c) Cross-sectional view of two weakly coupled DSDLs.

In a previous work [14], the CMN reduction schemes developed for weakly coupled DSDLs used strongly coupled turned traces instead of weakly coupled turned traces (as in the conventional scheme) and added guard traces. The substantial noise reduction obtained by the combined structures was verified in the time domain and the frequency domain. The conventional routing pattern comprises same-layer-routing-coupled turned traces (conventional scheme) for weakly coupled DSDLs. This paper proposes a new and more effective CMN reduction structure in which different-layer-routing-turned traces are used in weakly coupled DSDLs [Fig. 1(b)]. This new reduction structure adopts different-layer-routing-turned traces instead of conventional same-layer-routing-coupled turned traces in the turned-traces sections of DSDLs. The proposed reduction structure, involving different-layer-routing-turned traces, includes the original reduction scheme and improved reduction scheme, which will be introduced in the following section. Both schemes achieve superior CMN reduction performance compared with conventional schemes [14]. Various other schemes are compared in terms of CMN reduction performance. In further analyses of time- and frequency-domain results for the related structures, accuracy was enhanced using a 3-D full-wave simulator Computer Simulation Technology (CST) [15] and HFSS [16], respectively.

This paper is organized as follows. Section II describes the problem of interest. Section III introduces the two proposed CMN reduction schemes. The reductions of CMN achieved using proposed new schemes are investigated in the time and frequency domains. Signal integrity is also compared. Section IV compares CMN reduction performance in different routing layouts. The CMN reductions achieved by the proposed scheme and by previous schemes are compared. For verification purposes, Section V compares simulated and measured results. Finally, Section VI draws conclusions.

TABLE I
GEOMETRIC DIMENSIONS AND MATERIAL PROPERTIES OF PROPOSED STRUCTURES (FIG. 1)

ℓ_1	ℓ	W	S	D	ε_r
120mil	500mil	12mil	16mil	32mil	4.4

H_1	H_2	x	ℓ_{v1}	r_v	loss tangent
4mil	4mil	1.4mil	24mil	4mil	0.02

II. STATEMENT OF THE PROBLEM

The weakly coupled DSDLs are formed by coupled microstrip lines with multiple parallel differential trace pairs. For simplicity, DSDLs with three sections ($N = 3$), shown in Fig. 1, is adopted in this paper. Fig. 1(a) shows conventional DSDLs, which uses same-layer routing in turned-trace sections; Fig. 1(b) shows the proposed DSDL, which is discussed further in Section III. The structural parameters for the presented top and cross-sectional views of the two DSDLs are as follows: trace width (W) of the differential lines, the length (ℓ) of the parallel coupled traces, the length (ℓ_1) of the parallel coupled traces that are connected to a port, the heights (H_1, H_2) of the two substrates, the dielectric constant (ε_r) of the two substrates, the thickness (x) of the signal trace, the distance (D) between the pairs of differential traces, and the spacing (S) between the two differential serpentine traces. As defined in [3], the CMN voltage at the receiving end of DSDLs is

$$V_{c,\text{out}} = \frac{V_{o1} + V_{o2}}{2} \tag{1}$$

where V_{o1} and V_{o2} are the two voltages at the receiving end of the DSDLs.

Consider a conventional DSDLs with $N = 3$ on an FR4 PCB, as shown in Fig. 1(a), with the geometrical parameters that are specified in Table I. The differential impedance (Z_d) of the DSDLs is 100 Ω. The coupling coefficient [17] is approximately 0.074, which is weak. The DSDLs are driven by an ideal differential ramped step source with a magnitude of ±1 V and a rise time (t_r) of 50 ps. Although the dual back-to-back coupled turned traces do not introduce a length difference between the two traces of the DSDLs, as in dual back-to-back coupled bends in differential traces [10], the CMN is not completely compensated for by the dual back-to-back coupled turned traces [9]. The contributions to the CMN originate from the mismatch between the trace lengths of the individual coupled turned traces, the length of the parallel differential coupled traces between two coupled turned traces and the crosstalk between parallel pairs of differential coupled lines [9]. Fig. 2(a) shows the time-domain CMN ($V_{c,\text{out}}$) at the receiving end of the DSDLs, which was simulated using CST. In Fig. 2(b), the simulated magnitude of the differential-to-common mode conversion ($|S_{cd21}|$) [18] for conventional DSDLs with $N = 3$ is compared with that of a straight pair of differential lines of equal length. The simulation, which was performed in HFSS, clearly shows that the conventional
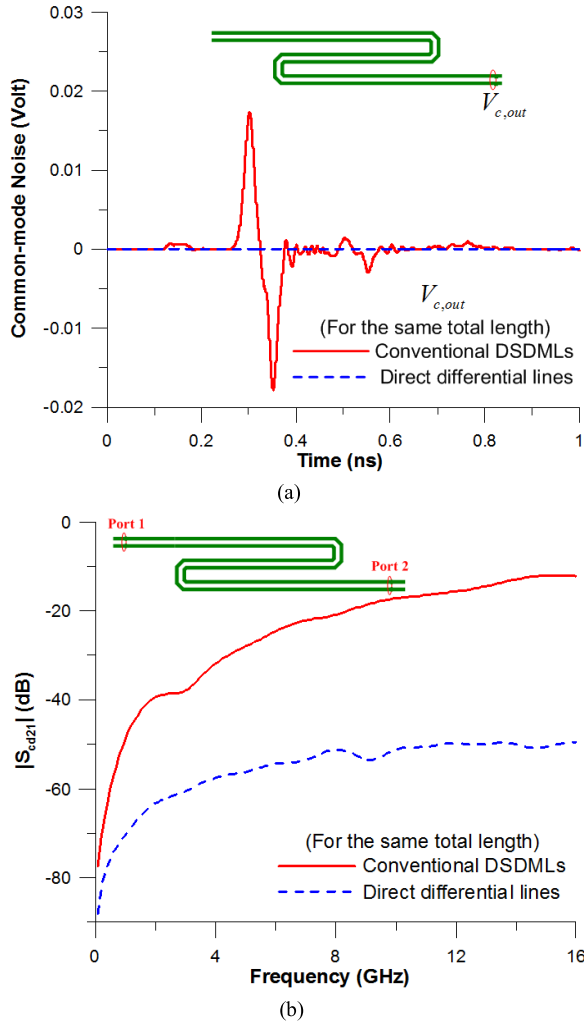
Fig. 2. Comparison of (a) time-domain CMN and (b) differential-to-common mode conversion by a conventional weakly coupled DSDLs ($N = 3$) and by a pair of straight differential lines of equivalent length.

Fig. 3. Top view of original reduction scheme, based on impedance-matched different-layer-routing-turned traces, for weakly coupled DSDLs.

DSDLs induce much greater differential-to-common mode conversion than the straight differential lines. Typically, the operation frequency range of the central processing unit (CPU) in typical electronic devices (e.g., notebook PC, tablet PC, etc.) is 1.9–3.2 GHz. The general rule for measuring electromagnetic radiated emission is for a device that generated frequencies above 1 GH, the upper range of the frequency measurement is the fifth harmonic of the highest frequency. Therefore, as discussed further in Sections II–IV below, this paper sets the upper frequency range of the measured CMN to 16 GHz.

Simulation results in the time domain and the frequency domain reveal that the CMN at the receiving end of the DSDLs is large. Therefore, reducing the CMN by DSDLs is essential for preventing EMI generated by cables or connectors, which can seriously damage electronic systems.

III. PROPOSED CMN REDUCTION SCHEME AND ANALYSIS

A. Proposed Original Reduction Scheme

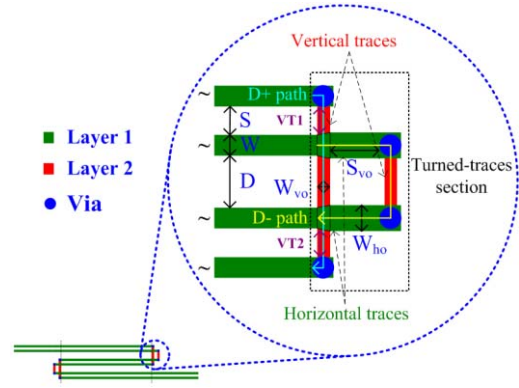Fig. 1(b) shows the proposed CMN reduction techniques for conventional weakly coupled DSDLs. The noise reduction

approach uses different-layer-routing-turned traces instead of the conventional coupled turned traces (same-layer-routing-turned traces) in turned-trace sections of DSDLs. The different layer traces in the turned-trace sections are connected by signal via without via stub. With regard to via stub effect, it is discussed further in the following. The vertical and horizontal traces of the turned-trace sections in layers 2 and 1, respectively, are considered single-end traces. The odd-mode impedance (Z_{odd}) of differential traces in conventional DSDLs is the looking into impedance from the single trace of differential traces with odd-mode signal excitation. Because the differential traces of the conventional DSDLs are symmetrical, Z_{odd} of the differential traces is 50 Ω [half of the differential impedance (100 Ω)]. To obtain a matching impedance, the impedance in the four traces of the turned-trace section is set to 50 Ω, which is equal to the odd-mode impedance of differential traces in the conventional DSDMLs. Fig. 3 shows the proposed CMN reduction scheme (original reduction scheme). The geometrical parameters of the different-layer-routing-turned traces are the trace width (W_{vo}) of the vertical traces (5 mil) and the trace width (W_{ho}) of the horizontal traces (14 mil) in the original reduction scheme. Hence, the D− path includes two taper structures, as shown in Fig. 3. These two taper structures just overlap the D+ path.

The purpose of the different-layer-routing-turned traces is to provide the same delay time for the two paths (D+ path and D− path) in the turned-trace section. In Fig. 3, the D+ path and D− path have two vias and crossing sections and have the same trace length in layer 2. For simplicity and to obtain approximately equal delay times in the two trace paths in the turned-trace section, length S_{vo} was set under the assumption that the delay time of S_{vo} is equivalent to the delay time of trace section VT1. Because S_{vo} approximated 26 mil, application of the proposed noise reduction resulted in almost zero difference between the delay times of the two paths of the turn-traces section which effectively reduced CMN.

Fig. 4 shows the comparison of the time-domain CMN ($V_{c,out}$) and differential-to-common mode conversion ($|S_{cd21}|$) for weakly coupled DSDLs obtained using the conventional scheme, the original reduction scheme, and the improved reduction scheme. Section III-C examines the improved
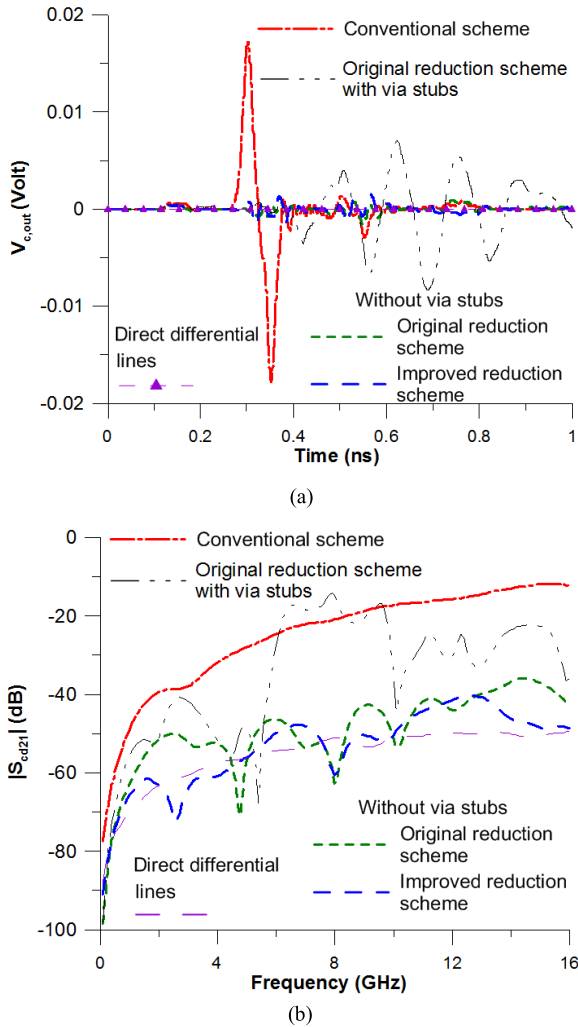
Fig. 4. Comparisons of (a) time-domain CMN ($V_{c,\text{out}}$) and (b) differential-to-common mode conversion ($|S_{\text{cd}21}|$) of weakly coupled DSDLs in conventional scheme, original reduction scheme, original reduction scheme with via stubs, and improved reduction scheme.

reduction scheme. In both time and frequency domains, the original reduction scheme generate significantly less CMN in DSDLs compared with the conventional scheme. In addition, Fig. 5 shows the comparison of the time-domain reflection (TDR) waveform and differential return loss ($|S_{\text{dd}11}|$) in DSDLs implementing using the conventional scheme, the original reduction scheme and the improved reduction scheme. Figs. 4 and 5 show significantly lower CMN in DSDLs with the original reduction scheme in both time and frequency domains. Fig. 5(a) and (b) also show that DSDLs in the original reduction scheme have significantly higher reflection noise in both time and frequency domains, respectively. Fig. 6 further shows that, in DSDLs in the original reduction scheme, the differential insertion loss ($|S_{\text{dd}21}|$) exhibits a ringing phenomenon caused by large reflection noise. Therefore, the following section investigates why reflection noise is high in the original reduction scheme.

B. Effect of via Stubs on Original Reduction Scheme

Although this paper did not consider via stubs in the signal vias of the proposed noise reduction scheme,
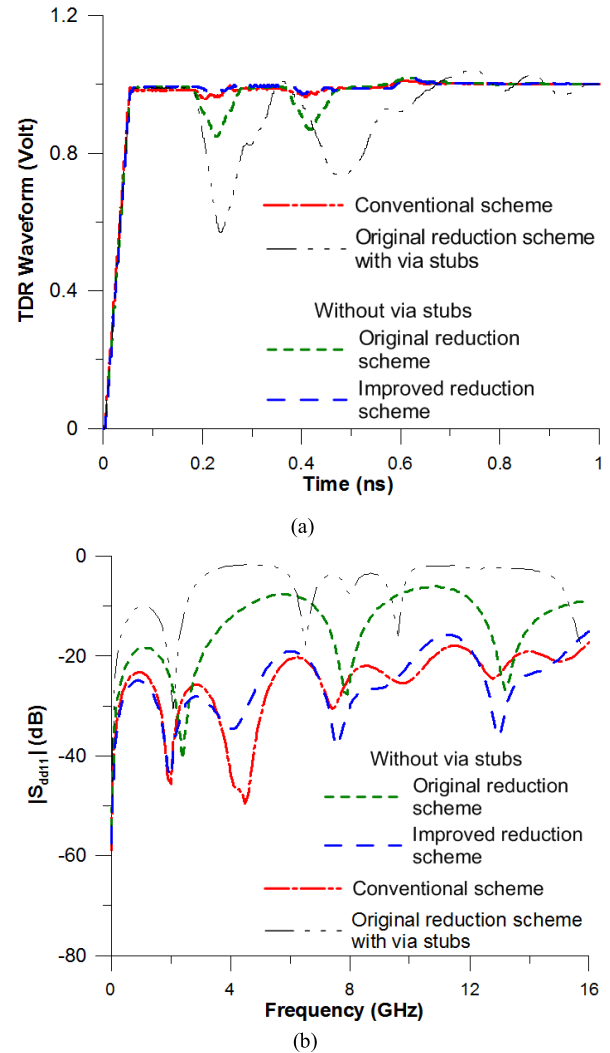

Fig. 5. Comparisons of (a) TDR waveform and (b) differential return loss ($|S_{\text{dd}11}|$) of weakly coupled DSDLs in conventional scheme, original reduction scheme, original reduction scheme with via stubs, and improved reduction scheme.

Fig. 6. Comparison of differential insertion loss ($|S_{\text{dd}21}|$) of weakly coupled DSDLs in conventional scheme, original reduction scheme, original reduction scheme with via stubs, and improved reduction scheme.
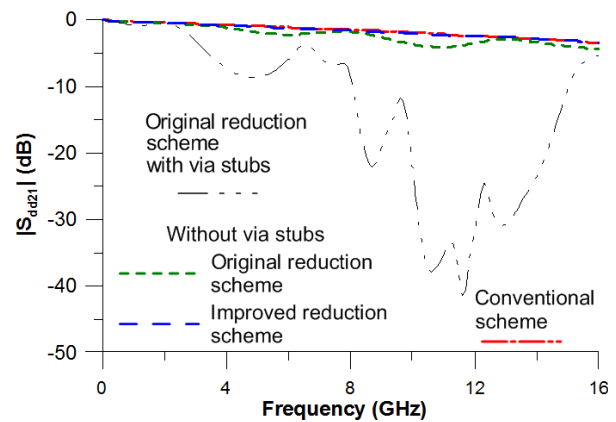
plated through-hole (PTH) vias are widely used to connect the surface metal layer interconnect to the inner metal layer one in a multilayer PCB (including thick PCBs such as those

used in servers) owing to their simple fabrication, simple layout, and low cost. For investigating the impact of via stub effect [19], [20] on the proposed noise reduction scheme, a simple thick PCB with total PCB height 2.6 mm, six metal plane layers, 12 signal layers is considered. The dielectric thickness in the two signal layers on the top and bottom of the PCB was 4 mil. The inner dielectric thickness of all layers is 5 mil. The radius of the antipad is 10 mil. The via stubs have no via pad. The length of each via stub is approximately 97 mil. Each different-layer-routing-turned area has four ground vias [21], [22]. Each ground via is near a signal via. The radius of the ground via is 8 mil.

It is well known that the via stub can excite a resonance frequency [19], [20], as shown in Fig. 6. Figs. 5(b) and 6 show that the large discontinuity in the via stubs significantly degrades both differential return loss ($|S_{dd11}|$) and insertion loss ($|S_{dd21}|$), respectively. Fig. 5(a) shows a severely degraded TDR waveform. The CMN reduction performances are also significantly degraded, not only in time domain $V_{c,out}$ [Fig. 4(a)], but also in frequency domain $|S_{cd21}|$ [Fig. 4(b)]. Therefore, the proposed reduction schemes eliminate the via stub structures. The via stub can be removed using black-drill via technology [23]. The proposed reduction schemes can also apply two via construction technologies: blind via and embedded/buried via [24], which are used in high-density interconnect (HDI) PCBs. However, the fabrication cost of the CMN reduction schemes proposed in this paper is slightly higher than that of schemes that use same-layer-routing-turned traces.

C. Reflection Noise in Original Reduction Scheme

Fig. 5(a) shows that, in the original reduction scheme, the TDR waveform of the weakly coupled DSDLs exhibits two large voltage drops. The TDR waveform of the DSDLs with the conventional scheme is well known to have small reflection noise composed of differential far-end crosstalk noise and bend effect noise [9], as represented by the red line shown in Fig. 5(a). Therefore, the comparison of the TDR waveforms of DSDLs using the conventional scheme with those using the original reduction scheme in Fig. 5(a) shows that the differential far-end crosstalk noise and bend effect noise are not the main contributors to the large voltage drops. In addition, because the vertical and horizontal traces of the turned-trace section of the DSDLs with the original reduction scheme exhibit matched impedance, the mutual capacitances between the perpendicular crossing traces cause large reflection noise.

The trace-crossing mutual capacitance (C_{tt}) can be extracted (at 5 GHz) using the Q3D extractor [25]. The trace-crossing mutual capacitance in the turned-trace section is approximately 0.059 pF. Fig. 7(a) shows the equivalent circuit model of the turned-trace section of DSDLs in the conventional reduction scheme. In both VT1 and VT2, the delay times approximate 3.6 ps, which is much shorter than the rise time of differential ramped step sources. Therefore, the electric length of VT1 and VT2 is too short to have any effect, and the PEC symmetry boundary of odd mode of the differential
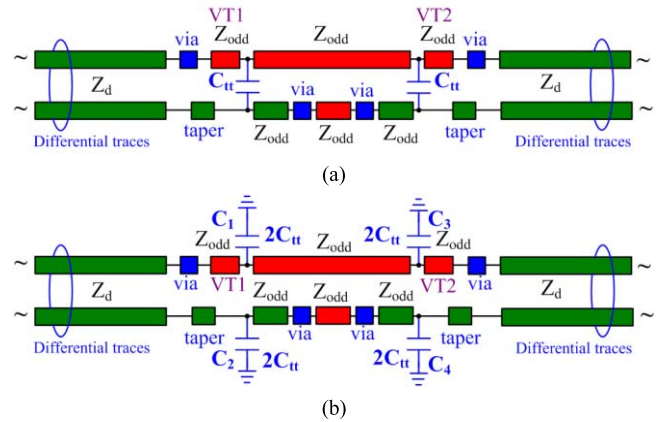

Fig. 7. Equivalent circuit models of turned-trace section of weakly coupled DSDLs in original reduction scheme with (a) shunt connection capacitors connected between two traces and (b) shunt connection capacitors connected between individual trace and ground.
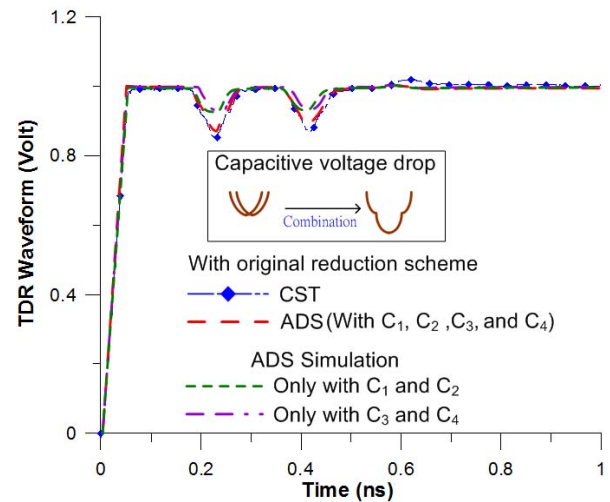

Fig. 8. Comparison of TDR waveforms simulated using CST and ADS for the DSDLs in original reduction scheme.

traces at the left/right end is extended to the middle of C_{tt} [Fig. 7(a)]. The electric length than approximates that of two $2C_{tt}$ [Fig. 7(b)] [26].

To verify the equivalent capacitances shown in Fig. 7(b), Fig. 8 shows the comparison of the TDR waveforms simulated by CST and ADS for DSDLs in the original reduction scheme. The ADS is used to simulate the equivalent circuit model [Fig. 7(b)] of the turned-trace section of the DSDLs. Clearly, as shown in Fig. 8, the TDR waveforms that are simulated using ADS are very close to those obtained using CST. Fig. 8 shows the comparison of the ADS simulations of TDR waveforms for the DSDLs in the original reduction scheme between those with only C_1 and C_2 and those with only C_3 and C_4. Because the delay time ($\sim$5.57 ps) between the two capacitors is shorter than the rise time, the two capacitive voltage drops almost overlap each other. Therefore, the voltage drop comprising the two capacitive voltage drops in the TDR waveform is larger than the capacitive voltage drop shown in Fig. 8. Moreover, the combined voltage drop is
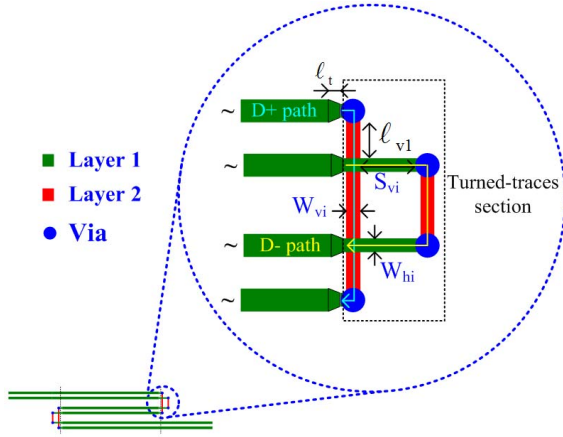
Fig. 9. Top view of the improved reduction scheme (narrow different-layer-routing-turned traces) for weakly coupled DSDLs.

almost double the individual capacitive voltage drop because of the very short delay ($\sim$5.57 ps) between the two capacitors (inset, Fig. 8). As in Fig. 5(a), the differential return loss ($|S_{dd11}|$) in the frequency domain shown in Fig. 5(b) is much larger in DSDLs in the original reduction scheme compared with those in other schemes.

D. Proposed Improved Reduction Scheme

Fig. 9 shows that the improved reduction scheme proposed in this paper mitigates large reflection noise in weakly coupled DSDLs by using narrow different-layer-routing-turned traces (narrow-width traces). The trace widths of the vertical (W_{vi}) and horizontal (W_{hi}) traces of the turned-trace section are both set to 4 mil. The impedances of the narrow vertical and horizontal traces are approximately 53.76 Ω (Z_1) and 85.26 Ω (Z_2), respectively. Four tapers are individually connected from differential traces (odd-mode impedance, Z_{odd}) to narrow-width vertical and horizontal traces. Each of the four tapers has a length (ℓ_t) of 4 mil. For simplicity, the delay times of the two trace paths in the turned-trace section S_{vh} are set to approximately 40 mil. The narrow vertical and horizontal traces of the turned-trace section can cause a small traces-crossing mutual capacitance (C'_{tt}), which can be extracted (at 5 GHz) using the Q3D extractor. The trace-crossing mutual capacitance achieved by the improved reduction scheme approximates 0.3 pF. For the same reason, the traces-crossing mutual capacitance (C'_{tt}) is equivalent to double the capacitance ($2C'_{tt}$) of the connection from each trace to ground. Therefore, the capacitance must be changed from 0.03 pF (C'_{tt}) to 0.06 pF ($2C'_{tt}$). Fig. 10(a) shows the equivalent circuit model of the turned-trace section obtained using the improved reduction scheme.

Connecting narrow-width vertical and horizontal traces between two pairs of differential traces (odd-mode impedance, 50 Ω) produces a positive voltage bulge [1] that compensates for the capacitive voltage drop. Therefore, the following section examines compensation for the voltage drop in the TDR waveform.

Table II shows the geometric dimensions and electric properties of the DSDLs with improved reduction scheme
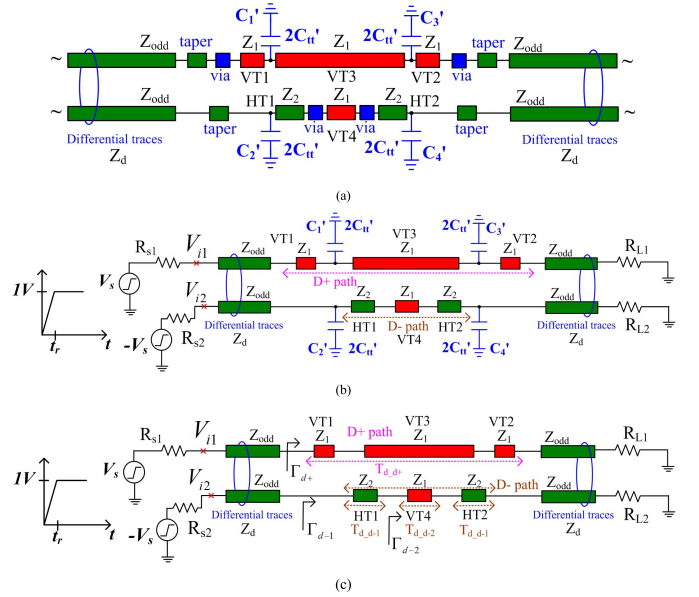

Fig. 10. (a) Equivalent circuit model of turned-trace section obtained using improved reduction scheme. Two simple equivalent circuit models from (a), (b) without taper and via models, and (c) without taper, via, and capacitor models.

TABLE II
GEOMETRIC DIMENSIONS AND ELECTRIC PROPERTIES
OF DSDLs IN IMPROVED REDUCTION SCHEME

	VT1	VT2	VT3	VT4	HT1	HT2
Length(mil)	26	26	44	44	29.5	29.5
Delay time(ps)	4.43	4.43	7.5	7.5	4.22	4.22

Z_{odd}	Z_1	Z_2		Γ_{d+}	Γ_{d-1}	Γ_{d-2}
50Ω	53.76Ω	85.26Ω		0.0362	0.2607	0.0362

$v_{r,c\_D+}(t)$	$v_{r,c\_D-}(t)$	$v_{r,h\_D+}(t)$	$v_{r,h\_D-1}(t)$	$v_{r,h\_D-2}(t)$
-0.03V	0.03V	0.0118V	-0.044V	-0.0054V

(narrow different-layer-routing-turned traces) Fig. 10(b) shows a simple equivalent circuit model shown in Fig. 10(a), without taper and via models because the tapers and vias are so small. For illustration purposes, Fig. 10(c) is a simple equivalent circuit model shown in Fig. 10(b) without taper- via and capacitor models. An ideal differential ramped step source with a magnitude of ± 1 V and a rise time (t_r) of 50 ps drives the equivalent circuit models [Fig. 10(b) and (c)] of the turned-trace section. Both the source resistances (R_{s1}, R_{s2}) and load resistances (R_{L1}, R_{L2}) are 50 Ω.

As shown in Fig. 10(b), the capacitors in the D+ and D$-$ paths can both produce capacitive reflection noise in the TDR waveforms of those two paths. Because the capacitor has a low capacitance, the magnitude of capacitive reflection noise ($v_{r,c}(t)$) associated with four capacitors can be estimated as [27]

$$v_{r,c}(t) = -\frac{Z_0 C}{2t_r}V_i \qquad (2)$$

where V_i is the initial voltages V_{i1} and V_{i2} on the two left ends of the differential traces and Z_0 is the line impedance

of the differential traces. Therefore, Z_0 is the odd-mode impedance, Z_{odd}. Furthermore, because the voltage width of the capacitive reflection noise ($v_{r,c}(t)$) approximates t_r (50 ps) [27] and the delay between the two capacitors is small ($\sim$7.14 ps), the two capacitive reflection noises can still be combined. Because the maximum voltage amplitude of the combined capacitive reflection noise is almost double that of the individual capacitive reflection noise, the maximum voltage amplitude of the combined capacitive reflection noise in the TDR waveforms for the D+ and D$-$ paths is approximately

$$v_{r,c\_D+}(t) = -Z_{\text{odd}}2C'_{\text{tt}}V_{i1}/t_r$$

and

$$v_{r,c\_D-}(t) = -Z_{\text{odd}}2C'_{\text{tt}}V_{i2}/t_r$$

respectively.

Fig. 10(c) shows that the positive ramped step source in the D+ path propagates from the leftmost differential trace to the rightmost differential trace through traces VT1, VT3, and VT2. The impedance of the VT1, VT3, and VT2 traces is higher than the line impedance (Z_{odd}) of the differential traces. This generates a positive reflection noise estimated as [27]

$$v_{r,h}(t) = \frac{V_i\Gamma}{t_r}2T_d, \quad 2T_d < t_r \tag{3}$$

where Γ is the reflection coefficient and T_d is the delay time of the narrow-width trace between the two lower impedance traces. Accordingly, the TDR waveform for the D+ path has a positive reflection noise, $v_{r,h\_D+}(t) = V_{i1}\Gamma_{d+}2T_{d\_d+}/t_r$. For the same reason, the TDR waveform for the D$-$ path has two positive reflection noises, $v_{r,h\_D-1}(t) = V_{i2}\Gamma_{d-1}4T_{d\_d-1}/t_r$ and $v_{r,h\_D-2}(t) = V_{i2}\Gamma_{d-2}2T_{d\_d-2}/t_r$.

Accordingly, because the times of the generation of all positive and negative reflection noise are very similar, the maximum voltage amplitude of the combined reflection noise ($v_{r,\text{TDR}}(t)$) in the TDR waveform of the differential signals ($V_{i1} - V_{i2}$) can be simplified as

$$\begin{aligned} v_{r,\text{TDR}}(t) \cong\ & v_{r,c\_D+}(t) - v_{r,c\_D-}(t) + v_{r,h\_D+}(t) \\ & - v_{r,hD-1}(t) - v_{r,h\_D-2}(t). \end{aligned} \tag{4}$$

Notably, the impedance must be considered if the via has a long length. However, the length and time delay of signal via approximate 2.6 mil and 0.45 ps, respectively. As the electrical length of the via is sufficiently short, the via effect is not considered. The related parameters and Table II show that the total combined reflection noise ($v_{r,\text{TDR}}(t)$) approaches zero. Therefore, the reflection noise in the TDR waveform shown in Fig. 5(a) and the differential return loss ($|S_{\text{dd11}}|$) shown in Fig. 5(b) can be reduced. Although the differential TDR waveform includes slight differential far-end noise [2] and residual reflection noise [Fig. 5(b)], the reflection noise is indeed smaller in weakly coupled DSDLs in the improved reduction scheme compared with those in the original reduction scheme. Notably, Fig. 5 shows that, because the reflection noise obtained by the conventional scheme slightly differs from that obtained by the improved

reduction scheme, reflection noise is acceptable in DSDLs in the improved reduction scheme. In DSDLs in the improved reduction scheme, resonance does not affect $|S_{\text{dd21}}|$ (Fig. 6). The differential return loss ($|S_{\text{dd21}}|$) of the DSDLs in the proposed scheme is comparable with that of the DSDLs in the conventional scheme. Additionally, the improved reduction scheme for the DSDLs improves both differential return loss and differential insertion loss.

Clearly, from Fig. 4(a), the original reduction scheme and the improved reduction scheme reduce the peak-to-peak amplitude of the time-domain CMN by approximately 93.3% and 91%, respectively, compared with the conventional scheme. Fig. 4(b) further shows that, compared with conventional DSDLs, the original reduction scheme reduces the differential-to-common mode conversion ($|S_{\text{cd21}}|$) by a large average of 20 dB in the 4–16 GHz range. The improved reduction scheme obtains a similar reduction in the 0.8–16 GHz range. However, both reduction schemes are effective over a very wide frequency range. Although, both the original reduction scheme and the improved reduction scheme achieved large reductions, CMN reduction performance is better in the improved reduction scheme.

The preceding simulation results indicate that, because the reflection noise for DSDLs in the original reduction scheme is larger than that of DSDLs in the improved reduction scheme, the better proposed CMN reduction scheme for the DSDLs is the improved reduction scheme. Therefore, the following analyses focus on the DSDLs with improved reduction scheme.

E. Transient Transmission Common-Mode Voltages in DSDLs

According to [9], the main contributors to CMN are the length mismatch in the coupled turned traces, the length of the parallel differential coupled traces, and the crosstalk between the parallel pairs of differential coupled lines. Therefore, this paper investigated the main contributors to CMN in DSDLs in the improved reduction scheme. Fig. 11(a) and (b) shows the comparison of the transient transmission CMNs between the DSDLs in the conventional scheme and in the improved reduction scheme, respectively. Neither of the two CMN waveforms ($V_{c,b}$ and $V'_{c,b}$) showed high CMN in DSDLs in the improved reduction scheme. Because the main purpose of proposed different-layer-routing-turned traces is to equalize the delay times associated with the two trace paths in the turned-trace section, the length mismatch of the two traces in the turned-trace section does not contribute to CMN in the DSDLs with the improved reduction scheme. Therefore, the effect of length mismatch of the turned traces in DSDLs with the improved reduction scheme is almost negligible.

In conventional DSDLs [Fig. 11(a)], the long parallel differential coupled traces of DSDLs causes residual CMN $V_{c,d}$, because long traces result in the a difference between the odd-mode and even-mode propagation velocities of the differential lines. Therefore, compensation for the differential signals is not complete when they propagate through the back-to-back dual coupled turned traces of conventional DSDLs [9].
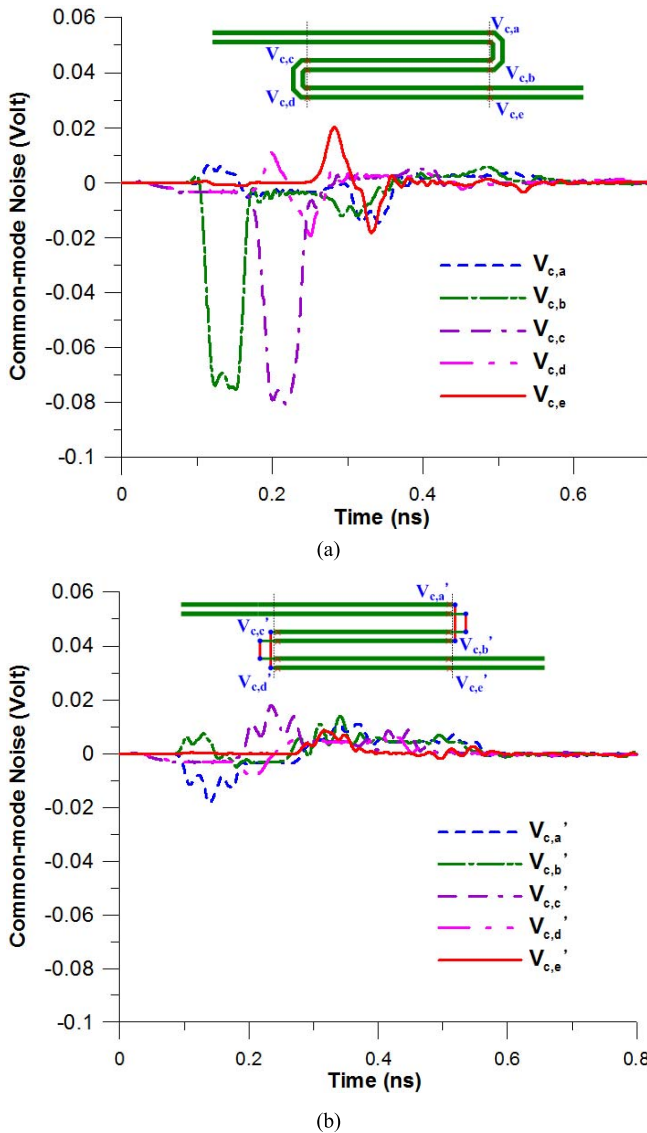
Fig. 11. Comparisons of transient transmission CMN in DSDLs in (a) conventional scheme and (b) improved reduction scheme.

Fig. 12. Comparisons of simulated (a) CMN ($V_{c,\text{out}}$) and (b) differential-to-common mode conversion ($|S_{\text{cd}21}|$) of DSDLs in the conventional scheme and in the improved reduction scheme for different lengths (ℓ).

However, in DSDLs in the improved reduction scheme, the effect of the length mismatch in the turned-trace section on CMN $V'_{c,b}$ is negligible. Therefore, the length of the parallel differential coupled traces does not contribute to CMN generation in DSDLs with the improved reduction scheme.

A comparison of the CMNs shown in Fig. 11(a) and (b) reveals that crosstalk noise between parallel pairs of differential coupled lines exists in DSDLs with the improved reduction scheme. The flat and wide voltage waveform sections with small magnitudes of $V'_{c,a}$, $V'_{c,b}$, $V'_{c,c}$, and $V'_{c,d}$ all belong to the near-end CMN. Additionally, near-end CMN cancellation caused symmetrical waveforms eliminates near-end CMN from $V_{c,e}$ and $V'_{c,e}$ in DSDLs in the conventional scheme and in the improved reduction scheme, respectively [9].

IV. FURTHER ANALYSIS AND DISCUSSION

A. Effect of Parallel Length

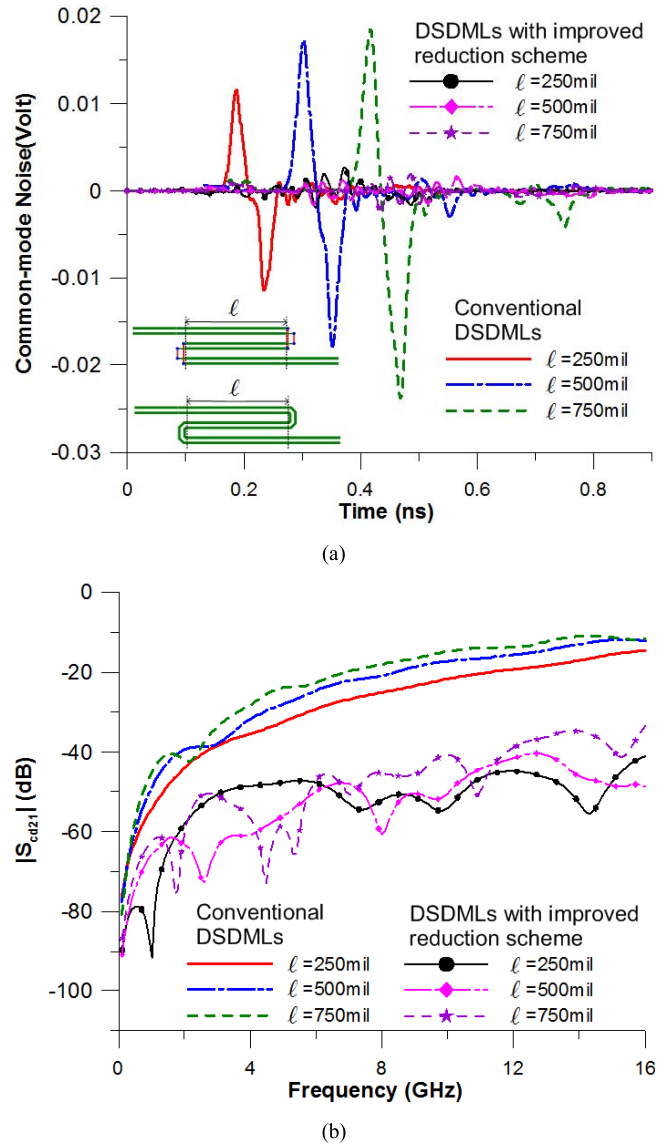Fig. 12 shows the comparison of the simulated time-domain CMN ($V_{c,\text{out}}$) and differential-to-common mode conversion ($|S_{\text{cd}21}|$) of DSDLs in the conventional scheme and in the improved reduction scheme for different line lengths (ℓ). According to [9], when the parallel differential coupled traces of conventional DSDLs are long, the peak-to-peak magnitude of CMN ($V_{c,\text{out}}$) is large. However, Fig. 12 shows that, in DSDLs in the improved reduction scheme, both the time-domain CMN ($V_{c,\text{out}}$) and the frequency-domain differential-to-common mode conversion ($|S_{\text{cd}21}|$) are very small and do not substantially differ at lengths from 250 to 750 mil. Restated, because the difference between the delays of the two traces of the turned-trace sections of DSDLs in the improved reduction scheme approaches zero, the turned-trace sections of middle differential traces (second pair of parallel differential traces) induce very little CMN and the effect of the length of the parallel differential coupled traces contributes only very slightly to CMN ($V_{c,\text{out}}$).
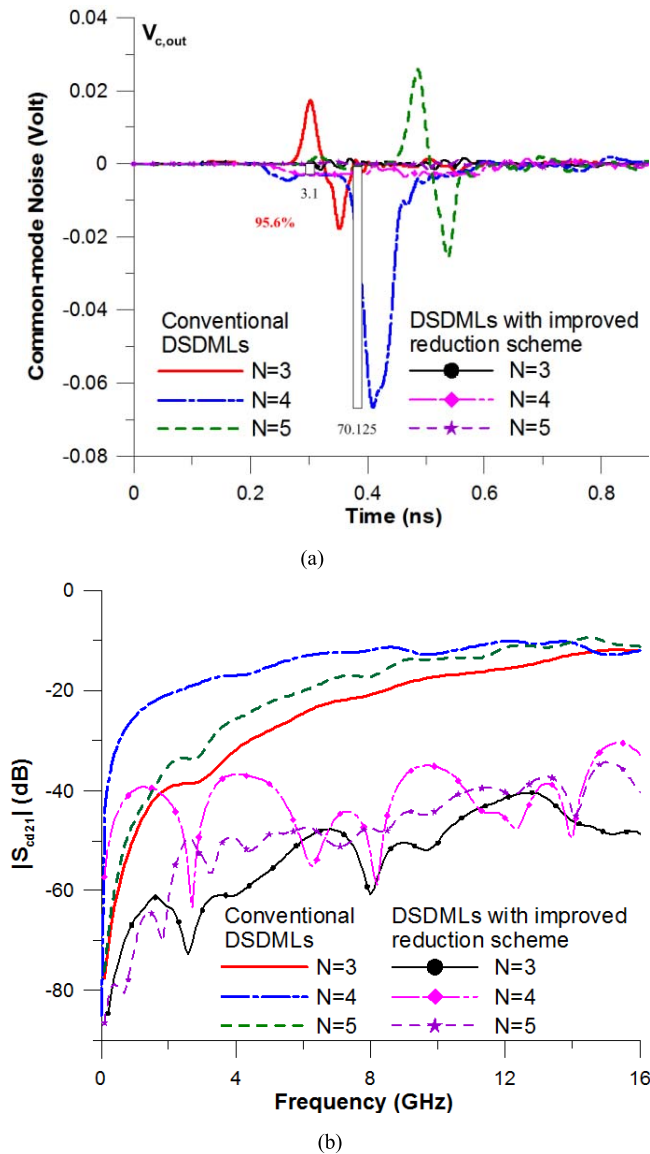
(a)

(b)

Fig. 13. Comparisons of simulated (a) CMN ($V_{c,\text{out}}$) and (b) differential-to-common mode conversion ($|S_{\text{cd}21}|$) of DSDLs with conventional scheme and improved reduction scheme for different numbers of sections (N).

B. Parallel Section Number Effect

Fig. 13 shows the comparison of simulated CMN ($V_{c,\text{out}}$) and differential-to-common mode conversion ($|S_{\text{cd}21}|$) between DSDLs with the conventional scheme and those with the improved reduction scheme for numbers of sections ($N = 3, 4, 5$). Fig. 13(a) and (b) shows that, in the conventional scheme, DSDLs with an even number of sections case have higher CMN compared with those with an odd number of sections owing to the length mismatch in the coupled turned traces. However, DSDLs with the improved reduction scheme with either an odd or an even number of sections exhibit significantly lower CMN in both the time domain [Fig. 13(a)] an in the frequency domain [Fig. 13(b)]. In the improved reduction scheme, the asymmetry results in a higher CMN in DSDLs with an even number of sections compared with those with an odd number of sections, especially at low frequencies.

Because the asymmetry prevents the near-end CMNs from cancelling each other, Fig. 13(a) shows that the CMN has a flat and wide waveform and a low voltage [9]. Therefore, the distance (D) between two parallel differential traces of the DSDLs must be sufficiently large to avoid generating large uncanceled near-end CMN.

Notably, spatial constraints in industrial PCBs may require a different routing scheme for DSDLs with $N = 4$. The improved reduction scheme is recommended for the DSDLs (with $N = 4$) because it greatly reduces CMN. The improved reduction scheme reduces the peak-to-peak amplitude of time-domain CMN by about 95.6%, from that of the conventional DSDLs ($N = 4$), as shown in Fig. 13(a). The average reduction of differential-to-common mode conversion ($|S_{\text{cd}21}|$) exceeds 20 dB in the range of about 2–16 GHz, as shown in Fig. 13(b).

C. Effect of Asymmetry

Spatial constraints on industrial PCBs for DSDLs usually require a routing scheme with various section lengths (L_2). Fig. 14(a) and (b) shows the comparison of the conventional scheme and improved reduction scheme, respectively, in terms of CMN ($V_{c,\text{out}}$) and differential-to-common mode conversion ($|S_{\text{cd}21}|$) in the DSDLs ($N = 5$) with various lengths L_2 of the parallel differential pairs. The time-domain results shown in Fig. 14(a) clearly indicate that the peak-to-peak voltage in the DSDLs can be significantly reduced using the improved reduction scheme. However, a smaller section length (L_2) (asymmetrical structure) corresponds to a wider near-end and lower peak-to-peak amplitude of CMN. The near-end part of CMN is wider because the near-end CMNs cannot completely cancel each other in the asymmetrical structure of the DSDLs [9]. According to the preceding analysis (Section IV-A), the low peak-to-peak amplitude of CMN results from the short length of the parallel differential pairs.

Fig. 14(b) clearly shows that, at high frequencies, CMN is significantly lower in the improved reduction scheme than in the conventional scheme. The figure also clearly reveals that the longest sections have CMN reductions over the widest range of (high) frequencies. Therefore, as the asymmetry in the structure increases (with a smaller section length L_2), CMN reduction occurs over a narrower frequency range. Additionally, from Fig. 14(b), the efficiency of CMN reduction is poor for small L_2 (asymmetrical structure), especially at low frequencies.

D. Comparison of CMN Achieved Using Different Reduction Schemes

In a previous CMN reduction scheme developed for weakly coupled DSDLs [14], strongly coupled turned traces were used instead of weakly coupled turned traces (conventional scheme). Guard traces were also added. This section compares the CMN reductions achieved using different reduction schemes. Fig. 15 shows the comparison of the simulated CMN ($V_{c,\text{out}}$) and differential-to-common mode conversion ($|S_{\text{cd}21}|$) of DSDLs with different reduction schemes. Fig. 15 shows the comparison of four cases: conventional DSDLs, DSDLs with
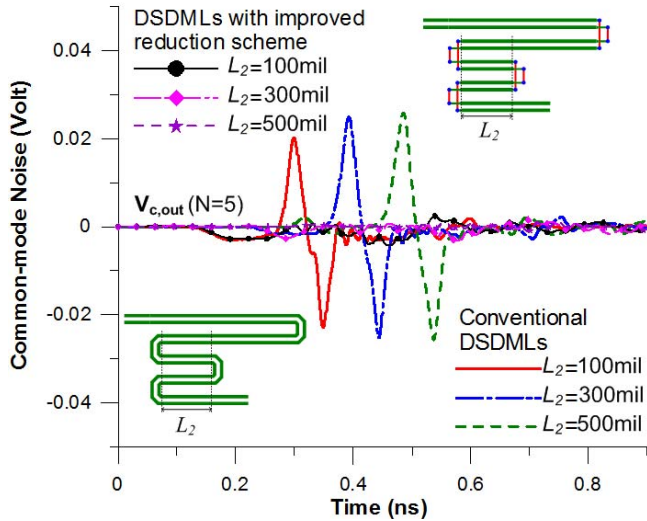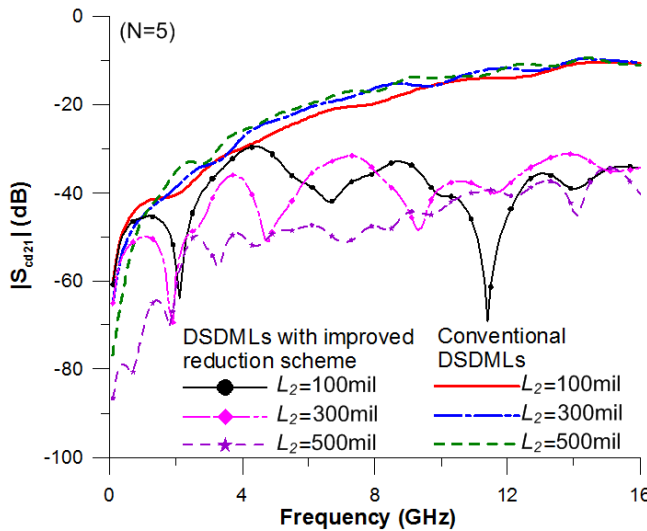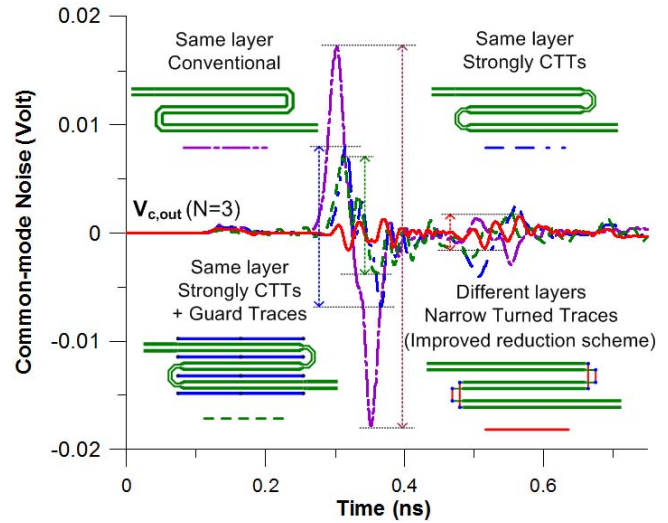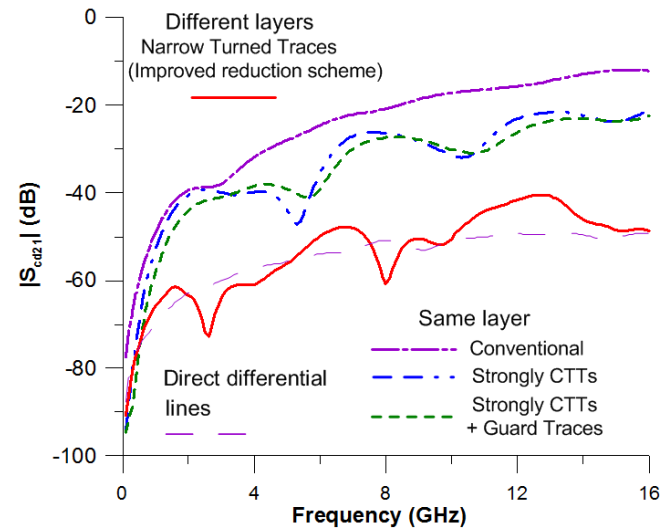
Fig. 14. Comparisons of simulated (a) CMN ($V_{c,\text{out}}$) and (b) differential-to-common mode conversion ($|S_{\text{cd21}}|$) in DSDLs in the conventional scheme and in the improved reduction scheme for different lengths (L_2).

Fig. 15. Comparisons of simulated (a) CMN ($V_{c,\text{out}}$) and (b) differential-to-common mode conversion ($|S_{\text{cd21}}|$) for DSDLs in different reduction schemes.

strongly coupled turned traces, DSDLs with strongly coupled turned traces and guard traces, and DSDLs with the improved reduction scheme (narrow turned traces). Same-layer-routing-coupled turned traces are used in three of the schemes: the conventional DSDLs, the DSDLs with strongly coupled turned traces, and the DSDLs with strongly coupled turned traces and guard traces. The DSDLs with the improved reduction scheme (narrow turned traces) involve different-layer-routing-turned traces.

Fig. 15(a) clearly shows that the improved reduction scheme reduces peak-to-peak CMN amplitude in strongly coupled turned traces, in strongly coupled turned traces, and in guard traces by approximately 58.5%, 68.6%, and 91%, respectively, compared with the conventional DSDLs. The improved reduction scheme provides the largest reduction of the peak-to-peak amplitude of CMN for the DSDLs. Fig. 15(b) further

shows that the improved reduction scheme provides the largest decrease in the differential-to-common mode conversion ($|S_{\text{cd21}}|$) for the DSDLs, that is, a decrease of at least 20 dB in the range 0.8–16 GHz. Fig. 15(b) shows that CMN reduction is achieved over a very wide frequency, that is, throughout almost the entire band (dc ∼16 GHz). According to a previous analysis, the difference between the delay times of the two traces in the turned-trace section with the improved reduction scheme approaches zero, and the CMN reduction is significant. However, in the case that involves strongly coupled turned traces, the reduction scheme involves the same-layer routing, so the difference between delay times cannot approach zero and the CMN reduction cannot be very large.

V. MEASUREMENT VALIDATION

The CMN reduction achieved by the proposed structure with different-layer-routing scheme was evaluated by simulations

TABLE III
GEOMETRIC DIMENSIONS AND MATERIAL
PARAMETERS OF MEASURED BOARDS

ℓ_1	ℓ	ℓ_t	ℓ_{vl}	W	W_{vi}	D
20mm	40mm	0.6mm	3mm	1.8mm	0.6mm	3mm

W_{vo}	W_{hi}	W_{ho}	S	S_{vo}	S_{vi}
0.9mm	0.6mm	2.25mm	1.8mm	2.5mm	2.5mm

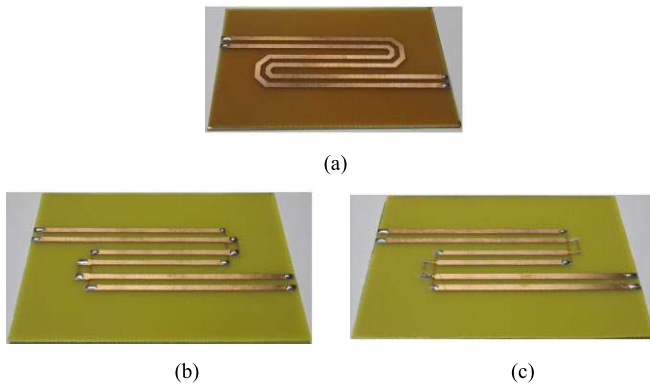| H_1	H_2	r_v	loss tangent	x	ε_r
0.6mm	0.6mm	0.25mm	0.02	0.035mm	4.4

Fig. 16. Measured boards for (a) conventional DSDLs, (b) DSDLs with original reduction scheme, and (c) DSDLs with improved reduction scheme.

and measurements for weakly coupled DSDLs in both the frequency and time domains. To clarify the comparison, measurements were obtained for three boards: 1) the conventional DSDLs; 2) the DSDLs with the original reduction scheme; and 3) the DSDLs with the improved reduction scheme. The laboratory implementation was simplified by using boards fabricated at millimeter scale. Table III presents geometric dimensions and material parameters of the boards. Fig. 16 shows photographs of the manufactured and measured boards. The simulations for time and frequency domains of the related measured structures were performed using 3-D full-wave simulator CST and HFSS, respectively.

The measurements obtained with a TEK/CSA8000 time-domain reflectometer and an Agilent/E5071B frequency-domain network analyzer were compared with the CST and HFSS simulation results. The launching voltage source is drawn from the reflectometer in the CST simulation.

Fig. 17 shows the simulated and measured differential TDR waveform, time-domain CMN, differential insertion loss ($|S_{d2d1}|$) and differential-to-common mode conversion ($|S_{c2d1}|$) for the DSDLs with the conventional scheme, the original reduction scheme, and the improved reduction scheme. The simulated results agree closely with the measurements. The deviations between the simulations and measurements can be due to the neglecting of the semirigid coaxial cable in the simulations, to small variations of the material properties of the substrate, to small variations in the manufacturing process,
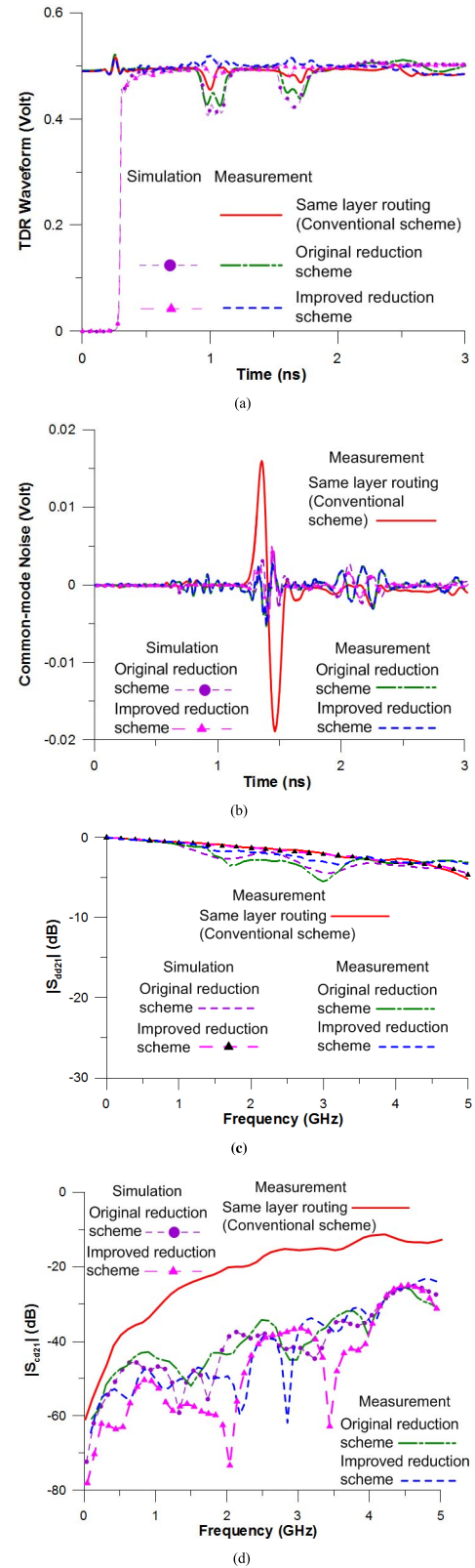

Fig. 17. Simulated and measured (a) differential TDR waveform, (b) CMN, (c) frequency-domain differential insertion loss ($|S_{dd21}|$), and (d) differential-to-common mode conversions ($|S_{cd21}|$) for DSDLs in conventional scheme, original reduction scheme, and improved reduction scheme.

to the definition of the port(s), and other factors. Despite the slight discrepancies, both the simulations and actual measurements confirmed the feasibility and usefulness of the

proposed CMN reduction schemes for weakly coupled DSDLs. Compared with the original reduction scheme, the improved scheme also obtained superior TDR waveforms, differential insertion loss ($|S_{\text{d2d1}}|$) and differential-to-common mode conversion ($|S_{\text{c2d1}}|$). That is, the comparisons again validated the superior performance of the proposed CMN reduction scheme for DSDLs.

Notably, for practical reasons concerning our laboratory, the geometrical dimensions that are used in this section differ from those used in Sections III and IV. However, the comparisons described in this section demonstrated the effectiveness of the proposed noise reduction schemes according to both simulated and actual results. That is, the comparison demonstrated that the simulation and analytical results for the structures proposed in Sections III and IV provide effective performance indices.

VI. CONCLUSION

To reduce CMN in conventional weakly coupled DSDLs in microstrip line structures, this paper proposes a new CMN reduction structure for using different-layer-routing-turned traces. Different-layer-routing-turned traces are substituted for same-layer-routing-coupled turned traces (conventional scheme) to achieve a delay time difference between the two traces of the turn-traces section to approach zero to reduce the CMN. Improved reduction schemes for using different-layer-routing-turned traces are proposed. All traces are impedance matched in the original scheme whereas all traces are narrow width in the improved scheme. In the time domain, these schemes achieve peak-to-peak amplitude reductions exceeding 90%. The DSDLs with the improved reduction scheme achieve average reductions of at least 20 dB in differential-to-common mode conversion ($|S_{\text{cd21}}|$) in the 0.8–16 GHz range.

Signal integrity performance, which is a function of differential return loss (reflection noise) and differential insertion loss is also better in the improved reduction scheme than in the original reduction scheme. Therefore, the improved reduction scheme is superior in terms of CMN reduction and signal integrity. Although the improved reduction scheme significantly reduces peak-to-peak amplitude of CMN in the time domain in asymmetric DSDLs, the improved scheme still produces small-amplitude near-end common-mode crosstalk. Furthermore, in the frequency domain, asymmetry caused by the short section length limits the potential CMN reduction at low frequencies. Therefore, symmetry is still an important requirement for CMN reduction in DSDLs in the improved reduction scheme. The improved reduction scheme achieves a larger CMN reduction in DSDLs compared with previous CMN reduction schemes (strongly coupled turned traces and guard traces).

Finally, the good agreement between the simulated and measured results demonstrates the effectiveness of the proposed CMN reduction schemes for weakly coupled DSDLs.
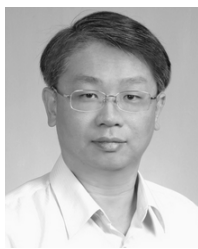
ACKNOWLEDGMENT

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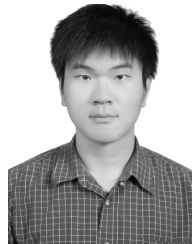
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