A Serpentine Guard Trace to Reduce the Far-End Crosstalk Voltage and the Crosstalk Induced Timing Jitter of Parallel Microstrip Lines

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***Abstract*—A serpentine guard trace is proposed to reduce the peak far-end crosstalk voltage and the crosstalk induced timing jitter of parallel microstrip lines on printed circuit boards. The vertical sections of the serpentine guard increase the mutual capacitance without much changing the mutual inductance between the aggressor and victim lines. This reduces the difference between the capacitive and inductive couplings and hence the far-end crosstalk. Comparison with the no guard, the conventional guard, and the via-stitch guard shows that the serpentine guard gives the smallest values in both the peak far-end crosstalk voltage and the timing jitter. The time domain reflectometer (TDR) measurement shows that the peak far-end crosstalk voltage of serpentine guard is reduced to 44% of that of no guard. The eye diagram measurement of pseudo random binary sequence (PRBS) data shows that the timing jitter is also reduced to 40% of that of no guard.**

***Index Terms*—Crosstalk, microstrip line, serpentine guard trace, timing jitter.**

I. Introduction

MICROSTRIP lines are widely used for chip-to-chip interconnect on printed circuit board (PCB) mainly for low cost. In the two parallel microstrip lines, a large impulse-type far-end crosstalk voltage appears at one side of the victim line, when a digital signal is applied at the opposite side of the aggressor line. This far-end crosstalk voltage reduces the eye opening and eventually decreases the maximum data rate that can be transmitted through the microstrip lines. This far-end crosstalk voltage is induced by the difference between the capacitive and inductive coupling ratios of two microstrip lines [1]. The capacitive coupling ratio (C_m/C_T) of the two microstrip lines is slightly smaller than the inductive coupling ratio (L_m/L_S), because the dielectric constant of surrounding air is smaller than that of the PCB dielectric material. C_m, C_T, L_m, and L_S represent the mutual capacitance, the sum of self capacitance and mutual capacitance, the mutual inductance and the self inductance per unit length, respectively. Although there is no far-end crosstalk induced in the strip lines, the strip lines are more costly than the microstrip lines because the strip lines need more PCB layers. To reduce the far-end crosstalk in the microstrip lines, the extra dielectric material can be deposited over the microstrip lines [2]. However, this extra material deposition is a cost-adding process. To reduce the far-end crosstalk, the spacing between the two signal lines can be widened or a guard line can be placed between the two signal lines. However, the spacing widening increases the PCB area and the guard line turned out to be not effective [3]. Also, the via-stitch guard was proposed, where ground vias were placed uniformly on the guard line [4], [5]. This via-stitch guard imposes the restriction on the PCB backside routing due to via holes. In this work, a guard trace with the serpentine form was proposed to reduce effectively both the far-end crosstalk voltage and the even–odd mode velocity mismatch of microstrip lines on PCB. The earlier version of this work was published in [6].

Manuscript received September 27, 2007; revised February 1, 2008. This work was supported in part by the BK21 Program of Korea and in part by IDEC. This work was recommended for publication by Associate Editor A. Maffucci upon evaluation of the reviewers comments.

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Digital Object Identifier 10.1109/TADVP.2008.924226

II. Crosstalk Between Coupled Microstrip Lines

A. Far-End Crosstalk Voltage

An isolated transmission line can be modeled by the uniformly distributed self capacitance (C_S) and self inductance (L_S). Fig. 1(a) shows a pair of coupled transmission lines. This pair of coupled transmission lines can be modeled by the uniformly distributed mutual capacitance (C_m) and mutual inductance (L_m) in addition to the self capacitance (C_S) and the self inductance (L_S), as shown in Fig. 1(b). In the coupled transmission lines shown in Fig. 1(a), the active transmission line to which the signal is applied is called the aggressor line and the passive transmission line to which no signal is applied is called the victim line. The far-end crosstalk voltage V_{fext} is the voltage induced at the receiving end of the victim line. The far-end crosstalk voltage waveform in the lossless case can be represented by (1) [1]

$$V_{fext}(t) = \frac{1}{2}\left(\frac{C_m}{C_T} - \frac{L_m}{L_S}\right) \cdot TD \cdot \frac{dV_a(t-TD)}{dt} \quad (1)$$

where TD is the propagation time through the transmission line, $V_a(t)$ is the applied voltage at the aggressor line. Because the inductive coupling (L_m/L_S) is larger than the capacitive coupling (C_m/C_T) in the microstrip line with one side exposed to air, $V_{fext}(t)$ has the negative pulse at the rising edge of $V_a(t)$.

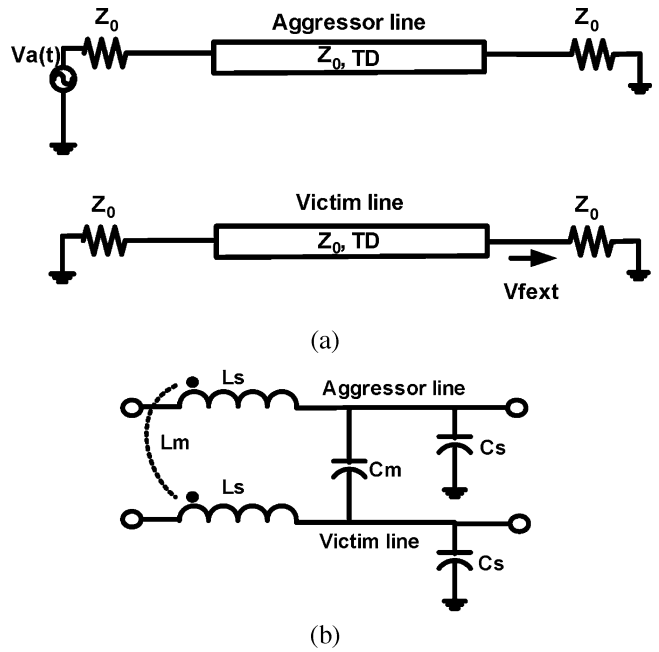


Fig. 1. (a) Coupled transmission line. (b) Model of a section.

B. Empirical Equations of Peak Far-End Crosstalk Voltage for Lossy Microstrip Lines

In the lossy transmission lines, the signal slope (dV_a/dt) is decreasing with distance significantly as the signal propagates along the transmission line. This is caused by the dielectric loss and skin effect. Thus, the far-end crosstalk voltage equation (1) must be modified to

$$V_{f\text{ext}}(t) = \frac{1}{2}\left(\frac{C_m}{C_T} - \frac{L_m}{L_S}\right) \cdot \frac{TD}{Len} \cdot \int_0^{Len} \frac{dV_a(x, t - TD)}{dt} \cdot \alpha\left(\frac{x}{Len}\right) \cdot dx \quad (2)$$

where x is the distance from the signal input point to a point on the microstrip line. $x = 0$ indicates one end of the microstrip line, where the input signal source is attached. $x = Len$ indicates the opposite end of the microstrip line, where the far-end crosstalk voltage is observed. $\alpha(x/Len)$ is the transmission ratio as the crosstalk signal propagates from x to Len along the victim line. Although the lossy transmission line equations can be solved analytically in the frequency domain, the general voltage waveform equation in the time domain cannot be derived analytically. Thus, two empirical equations have been developed in this work. One is the equation of the voltage waveform slope (dV_a/dt). The other is the equation of the transmission ratio $\alpha(x/Len)$.

The circuit simulation program SPICE was used to derive these two empirical equations for the FR4 microstrip lines [7]. The data fitting method applied to the SPICE simulation results gave the equations of dV_a/dt and $\alpha(x/Len)$, as follows:

$$\frac{dV_a(x,t)}{dt} = \frac{4}{1 + \left(2.416 \cdot \left(\frac{R_s}{R_{s0}}\right)^{0.502} + 7.400 \cdot \left(\frac{G_d}{G_{d0}}\right)^{0.664}\right) \cdot x} \times \left[\frac{V}{ns}\right] \quad (3)$$

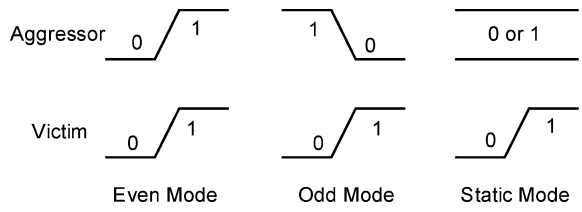


Fig. 2. Signal modes in a pair of coupled transmission lines.

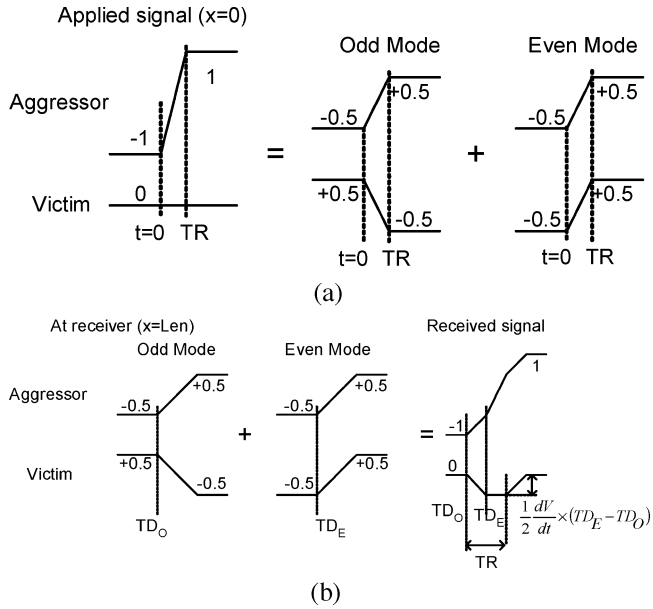


Fig. 3. An alternative view of the crosstalk voltage due to the velocity mismatch between even and odd mode signals. (a) Applied signal $(x = 0)$. (b) Received signal $(x = Len)$.

$$\alpha\left(\frac{x}{Len}\right) = 0.47 \cdot \left(1 - \frac{x}{Len}\right)^2 - 1.04 \cdot \left(1 - \frac{x}{Len}\right) + 1 \quad (4)$$

The substitution of (3) and (4) into (2) gives an empirical equation of the far-end crosstalk voltage waveform for the lossy transmission lines, as follows:

$$\text{Peak } V_{fext} = 0.42\left(\frac{C_m}{C_T} - \frac{L_m}{L_S}\right) \cdot TD \qquad \left[\frac{V}{ns}\right] \quad (5)$$

where the unit of TD is nano-second.

C. Even–Odd Mode Velocity Mismatch

The combination of the signals applied to a pair of coupled transmission lines can be classified into three categories, as shown in Fig. 2. The even mode refers to the case where the two signals make transitions in the same direction at a given instance of time. The odd mode refers to the case where the two signals make transitions in the opposite direction at a given instance of time. The static mode refers to the case where one signal makes a transition while the other signal does not change with time.

Fig. 3 shows an alternative way of deriving the far-end crosstalk voltage waveform represented by (1). Fig. 3(a) shows the signal waveforms at the transmitter side $(x = 0)$. A rising signal with the rise time of TR is applied at the aggressor line.

No signal is applied at the victim line. This combination of signal is decomposed into the odd mode and the even mode, as shown in Fig. 3(a). If we assume the lossless transmission line, both the even mode signal and the odd mode signal propagate along the transmission line without any distortions. Fig. 3(b) shows the signal waveforms at the receiver side ($x = Len$). The odd mode signal of Fig. 3 consists of a rising signal at the aggressor line and a falling signal at the victim line. The rising signal at the aggressor line induces a negative-pulse far-end crosstalk voltage at the victim line and the falling signal at the victim line induces a positive-pulse far-end crosstalk voltage at the aggressor line. The superposition of a negative pulse to a falling signal speeds up the transition of falling signal. Likewise, the superposition of a positive pulse to a rising signal speeds up the transition of rising signal. Therefore, the odd mode signal propagates faster than the static mode signal. The propagation velocity of the static mode signal is the same as that of the signal which propagates along the isolated transmission line without coupling. Similarly, the even mode signal propagates more slowly than the static mode signal.

For the quantitative analysis, the difference in propagation times between the even and odd mode signals can be represented by (6) [8]:

$$\begin{aligned} TD_E - TD_O &= Len \cdot \left(\sqrt{(L_S + L_m)(C_T - C_m)} \right. \\ &\qquad \left. - \sqrt{(L_S - L_m)(C_T + C_m)} \right) \\ &\approx TD \cdot \left(\frac{L_m}{L_S} - \frac{C_m}{C_T} \right) \end{aligned} \tag{6}$$

where TD_E and TD_O are the propagation times of the even and odd mode signals, respectively. Len is the length of transmission line. TD is the propagation time of static mode signal, which is equal to $Len \cdot \sqrt{L_S C_T}$. In the microstrip lines, TD_E is larger than TD_O because L_m/L_S is larger than C_m/C_T due to the surrounding air above the microstrip lines. When one of two independent random data patterns is applied to the aggressor line and the other to the victim line, a random sequence of odd, even, and static modes appears in time. This splits the data edge timing of eye patterns into three distinct groups. Thus, the crosstalk induces the timing jitter in eye patterns.

Equations (1) and (6) show that both the far-end crosstalk voltage and the even–odd mode velocity mismatch are proportional to the same factor, which is the difference between the inductive and capacitive coupling coefficients ($|L_m/L_S - C_m/C_T|$). In this work, a serpentine guard is proposed to increase the mutual capacitance without much increasing the mutual inductance.

III. Serpentine Guard

A. Structure of Serpentine Guard

Fig. 4(a) shows a pair of coupled microstrip lines without guard trace. They are placed on FR4 PCB with the dielectric thickness of 200 μm (8 mil). The width of each microstrip line is 350 μm (14 mil). The thickness of copper is 17.5 μm(0.7 mil). The spacing between the aggressor line and the victim line is 1050 μm (42 mil), that is three times the transmission line width. Fig. 4(b)–(d) shows a pair of microstrip lines, with a guard line added between the two microstrip lines. The spacing between the aggressor and victim lines are maintained to be the same value of 1050 μm (42 mil) for fair comparison.

Fig. 4(b) shows the conventional guard, which is a bare transmission line terminated at both ends. Fig. 4(c) shows the via-stitch guard, which is a terminated transmission line with vias placed uniformly along the guard line. The vias connect the guard microstrip line to the ground plane. The via-stitch guard is more effective than the conventional guard in reducing the far-end crosstalk, because the guard trace with vias can maintain the ground potential at every via point and this reduces both L_m and C_m. However, the via-stitch guard has a disadvantage that the opposite side of PCB along the microstrip lines can not be used for routing due to the vias.

Fig. 4(d) shows a serpentine guard, in which the combination of a parallel section and a vertical section is repeated along the transmission line. The parallel sections are located alternately close to the aggressor line and to the victim line, along the transmission line. A vertical section connects the parallel section close to the aggressor line and the parallel section close to the victim line. There is no magnetic coupling between the aggressor line and the vertical section of serpentine guard because the direction of the current flow in the vertical section is perpendicular to that in the aggressor line. Thus, the vertical section of the serpentine guard increases the mutual capacitance without increasing the mutual inductance between the aggressor line and the guard trace. Due to the symmetry of layout, the mutual capacitance between the victim line and the guard trace is also increased. Because both the mutual capacitance between the aggressor line and the guard trace and the mutual capacitance between the victim line and the guard trace are increased, the mutual capacitance between the aggressor line and the victim line is also increased.

To prove that the serpentine guard increases the mutual capacitance between the aggressor and victim lines, a lengthwise unit section of serpentine guard and its equivalent circuit in terms of capacitance are shown in Fig. 5(a) and (b). The mutual capacitance C_m between the aggressor and victim lines in Fig. 5(b) can be derived as (7). For this derivation, the aggressor line is connected to a 1 V voltage source and the victim line is connected to ground

$$C_m = C_{13} + \frac{C_{12} \cdot C_{23}}{C_2 + C_{12} + C_{23}} \tag{7}$$

where C_{12} is the mutual capacitance between the aggressor line and the guard trace, and C_{23} is the mutual capacitance between the guard trace and the victim line. C_{13} is the mutual capacitance between the aggressor and victim lines with the serpentine guard connected to ground. C_2 is the self capacitance of the serpentine guard to ground. Because the self capacitance C_2 is much larger than the sum of the mutual capacitances C_{12} and C_{23}, C_m increases with the increase of C_{12} and C_{23}. To further increase C_m, C_2 can be decreased by shrinking the width of the guard trace.

Table I shows the comparison of capacitances calculated by using a field solver [9]. C_{12} and C_{23} can be represented with C_{pn}, C_{pw}, and C_{mv} shown in Fig. 5(a), as $C_{12} = C_{23} = (C_{pn} + C_{pw} + 2C_{mv}/2)$. The field solver simulation gave the values of C_{pn}, C_{pw}, and C_{mv} to be 11.5 pF/m, 3.0 pF/m, and 5.2 pF/m,

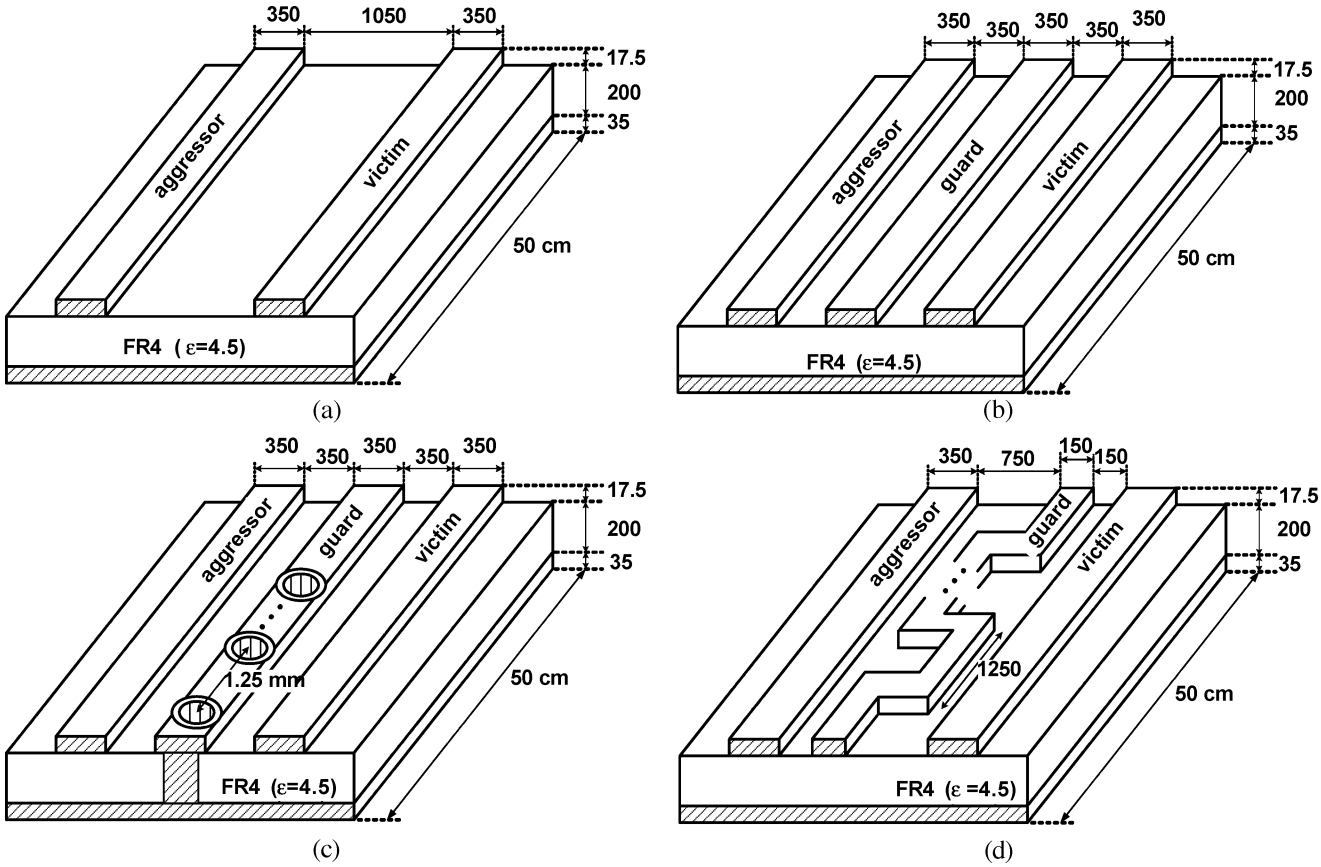


Fig. 4. Guard traces. (a) No guard. (b) Conventional guard. (c) Via-stitch guard. (d) Serpentine guard (unit: μm).

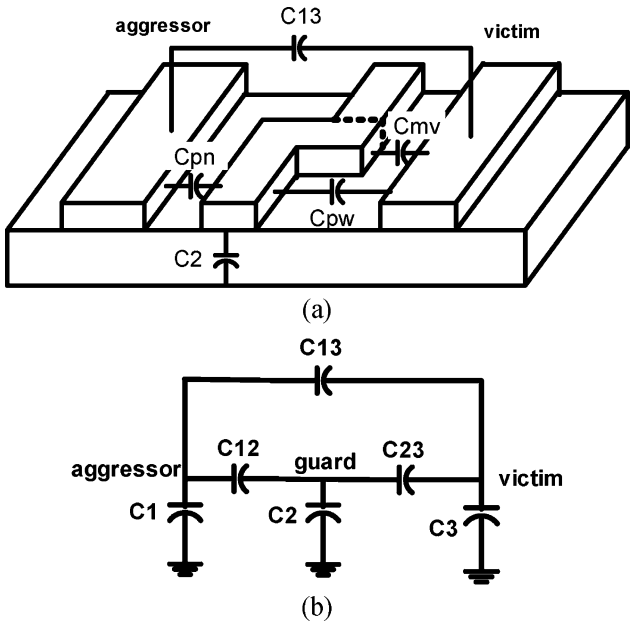


Fig. 5. (a) Section of two microstrip lines with a serpentine guard. (b) Equivalent circuit.

respectively. Compared to the conventional guard, the C_{12} and C_{23} of serpentine guard were increased by more than twice and the C_2 of serpentine guard was reduced by around half. This increases the mutual capacitance C_m between the aggressor and victim lines by around 2.5 times that of conventional guard.

TABLE I
MUTUAL CAPACITANCE EXTRACTED FROM FIELD SOLVER

	No guard	Conv. guard	Serp. guard
C_{13} [pF/m]	0.70	0.70	0.70
C_{12} [pF/m]	-	5.52	12.5
C_{23} [pF/m]	-	5.52	12.5
C_2 [pF/m]	-	130	73.6
C_m [pF/m]	0.70	0.92	2.28

TABLE II
MEASURED L_S, L_M, C_T, C_M USING LCR METER

	No guard	Conv. guard	Via guard	Serp. guard
L_S [nH/m]	456	456	452	456
L_m [pF/m]	16.8	16.7	7.84	16.0
C_T [pF/m]	119	122	121	125
C_m [pF/m]	0.90	1.90	0.40	3.10
C_m/C_T -L_m/L_S	-0.029	-0.021	-0.014	-0.010

B. SPICE LRGC Parameters

To calculate the LRGC matrix of the SPICE lossy transmission line model [10] for the four cases shown in Fig. 4, the microstrip transmission lines fabricated on FR4 PCB were measured by using an LCR meter and a vector network analyzer (VNA). The LCR meter data were used to calculate the lossless parameters. The VNA data [7] were used to calculate the loss parameters.

Table II shows the LCR meter data, which are L_S, L_m, C_T, and C_m, for the four cases shown in Fig. 4. In the LCR meter

TABLE III
MEASURED R AND G PARAMETERS FOR HSPICE W MODEL OF MICROSTRIP LINE

R_{DC} $[\Omega/m]$	R_{AC} $[\Omega/m\cdot\sqrt{Hz}]$	G_{DC} $[S/m]$	G_{AC} $[S/m\cdot Hz]$
2.721	8.086E-4	3.937E-9	1.807E-11

measurement, the signal amplitude was 100 mV and the frequency was 1 MHz for the inductance measurement and 75 KHz for the capacitance measurement. In Table II, the values of L_S and C_T are approximately the same within 5% for all the four cases. L_m is also approximately the same within 5% for the three cases excluding the via-stitch guard. However, C_m of the serpentine guard is about 3.4 times that of no guard. This C_m ratio is close to the field solver C_m ratio of 3.3. Also, the serpentine guard C_m is about 1.6 times the conventional guard C_m. The via-stitch guard showed the significant reduction of both C_m and L_m by about 45% compared to the no guard case.

Table III shows the loss parameters of the SPICE LRGC matrix for the FR4 microstrip lines used in this work. These parameters were calculated from the *S*-parameter measurement using a 5-GHz VNA [7]. G_d is the ac conductance parameter due to the dielectric loss. R_s is the ac resistance due to the skin effect. The SPICE LRGC matrices for the four pairs of microstrip lines in Fig. 4 can be obtained from the parameters shown in Tables II and III.

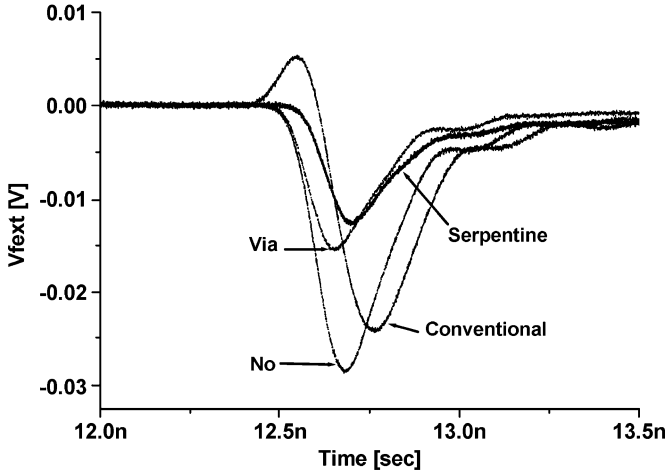
IV. MEASUREMENTS AND COMPARISON

A. Far-End Crosstalk Voltage

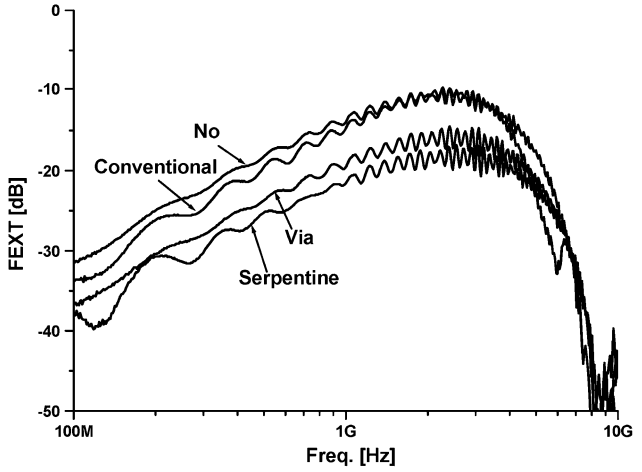
Fig. 6(a) shows the far-end crosstalk voltage waveforms measured by using time domain reflectometer (TDR) for the four cases shown in Fig. 4. A 0.4-V step pulse with an initial rise time of 50 ps is applied to one end of the aggressor line. The crosstalk voltage waveform is measured at the opposite end of the victim line. All ends of the aggressor and victim lines are terminated by 50 Ω. Both ends of the serpentine guard are terminated by 75-Ω resistors, which match the characteristic impedance of the guard microstrip line. The serpentine guard gave the smallest peak far-end crosstalk voltage, which is about 44% of that of no guard.

Table IV shows the comparison of the measured peak far-end crosstalk voltage with the calculated value using (2) and (5). In the calculation, the measured values of L_S, L_m, C_T, and C_m in Table I are used. Also, the propagation time TD in (2) is set to the measured values of 3.05, 3.06, 3.05, and 3.08 ns, for no guard, conventional guard, via-stitch guard, and serpentine guard, respectively. The calculated values show fair agreements with the measured values within 15% error except the no guard case, where the error is about 30%.

Fig. 6(b) shows the measured frequency-domain far-end crosstalk (S21) by using a VNA for the four cases shown in Fig. 4. It indicates that the serpentine guard gives the smallest crosstalk for all the frequency range of interest. Both Fig. 6(a) and (b) reveal the same tendency of far-end crosstalk for all the four cases compared. At very high frequency, the S21 deceases with frequency because of the high frequency loss of microstrip lines.



(a)



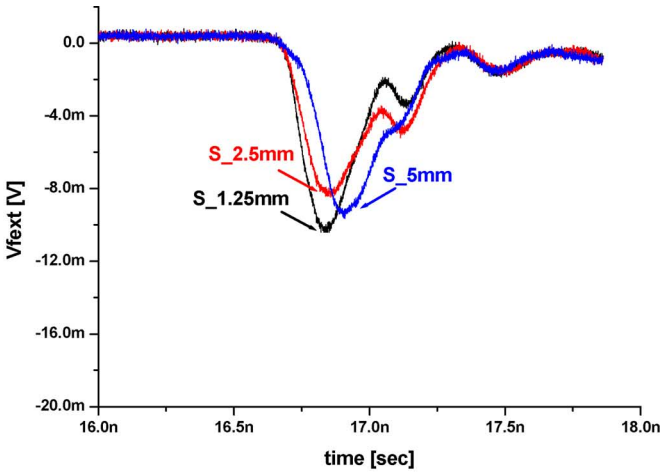
(b)

Fig. 6. (a) Measured time-domain far-end crosstalk voltage waveform. (b) Measured frequency-domain S21 (FEXT).

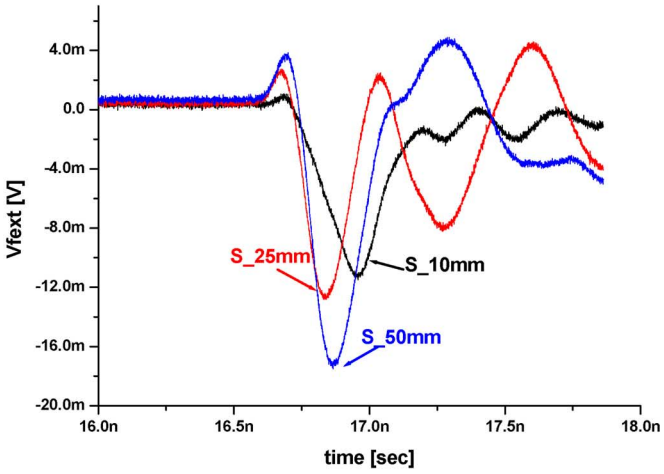
TABLE IV
COMPARISON OF PEAK FAR-END CROSSTALK VOLTAGE BETWEEN CALCULATION AND MEASUREMENT

	No guard	Conv. guard	Via guard	Serp. guard
Eq.(2)	-37.1	-27.0	-17.9	-12.9
Measurement	-28.6	-24.3	-15.8	-12.7
Error [%]	29.7	11.1	13.3	1.57

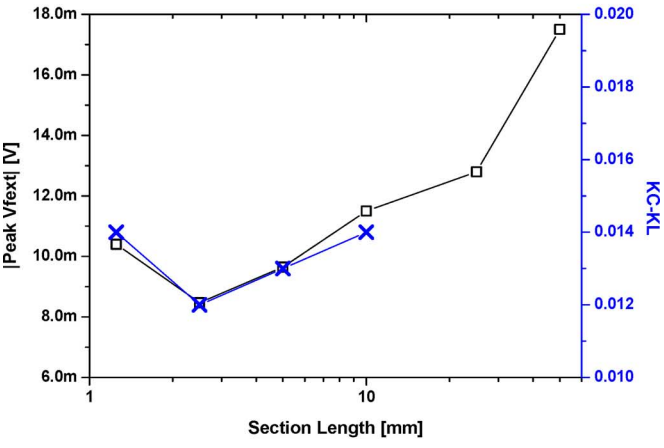
Fig. 7(a) and (b) shows the far-end crosstalk voltage waveforms with the change of the parallel section length in the serpentine guard. The parallel section length is changed from 1.25 to 50 mm. The length of the entire transmission line is 40 cm. When the parallel section length is relatively large, such as 50 or 25 mm, large reflections are observed. As the parallel section length is reduced, the peak far-end crosstalk voltage is also reduced. However, if the parallel section length is reduced to a too small value such as 1.25 mm, the peak far-end crosstalk voltage is increased. This phenomenon is considered to be due to the increase of coupling between the vertical sections of the serpentine guard. Thus, the peak far-end crosstalk voltage reaches its minimum value at the parallel section length of around 2.5 mm



(a)



(b)



(c)

Fig. 7. Measured far-end crosstalk voltage (a) section length 1.25 mm ∼ 5 mm. (b) Section length 10 mm ∼ 50 mm. (c) Peak far-end crosstalk voltages with different section lengths (square: from Fig. 7(a) and (b); cross: KC-KL from TDR measurements).

[Fig. 7(c)]. The difference between the inductive and capacitive coupling coefficients (KC-KL) is also shown in Fig. 7(c) for comparison. The KC-KL values were extracted from the characteristic impedances and the propagation delay times of the even and odd modes, which are measured by using a differential TDR.

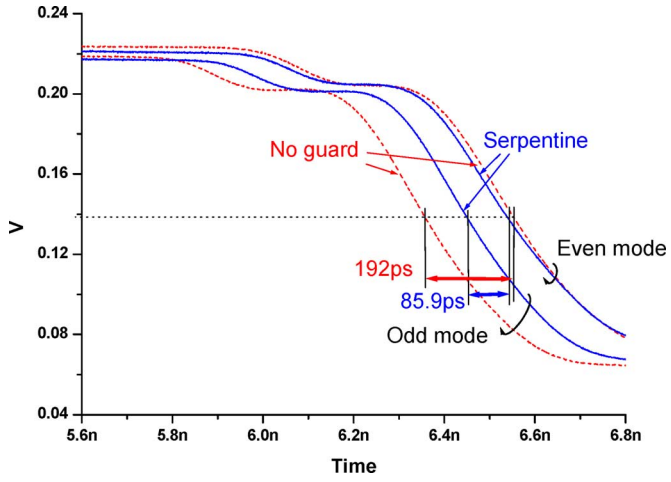


Fig. 8. Measured output waveforms (even and odd mode).

B. Even–Odd Mode Velocity Mismatch

The serpentine guard can reduce the timing jitter due to the even–odd mode velocity mismatch. The even–odd mode velocity mismatch is caused by the same mechanism as the far-end crosstalk voltage, as shown in Fig. 3, (1), and (4). Both of them are caused by the difference between the capacitive and inductive coupling ratios. Because the serpentine guard reduces the difference between these two ratios, it can be used to reduce both the far-end crosstalk voltage as well as the timing jitter due to the even–odd mode velocity mismatch.

The difference in propagation times between the even and odd mode signals was measured for the four cases shown in Fig. 4. A differential TDR was used for this measurement. The even and odd mode propagation times TD_E and TD_O were measured as the time points at which the received signal reaches its 50% value with both aggressor and victim lines shorted to ground at the far-end points.

Fig. 8 shows the comparison of the measured TDR waveforms between no guard and the serpentine guard. Although both even and odd mode signals start simultaneously at the input point, the odd mode signal arrives the end point earlier than the even mode signal. The propagation times of the even mode signals (TD_E) are almost the same for both cases, but the propagations times of the odd mode signals (TD_O) are quite different. The serpentine guard increased TD_O without much changing TD_E, compared to the no guard case. As shown in (4), TD_E and TD_O are represented by $\sqrt{(L_S + L_m)(C_S)}$ and $\sqrt{(L_S - L_m)(C_S + 2C_m)}$, respectively. This indicates that the serpentine guard increases the mutual capacitance C_m without much changing L_m, compared to the no guard case. The difference between TD_E and TD_O of the serpentine guard was reduced to 45% that of no guard.

Fig. 9 shows the simulated eye diagram of the received signal at the victim line end for the four cases when the independent pseudo random binary sequence (PRBS) signals are applied at both the aggressor line and the victim line. The LRGC parameters shown in Tables II and III are used in this SPICE simulation. A 100 Mbps $2^7 - 1$ PRBS signal is applied to the aggressor line. A 100 Mbps $2^{15} - 1$ PRBS is applied to the victim line. The voltage swing and the rise time are 0.5 V and 100 ps, respectively, for both the aggressor and victim line signals. A relatively slow signal of 100 Mbps is used to measure

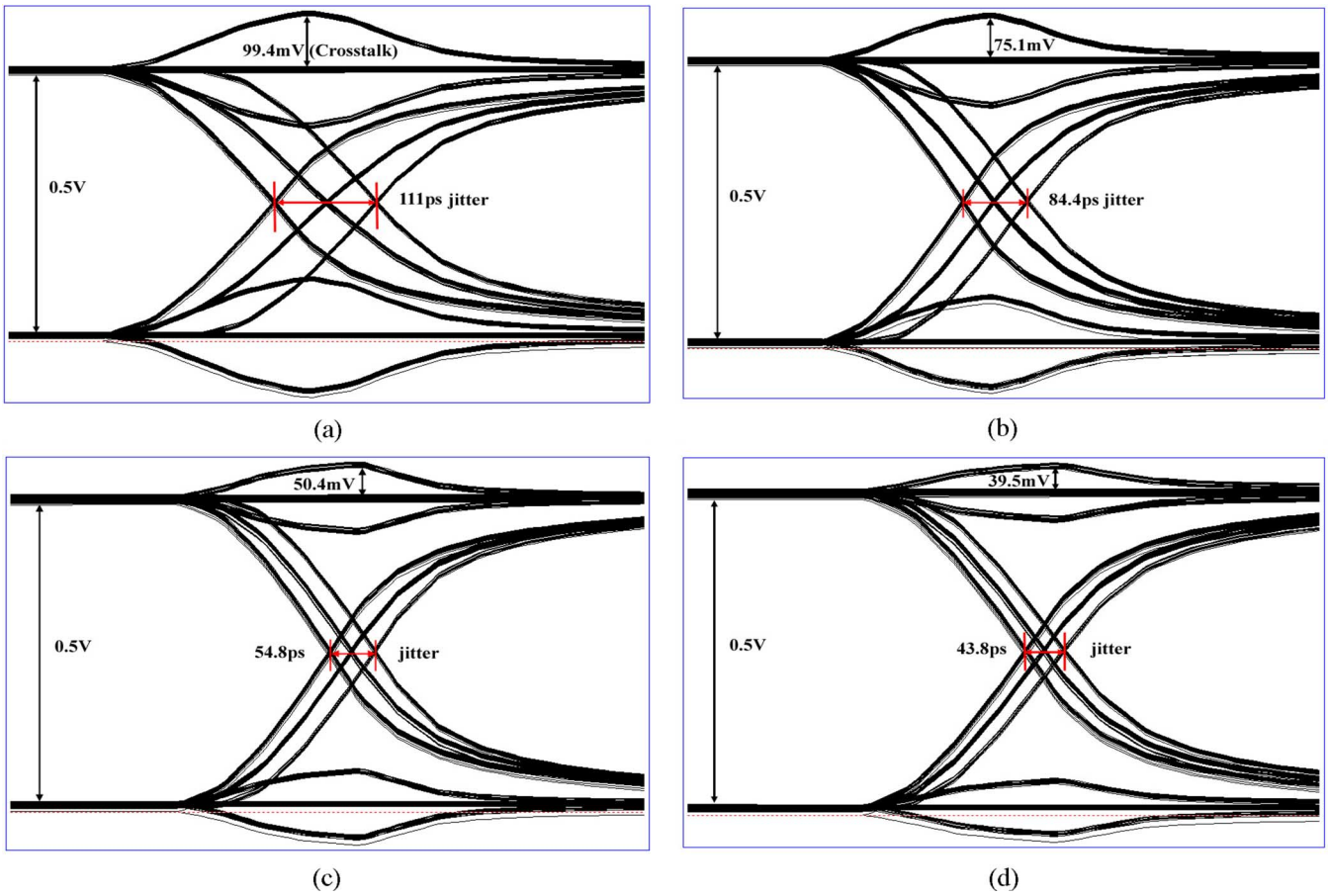


Fig. 9. SPICE of 100 Mbps PRBS. (a) No guard. (b) Conventional guard. (c) Via-stitch guard. (d) Serpentine guard.

the effect of crosstalk alone without being affected by the intersymbol interference (ISI). The jitter of the serpentine guard is reduced to about 40% of that of no guard. The overshoot or undershoot voltage from the dc level in Fig. 9 represents the far-end crosstalk voltage. The peak overshoot value is reduced to 39.5 mV in the serpentine guard, while it is 99.4 mV in the no guard case. Thus, the serpentine guard reduced the overshoot voltage to 40% of that of no guard. This ratio is fairly consistent with the measured peak far-end crosstalk voltage ratio of 44% in Fig. 6, the measured propagation time mismatch ratio of 45% in Fig. 8 and the simulated jitter ratio of 39% in Fig. 9.

Fig. 10 shows the measured eye diagrams of the received signal for the four cases shown in Fig. 4. A 100 Mbps PRBS signal with a 0.5 V swing is used in the measurement. The synchronized pseudo random signals are applied to both the aggressor and victim lines. A $2^7 - 1$ PRBS signal and a $2^{31} - 1$ PRBS signal are applied to the aggressor line and the victim line, respectively. The jitters are measured to be 37 and 91 ps, for the serpentine guard and the no guard, respectively. The jitter of the serpentine guard is 41% of that of no guard. These measured data agree with the simulation results shown in Fig. 9. The measured peak crosstalk voltages are 92.0, 78.0, 53.5, and 43.5 mV, for no guard, conventional guard, via-stitch guard and serpentine guard, respectively. The voltage ratios are almost the same as those of the TDR measurements in Fig. 6.

Fig. 11 shows the eye diagrams of the received signal with the data rate of 3.3 Gbps, with and without crosstalk. For the case with the crosstalk, the $2^7 - 1$ and $2^{31} - 1$ PRBS signals are applied to the aggressor line and the victim line, respectively. For the case without crosstalk, a $2^{31} - 1$ PRBS signal is applied to the victim line alone, with the aggressor line left terminated at both ends. Without crosstalk, only the ISI effect is observed. With the crosstalk both the ISI and crosstalk effects are observed. The peak-to-peak crosstalk induced jitter $(J_{\mathrm{pp.xt}})$ is calculated by subtracting the timing jitter without crosstalk from that with crosstalk [8]. The $\mathrm{J_{pp.xt}}$ values are 36.6 and 93.7 ps, for the serpentine guard and no guard, respectively. These $J_{\mathrm{pp.xt}}$ values from the 3.3 Gbps measurements are in good agreements with the $J_{\mathrm{pp.xt}}$ values from the 100 Mbps measurements shown in Fig. 10, which are 37.0 and 91.0 ps for the serpentine guard and no guard, respectively.

Fig. 12 shows the difference in propagation times between the even and odd mode signals for the four cases shown in Fig. 4. This difference in the propagation times directly corresponds to the timing jitter. Fig. 12 includes the differential TDR measurement (Fig. 8) and the 100 Mbps eye diagram measurement (Fig. 10) and the 3.3 Gbps eye diagram measurement (Fig. 11). Except the conventional guard, all three measurements show good agreements within 15%. The value of the serpentine guard was the smallest in four cases in Fig. 4 and was reduced to about 40% of that of no guard.

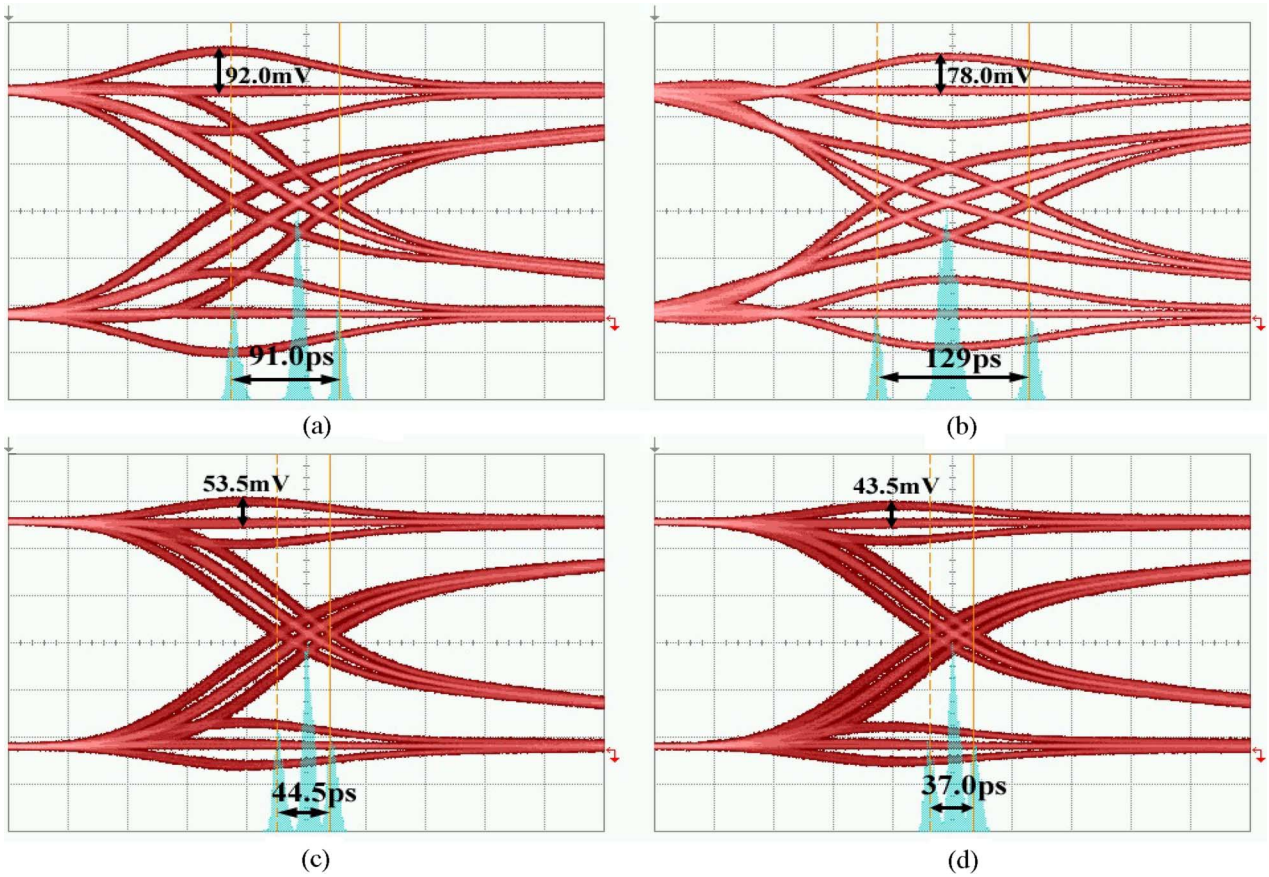


Fig. 10. Measurement of eye diagrams at 100 Mbps PRBS. (a) No guard. (b) Conventional guard. (c) Via-stitch guard. (d) Serpentine guard.

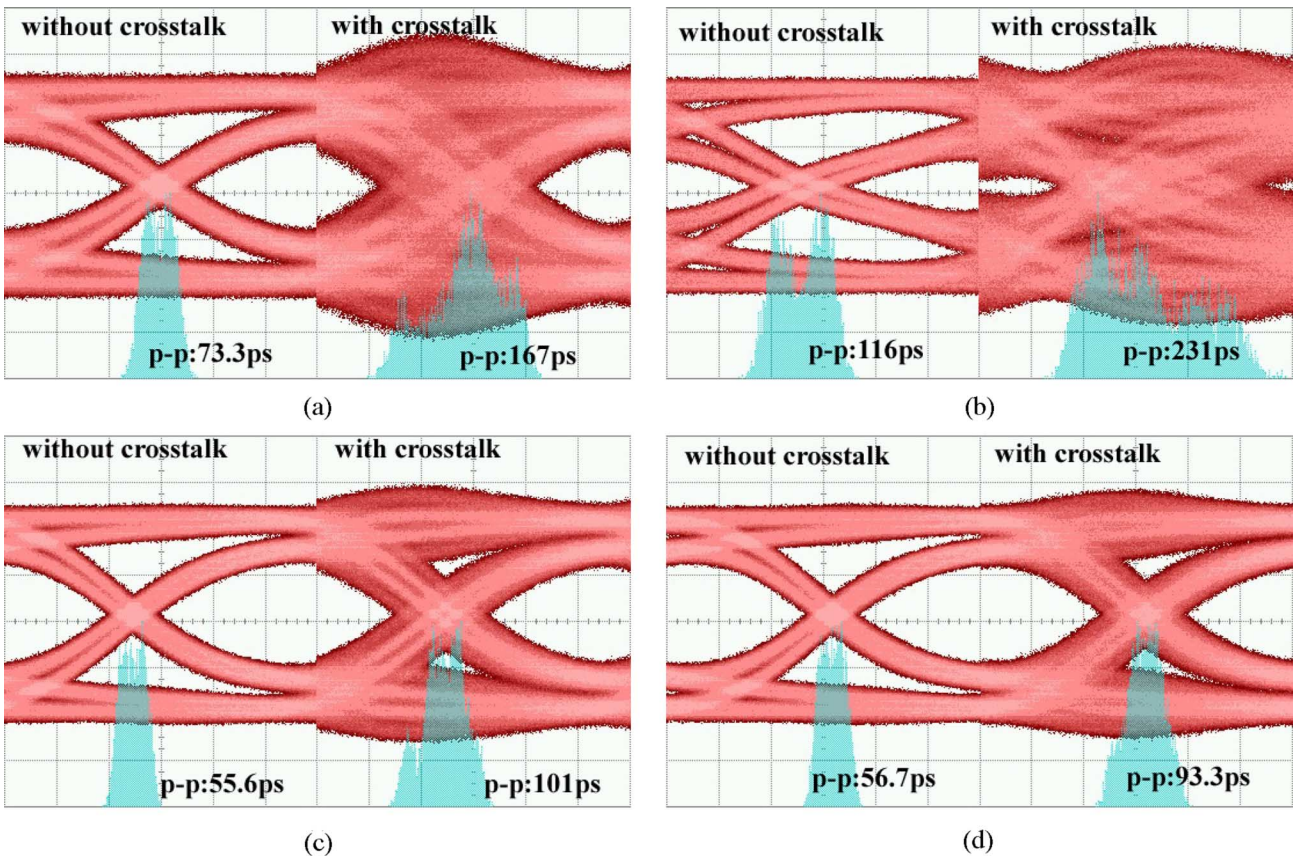


Fig. 11. Measurement of eye diagrams at 3.3 Gbps PRBS. (a) No guard. (b) Conventional guard. (c) Via-stitch guard. (d) Serpentine guard.

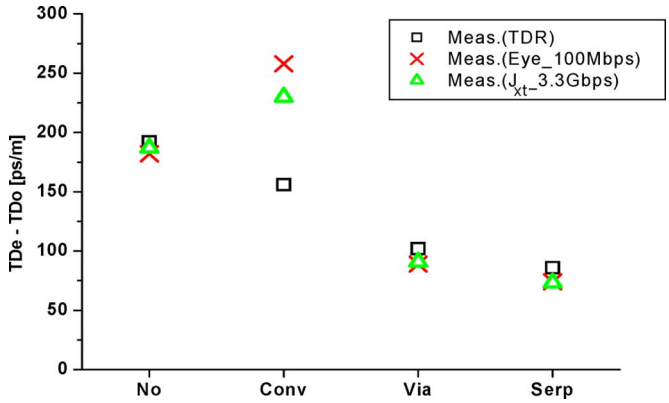


Fig. 12. Difference in propagation times between even and odd modes.

V. Conclusion

A serpentine guard trace reduces both the peak far-end crosstalk voltage and the timing jitter due to the even–odd mode velocity mismatch of microstrip lines. The measurements of L_S, L_m, C_T, and C_m show that the serpentine guard reduces the difference between the capacitive and inductive couplings by increasing the mutual capacitance without changing the mutual inductance.

The TDR measurement, the 100-Mbps eye diagram measurement and the 3.3-Gbps eye diagram measurement are performed for the no guard, the conventional guard, the via-stitch guard, and the serpentine guard. Among these four cases, the serpentine guard gives the smallest values in both the peak far-end crosstalk voltage and the timing jitter. The serpentine guard values are about 40% of the no guard values.

References

[1] Y. S. Sohn, J. C. Lee, and H. J. Park, "Empirical equations on electrical parameters of coupled microstrip lines for crosstalk estimation in printed circuit board," *IEEE Trans. Adv. Packag.*, vol. 24, no. 4, pp. 521–527, Nov. 2001.

[2] T. R. Gazizov, "Far-end crosstalk reduction in double-layered dielectric interconnects," *IEEE Trans. Electromagn. Compat.*, vol. 43, no. 4, pp. 566–572, Nov. 2001.

[3] D. Brooks, *Signal Integrity Issues and Printed Circuit Board Design*. New York: Prentice Hall, 2003, pp. 233–234.

[4] I. Novak, B. Eged, and L. Hatvani, "Measurement by vector-network analyzer and simulation of crosstalk reduction on printed circuit boards with additional center traces," in *Instrumentation Measurement Technol. Conf.*, Irvine, CA, May 1993, pp. 269–274.

[5] L. Zhi, W. Qiang, and S. Changsheng, "Application of guard traces with vias in the RF PCB layout," in *3rd Int. Symp. Electromagn. Compat.*, Beijing, China, May 21–24, 2002, pp. 771–774.

[6] K. Lee, H.-B. Lee, H.-K. Jung, J.-Y. Sim, and H.-J. Park, "Serpentine guard trace to reduce far-end crosstalk and even-odd mode velocity mismatch of microstrip lines by more than 40%," in *Electron. Compon. Technol. Conf.*, Reno, NV, 2007, pp. 329–332.

[7] H.-B. Lee, K. Lee, H.-K. Jung, and H.-J. Park, "Extraction of LRGC matrices For 8-coupled uniform lossy transmission lines using 2-port VNA measurements," *IEICE Trans. Electron.*, vol. E89-C, no. 3, pp. 410–419, March 2006.

[8] J. F. Buckwalter and A. Hajimiri, "Cancellation of crosstalk-induced jitter," *IEEE J. Solid State Circuits*, vol. 41, no. 3, pp. 621–632, Mar. 2006.

[9] *"Ansoft HFSS user's Guide—High Frequency Structure Simulator,"* Ansoft Korea, 2003.

[10] *"Star HSPICE Manual,"* Dec. 1999.

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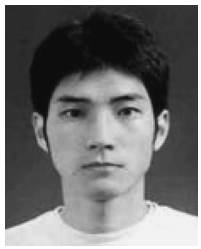

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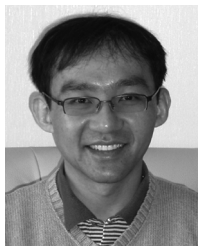

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