Fundamentals of Power Integrity

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2017 IEEE EMC/SIPI Symposium
8/7-8/11, 2017, Washington DC

Content

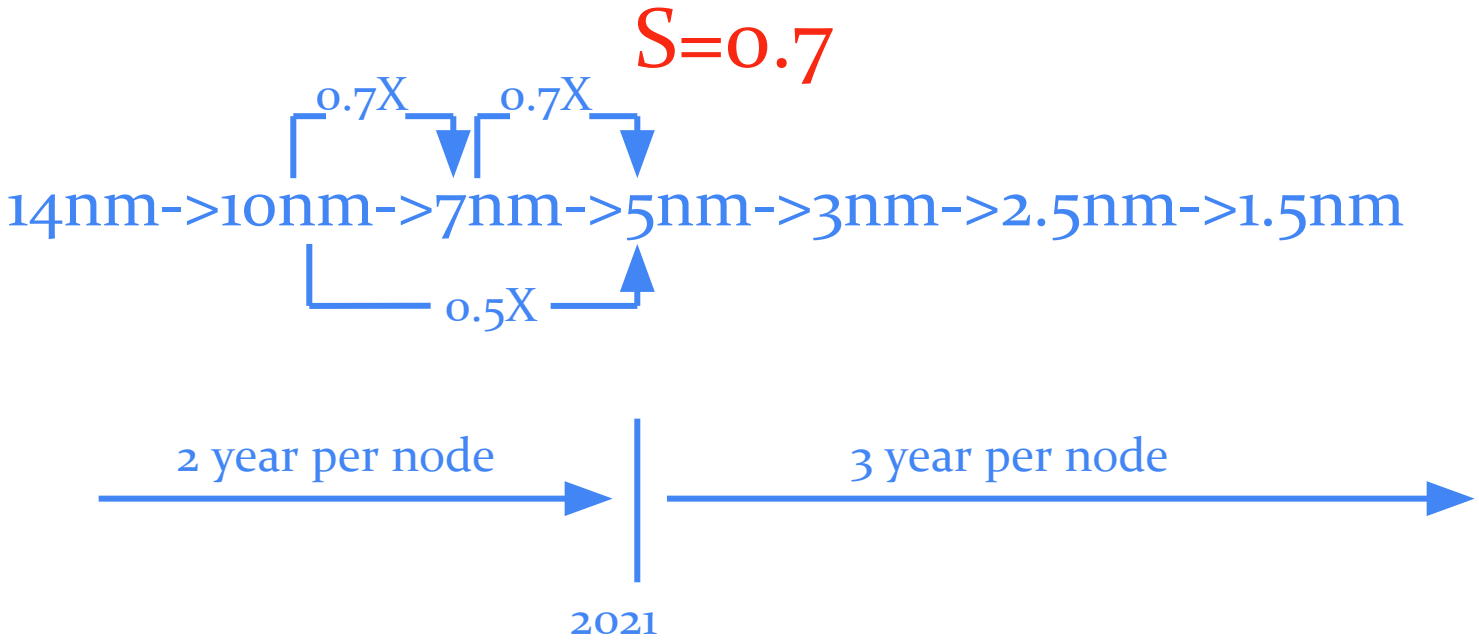
- Industry trend and power integrity challenges
- Capacitor
- Power impedance measurement
- Power decoupling strategy
- Target impedance
- On-die power integrity analysis
- Package-level power integrity analysis
- Die/Package/Board co-design methodology
- SSO and SSI
- Open topics and Q&A

Industry trend and power integrity challenges

- Technology nodes
- ITRS Roadmap
- Derived data from ITRS roadmap

Technology Nodes (2015 ITRS report)

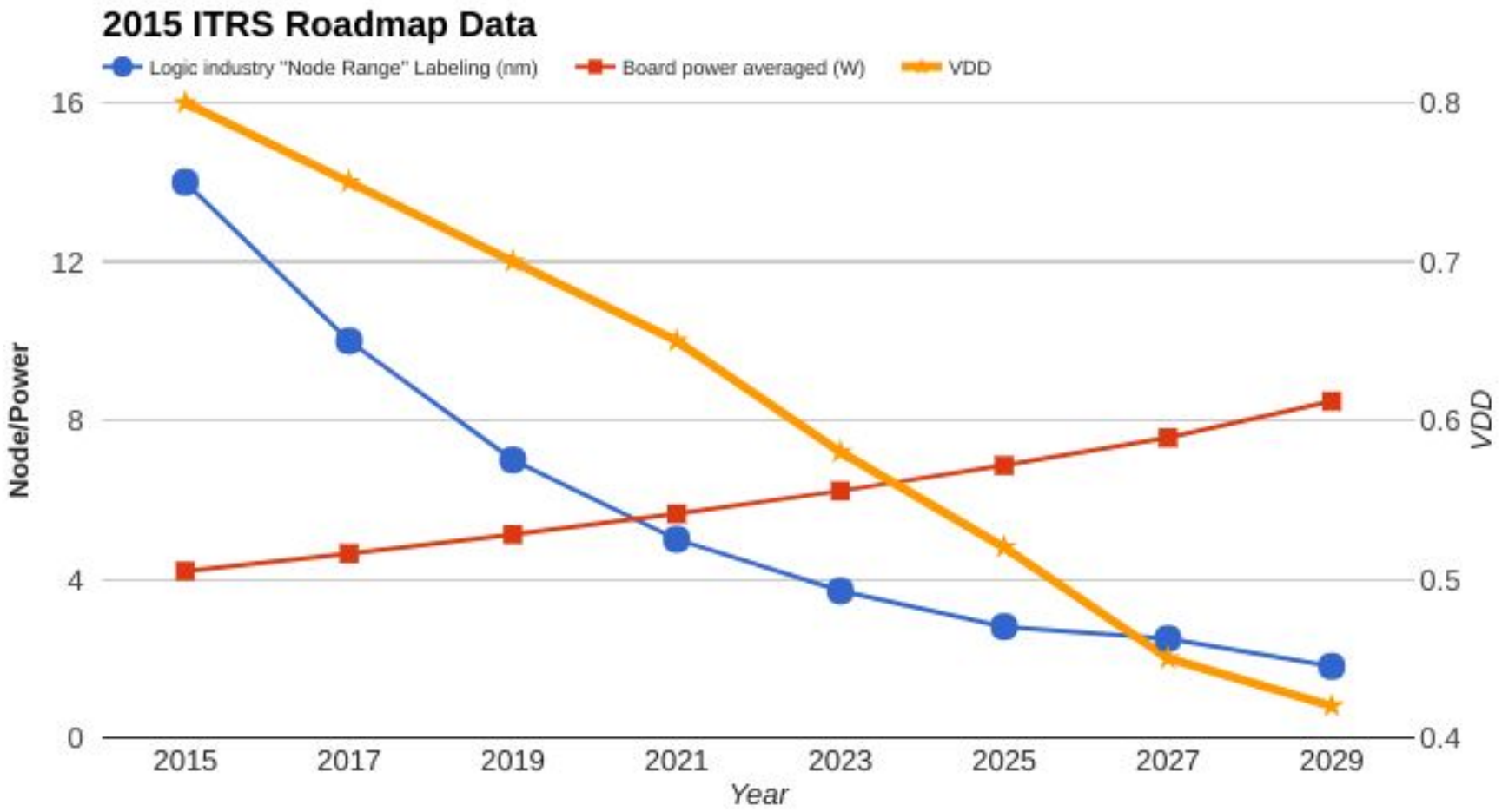
MOS Transistor Scaling (1974 to present)



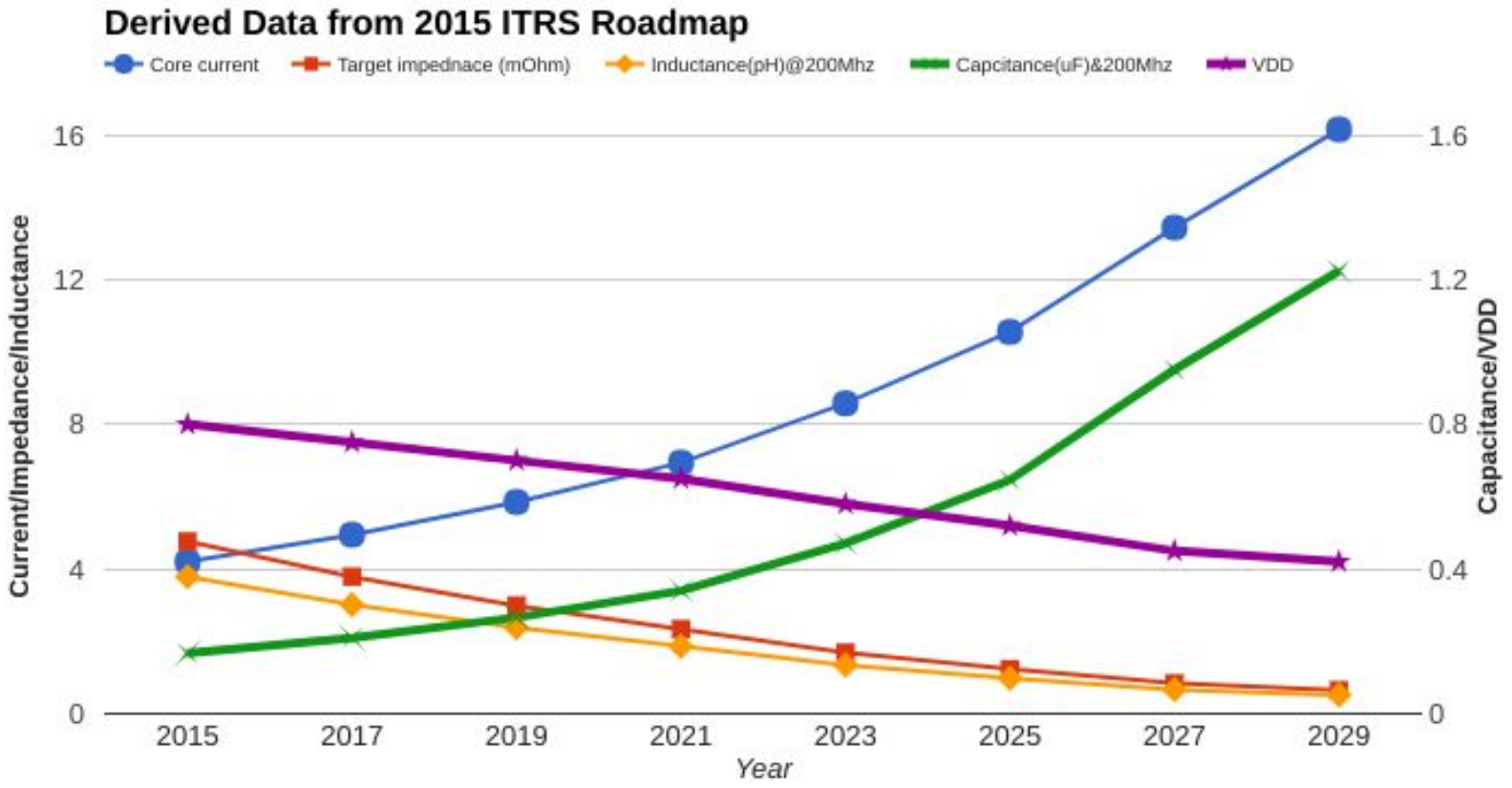
Electrical Properties of Transistors

YEAR OF PRODUCTION	2015	2017	2019	2021	2024	2027	2030
Logic device technology naming	P70M56	P48M36	P42M24	P32M20	P24M12G1	P24M12G2	P24M12G3
Logic industry "Node Range" Labeling (nm)	"16/14"	"11/10"	"8/7"	"6/5"	"4/3"	"3/2.5"	"2/1.5"
Logic device structure options	FinFET FDSOI	FinFET FDSOI	FinFET LGAA	FinFET LGAA VGAA	VGAA, M3D	VGAA, M3D	VGAA, M3D
DEVICE ELECTRICAL SPECS							
Power Supply Voltage - Vdd (V)	0.80	0.75	0.70	0.65	0.55	0.45	0.40

2015 ITRS Mobile Roadmap data



Derived data from 2015 ITRS Mobile

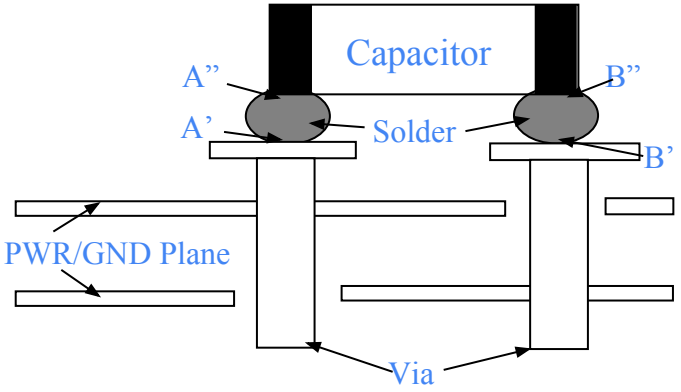


Assumptions: 80% power is for Core, +/-5% allowable voltage noise, and Dynamic current is 2X of average.

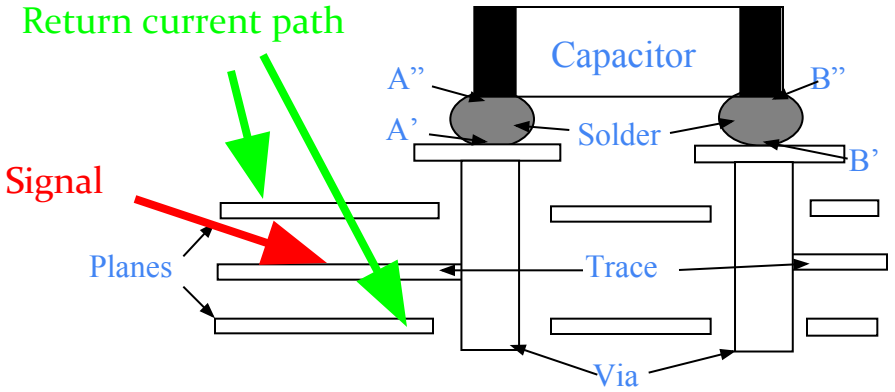
Capacitor

- Types of capacitor on the PCB board
- Why capacitor for power delivery system?
- Elements of the inductance for the capacitor mounted on the PCB board
- The challenges on the definition and measurement of the inductance for the capacitor
- A proposal on inductance measurement method
- For the decoupling caps, is the self inductance really important?

Type of capacitors on the PCB board

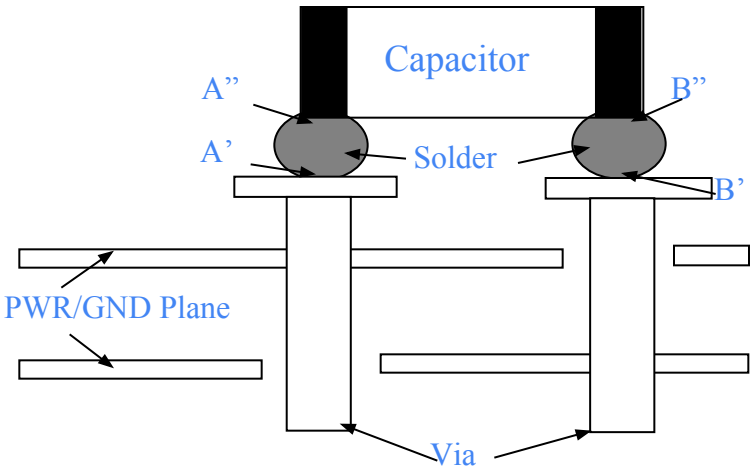


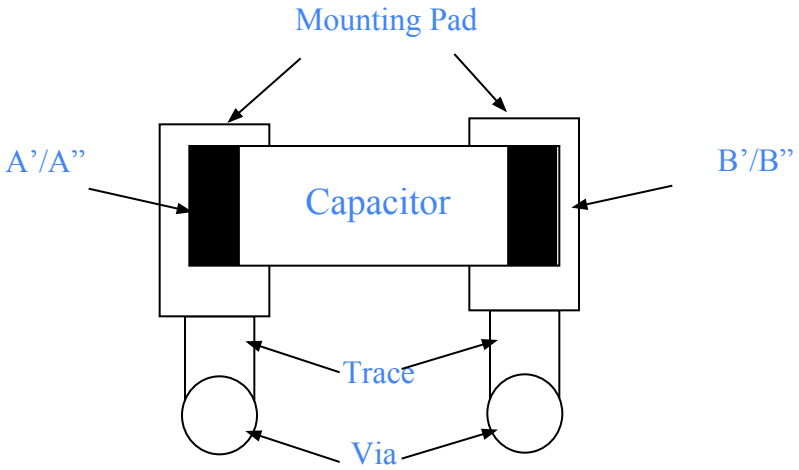
Decoupling caps for Power Supplies



DC blocking caps for high-speed differential signals

Elements of the inductance for the caps on PCB





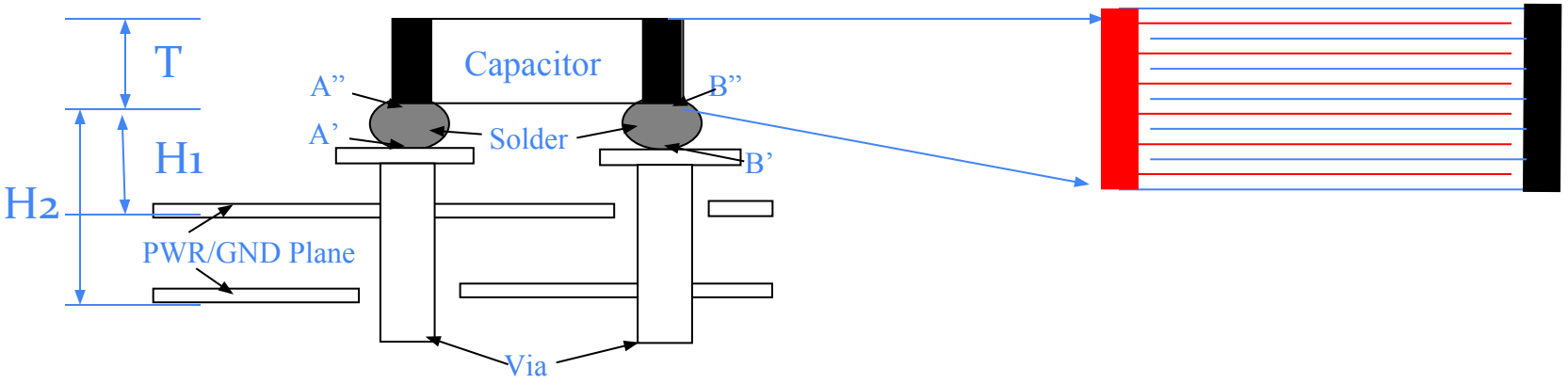
The current path (associated inductances) with different types of capacitor:

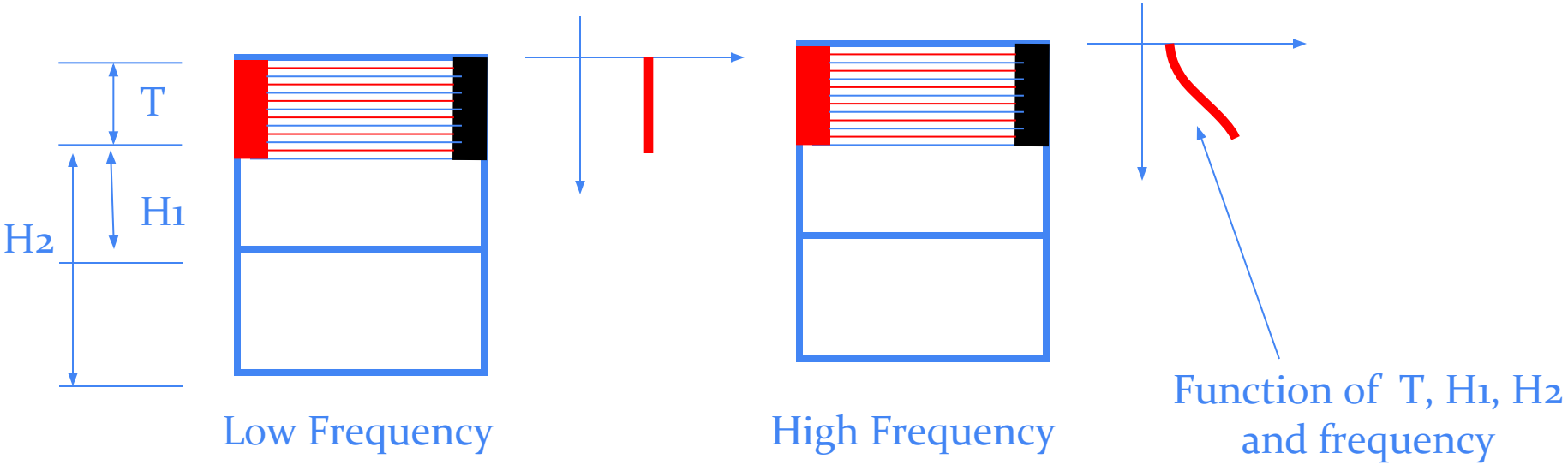
Decoupling cap: Power/Ground plane+Vias+Traces-on-top-layer+Pads+solders+capacitor
DC-blocking cap: Signal/return+Vias+Traces-on-top-layer+Pads+solders+capacitor

Examples:

- L_total=(L_planes+L_vias+L_traces+L_pads+L_solder) +(L_capacitor)+/-2*M_mutuals
- Mutual inductance is complicated and its value varies with different ways of capacitor mounting structures.

Example of current distribution at different frequencies



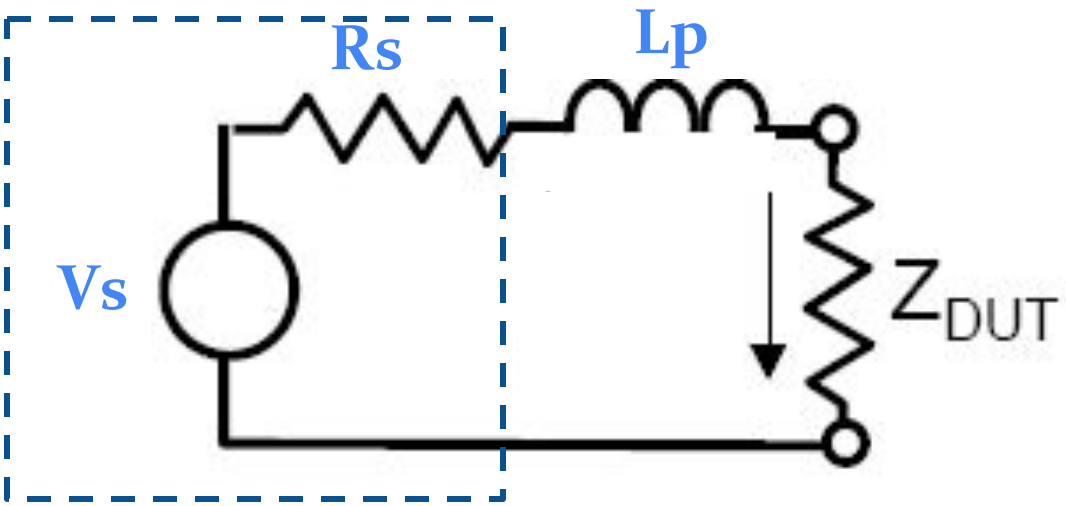


Power impedance measurement

- The simplest way and its problem
- The advanced power impedance measurement method

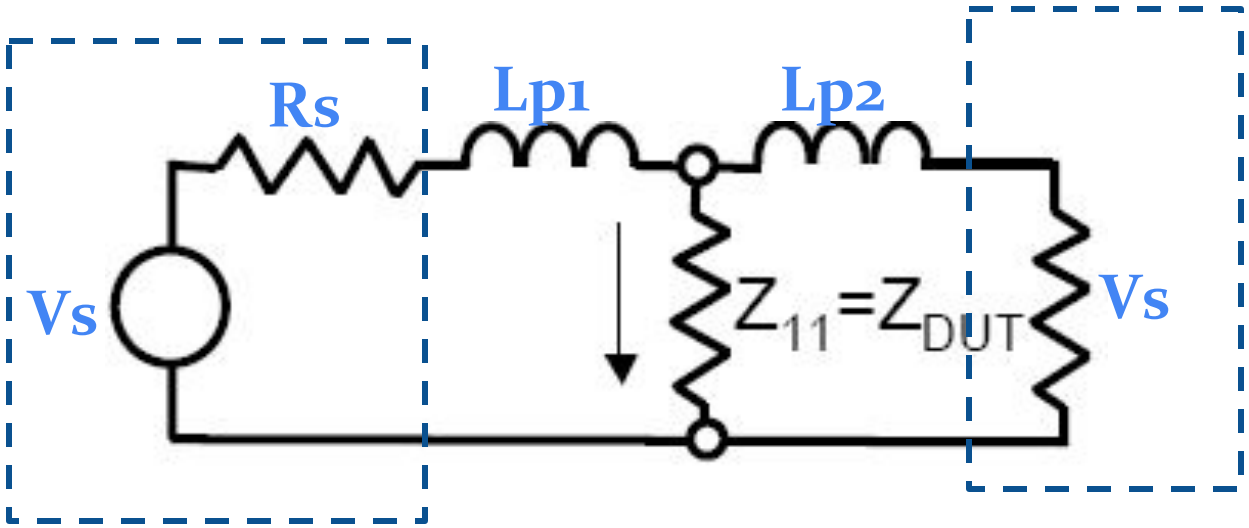
The simplest way and its problem

- Lp and Z_dut are in series and it is impossible to de-embed it from the measurement
- Lp/Zp could usually much high impedance than power impedance at high-frequency
- VNA S11 uncertainty is high compared with S21



The enhanced measurement method

- Using S21 instead of S11. Similar the Wheatstone bridge method
- The impact of Lp1 and Lp2 is much less



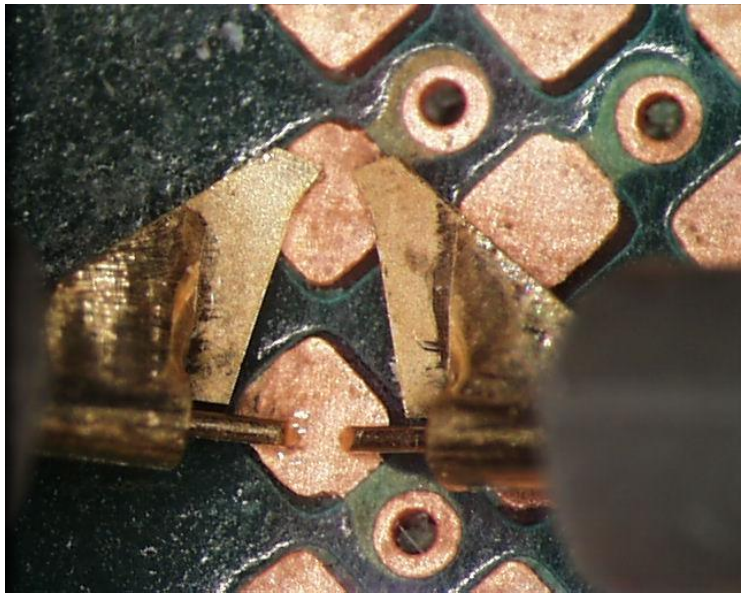
The enhanced measurement method

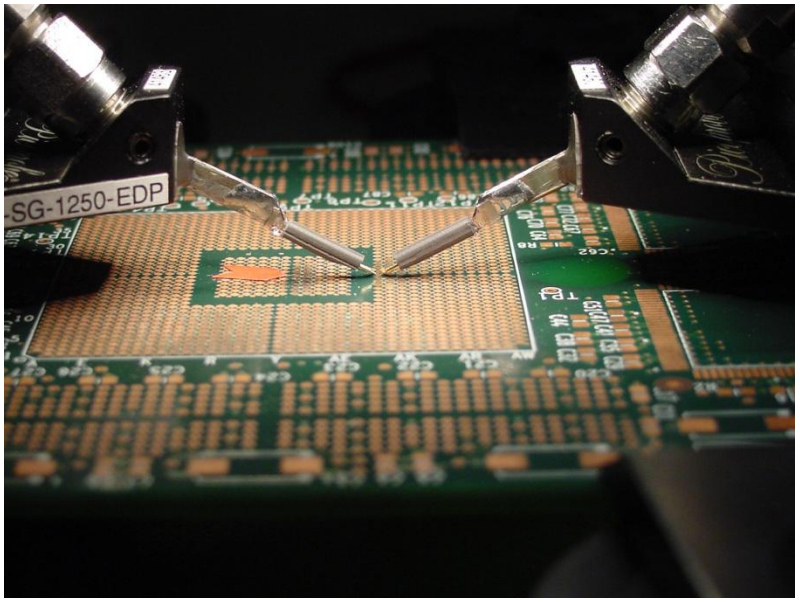
- If Lp is small and Zdut<<Zs, Zdut=25*S21 (Ohm)
- For better accuracy, the following equation can be used:

$$Z_{ii} = S_{21}\frac{Z_1}{2}\frac{1}{1-S_{21}\dfrac{Z_1+Z_2}{2Z_2}} \approx S_{21}*25*\frac{1+j\omega\tau_p}{1-S_{21}}$$

$$Z_1 = 50+j\omega L_{p1} \quad Z_2 = 50+j\omega L_{p2} \quad \tau_p = L_p/50$$

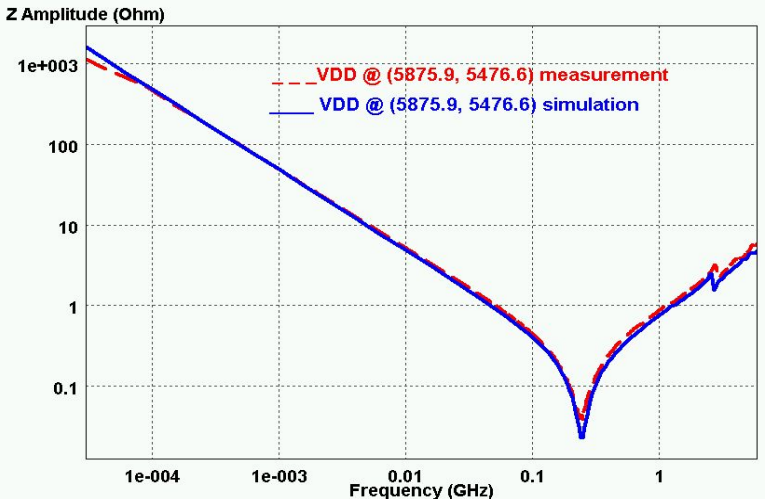
Lab measurement setup

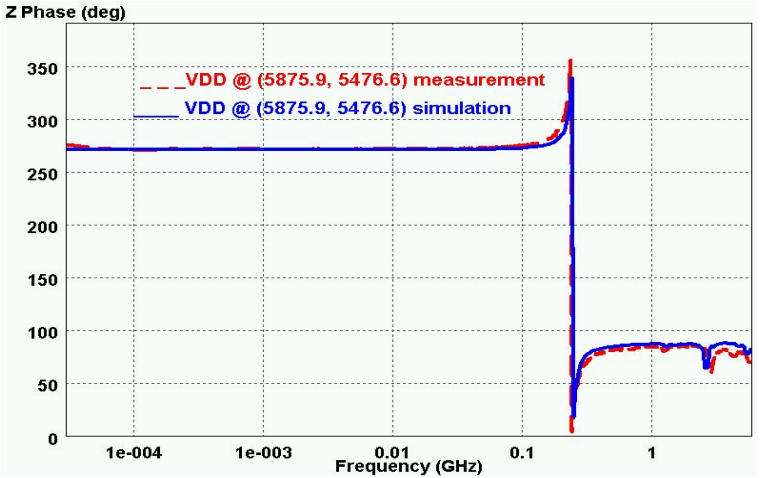


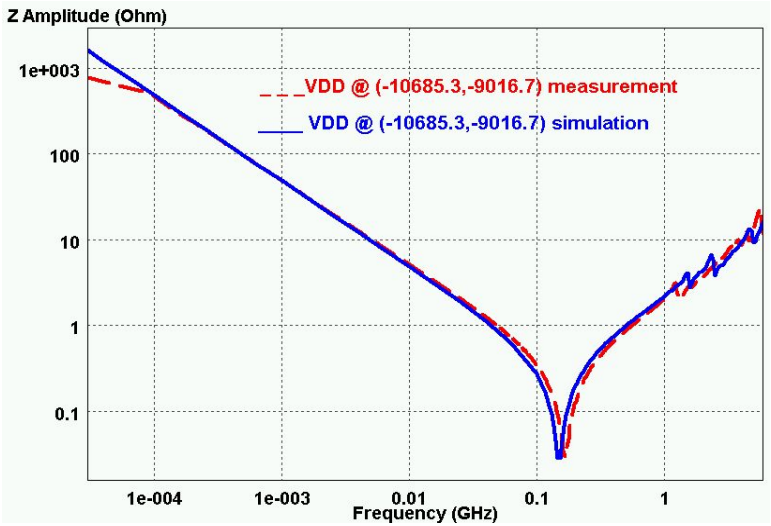


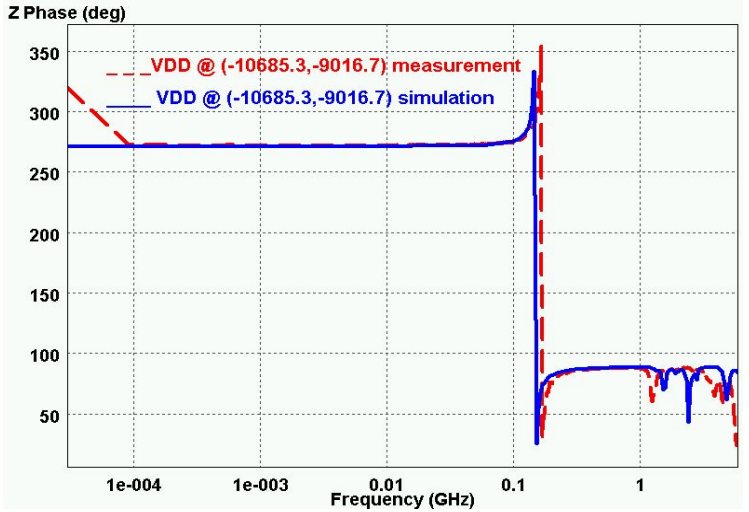
Detailed info about measurement method can be found at
http://home.att.net/~istvan.novak/papers.html

Lab measurement vs simulation









Power decoupling strategy

- Source of power supply noises
- Back to the basic
- A typical power decoupling system

Sources of power supply noises

- Switching current from core logic, memory and IOs
- Coupled noise from signal traces/vias on the package and PCB
- Coupled noise from other power supplies
- Switching power supply source

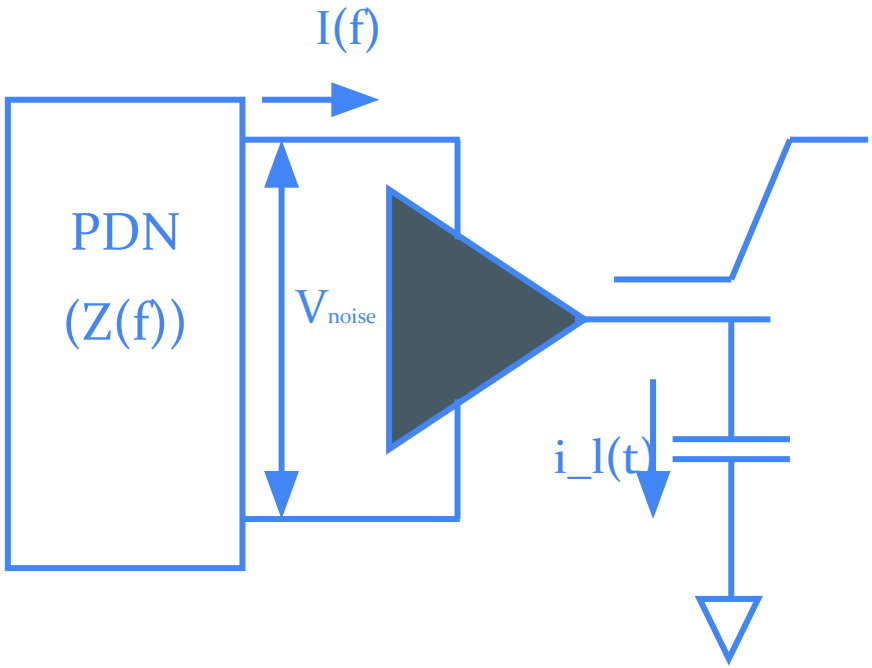
Back to the basic

$$i\_l(t)=C\_load*dV/dt$$

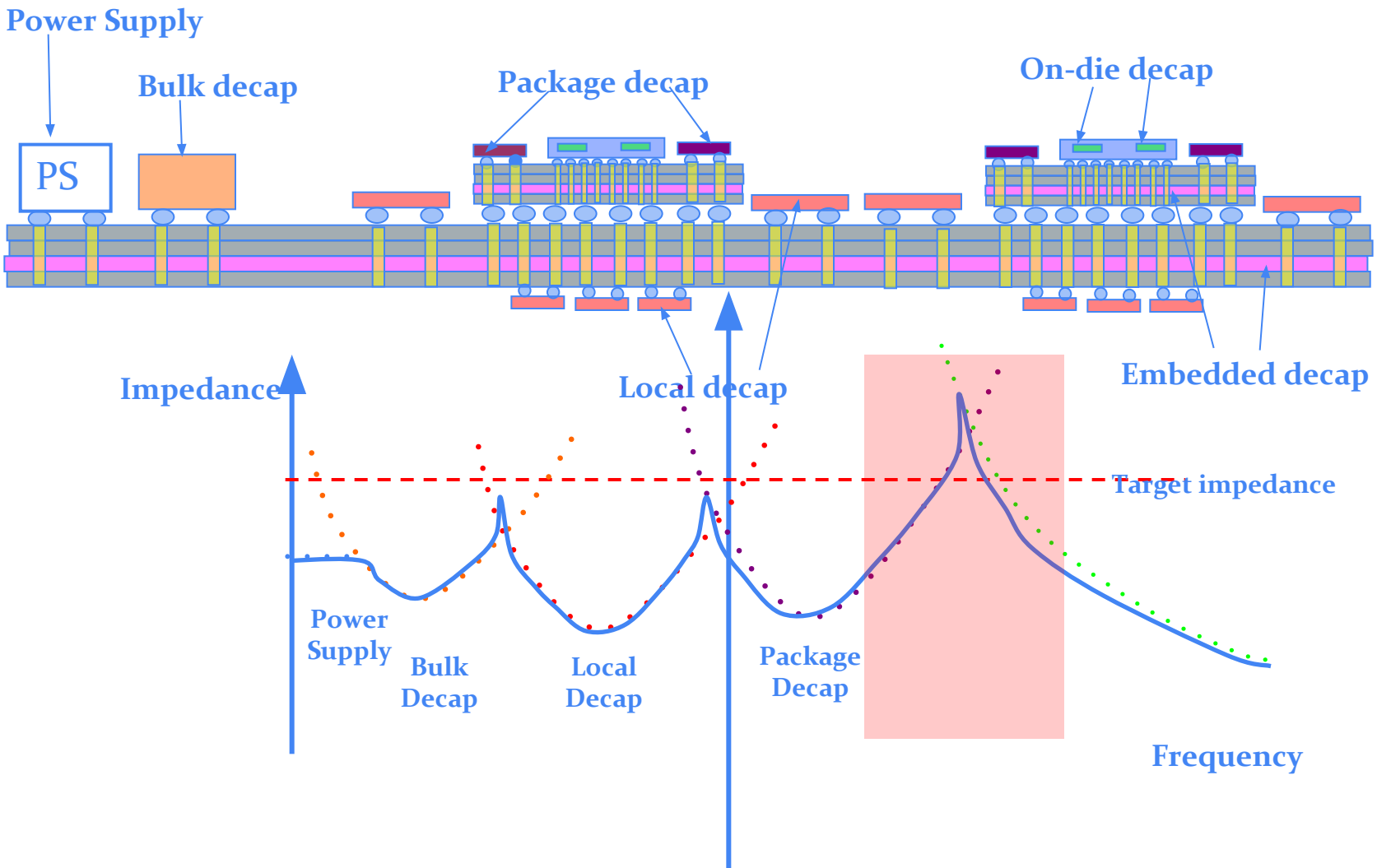
$$Vnoise(f)=I(f)*Z(f)$$

$$Z\_inductor(f)=j*2*pi*f*L$$

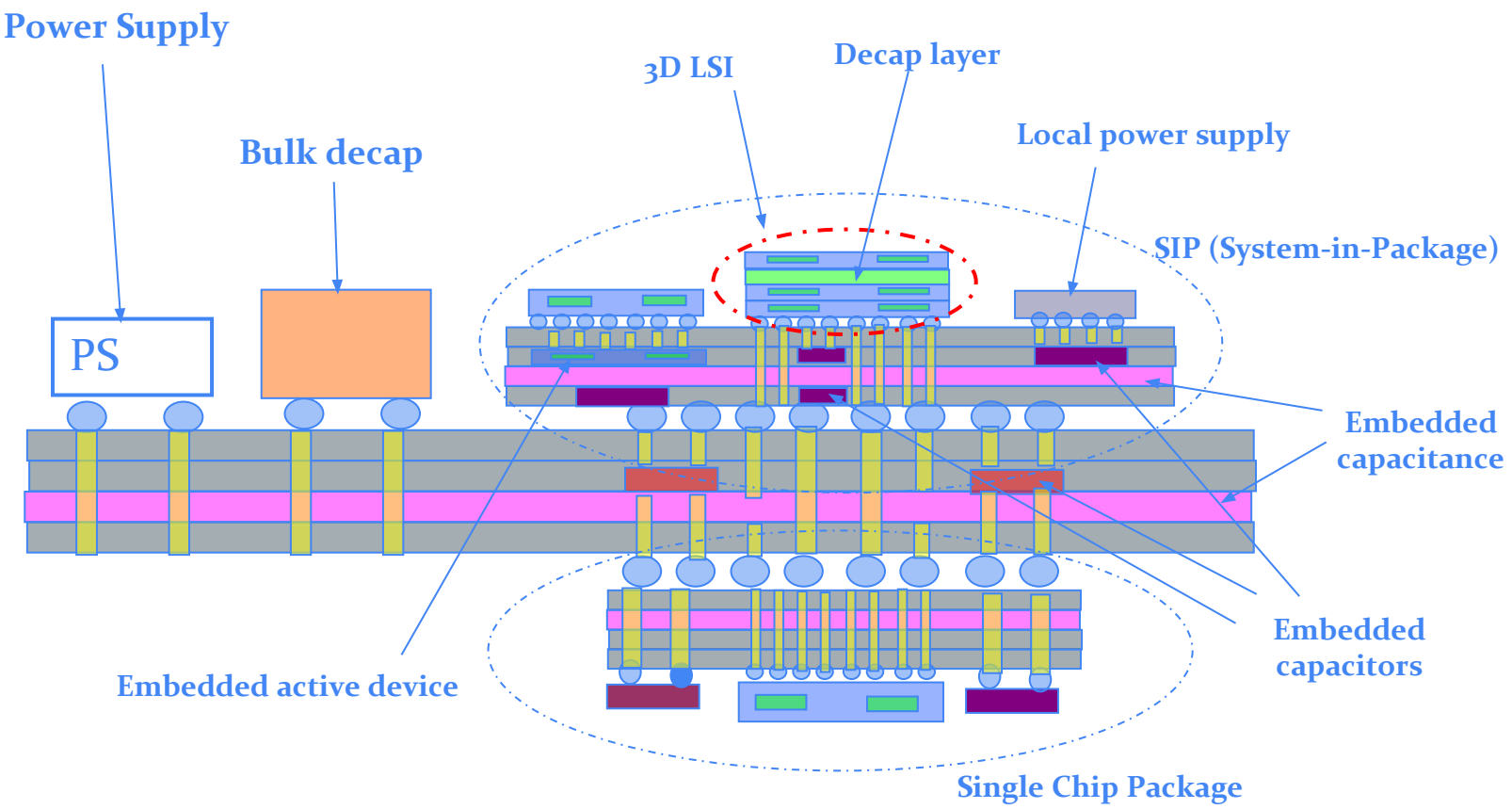
$$Z\_capacitor=-j*C/(2*pi*f)$$



A typical power decoupling system



Future's technology: SIP with embedded technology

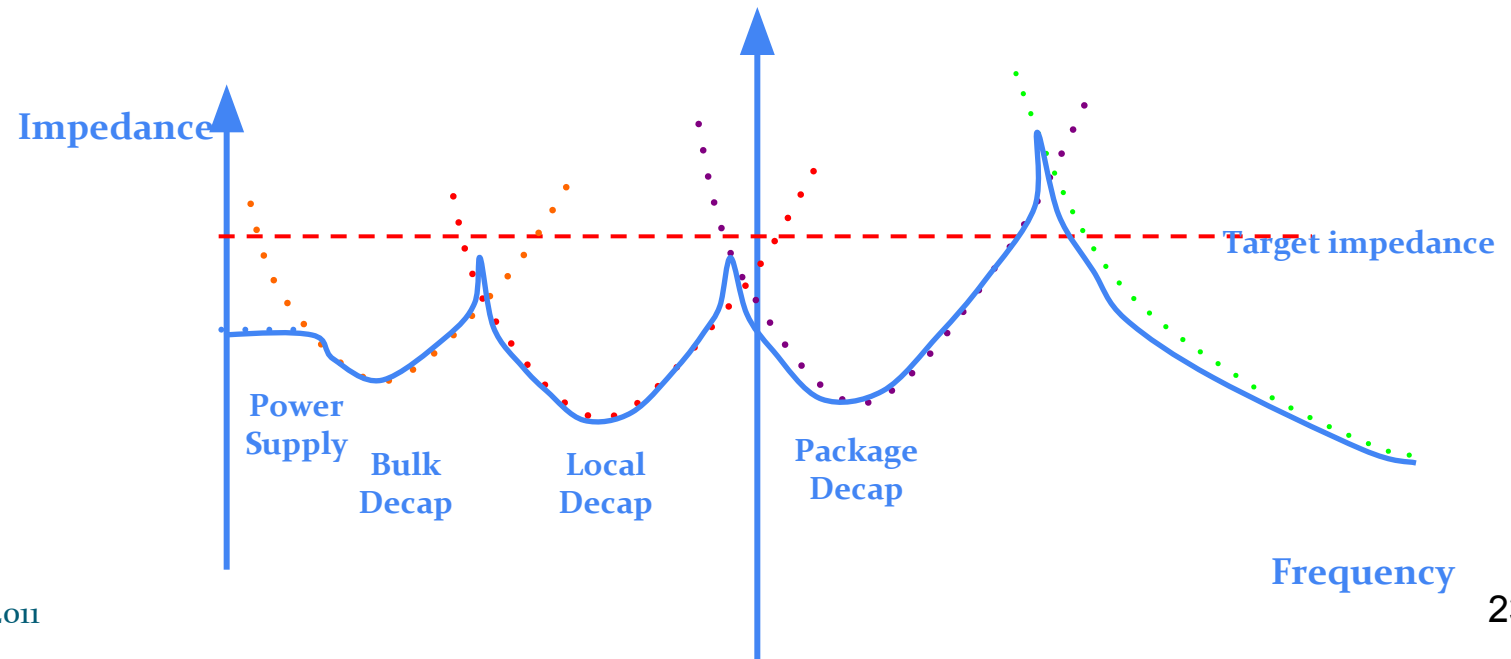


Target impedance

- How to define it?

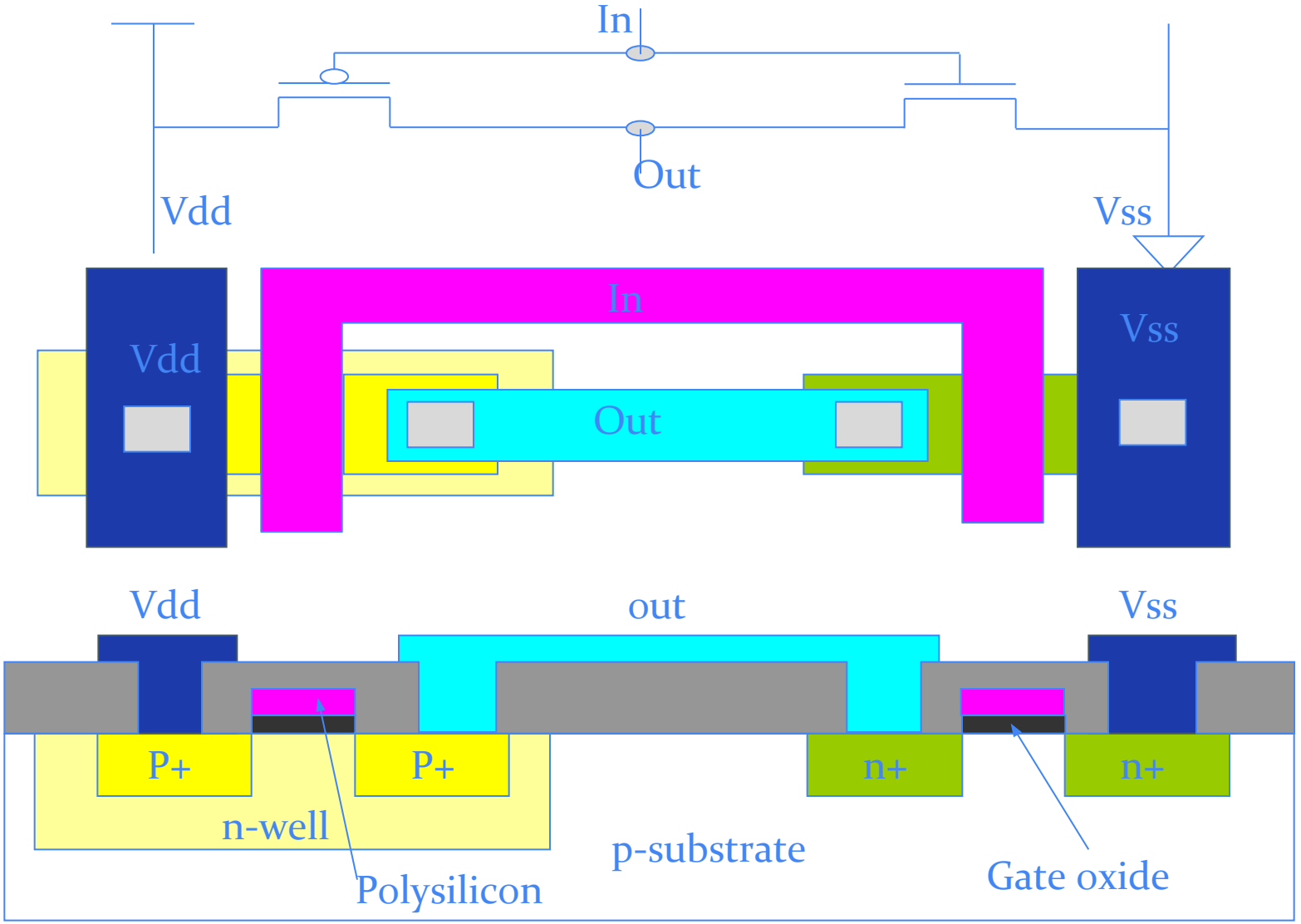
$$Z_T = \frac{\text{Vdd} \times \text{ripple}}{50\% \times I_{\max}} \quad (\Omega)$$

- The pros and cons of target impedance method

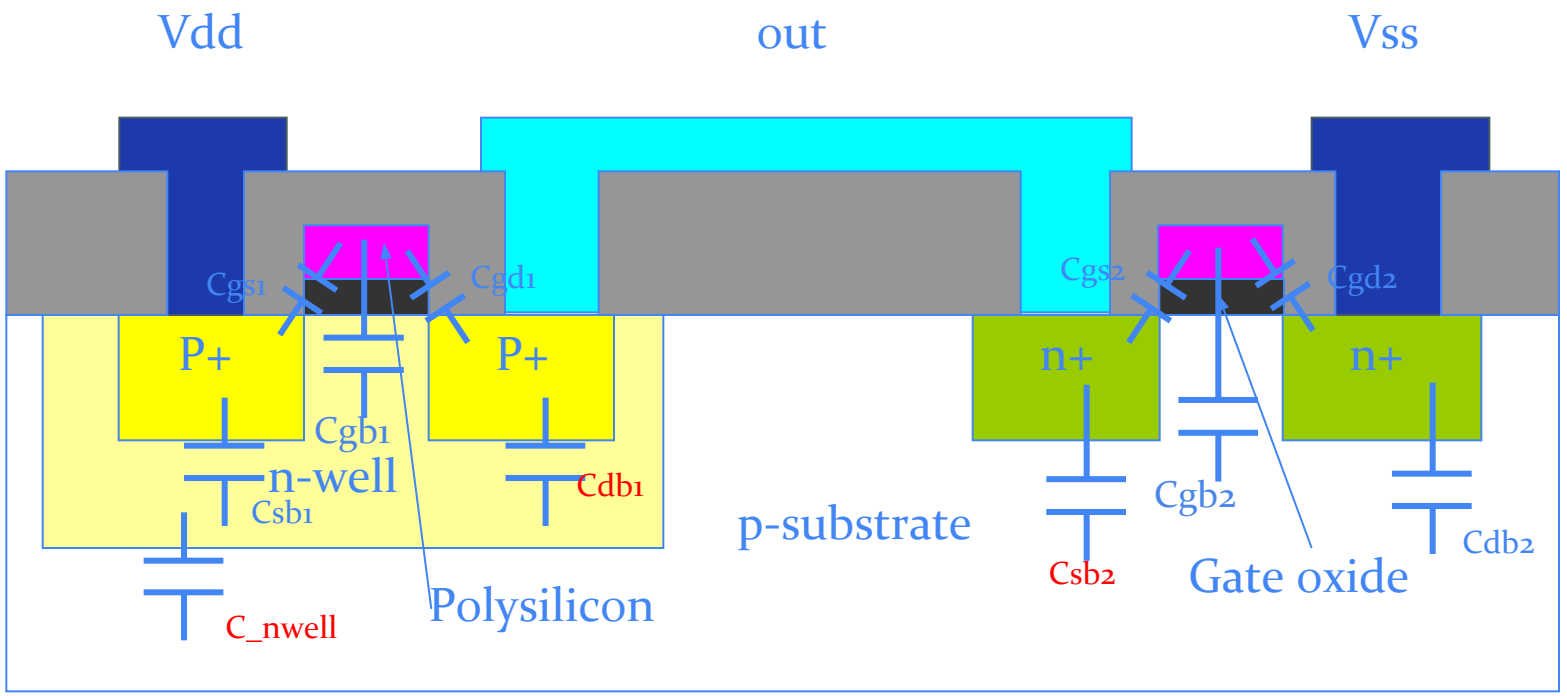


On-Die Power Integrity Analysis

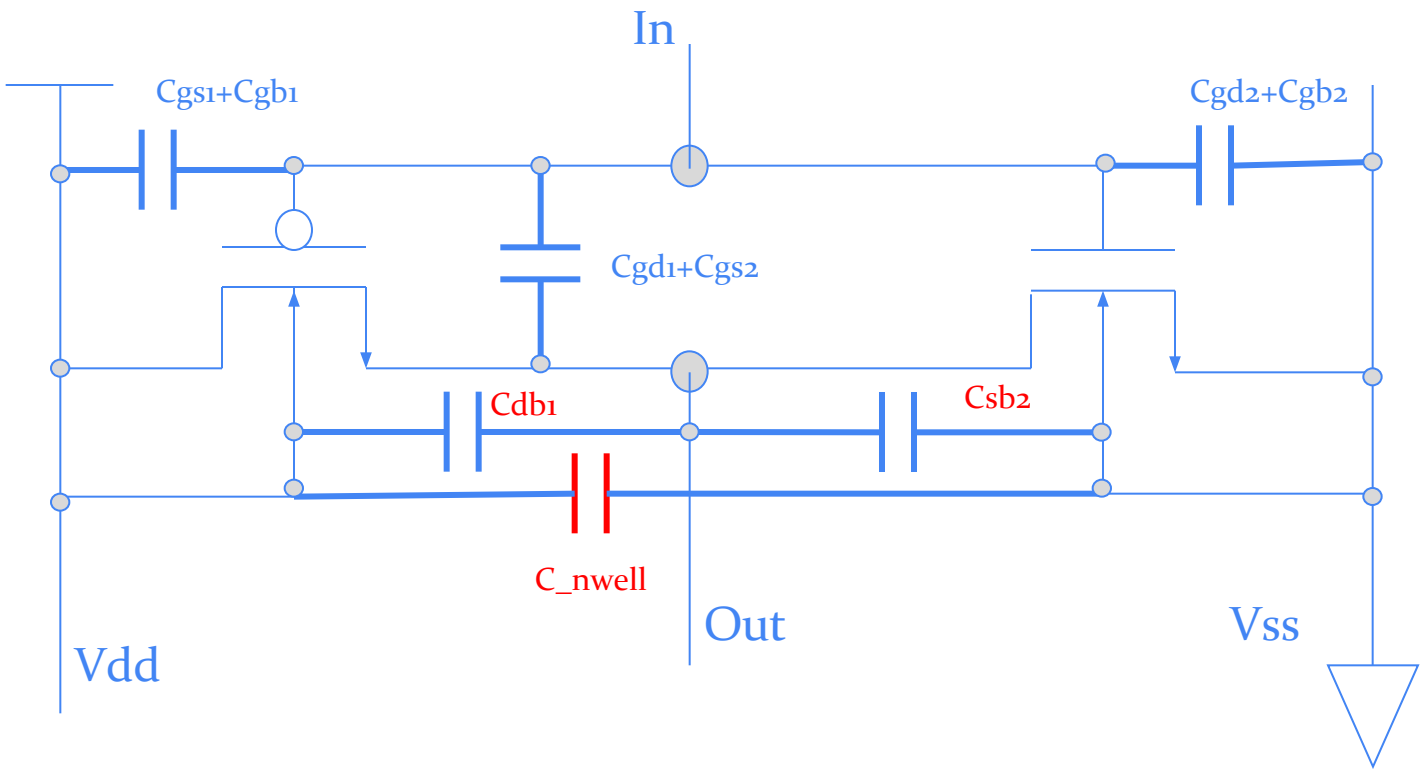
Parasitic capacitance from transistors



Parasitic capacitances on silicon



Capacitance representation in circuit



On-die decap information

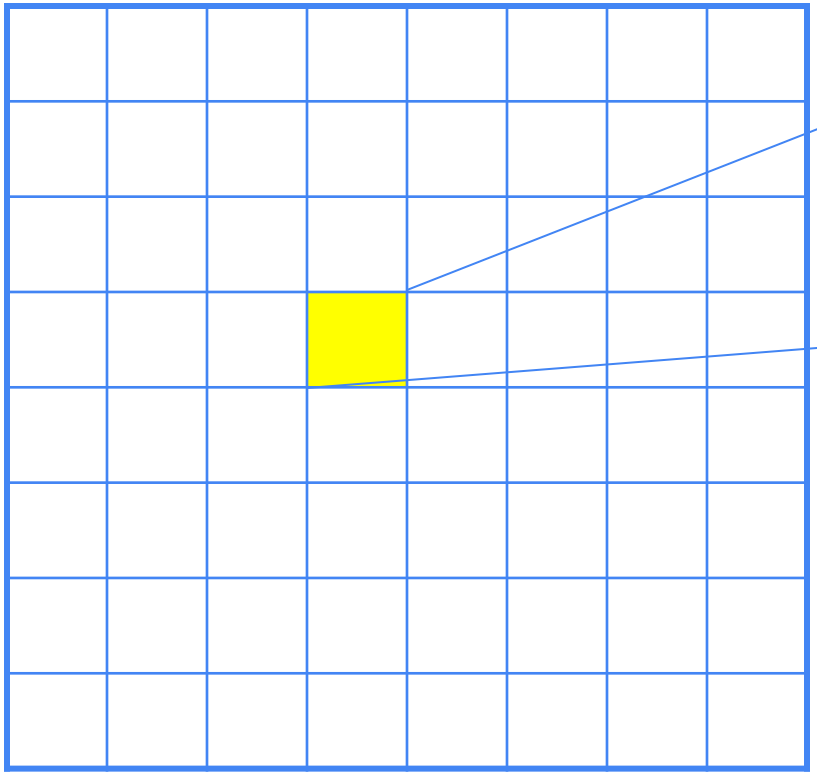
On-die capacitance can come from:

- Gate (Switching noise source)
- RAM (Switching noise source)
- Wire
- N-well
- Decap cells
- Filler cells
- MIM (metal-insulator-metal) capacitor
- MOM (metal-oxide-metal) capacitor

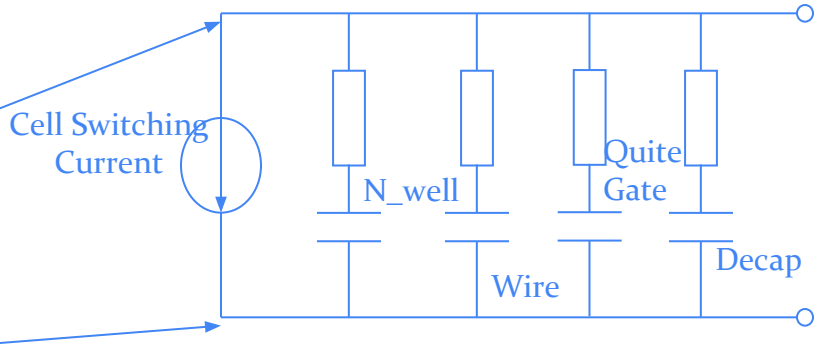
Important parameters for on-die capacitance

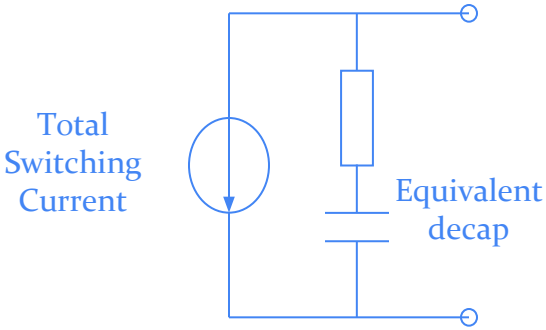
- Decap per gate (state dependant)
- Decap per RAM bit (state dependant)
- N-well decap per core area
- Decap per wire length
- MIM/MOM decap per area

On-die power delivery modeling



Distributed Power Delivery model





Simplified lumped power delivery model

Distributed vs lumped on-die model

- Distributed model

  Good for detailed spatial on-die noise analysis. Useful for on-die decap placement. Long run time; should be limited to on-die study only.

- Lumped model

  Simple and easy to use for system-level analysis. Good enough for on-package and on-pcb decap placement studies.

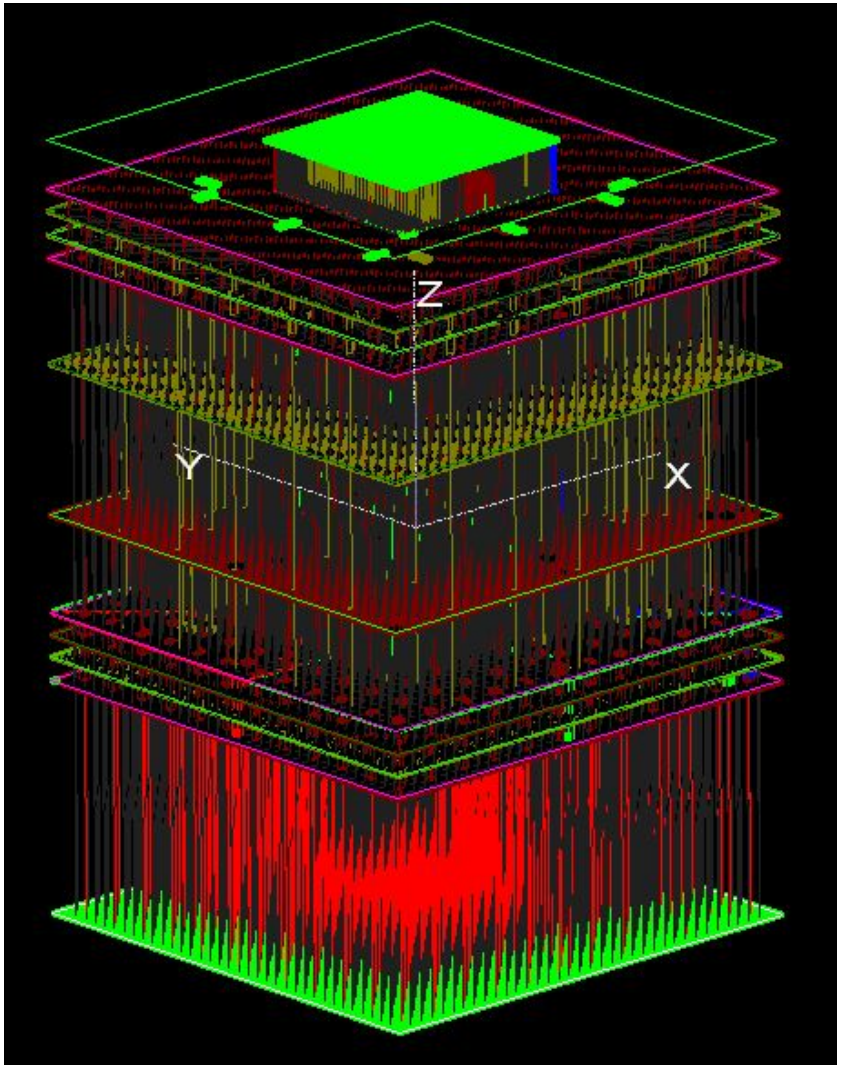
Package-level power integrity analysis

Study and Implementation on package

- Package stackup is optimized for Power Integrity
  - Power/Ground pins are optimized for decap placement on the PCB
  - Design rules are implemented to minimize the IR drop and loop inductance on the package
  - On-package or embedded LICC* Decaps are available
  - Two pins are dedicated for on-die VDD noise measurement
- Complete package models are available for Power Integrity analysis

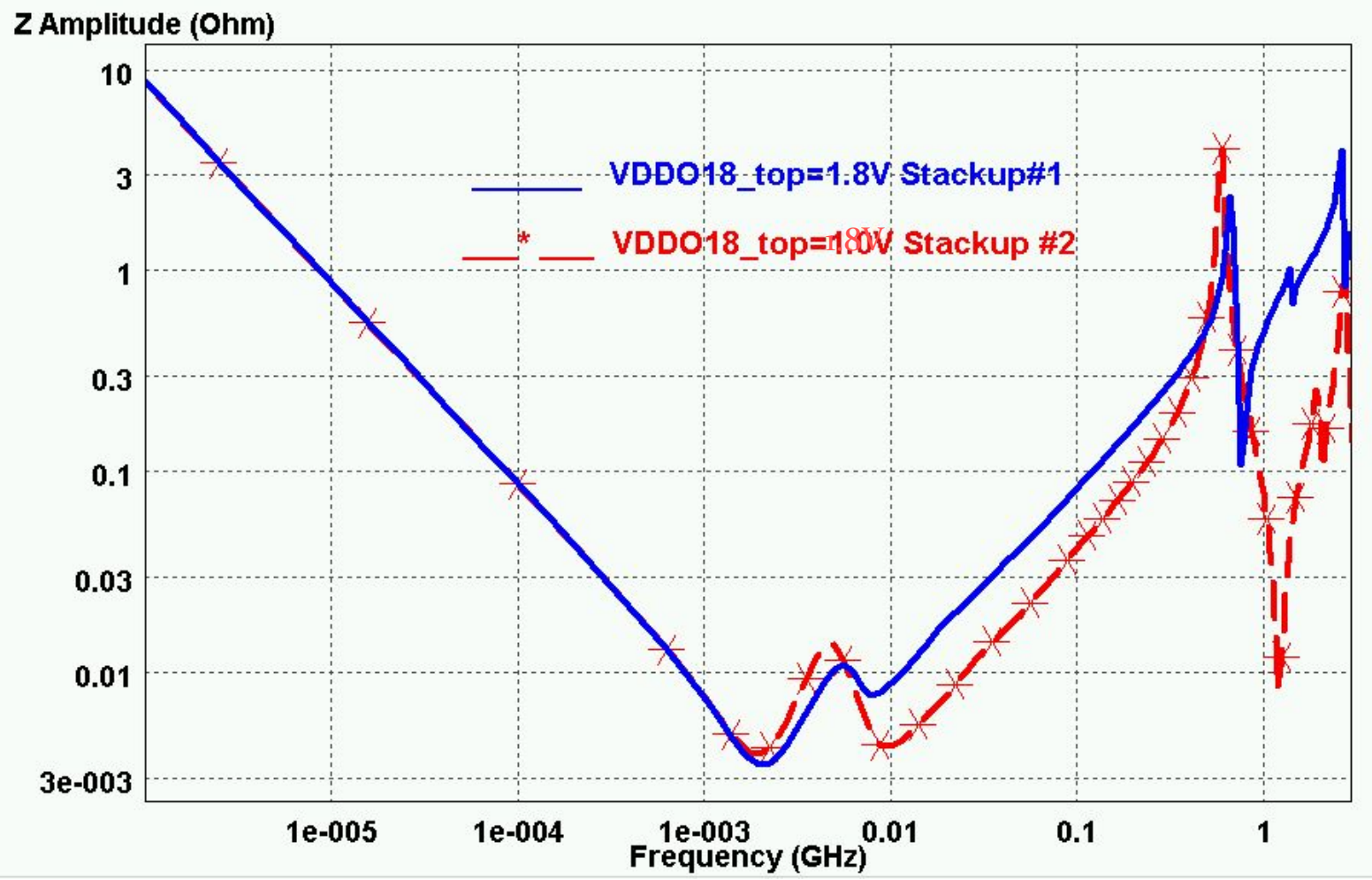
* LICC: Low Inductance Chip Capacitor

Package Stackup

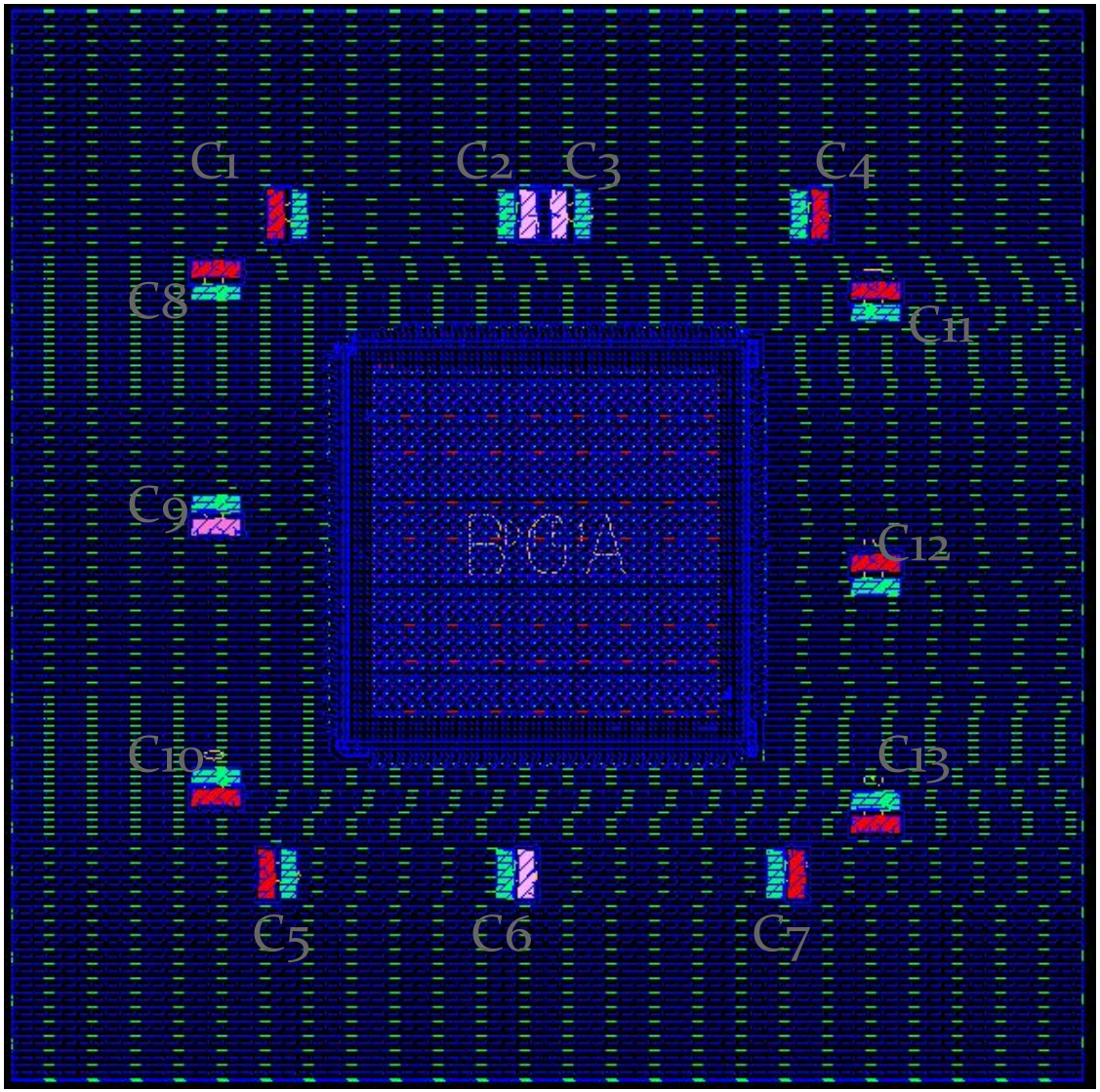


Layers	Thickness	Material	Loss tangent (1Ghz)	Dieletric Constant	Via/Plane Conductivity (S/m)
Underfill layer	70um	HLU1/ 63/37 Sn/Pb	0.0123	3.92	5.88E+06
Solder Maskr	25um	Build up	0.012	4.3	5.88E+06
Layer 01	15um	ED Copper			4.48E+07
Dieletric 01	35um	Build up	0.022	3.5	4.48E+07
Layer 02	15um	ED Copper			4.48E+07
Dieletric 02	35um	Build up	0.022	3.5	4.48E+07
Layer 03	15um	ED Copper			4.48E+07
Dieletric 03	35um	Build up	0.022	3.5	4.48E+07
Layer 04	18um	ED Copper			4.48E+07
Dieletric 04	200um	BT	0.013	4.7	4.48E+07
Layer 05	35um	ED Copper			4.48E+07
Dieletric 05	300um	BT	0.013	4.7	4.48E+07
Layer 06	35um	ED Copper			4.48E+07
Dieletric 06	200um	BT	0.013	4.7	4.48E+07
Layer 07	18um	ED Copper			4.48E+07
Dieletric 07	35um	Build up	0.022	3.5	4.48E+07
Layer 08	15um	ED Copper			4.48E+07
Dieletric 08	35um	Build up	0.022	3.5	4.48E+07
Layer 09	15um	ED Copper			4.48E+07
Dieletric 09	35um	Build up	0.022	3.5	4.48E+07
Layer 10	15um	ED Copper			4.48E+07
Solder Maskr	25um	Build up	0.012	4.3	5.88E+06
Solder Ball	480um	Air/ 63/37 Sn/Pb	0	1	5.88E+06

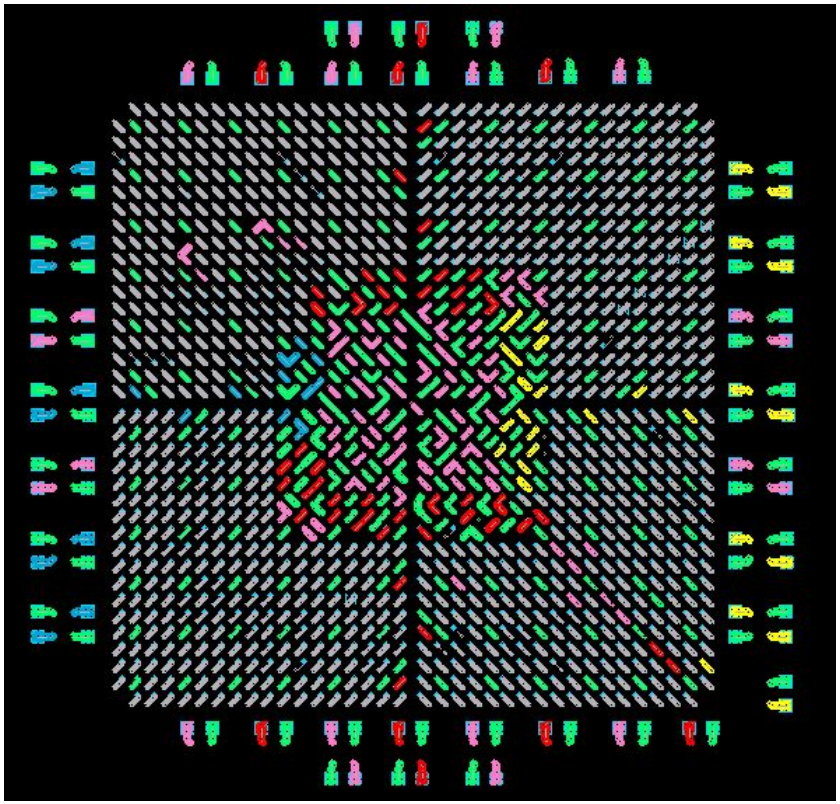
PCB stackup impact on VDDIO



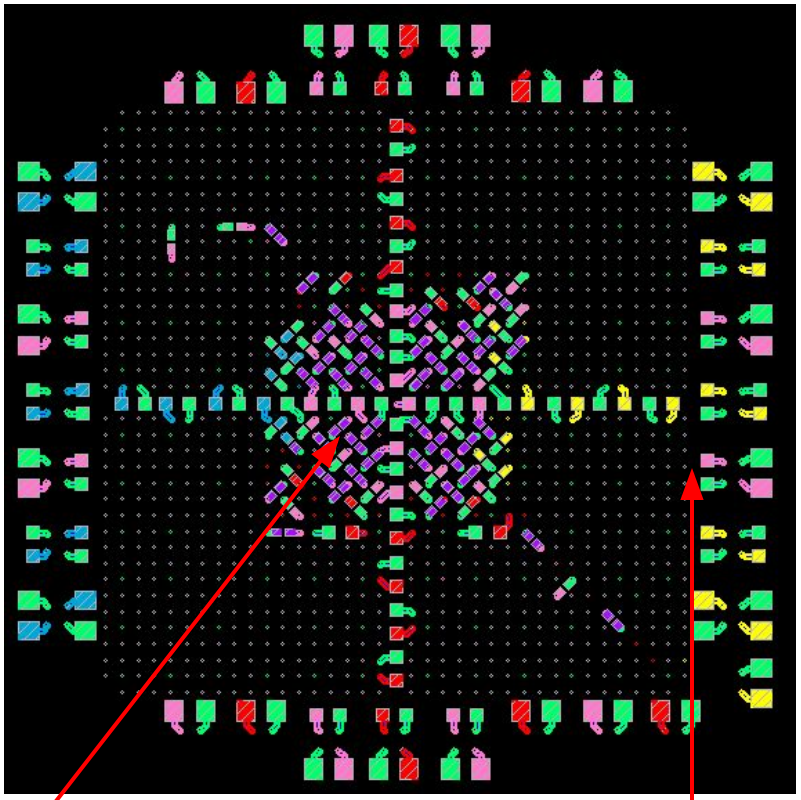
On-package LICC decaps are available



Power/GND pins are optimized for 0402 and 0603 decap placement on PCB



Top

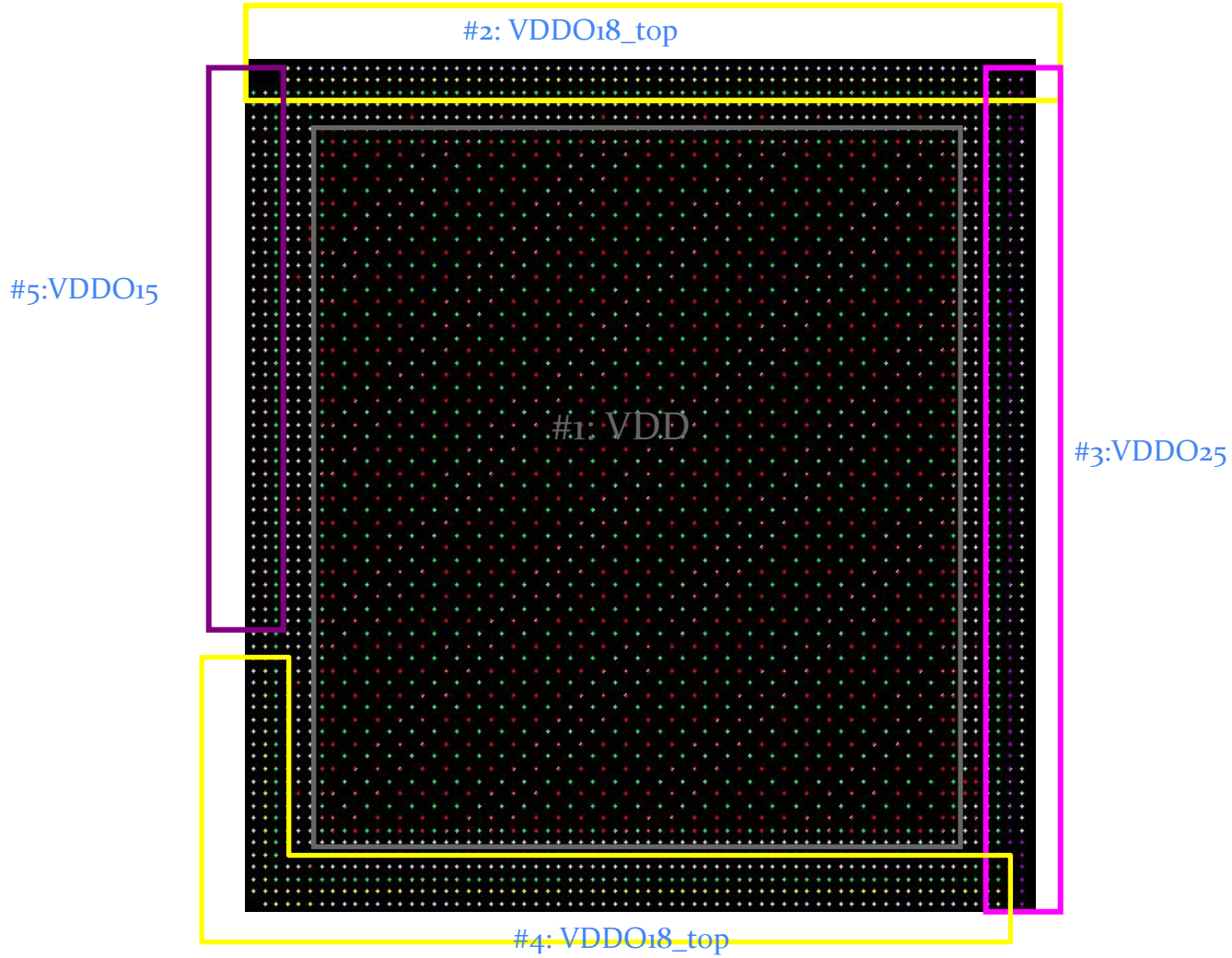


Bottom

Complete package model for power integrity analysis

- Extracted the S-parameters of the complete package model
- Package model only includes power and ground nets
- The “ports” are defined at the *bump*, *pin* and *on-package decap* pads

Port locations



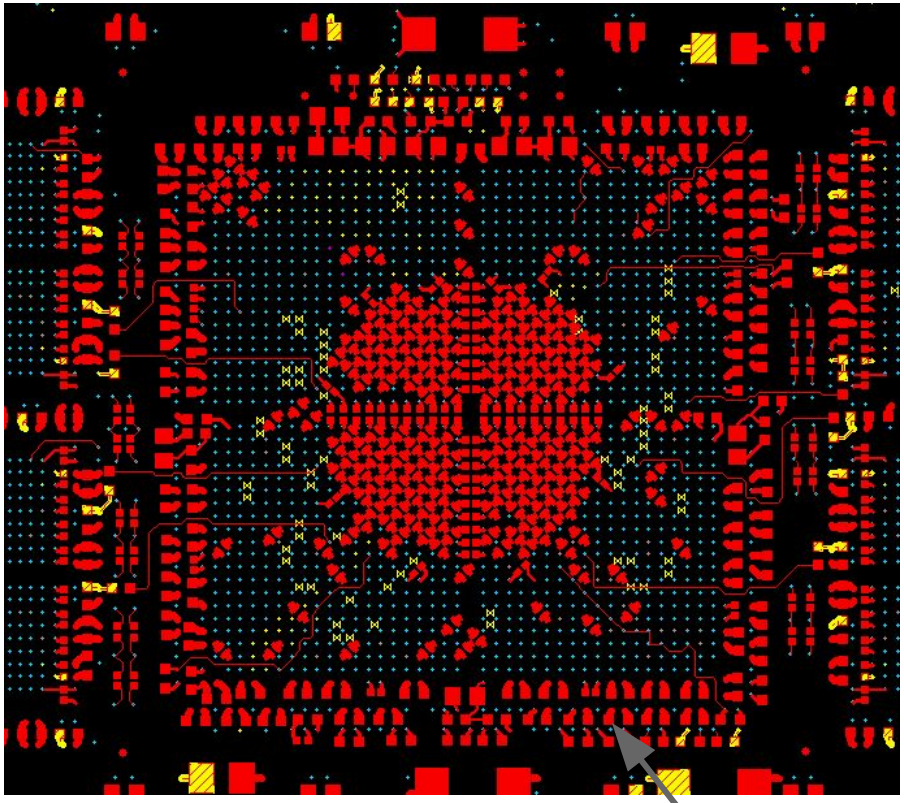
Package electrical performance

Net name	C_pkg	R_bump_ball at 1KHz	R_bump_ball at 100MHz	L_bump_ball (pH)	Resonant frequencency
VDD	3.46nF	9.71E-05	2.12E-04	6.42	1.15GHz
VDDIO18_top	0.275nF	8.04E-04	1.78E-03	37.5	1.50GHz
VDDIO25	0.286nF	8.34E-04	1.85E-03	43.1	1.37GHz
VDDIO18_bot	0.404nF	5.37E-04	1.31E-03	23.45	1.46GHz
VDDIO15	0.169nF	1.25E-03	2.67E-03	60.08	1.63GHz

Study and Implementation on PCB

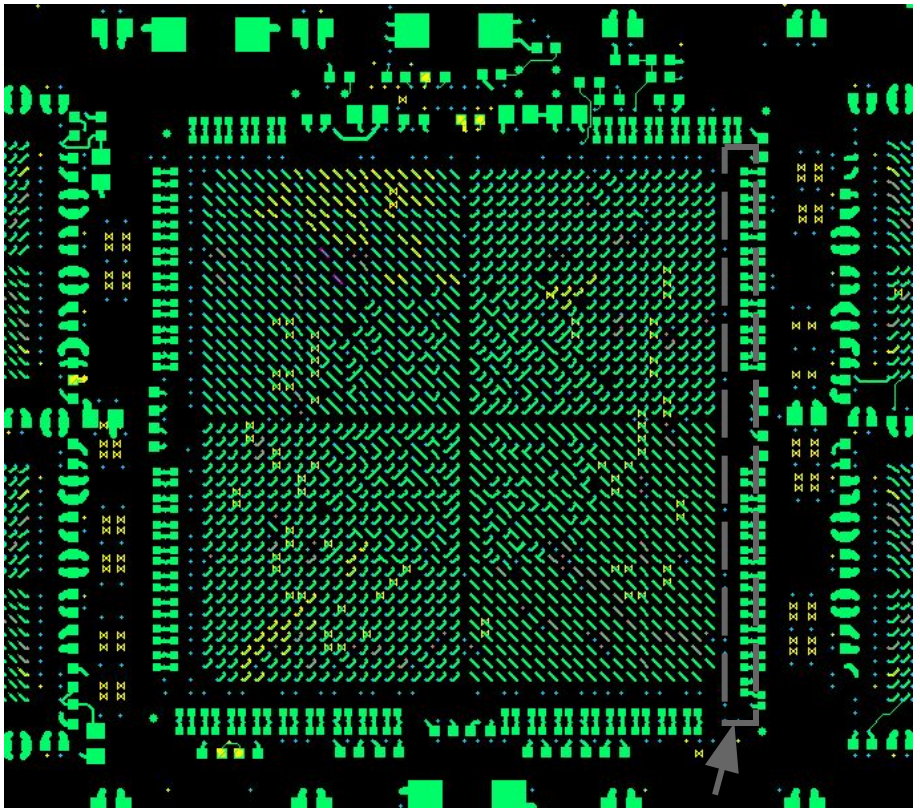
- PCB stackup is optimized for Power Integrity
- 45 degree 0402 decaps are placed under BGA
- Extensive simulations are performed to optimize the decap placement
- Additional decap pads are placed for lab debug

Decap placement on PCB



Bottom

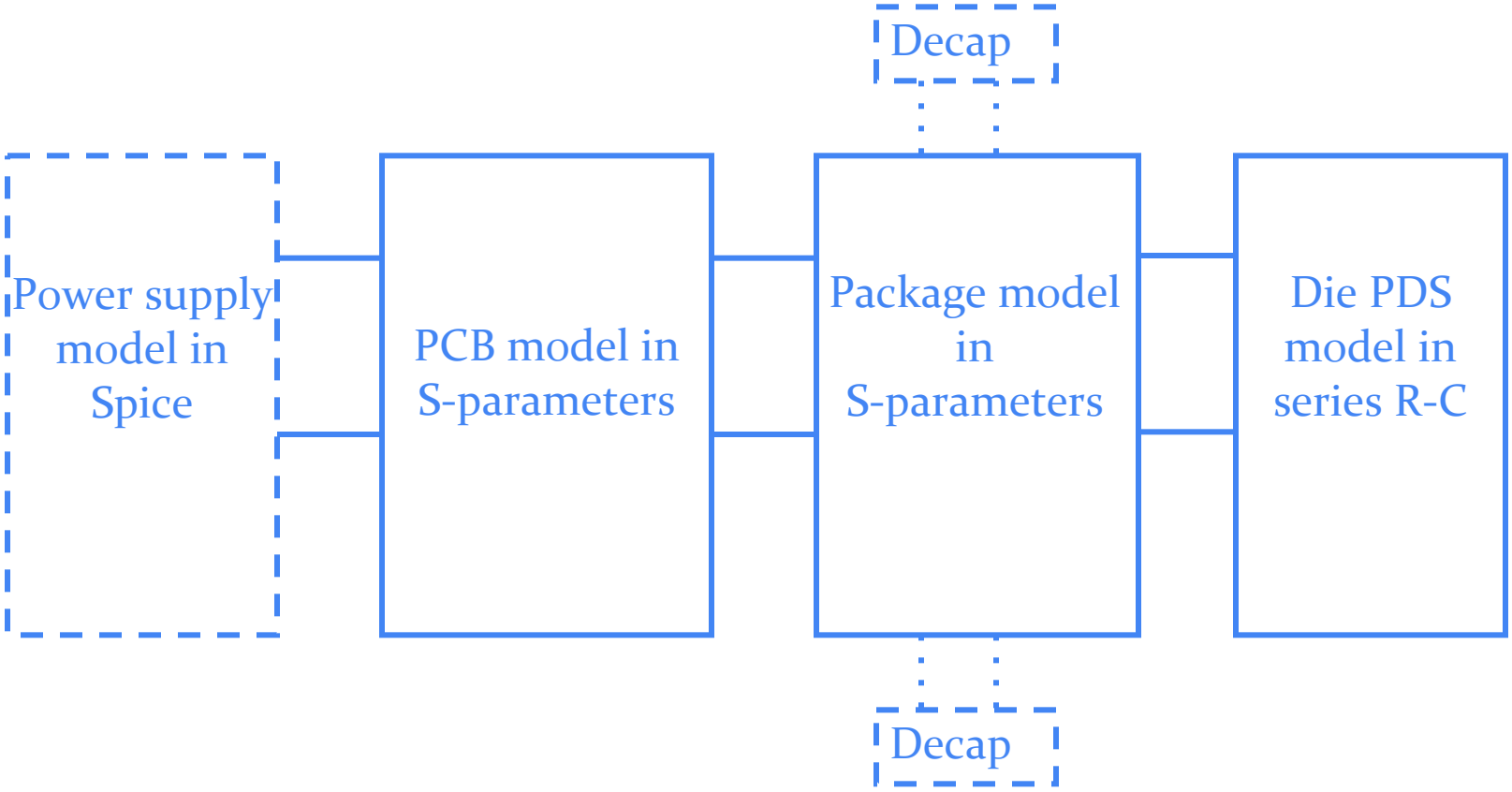
More decaps are placed than needed in the simulations



Top

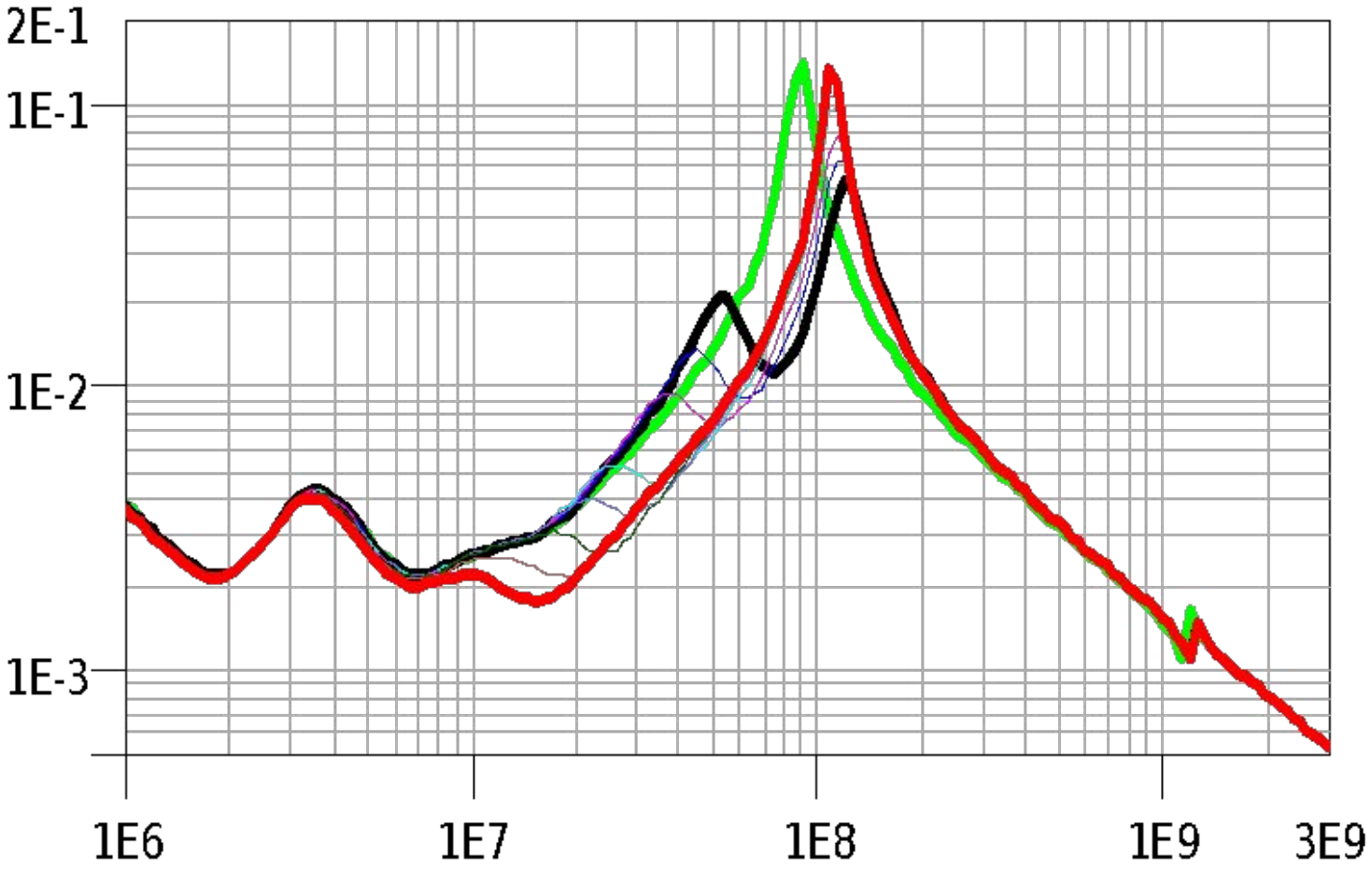
Cap pads for debug purpose

Die/Package/Board co-design methodology



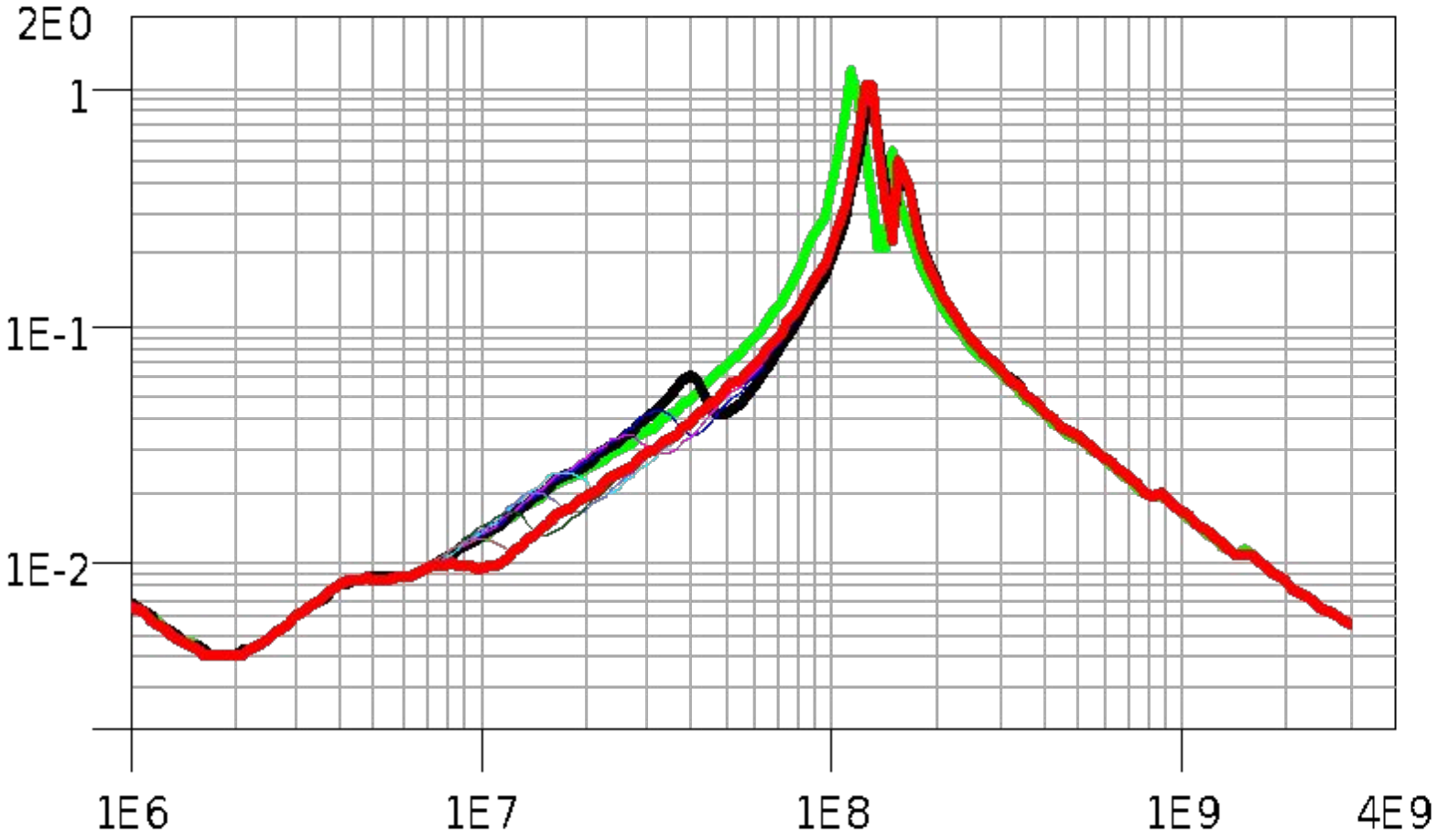
Package decap impact on VDD

Assume on-die C_VDD=100nF and R_VDD=1e-4



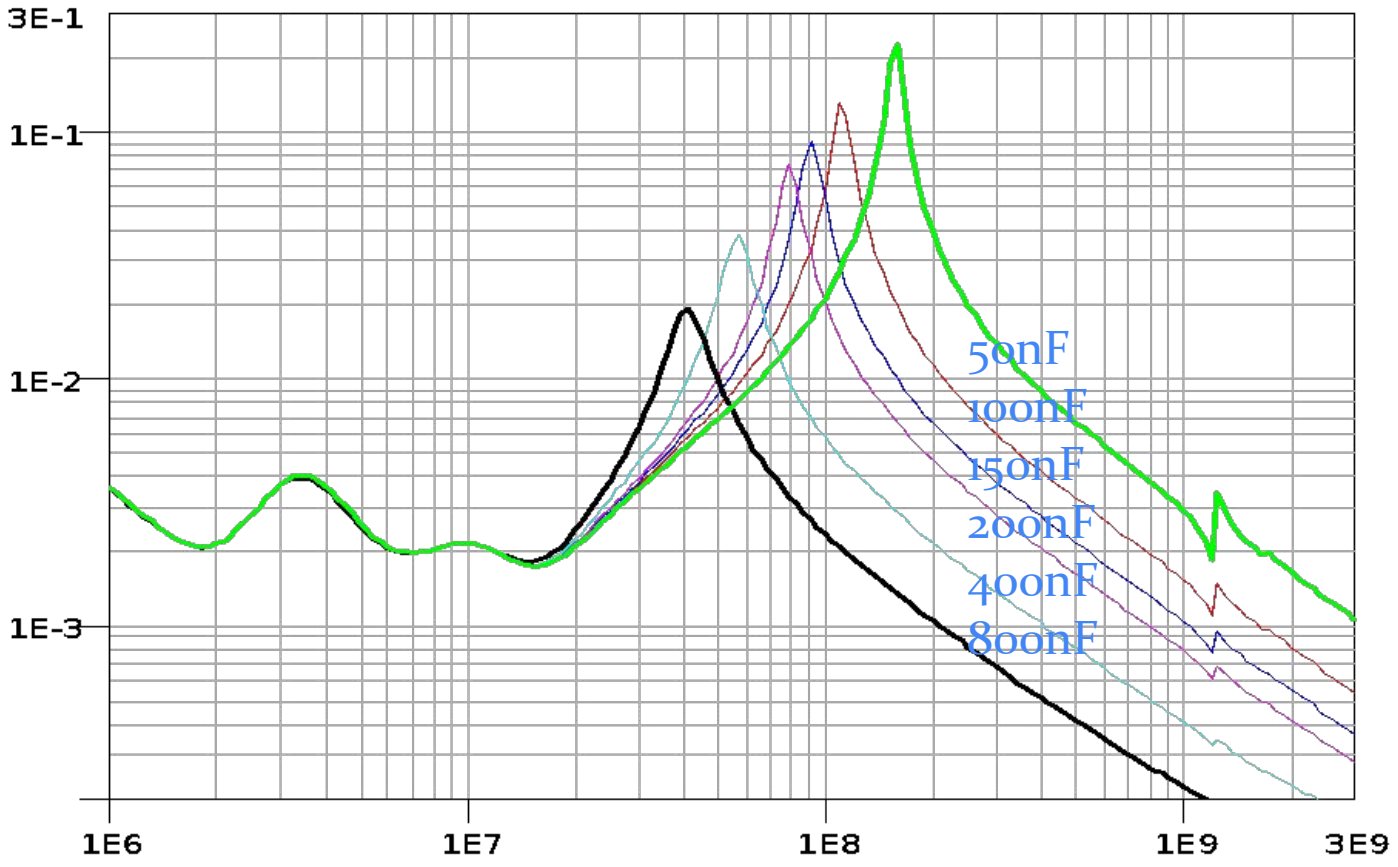
Package decap impact on VDDO18

Assume on-die C_VDDO18_top=10nF and R_VDDO18_top=1e-3



On-die decap impact on VDD

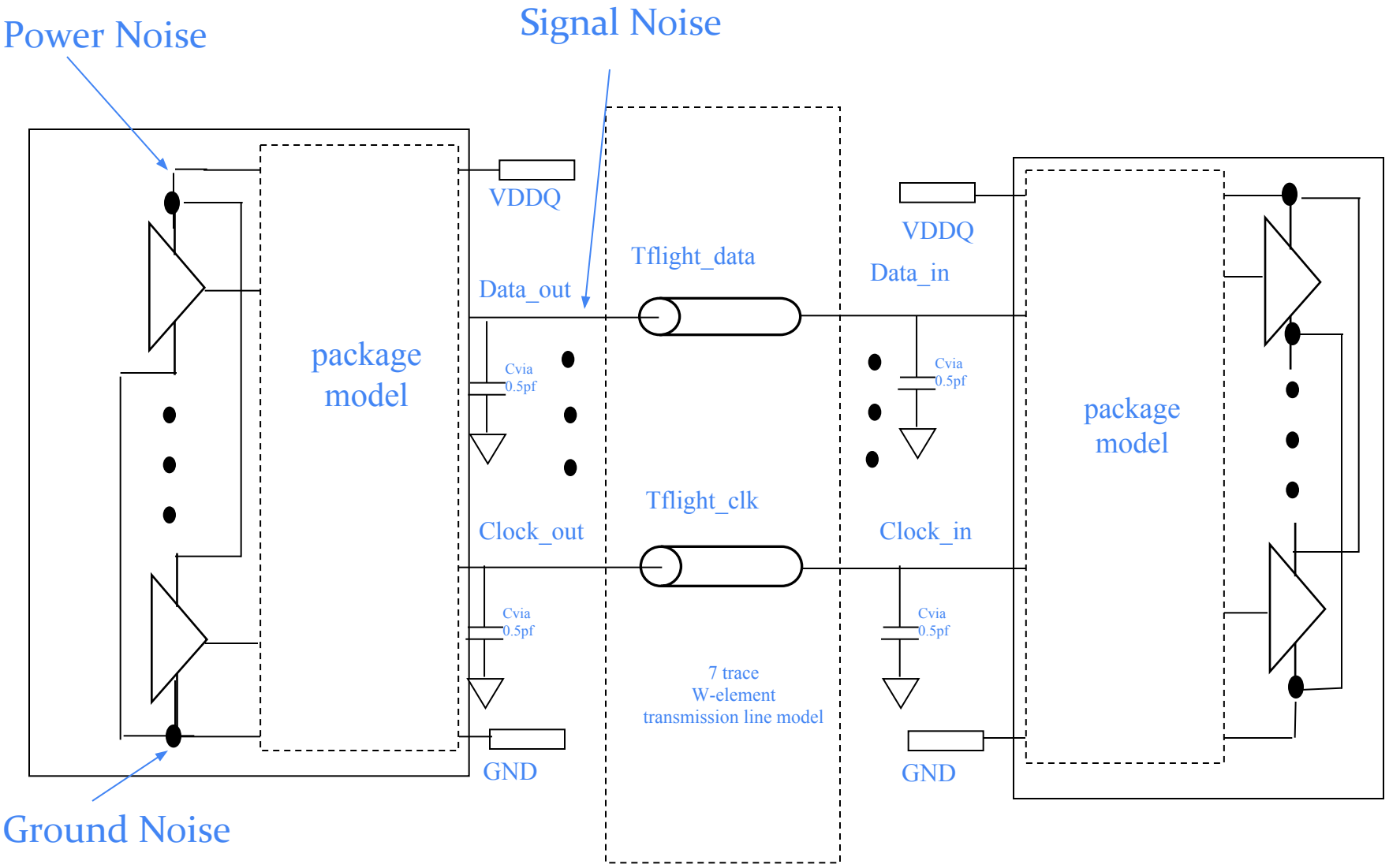
Assume all package decap are filled with 0.22uF decap and the on-die decap ESR=0.1mOhm



Power integrity simulation for inter-chip high-speed interfaces

- Power noise can introduce additional jitter and timing penalty which can reduce eye diagram and setup/hold of high-speed interface.
- Severe power noise can cause abnormal clock glitches and functional failures.
- The end-to-end SI/PI co-simulation and timing/eye diagram analysis are recommended for this type of interfaces.

Typical SSO/SSI noise simulation



Open topics and Q&A

Thank you