Power Integrity Concepts for High-Speed Design on Multi-Layer PCBs

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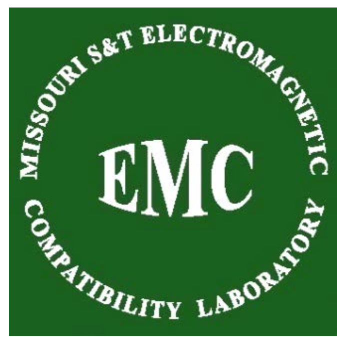
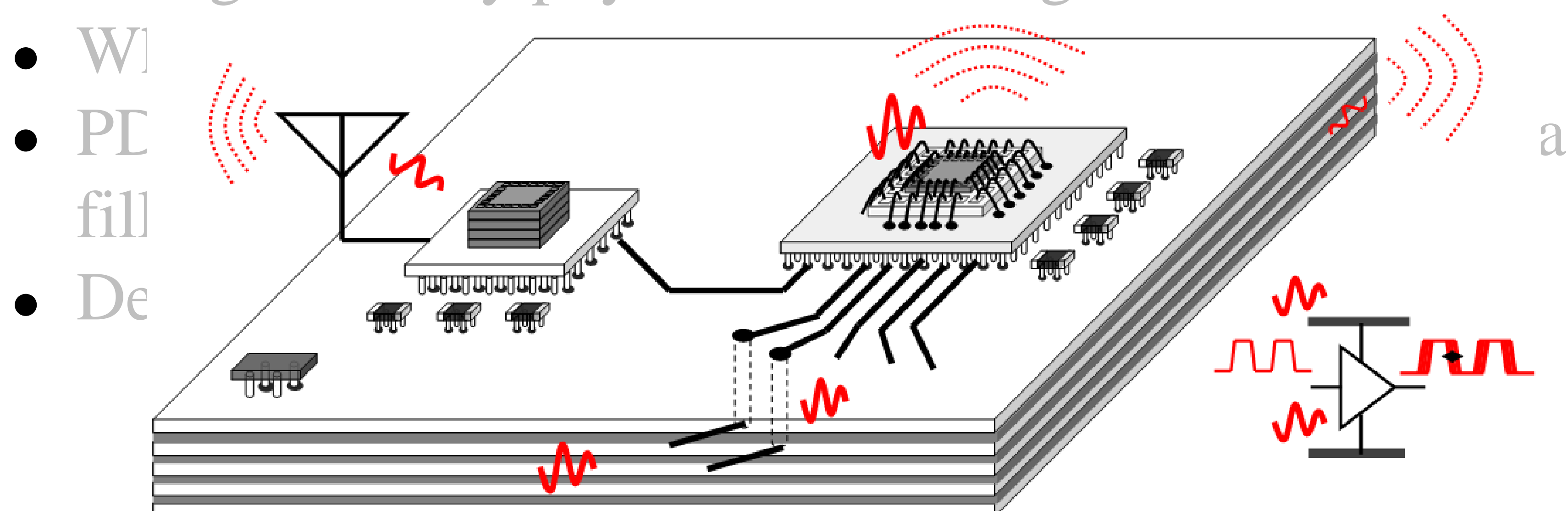


PI Module – Physics

- The PDN problem and some preliminaries
  - What PI design impacts
  - Design choices
  - A quick reminder of
    - circuit element behavior with frequency
    - current physics
- Charge delivery physics for PI design



PDN Problem

High-speed, integrated, and mixed electronic system

IC EMI source model?

PKG

3D IC

IC Die

Power Distribution Network

Decap

VRM

Jitter

Effect of PDN noise on I/O jitter

Power Distribution Network

- VRM
- Decoupling capacitors
- Power net area fills

Geometry and Inductance Decomposition

Silicon Die

GND1
GND2
GND3
PWR
GND4
GND5
GND6

L_{above}

L_{PCB_Decap}

L_{PCB_IC}

L_{PCB_Plane}

L_{PCB_Decap}

L_{PCB_Decap}

L_{above}

L_{above}

Voltage

VDD

V_{ripple}

Time

$|Z_{PDN}|$

C_{Decap}

L_{PCB_EQ}

C_{Plane}

L_{PCB_IC}

Frequency

PCB PDN Design Considerations

2a. Decoupling capacitors
- top
- bottom,
- beneath IC?

2b. Decoupling capacitor connection -
- PWR/GND via geometry
- Package size

IC

Decaps

1. Power plane(s)
   - location in stack
   - spacing to power return plane
   - total area fill
   - special materials

2a. Decoupling capacitors
- value(s)
- Number (total C)

IC pins

Effect of other ground/reference planes?

2c. Decoupling capacitor layout
- How close to IC?
- Shape – ring IC, on one side?

3. IC PWR/GND
- Number pins
- pin pattern
- Pitch
- on-package decaps

PWR

GND

Reminder – Circuit Model Behavior with Frequency

$|Z|(dB\Omega)$

$-\frac{20dB}{decade}$

$\log_{10} f$

$|Z|(dB\Omega)$

$-\frac{20dB}{decade}$

$+\frac{20dB}{decade}$

$\log_{10} f$

$|Z|(dB\Omega)$

$+\frac{20dB}{decade}$

$\log_{10} f$

$|Z|(dB\Omega)$

$+\frac{20dB}{decade}$

$-\frac{20dB}{decade}$

$\log_{10} f$

Reminder: Current Behavior

Conduction current – carried by electrons $\vec{J}_{cond} = \sigma \vec{E}$ → impeded by

Displacement current – carried by $\vec{J}_{displ} = \varepsilon \frac{d\vec{E}}{dt}$ → admitted by

Signal

GND

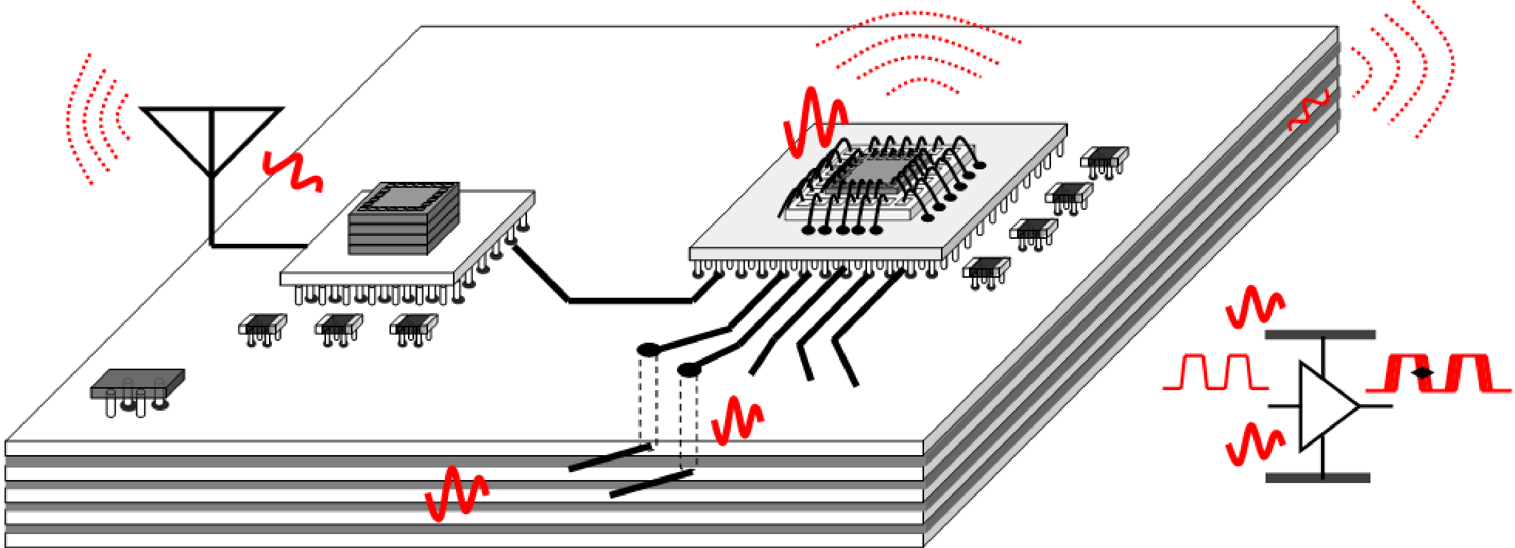
- +

Current on a line for high-speed data

Model with lumped elements if geometry electrically short

PI Module – Physics

- The PDN problem and some preliminaries
- Charge delivery physics for PI design
- Why Z_{target} is used – an FPGA example
- PDN design – multi-layer PCBs with power layer area fills
- Design flow for package/PCB PI co-design

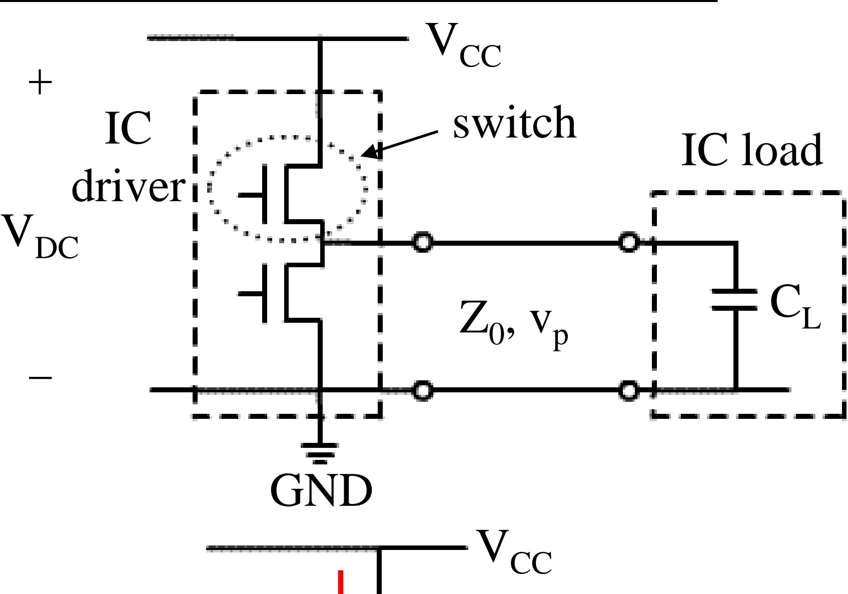


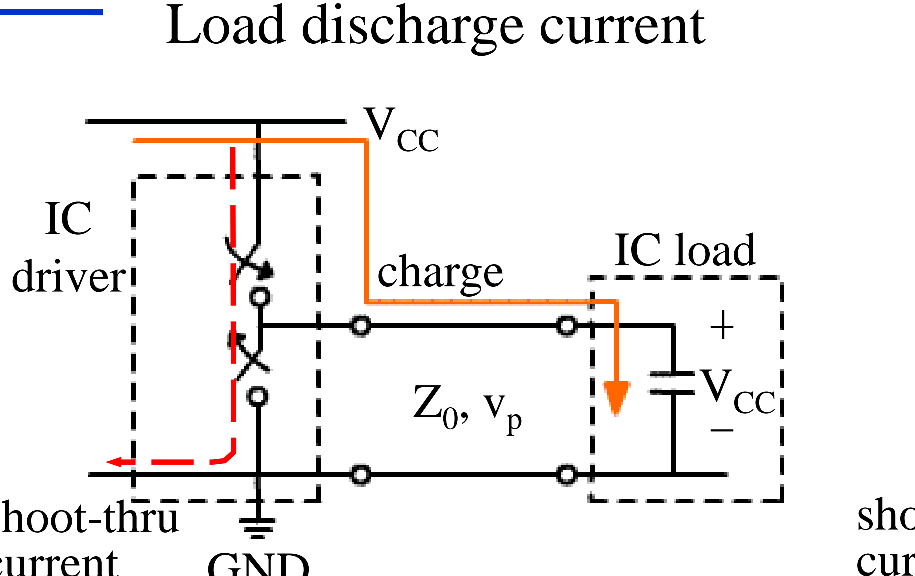
Logic Transitions and Current Draw

Shoot-thru current (and everything else we can't account for)

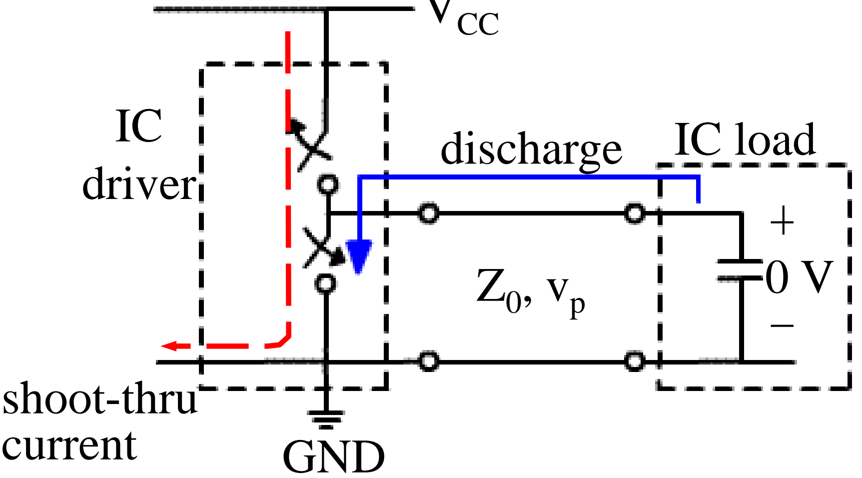
Load charging current

Load discharge current





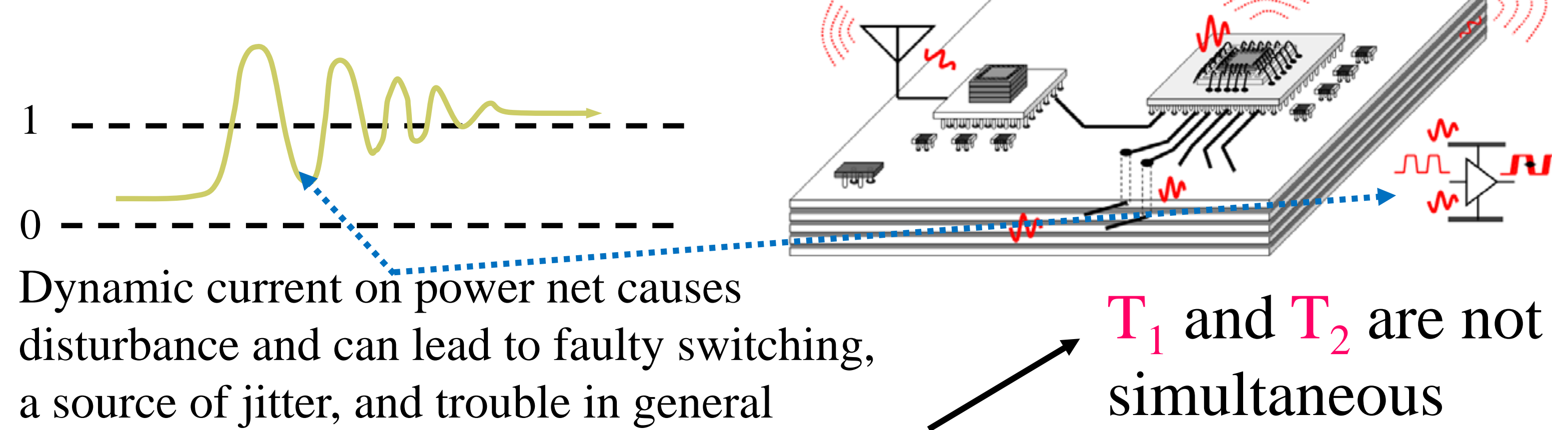
LO to HI



HI to LO

This charge to support IC switching must be provided by the PDN – package, PCB

Voltage Switching/Dynamic Current Draw Distrubances



Dynamic current on power net causes disturbance and can lead to faulty switching, a source of jitter, and trouble in general

T_1 and T_2 are not simultaneous

banks of transistors for the PMOS and NMOS not perfectly synchronized

V_{PWR}

+

$V_{PWR}+V_{Noise}$

–

GND

T_1

T_2

IC driver

charging current

IC load

+

V_{CC}

–

shoot thru current a trouble-maker

v_L

i_{logic}

i_{IC}

i_{st}

The Objective and Guiding Physics: Conduction Current Path results in Inductance

Looking from the IC

Top decoupling capacitors

Decoupling capacitors sharing IC vias

Bottom decoupling capacitors

The Objective and Guiding Physics: Condution Current Path results in Inductance

Key Point – Current Path and Inductance

Four contributions (current path pieces) to the Z_{PDN} inductance

Looking from the IC

Top decoupling capacitors

IC

Above PCB to decaps

caps-to-PWR planes

$Z_{PCB-in}(j\omega)$

GND

GND

GND

GND

PWR

GND

pkg-to-PWR planes

in PWR planes

GND

GND

GND

Decoupling capacitors sharing IC vias

Bottom decoupling capacitors

The Objective and Guiding Physics:

Current Path results in Inductance

And a (relatively) Simple Z_{PDN}

PCB Example (no package or die here)

Engineer L_{PCB_IC} and L_{PCB_EQ} to meet the target impedance

Z_{PDN} 17 IC Power Pins

Z_{PDN} (Ω)

Frequency[GHz]

10^2, 10, 10^{-2}; 10^{-4}, 10^{-2}, 10^0

1 decap

19 decaps

43 decaps

Z_{target}

L_{PCB_IC}

Due to vias in PCB connecting package to PCB PDN area fills

increasing parallel paths, decreasing inductance

L_{PCB_EQ}

L_{PCB_IC} + L due to all parallel paths for decoupling capacitors

Ideally for PDN Design

1. Develop noise voltage specifications for the PCB or at the package connections (specs in TD, but can transform to FD)

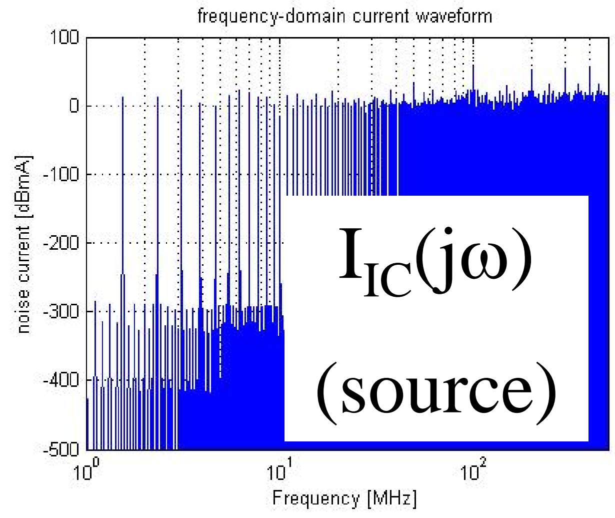
$$V(\omega) = Z_{PDN}(\omega) \times I_{IC}(\omega)$$

2. Calculate the dynamic current draw

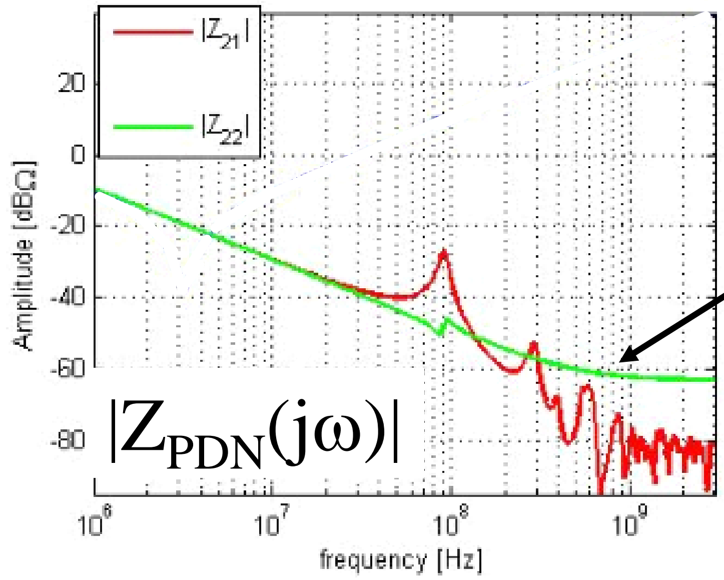
3. THEN the PCB/package PDN $Z_{PDN}(j\omega)$ can be engineered to meet noise voltage specifications

- Plane stackup, area fills, materials
- Number of decoupling capacitors
- Location, pattern, values and package size of SMT decoupling capacitors

The Reality for Dynamic Current Draw



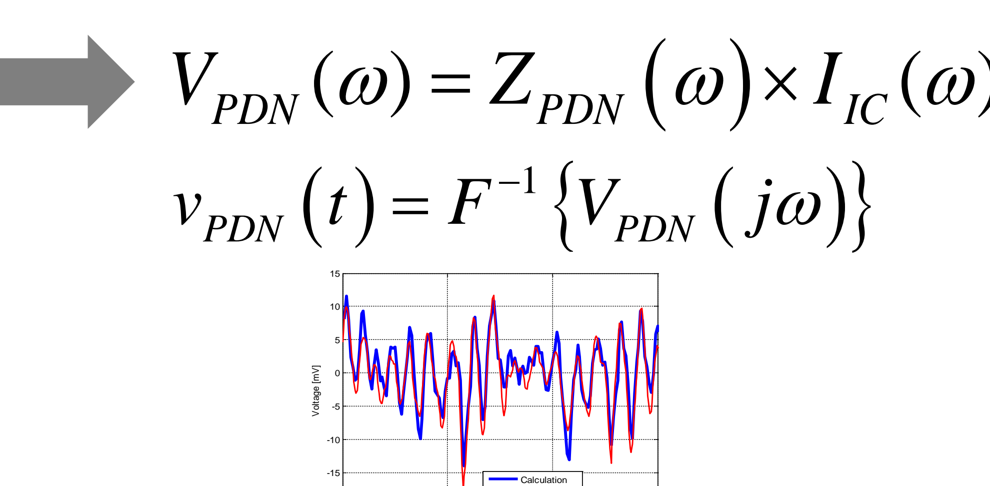
X



Determining the dynamic current draw is difficult

- Tool – in-house or commercial
- Approximate current draw waveform – pulse width, pulse amplitude, pulse sequence

and then specify Z_{target}



$$V_{PDN}(\omega) = Z_{PDN}(\omega) \times I_{IC}(\omega)$$

$$v_{PDN}(t) = F^{-1}\{V_{PDN}(j\omega)\}$$

Engineering $|Z_{PDN}(j\omega)|$ - the Alternative

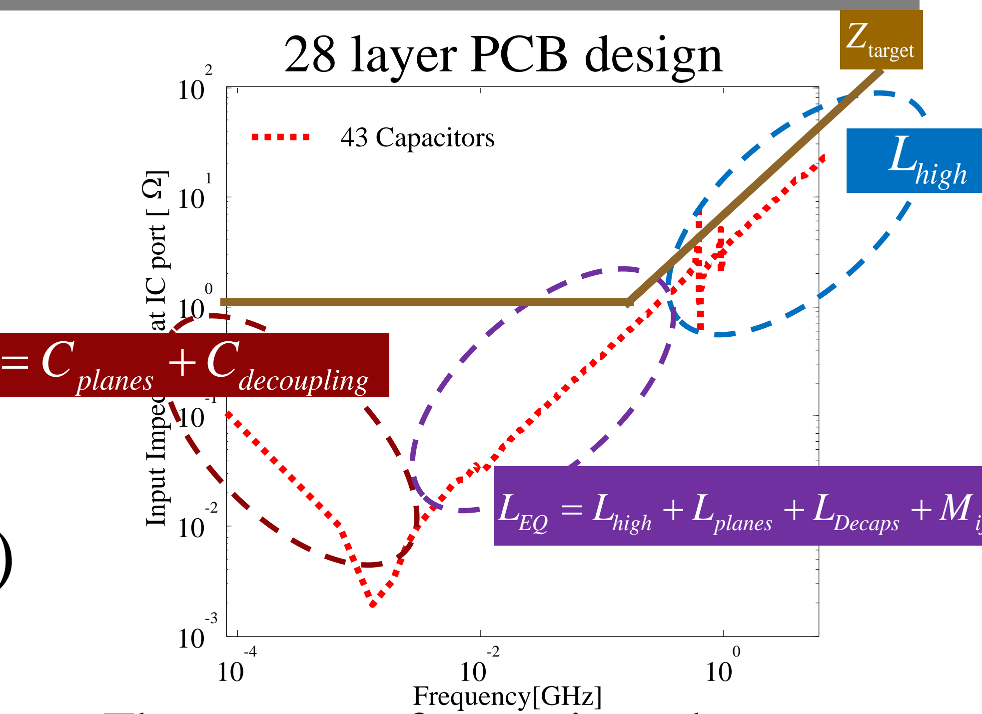
Choices for PCB PDN design

- Layer stackup, area fill dimensions, and plane separation (maybe)
- Number, value, pattern, location (top/bottom), proximity

work at these design decisions with a limited knowledge of $I_{IC}(\omega)$

$$V_{PDN}(\omega) = Z_{PDN}(\omega) \times I_{IC}(\omega)$$

Select $|Z_{PDN}(j\omega)|$ to meet noise voltage specifications



The concept of target impedance – not entirely satisfactory, but since the physics are dominated by inductance, there will be a limiting value.

Key Point – Use Z_{target} for Design

- Design choices (related to geometry)
  - Layer of power net area fill on PCB (and GND power return)
  - Decoupling capacitors

  will be driven by achieving a specified Z_{target}
- The PDN impedance behavior in frequency is dominated by inductance (with some lumped element resonances) and use design choices to lower inductance in a frequency range corresponding to current path geometry

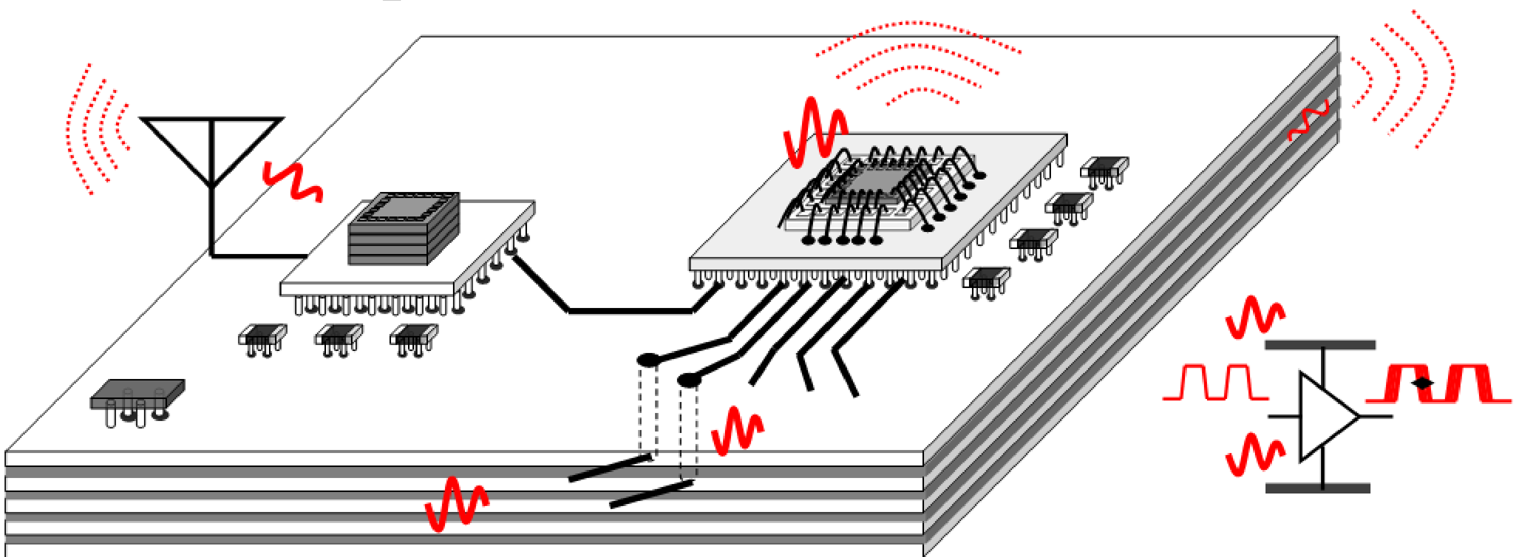
IC
Z_{PDN}
19 Decoupling capacitors at the top
17 Decoupling capacitors Sharing IC vias
7 Decoupling capacitors at the Bottom

Z_{PDN} 17 IC Power Pins

Input Impedance at IC Port [Ω]
10^{2}
10^{0}
10^{-2}
Step1
Step2
Step3
Z_{target}
10^{-4}
10^{-2}
10^{0}
Frequency[GHz]

PI Module – Physics

- The PDN problem and some preliminaries
- Charge delivery physics for PI design
- PDN design – multi-layer PCBs with power layer area fills
- Design flow for package/PCB PI co-design
- an FPGA example

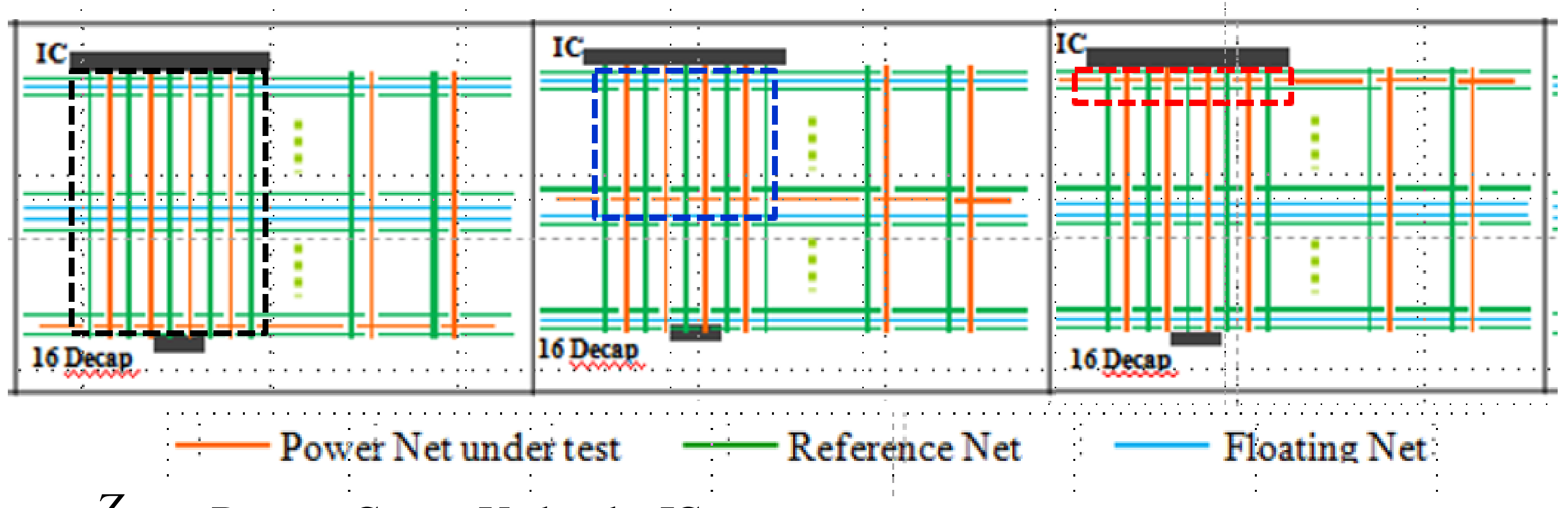


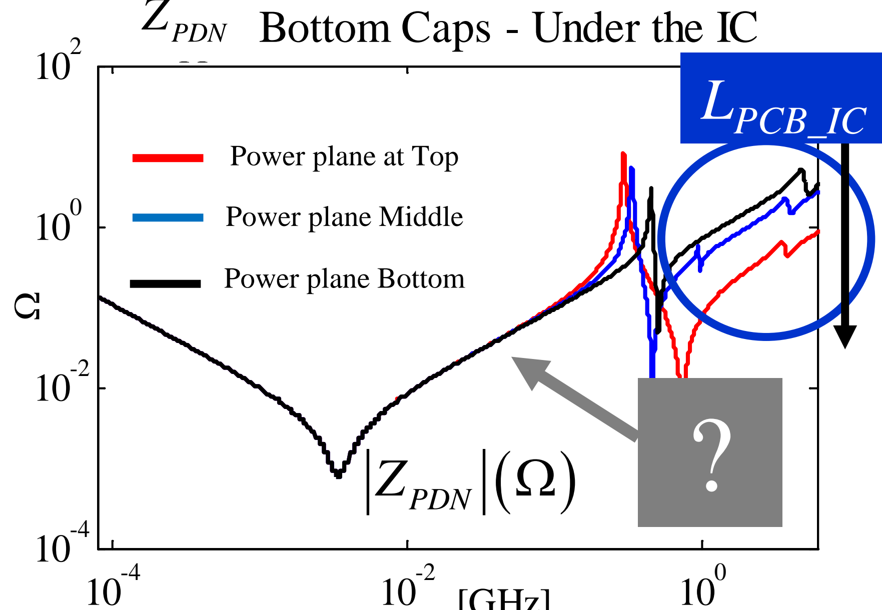
Power Plane and Capacitor Location Matrix

	Power plane at mid	Power plane at top	Power plane at bottom
Top decaps only	IC 16 Decaps	IC 16 Decaps	IC 16 Decaps
Bottom decaps only Away from the IC	IC 16 Decap	IC 16 Decap	IC 16 Decap
Bottom decaps only Under the IC	IC 16 Decap	IC 16 Decap	IC 16 Decap

Power Net under test — Reference Net — Floating Net

L_{high} – Power Plane Location in Layer Stack





Decreasing current path and inductance from package balls to PDN power layer net

Power layer closest to the IC minimizes IC to power plane inductance. (Recall that $j\omega L_{PCB_IC}$ is the impedance limit above a few MHz.)

Capacitor Location – Top, Bottom, at IC

	Power plane at mid	Power plane at top
Top decaps only	IC, 16 Decaps	IC, 16 Decaps
Bottom decaps only Away from the IC	IC, 16 Decap	IC, 16 Decap
Bottom decaps only Under the IC	IC, 16 Decap	IC, 16 Decap

Power Net under test — Reference Net

Z_{PDN}|- Top Pwr

Legend: Top Cap; Bottom Cap-Away; Bottom Cap- Under the IC

Axes: Ω (10^{-4} to 10^{2}) vs. [GHz] (10^{-4} to 10^{0})

Annotations: L_{PCB_EQ}, L_{PCB_IC}

Z_{PDN} - Middle PWR

Legend: Top Cap; Bottom Cap-Away; Bottom Cap- Under the IC

Axes: Ω (10^{-4} to 10^{0}) vs. [GHz] (10^{-4} to 10^{0})

Annotations: L_{PCB_EQ}, L_{PCB_IC}

Capacitors placed on the side closest to the power plane reduces the inductance from the capacitor to power plane and L_{EQ}. The current path length/area is smallest.

L_{EQ} – Power Plane Location in Layer Stack

Power planes – mid | Power planes – top | Power planes – bottom

IC 16 Decaps | IC 16 Decaps | IC 16 Decaps

Z_{PDN}· Top Cap

- Power plane at Top
- Power plane Middle
- Power plane Bottom

Ω; 10^{-4}, 10^{-2}, 10^{0}, 10^{2}; 10^{-4}, 10^{-2}, 10^{0} [GHz]

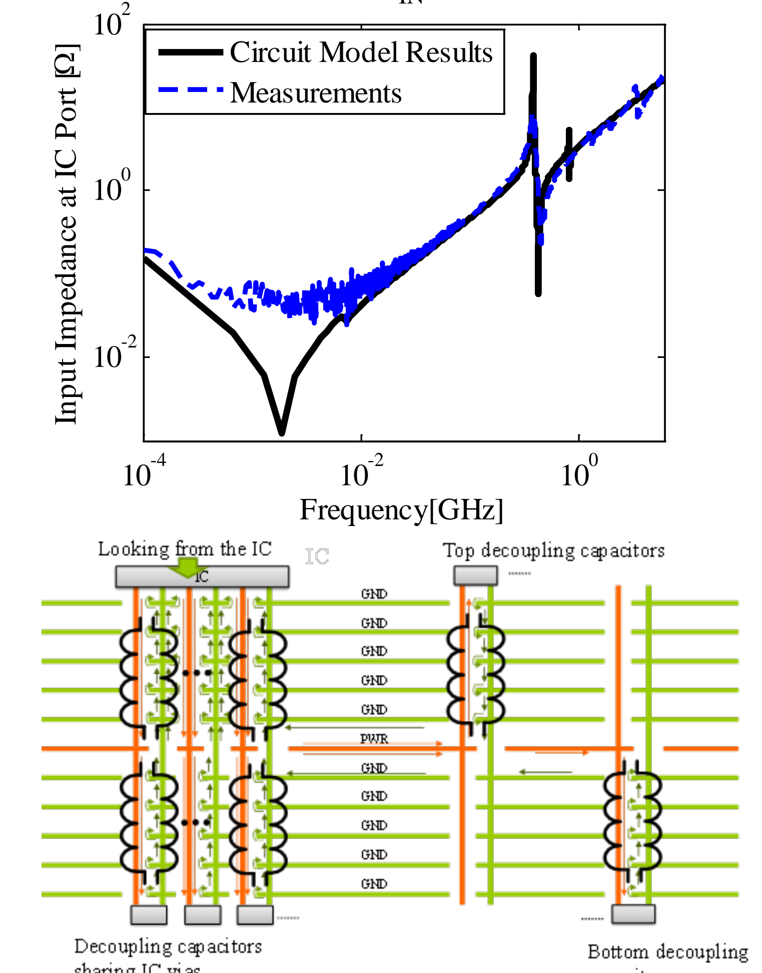
L_{PCB_IC}

L_{PCB_EQ}

L_{PCB_EQ} is also decreasing because the L from the decoupling capacitors to the power planes AND the package balls to the power planes is decreasing

Key Points

- The shape of the Z_{PDN} curve is relatively simple, even though the geometry of the PDN on a multi-layer PCB is complicated
- The current-path physics governing the impedance are dominated by inductance and lumped element resonances above approximately 1 MHz
- The inductance is dominated by the current path – geometry "length/area" (series inductance), and the number of parallel paths (parallel inductance) and this will drive the design approach ("small loops and many loops")



- Where power layers are located in stackup
- Package ball pitch
- Decoupling capacitor interconnect

- Number of PWR/GND vias in package
- Number of decoupling capacitors

PI Module – Physics

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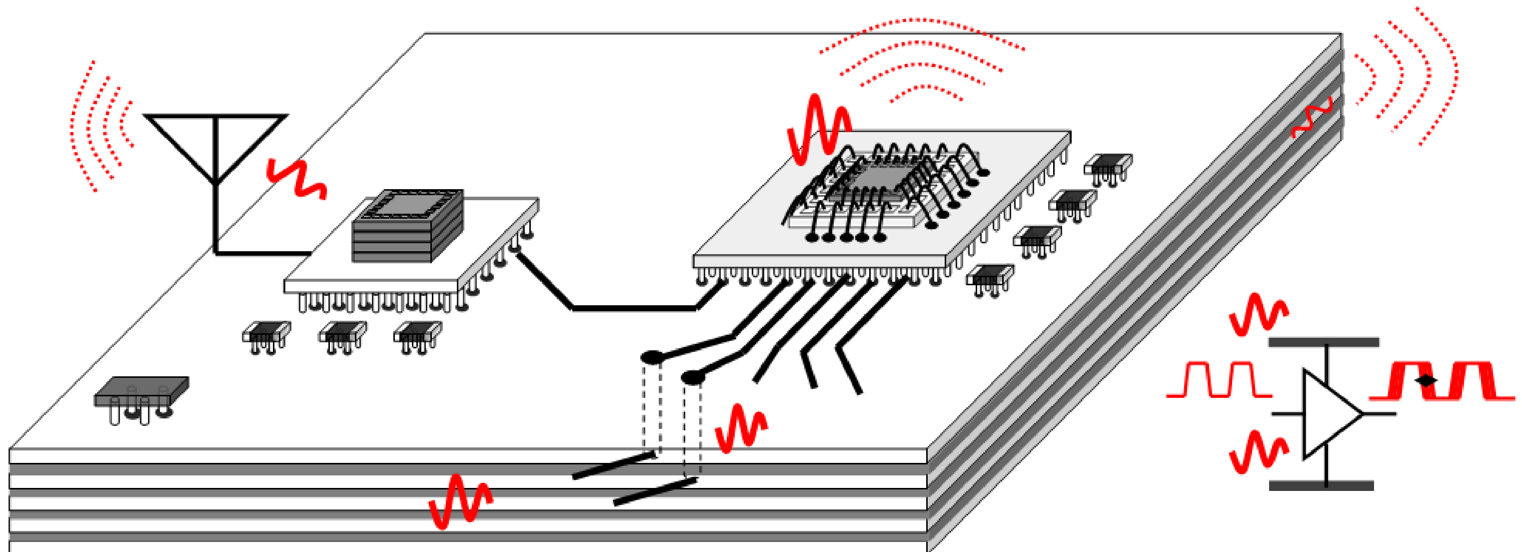
- PDN design – multi-layer PCBs with power layer area fills
- SMT decoupling
- Design flow for package/PCB PI co-design

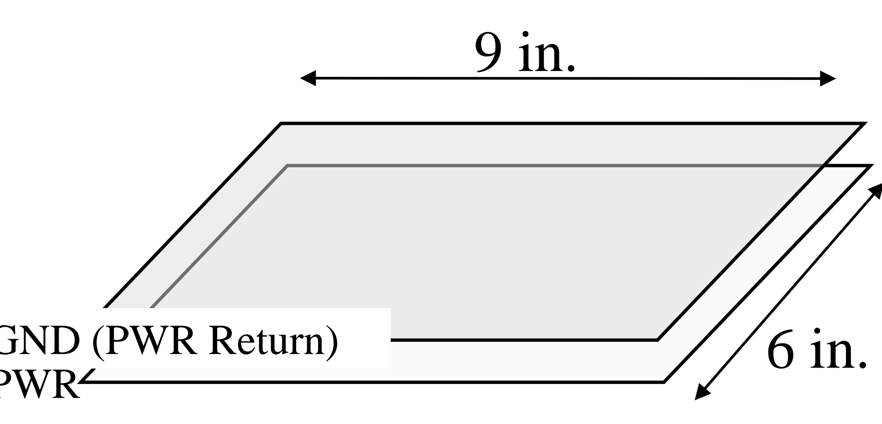


Two Approaches for SMT Decoupling

- Use an array of capacitor values:
  - This may be the best known approach in the signal integrity design community
  - Rationale: to maintain a flat impedance profile below a target impedance over a wide frequency range
  - Typically a logarithmically spaced (10, 22, 47, 100, 220, 470nF, etc.) array of 3 values per decade.
- Use a large capacitor value in the package size
  - This is less well-known, but an approach in the EMI design community
  - Rationale: to keep impedance as low as possible, less emphasis on a target impedance and a flat profile

Decoupling Strategy – Geometry

Capacitor Description					# of Caps		
Value (nF)	ESR (mΩ)	ESL (nH)	Inter-connect (nH)	Type	A	B	B1
3.30E+06	60	15	2	E-lytic	1	1	1
100000	11	1.4	2	1812	4	16	16
47000	12	1.4	2	1812	4		
22000	14	1.4	2	1812	4		
10000	16	1.4	2	1812	4		
4700	16	0.5	1.6	0603	4	24	
2200	19	0.5	1.6	0603	4		
1000	23	0.5	1.6	0603	4		
470	29	0.5	1.6	0603	4		
220	23	0.5	1.6	0603	4		
100	30	0.5	1.6	0603	4		
47	40	0.4	1.35	0402	4	20	44
22	55	0.4	1.35	0402	4		
10	75	0.4	1.35	0402	4		
4.7	104	0.4	1.35	0402	4		
2.2	211	0.4	1.35	0402	4		
Total # of Decoupling Capacitors =					61	61	61
Total Capacitance (milliF) =					4.05	5.01	4.90



t=10 mils.

tan δ = 0.02

ε_r=4.5

Approaches for SMT Decoupling Values

- Approach A : values of decoupling capacitors logarithmically spaced, i.e. 3 values per decade: 10, 22, 47, 100, etc.
- Approach B : largest values of decoupling available in two package sizes, i.e., 0603 and 0402
- Approach B1 : largest values of decoupling available in one package size, i.e., 0402.

Z_{PDN}

Approach A
Approach B
Approach B1

Target Impedance

decoupling capacitors

-20 dB/dec

+20 dB/dec

10
0
-10
-20
-30
-40
-50
-60
-70

0.001 0.01 0.1 1 10 100 1000

Frequency (MHz)

<u>Both</u> approaches can meet the design specs relative to the target impedance

Practices for Mounting SMT Capacitors

practical

.110" X .110"

best	ok	poor

0.028" DIAMETER VIA HOLE

0.045" SQUARE BONDING PAD

P1 P2 P3 P4 P5 P6 P7

0.030" WIDTH TRACE, 0.47" LONG

0.008" WIDTH TRACE, 0.16" LONG

0.008" WIDTH TRACE, 0.47" LONG

Looking from the IC

IC

Top decoupling capacitors

Above PCB to decaps

caps-to-PWR planes

pkg-to-PWR planes

in PWR planes

$Z_{PCB-in}(j\omega)$

GND

PWR

Decoupling capacitors sharing IC vias

L_{above}

Decoupling Capacitor

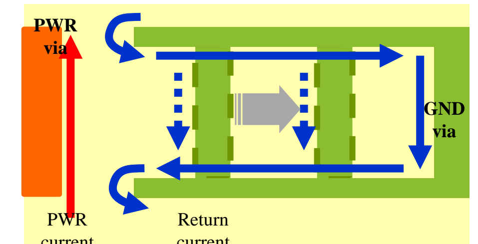
GND

d

PWR

Adding trace length, adds inductance to the interconnect:

- “loop area” above the planes – L_{above}
- Area between the power and GND return vias vertically connecting to the PWR planes



Design Geometry, Current Path, and Z_{PDN}

Capacitors
Power Via
Ground Via
Local Decoupling capacitors
Power Fill on Inner Layer
Bulk Decoupling
IC region
Voltage Regulator Module

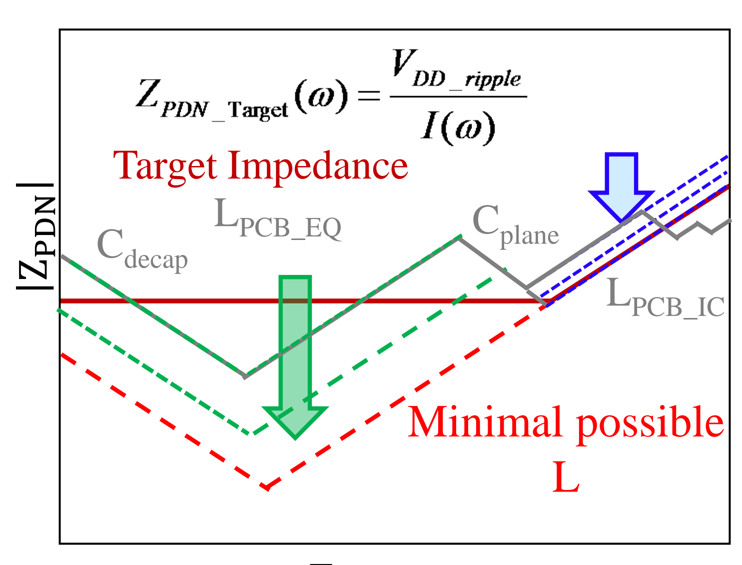
Looking from the IC
IC
Top decoupling capacitors
GND
PWR
$Z_{PCB-in}(j\omega)$

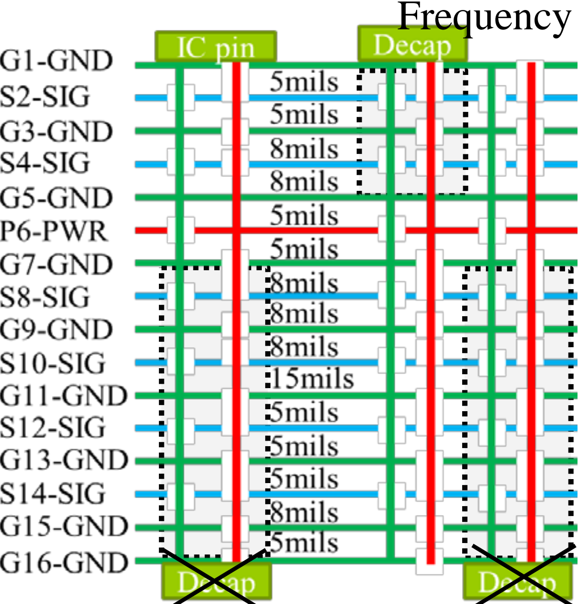
Step1 - 1 Capacitor
Step2 - 19 Capacitors
Step3 - 43 Capactors
$C_{eq} = C_{planes} + C_{decoupling}$
L_{PCB_IC}
$L_{PCB_IC} + L_{planes} + L_{PCB_Decaps} + M_{ij}$
Input Impedance at Port [Ω]
Frequency[GHz]

Port
IC power via
Top Decoupling Capacitors
GND
PWR
Decoupling Capacitors Sharing IC vias
Bottom Decoupling capacitors

Design Implications

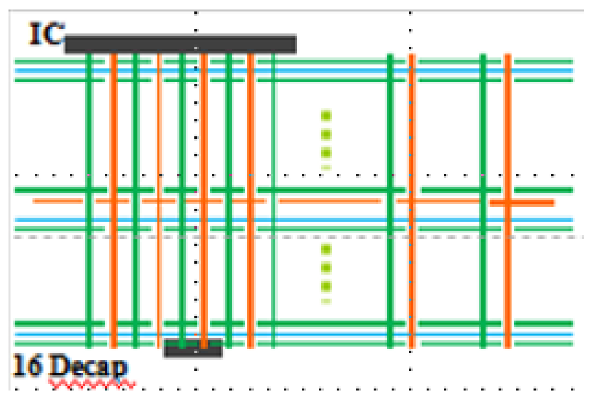
- PWR/GND plane pair nearer to the IC in stackup will minimize L_{PCB_IC} from package balls to power net area fill (smaller loop)
- PWR/GND plane pairs closely spaced will reduce L_{PCB_plane}.
- Place caps close to the power layer to minimize the inductance from the capacitor to the power net area fill layer, i.e., L_{PCB_decaps}. (minimize the loop)

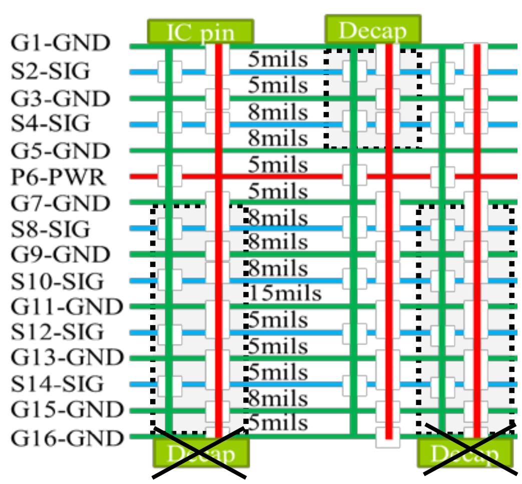




Design Implications

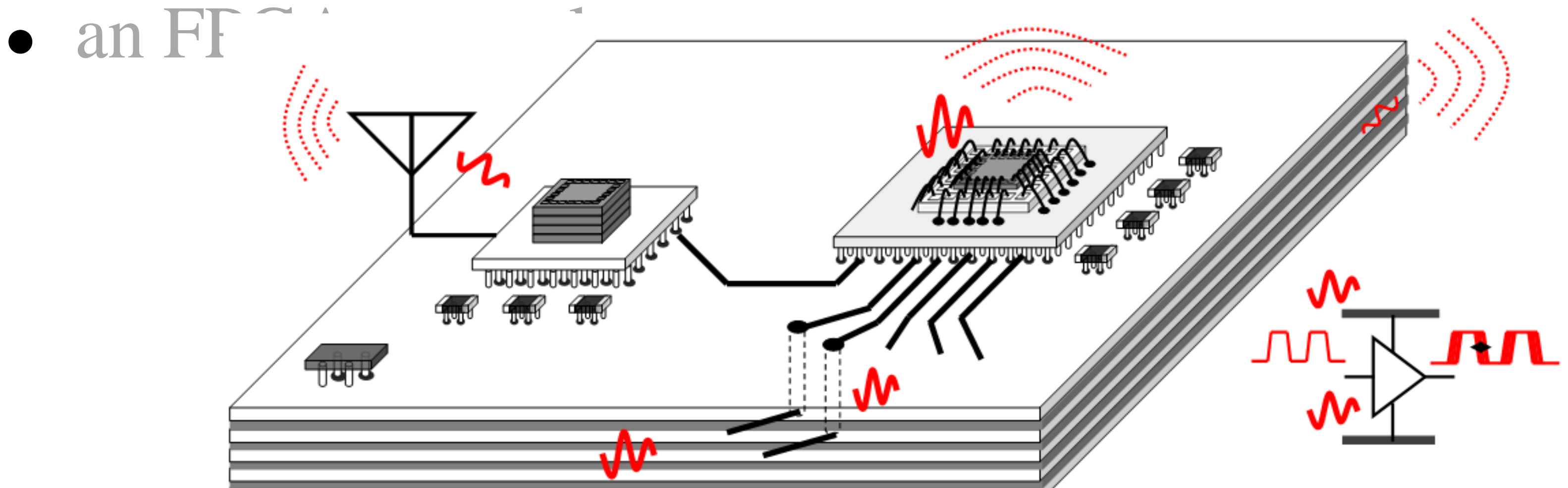
- Placing caps on the underside of PCB opposite package can benefit the design
  - if the path(s) from the package to bottom of the PCB is comparable to the pkg/planes/decap path due to mutual inductance of the via grid power pattern
  - Unless the pkg/planes/decap path is shorter due to PWR/GND near package in stackup
- Power and ground vias placed adjacent to the caps reduces the inductance in the current return path (or in the bonding pads). (smaller loops)
- Capacitor arrangements that utilize mutual inductance, e.g., doublet, or 3-terminal capacitor, can significantly reduce L_{PCB_decaps}.
- Using a large capacitance value in a given package size can meet the low-frequency target impedance, and inductance can be reduced by adding more capacitors. (many parallel paths)





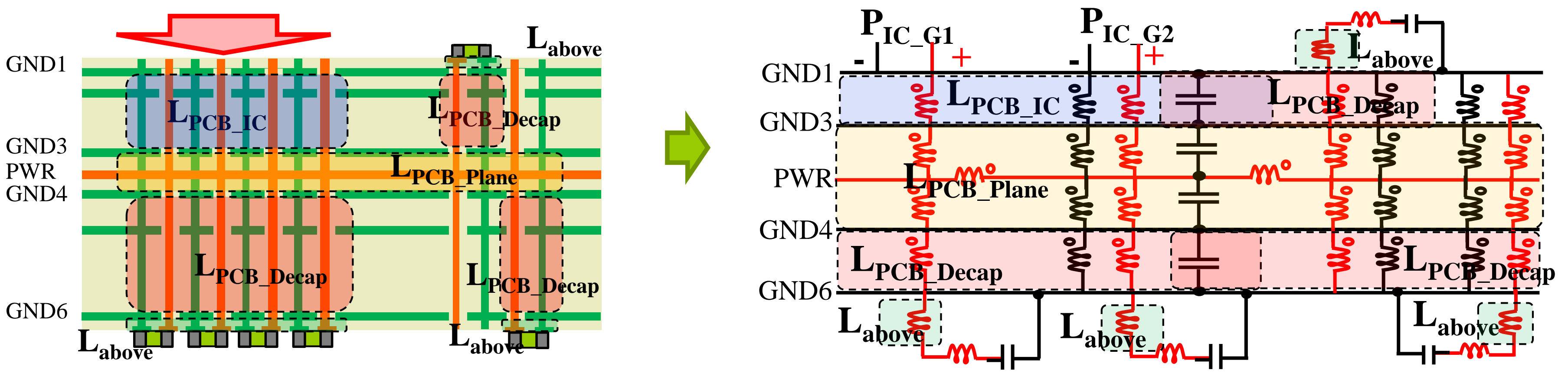
PI Module – Physics

- The PDN problem and some preliminaries
- Charge delivery physics for PI design
- PDN design – multi-layer PCBs with power layer area fills
- Time-domain and frequency domain through a circuit model
- Design flow for package/PCB PI co-design
- an F

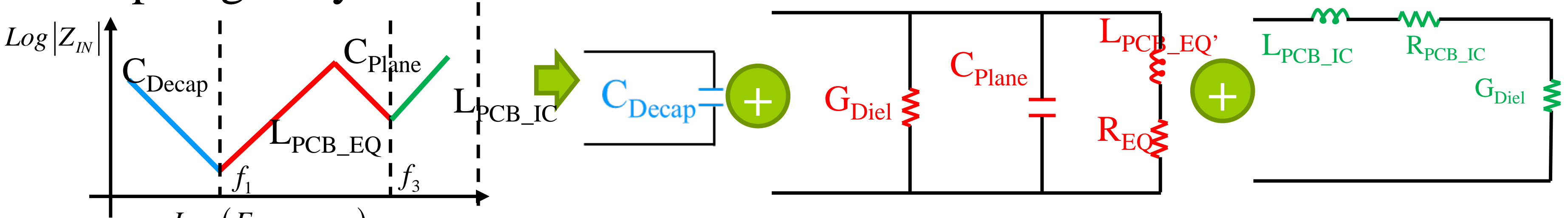


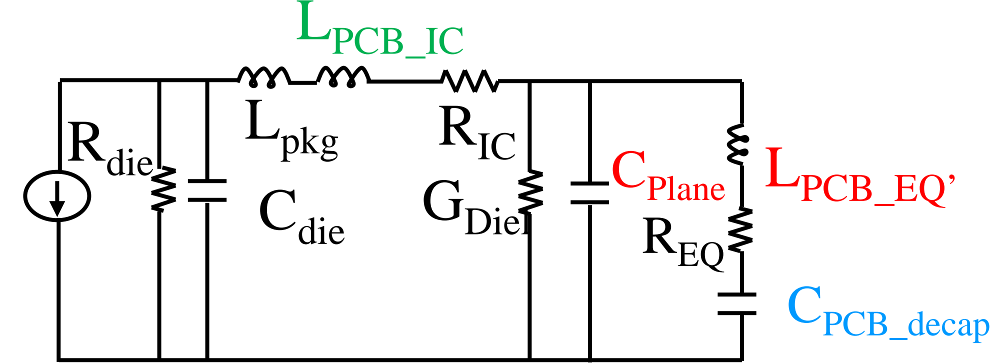
Circuit Model for PCB PDN

Based on physics-based circuit model



Topologically correct behavioral circuit model





$$L_{PCB_EQ'} = L_{PCB_Decap} + L_{above} + L_{PCB_Plane}$$

V_{ripple} Calculation

Voltage ripple specification

Voltage
VDD
VDD voltage ripple/droop
Time

Switching current profile

I
Time
F
F^{-1}
I
Frequency

Voltage ripple simulation

P_{IC_G1}
P_{IC_G2}
GND1
GND3
PWR
GND4
GND6
L_{PCB_IC}
L_{PCB_Decap}
L_{PCB_Plane}
L_{above}

L_{PCB_IC}
R_{die}
C_{die}
L_{pkg}
R_{IC}
G_{Diel}
C_{Plane}
$L_{PCB_EQ'}$
R_{EQ}
C_{PCB_decap}

Voltage ripple mathematical calculation

$I(\omega)$
f
$Log(Z_{in})$
$Log(frequency)$
$V(\omega)$
f
F^{-1}
Voltage
Time

Voltage Ripple Separation

L_{PCB_IC}

$|Z_{PDN}|$

$phase(Z_{PDN})$

$L_{PCB_EQ} - L_{PCB_IC}$

Frequency

Voltage [V]

Time [ns]

Voltage Ripple

V_{ripple_spec}

Voltage [V]

Time [ns]

$|Z_{PDN}|$

C_{decap}

L_{PCB_EQ}

C_{plane}

C_{PCB_IC}

ΔL_{PCB_EQ}

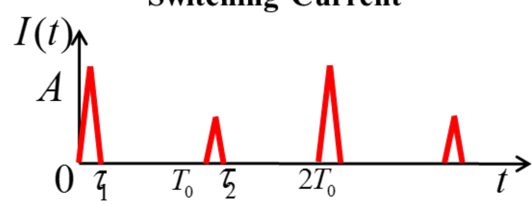
Frequency

Minimal possible L

Voltage [V]

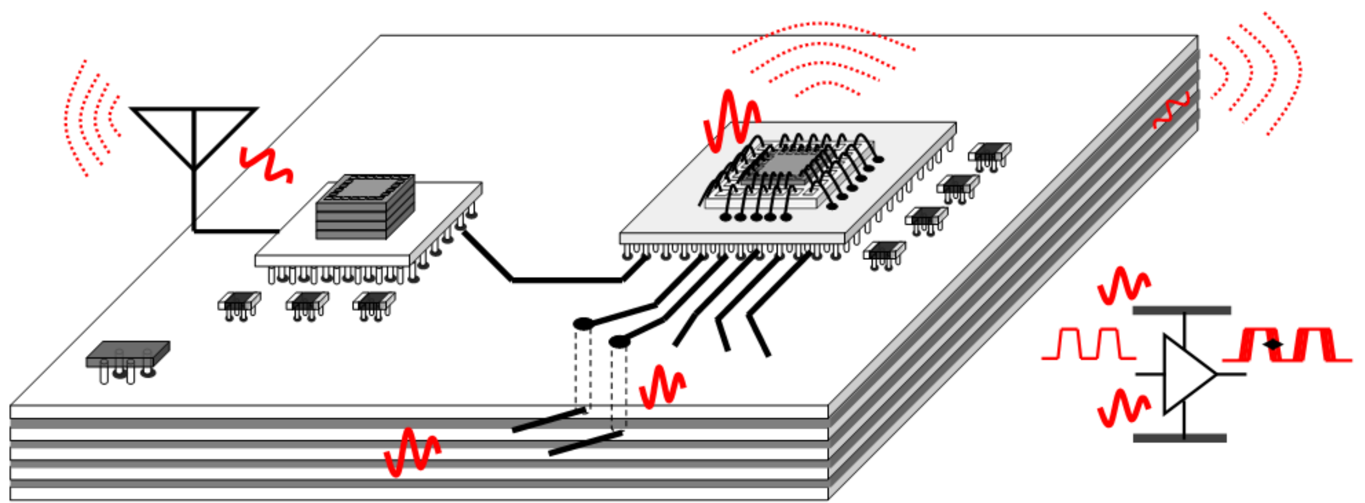
Time [ns]

Switching Current



PI Module – Appendix

- The PDN problem and some preliminaries
- Charge delivery physics for PI design
- PDN design – multi-layer PCBs with power layer area fills
- Design flow for package/PCB PI co-design
- an FPGA example



A Systematic Approach for Achieving PI

IC
C_{die}
R_{die}
GND
PWR
Package PDN
L_{pkg}
C_{pkg}
decap
L_{ball}
L_{ball}
GND
PWR
L_{PCB}
C_{PCB}
PCB PDN

$|Z_{PDN}|$

$20\frac{dB}{decade}$

no on package decoupling

low-frequency capacitance

pkg vias to IC

PCB + board decoupling

PCB vias to pkg

pkg+ on-pkg decap

On-die capacitance

$\log_{10} f$

PCB PDN Design Considerations

2a. Decoupling capacitors
- top
- bottom,
- beneath IC?

2b. Decoupling capacitor connection -
- PWR/GND via geometry
- Package size

IC

Decaps

1. Power plane(s)
   - location in stack
   - spacing to power return plane
   - total area fill
   - special materials

2a. Decoupling capacitors
- value(s)
- Number (total C)

IC pins

Effect of other ground/reference planes?

2c. Decoupling capacitor layout
- How close to IC?
- Shape – ring IC, on one side?

3. IC PWR/GND
- Number pins
- pin pattern
- Pitch
- on-package decaps

PWR

GND

Design Flow – Package

DC power determines minimum number power interconnects (IR drop, current)

Package ball **pitch** determines minimum achievable high-frequency Z_{target}

Choose **number (and pattern)** PWR/GND vias to meet high-frequency target impedance for specified PCB power area fill layer* → L_{PCB_IC}

Trade-off

On-package decaps reduce minimum overall achievable high-frequency target impedance seen by IC

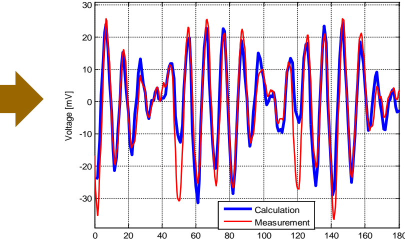
IC
C_{die}
R_{die}
GND
PWR
Package PDN
SMT C
L_{pkg}
C_{pkg}
M
L_{ball}
C_{ball}
GND
PWR
L_{PCB}
C_{PCB}
PCB PDN

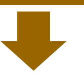
$|Z_{PDN}|$
$20 \frac{dB}{decade}$
no on package decoupling
low-frequency capacitance
pkg vias to IC
PCB + board decoupling
PCB vias to pkg
pkg+ on-pkg decap
On-die capacitance
$\log_{10} f$

* PCB/package co-design step

Design Flow – PCB

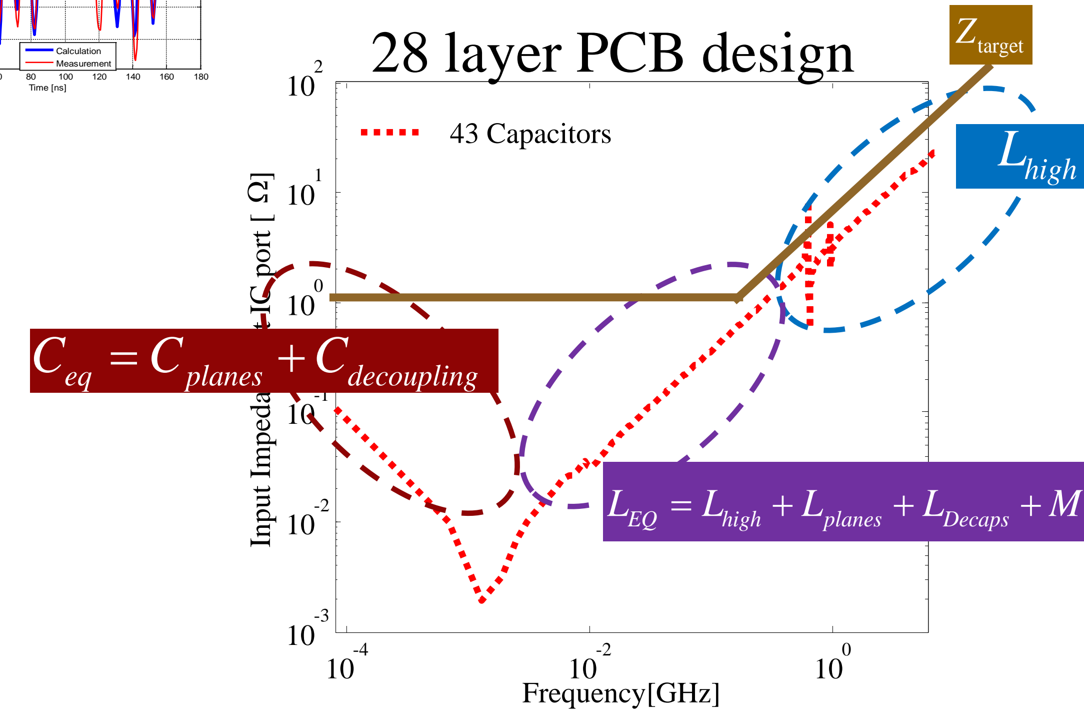
Peak **voltage ripple/droop** determines Z_{target}





IC/ASIC PWR/GND **pin-out number (and pattern)** determines minimal $\rightarrow L_{high}$

Choose PWR/GND area fill **layer** to meet high-frequency target impedance $\rightarrow L_{high}$



Number of decaps and placement determines $\rightarrow L_{EQ}$

to meet Z_{target}

value of decaps determines low-frequency impedance to meet Z_{target}