Power Integrity Concepts for High-Speed Design on Multi-Layer PCBs

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PI Module – Physics

- The PDN problem and some preliminaries
  - What PI design impacts
  - Design choices
  - A quick reminder of
    - circuit element behavior with frequency
    - current physics

- Charge delivery physics for PI design


**PDN Problem**

*High-speed, integrated, and mixed electronic system*

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**Power Distribution Network**
- VRM
- Decoupling capacitors
- Power net area fills

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IC EMI source model?

Effect of PDN noise on I/O jitter
Geometry and Inductance Decomposition
PCB PDN Design Considerations

2a. Decoupling capacitors
- top
- bottom,
- beneath IC?

2b. Decoupling capacitor connection -
- PWR/GND via geometry
- Package size

2c. Decoupling capacitor layout
- How close to IC?
- Shape – ring IC, on one side?

1. Power plane(s)
- location in stack
- spacing to power return plane
- total area fill
- special materials

Effect of other ground/reference planes?

3. IC PWR/GND
- Number pins
- pin pattern
- Pitch
- on-package decaps

Decaps

IC pins

IC

PWR
GND
Reminder – Circuit Model Behavior with Frequency

\[ Z'(dB\Omega) \]

\[ \frac{20dB}{\text{decade}} \]

\[ \log_{10} f \]

\[ Z'(dB\Omega) \]

\[ \frac{20dB}{\text{decade}} \]

\[ \log_{10} f \]
Reminder: Current Behavior

- **Conduction current** – carried by electrons
  \[ \vec{J}_{\text{cond}} = \sigma \vec{E} \]

- **Displacement current** – carried by
  \[ \vec{J}_{\text{displ}} = \varepsilon \frac{d\vec{E}}{dt} \]

Model with lumped elements if geometry electrically short

Current on a line for high-speed data
PI Module – Physics

- The PDN problem and some preliminaries
- Charge delivery physics for PI design
- Why $Z_{target}$ is used – an FPGA example
- PDN design – multi-layer PCBs with power layer area fills
- Design flow for package/PCB PI co-design
Logic Transitions and Current Draw

- Shoot-thru current (and everything else we can’t account for)
- Load charging current
- Load discharge current

This charge to support IC switching must be provided by the PDN – package, PCB
Voltage Switching/Dynamic Current Draw Disturbances

Dynamic current on power net causes disturbance and can lead to faulty switching, a source of jitter, and trouble in general.

$T_1$ and $T_2$ are not simultaneous

- **VPWR**: Power supply voltage
- **V_{PWR} + V_{Noise}**: Power supply with noise
- **VCC**: Supply voltage for IC
- **IC load**: Integrated Circuit load
- **GND**: Ground
- **shoot thru current**: A trouble-maker

banks of transistors for the PMOS and NMOS not perfectly synchronized
The Objective and Guiding Physics: Conduction Current Path results in Inductance
The Objective and Guiding Physics: Conduction Current Path results in Inductance.
Key Point – Current Path and Inductance

Four contributions (current path pieces) to the $Z_{\text{PDN}}$ inductance

Looking from the IC

Decoupling capacitors sharing IC vias

Top decoupling capacitors

Above PCB to decaps

caps-to-PWR planes

in PWR planes

Bottom decoupling capacitors

pkg-to-PWR planes

$Z_{\text{PCB-in}} (j\omega)$

GND

GND

GND

PWR

GND

GND

GND

GND

GND

GND

GND

GND

GND

GND
The Objective and Guiding Physics:
Current Path results in Inductance

And a (relatively) Simple $Z_{PDN}$

PCB Example
(no package or die here)

Engineer $L_{PCB\_IC}$ and $L_{PCB\_EQ}$ to meet the target impedance

$L_{PCB\_IC} + L$ due to all parallel paths for decoupling capacitors

$Z_{PDN}$ 17 IC Power Pins

Due to vias in PCB connecting package to PCB PDN area fills

increasing parallel paths, decreasing inductance

$Z_{target}$

PCB Example (no package or die here)
Ideally for PDN Design

1. **Develop** noise voltage specifications for the PCB or at the package connections (specs in TD, but can transform to FD)

\[ V(\omega) = Z_{PDN}(\omega) \times I_{IC}(\omega) \]

2. Calculate the dynamic current draw

3. **THEN** the PCB/package PDN \( Z_{PDN}(j\omega) \) can be engineered to meet noise voltage specifications

- Plane stackup, area fills, materials
- Number of decoupling capacitors
- Location, pattern, values and package size of SMT decoupling capacitors
The Reality for Dynamic Current Draw

Determining the dynamic current draw is difficult

- Tool – in-house or commercial
- Approximate current draw waveform – pulse width, pulse amplitude, pulse sequence

and then specify $Z_{target}$

\[ V_{PDN}(\omega) = Z_{PDN}(\omega) \times I_{IC}(\omega) \]

\[ v_{PDN}(t) = F^{-1} \left\{ V_{PDN}(j\omega) \right\} \]
Engineering $|Z_{PDN}(j\omega)|$ - the Alternative

Choices for PCB PDN design

- Layer stackup, area fill dimensions, and plane separation (maybe)
- Number, value, pattern, location (top/bottom), proximity

work at these design decisions with a limited knowledge of $I_{IC}(\omega)$

$$V_{PDN}(\omega) = Z_{PDN}(\omega) \times I_{IC}(\omega)$$

Select $|Z_{PDN}(j\omega)|$ to meet noise voltage specifications

The concept of target impedance – not entirely satisfactory, but since the physics are dominated by inductance, there will be a limiting value.
Key Point – Use $Z_{\text{target}}$ for Design

- Design choices (related to geometry)
  - Layer of power net area fill on PCB (and GND power return)
  - Decoupling capacitors will be driven by achieving a specified $Z_{\text{target}}$

- The PDN impedance behavior in frequency is dominated by inductance (with some lumped element resonances) and use design choices to lower inductance in a frequency range corresponding to current path geometry
PI Module – Physics

- The PDN problem and some preliminaries
- Charge delivery physics for PI design
- PDN design – multi-layer PCBs with power layer area fills
- Design flow for package/PCB PI co-design
- an FPGA example
## Power Plane and Capacitor Location Matrix

<table>
<thead>
<tr>
<th>Top decaps only</th>
<th>Power plane at mid</th>
<th>Power plane at top</th>
<th>Power plane at bottom</th>
</tr>
</thead>
<tbody>
<tr>
<td>IC</td>
<td>16 Decaps</td>
<td>IC</td>
<td>16 Decaps</td>
</tr>
<tr>
<td>IC</td>
<td>16 Decaps</td>
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<tr>
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<td>IC</td>
<td>16 Decaps</td>
</tr>
</tbody>
</table>

- **Power Net under test**: Orange line
- **Reference Net**: Green line
- **Floating Net**: Blue line
$L_{high}$ – Power Plane Location in Layer Stack

Power planes – bottom, middle, top

$Z_{PDN}$ Bottom Caps - Under the IC

Decreasing current path and inductance from package balls to PDN power layer net

Power layer closest to the IC minimizes IC to power plane inductance. (Recall that $j\omega L_{PCB\_IC}$ is the impedance limit above a few MHz.)
Capacitors placed on the side closest to the power plane reduces the inductance from the capacitor to power plane and $L_{EQ}$. The current path length/area is smallest.
$L_{EQ}$ – Power Plane Location in Layer Stack

$L_{PCB_{-}EQ}$ is also decreasing because the $L$ from the decoupling capacitors to the power planes AND the package balls to the power planes is decreasing.
Key Points

1. The shape of the $Z_{PDN}$ curve is relatively simple, even though the geometry of the PDN on a multilayer PCB is complicated.

2. The current-path physics governing the impedance are dominated by inductance and lumped element resonances above approximately 1 MHz.

3. The inductance is dominated by the current path – geometry “length/area” (series inductance), and the number of parallel paths (parallel inductance) and this will drive the design approach (“small loops and many loops”).

- Where power layers are located in stackup
- Package ball pitch
- Decoupling capacitor interconnect

- Number of PWR/GND vias in package
- Number of decoupling capacitors
PI Module – Physics

- The PDN problem and some preliminaries
- Charge delivery physics for PI design
- PDN design – multi-layer PCBs with power layer area fills
- SMT decoupling
- Design flow for package/PCB PI co-design
Two Approaches for SMT Decoupling

● Use an **array** of capacitor values:
  – This may be the best known approach in the signal integrity design community
  – Rationale: to maintain a flat impedance profile below a target impedance over a wide frequency range
  – Typically a logarithmically spaced (10, 22, 47, 100, 220, 470nF, etc.) array of 3 values per decade.

● Use a **large** capacitor value in the package size
  – This is less well-known, but an approach in the EMI design community
  – Rationale: to keep impedance as low as possible, less emphasis on a target impedance and a flat profile
# Decoupling Strategy – Geometry

## Capacitor Description

<table>
<thead>
<tr>
<th>Value (nF)</th>
<th>ESR (mΩ)</th>
<th>ESL (nH)</th>
<th>Inter-connect (nH)</th>
<th>Type</th>
<th>A</th>
<th>B</th>
<th>B1</th>
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<tbody>
<tr>
<td>3.30E+06</td>
<td>60</td>
<td>15</td>
<td>2</td>
<td>E-lytic</td>
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<td>1.35</td>
<td>0402</td>
<td>4</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Summary

- **Total # of Decoupling Capacitors**: 61 61 61
- **Total Capacitance (milliF)**: 4.05 5.01 4.90

- **Dimensions**:
  - Width: 9 in.
  - Height: 6 in.

- **Materials**:
  - Thickness: t = 10 mils.
  - Dielectric Loss: tan δ = 0.02
  - Dielectric Constant: εᵣ = 4.5
Approaches for SMT Decoupling Values

- Approach A: values of decoupling capacitors logarithmically spaced, i.e. 3 values per decade: 10, 22, 47, 100, etc.

- Approach B: largest values of decoupling available in two package sizes, i.e., 0603 and 0402

- Approach B1: largest values of decoupling available in one package size, i.e., 0402.

*Both approaches can meet the design specs relative to the target impedance*
Practices for Mounting SMT Capacitors

Adding trace length, adds inductance to the interconnect:

- “loop area” above the planes – $L_{\text{above}}$
- Area between the power and GND return vias vertically connecting to the PWR planes
Design Geometry, Current Path, and $Z_{PDN}$

Local Decoupling capacitors

Power Fill on Inner Layer

Bulk Decoupling

IC region

Voltage Regulator Module

Design Geometry, Current Path, and $Z_{PDN}$

Step 1 - 1 Capacitor
Step 2 - 19 Capacitors
Step 3 - 43 Capacitors

$C_{eq} = C_{planes} + C_{decoupling}$

$Z_{PCB-in}(j\omega)$

Looking from the IC

Top decoupling capacitors

Design Geometry, Current Path, and $Z_{PDN}$

$\mathbf{L}_{PCB\_IC}$

Input Impedance at IC port $\Omega$

Step 1 - 1 Capacitor
Step 2 - 19 Capacitors
Step 3 - 43 Capacitors

$\mathbf{L}_{PCB\_IC} + \mathbf{L}_{planes} + \mathbf{L}_{PCB\_Decaps} + \mathbf{M}_{ij}$

Decoupling Capacitors Sharing IC vias

Bottom Decoupling capacitors

IC power via

$\mathbf{GND}$

$\mathbf{PWR}$
Design Implications

- PWR/GND plane pair nearer to the IC in stackup will minimize $L_{PCB\_IC}$ from package balls to power net area fill (smaller loop)
- PWR/GND plane pairs closely spaced will reduce $L_{PCB\_plane}$.
- Place caps close to the power layer to minimize the inductance from the capacitor to the power net area fill layer, i.e., $L_{PCB\_decaps}$ (minimize the loop)
Design Implications

- Placing caps on the underside of PCB opposite package can benefit the design
  - if the path(s) from the package to bottom of the PCB is comparable to the pkg/planes/decap path due to mutual inductance of the via grid power pattern
  - Unless the pkg/planes/decap path is shorter due to PWR/GND near package in stackup

- Power and ground vias placed adjacent to the caps reduces the inductance in the current return path (or in the bonding pads). (smaller loops)

- Capacitor arrangements that utilize mutual inductance, e.g., doublet, or 3-terminal capacitor, can significantly reduce $L_{\text{PCB\_decaps}}$

- Using a large capacitance value in a given package size can meet the low-frequency target impedance, and inductance can be reduced by adding more capacitors. (many parallel paths)
The PDN problem and some preliminaries
Charge delivery physics for PI design
PDN design – multi-layer PCBs with power layer area fills
Time-domain and frequency domain through a circuit model
Design flow for package/PCB PI co-design
an FPGA example
Circuit Model for PCB PDN

Based on physics-based circuit model

Topologically correct behavioral circuit model

\[ L_{PCB\_EQ'} = L_{PCB\_Decap} + L_{above} + L_{PCB\_Plane} \]
**V_{ripple} Calculation**

Voltage ripple specification

Voltage ripple simulation

Switching current profile

Voltage ripple mathematical calculation
Voltage Ripple Separation

Voltage Ripple

Minimal possible L

Switching Current

$I(t)$

$A$

$0 \frac{T}{\tau} 2\frac{T}{\tau}$
PI Module – Appendix

- The PDN problem and some preliminaries
- Charge delivery physics for PI design
- PDN design – multi-layer PCBs with power layer area fills
- Design flow for package/PCB PI co-design
- an FPGA example
A Systematic Approach for Achieving PI

- Low-frequency capacitance
- 20 dB per decade
- No on-package decoupling
- PCB vias to IC
- PCB vias to pkg
- pkg+ on-pkg decap
- On-die capacitance

\[ |Z_{PDN}| \]
PCB PDN Design Considerations

2a. Decoupling capacitors
- top
- bottom,
- beneath IC?

2b. Decoupling capacitor connection -
- PWR/GND via geometry
- Package size

2c. Decoupling capacitor layout
- How close to IC?
- Shape – ring IC, on one side?

1. Power plane(s)
- location in stack
- spacing to power return plane
- total area fill
- special materials

Effect of other ground/reference planes?

3. IC PWR/GND
- Number pins
- pin pattern
- Pitch
- on-package decaps

IC pins

Decaps

IC

1. Power plane(s)
2. Decoupling capacitors
3. IC PWR/GND

PWR
GND
**Design Flow – Package**

**DC power** determines minimum number power interconnects (IR drop, current)

Package ball **pitch** determines minimum achievable high-frequency $Z_{\text{target}}$

Choose **number** *(and pattern)* PWR/GND vias to meet high-frequency target impedance for specified PCB power area fill layer $\rightarrow L_{\text{PCB IC}}$

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On-package decaps reduce minimum overall achievable high-frequency target impedance seen by IC

* PCB/package co-design step
Design Flow – PCB

Peak voltage ripple/droop determines $Z_{\text{target}}$

IC/ASIC PWR/GND pin-out number (and pattern) determines minimal $\rightarrow L_{\text{high}}$

Choose PWR/GND area fill layer to meet high-frequency target impedance $\rightarrow L_{\text{high}}$

Number of decaps and placement determines $\rightarrow L_{\text{EQ}}$

to meet $Z_{\text{target}}$

$C_{eq} = C_{\text{planes}} + C_{\text{decoupling}}$

$Z_{\text{target}}$

$L_{\text{high}}$

$C_{eq} = C_{\text{planes}} + C_{\text{decoupling}}$

$Z_{\text{target}}$

$L_{\text{EQ}} = L_{\text{high}} + L_{\text{planes}} + L_{\text{Decaps}} + M$

Input Impedance at IC port [Ω]

Frequency [GHz]

28 layer PCB design

43 Capacitors