PDNpowerIntegrity.com

TELEDYNE LECROY
Everywhereyoulook™

Principles of Power Integrity for PDN Design:

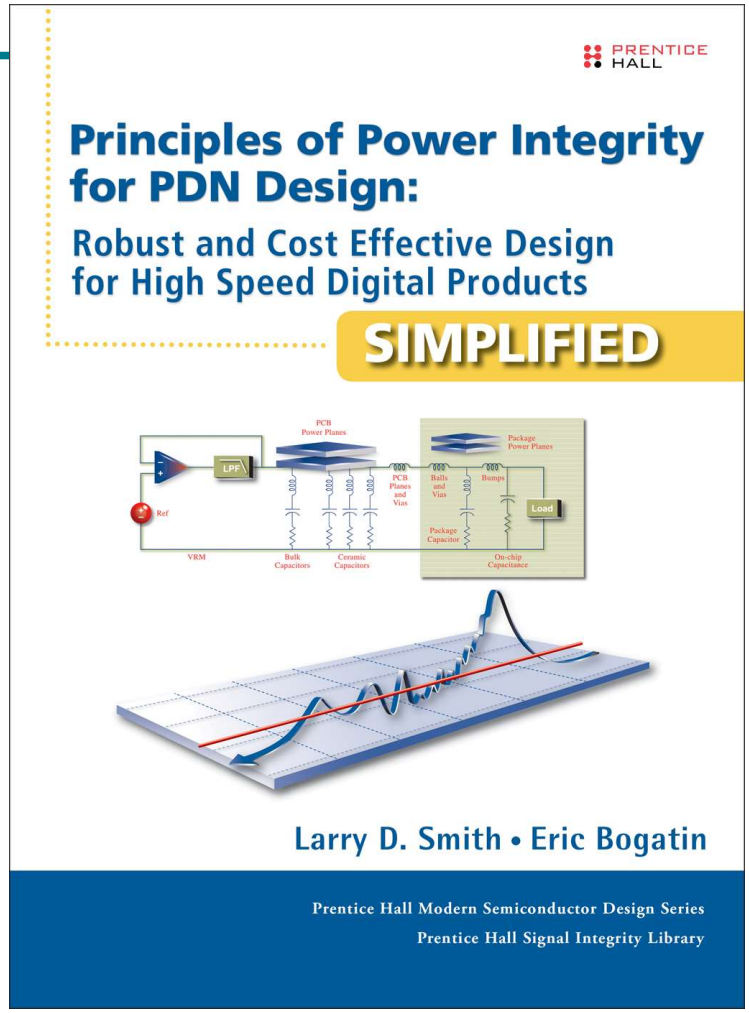
Larry Smith
Principal Power Integrity Engineer
larry.smith@pdnpowerintegrity.com

Eric Bogatin
Signal Integrity Evangelist
eric@bethesignal.com

Copies of this presentation are available on the Signal Integrity Academy web site: www.beTheSignal.com, Videos, Recorded Presentations, Webinars Course, section 60

Recent Publication from Larry and Eric

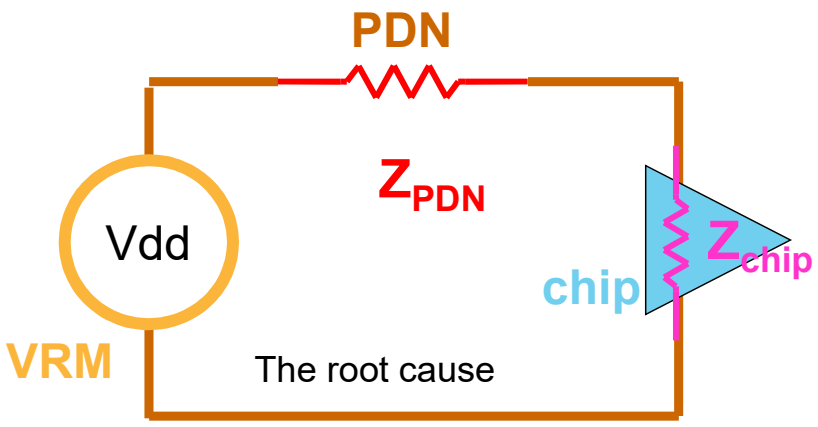
- Most of this tutorial is covered in book
  - Chapter 4: Inductance and PDN Design
  - Chapter 5: MLCC capacitors
  - Chapter 8: PDN Ecology
  - Chapter 9: Transient Currents
  - Chapter 10: PDN Resonant Calculator

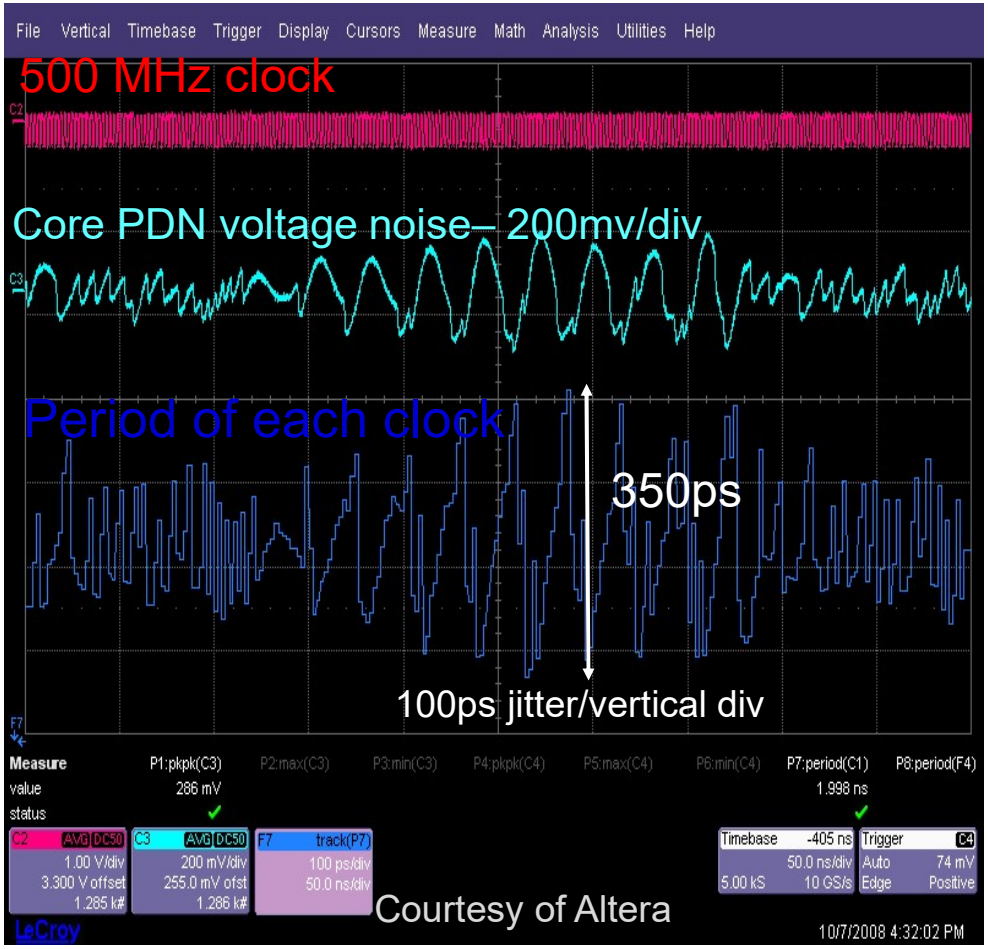


Agenda – Principles of Power Integrity for PDN Design

- The “Scope” of the Power Distribution Network (PDN)
- Target Impedance, PDN Topology and Transient Current Introduction
- Capacitance, Inductance and Resistance, and PDN Ecology
- Transient Currents – more details
- VRM, Switched Capacitor Load and PDN Resonant Calculator
- Measurements, Frequency and Time Domain Measurements and PDN Correlation

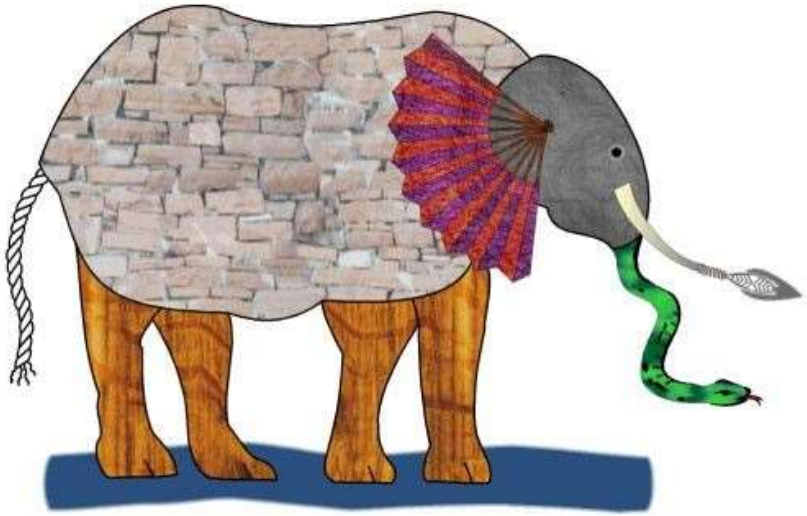
Why Do we Care? One Example: Vdd Self Aggression Noise: problem and root cause





- 500 MHz clock (2 nsec period)
- Multiple drivers drawing current through PDN at 1 Gbps, PRBS
- PDN noise causes clock jitter ~ 1 psec/mV

Why PDN Design is Confusing



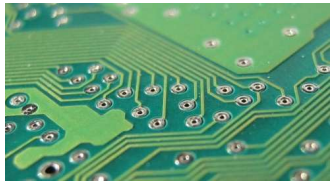
What's an elephant? …it depends
...on what is important to you

- Is it VRM noise? VRM stability?
- Is it decoupling capacitor selection?
- Is it cavity noise due to signals switching return planes?
- Is it noise on the I/O rails?
- Is it noise on the PLL or ADC rails?

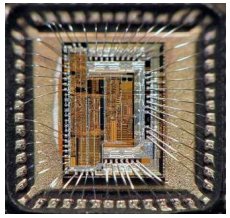
What is the PDN?

Generation (pollution →)

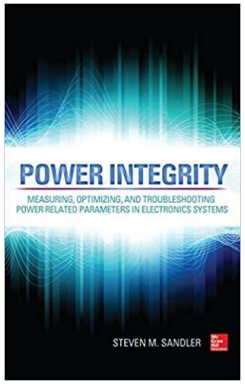
distribution

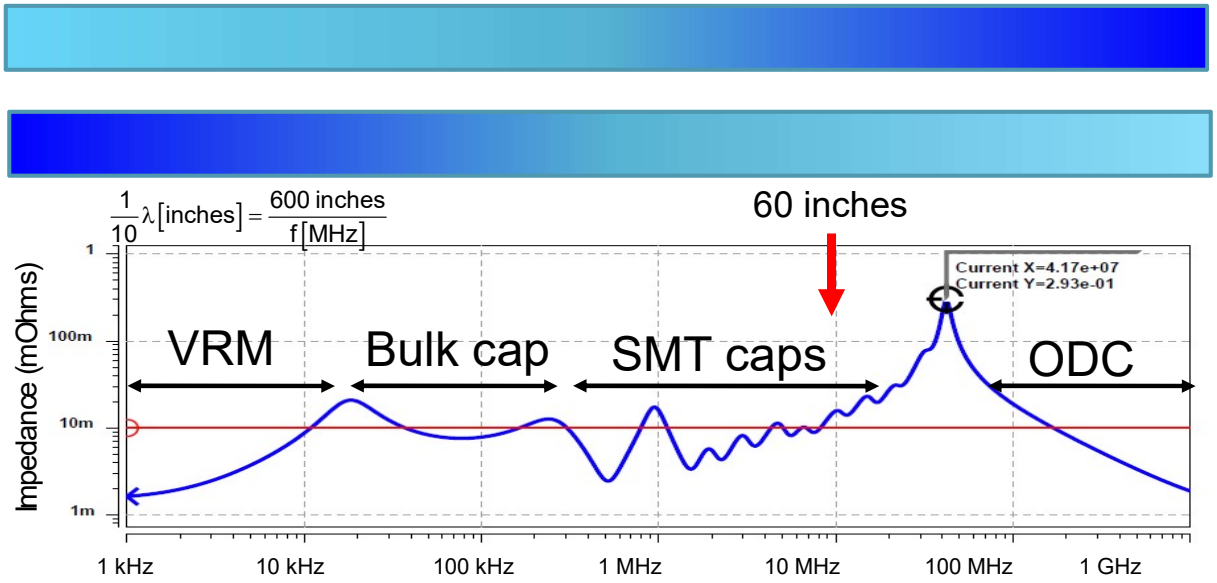


(← Self) consumption

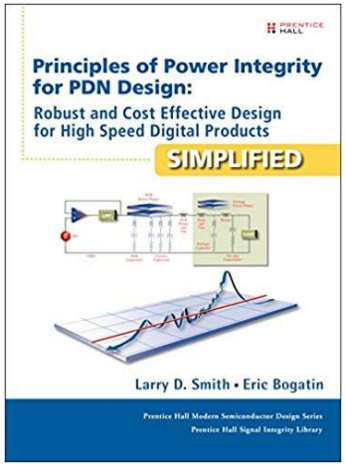


From the VRM's perspective





From the die's perspective



> 4 orders of Magnitude in Current Load

Max current per rail

100 A

10 A

1 A

0.1 A

Power generation

Multi-phase

Buck

Power sequencing

Buck-boost

Power management IC

Linear

Low Drop Out

Battery

Boost

Energy harvesting

Power consumption

Server class

Motherboards

Automotive

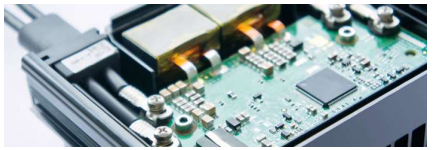
Consumer

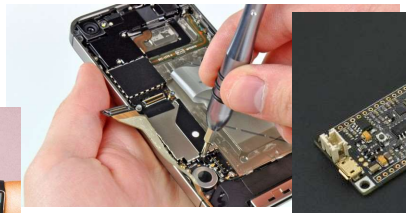
Portable/wireless

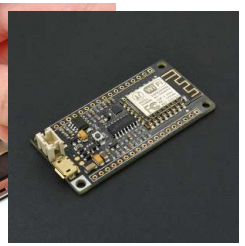
Embedded

Wearable

Internet of Things



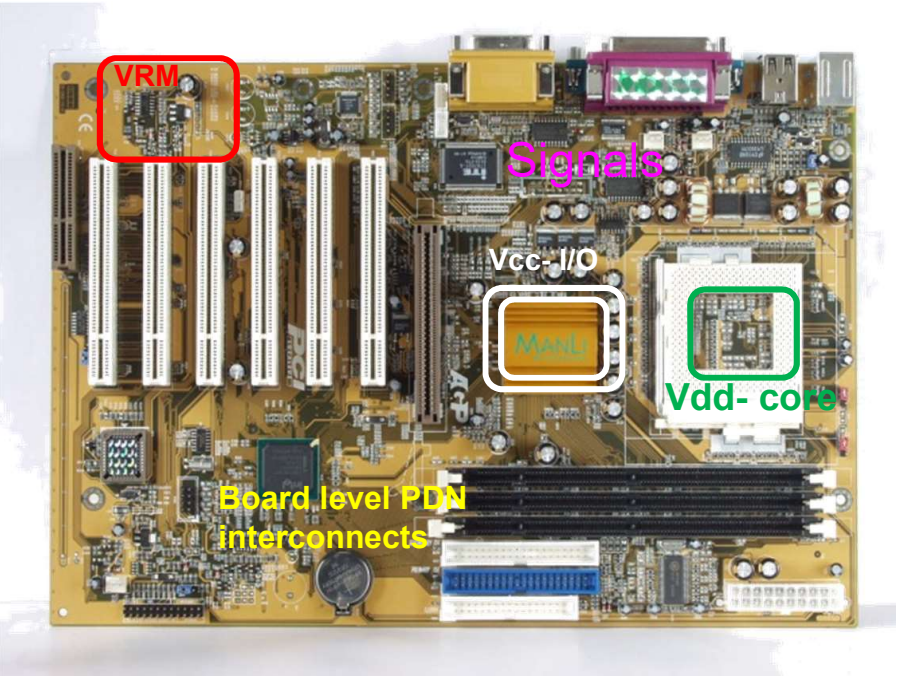




Classification of PDN Loads

- IO – Jitter is important
  - DDR
  - Serdes
  - General Purpose IO
- Logic Cores – Fmax, Vmin, voltage droops are important
  - Microprocessors
  - Graphics Processors
  - Modem

Why PDN Design is so Confusing:
It's not just 1 problem and root cause, it's 12



- Self aggression noise
  - From VRM on VRM
  - From Vcc on Vcc
  - From Vdd on Vdd
  - From signals on signals (discontinuities)
- "Pollution" of the board/pkg interconnects
  - From VRM
  - From I/O
  - From core
  - From signals
- Mutual aggressors: cross talk coupling from the PDN
  - To VRM
  - To I/O
  - To core
  - To signals

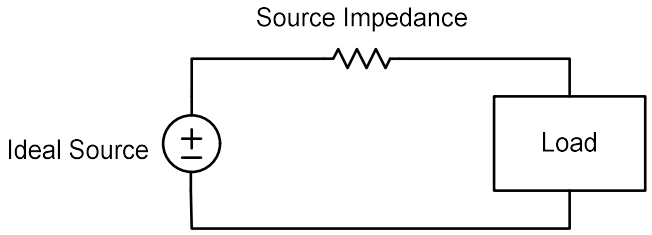
Putting the PDN in perspective:

Target Impedance, PDN Topology and Transient Currents

Larry Smith

Target Impedance Definition

- Based on Ohms Law
- Two easily understood and difficult to obtain parameters
  - Tolerance
  - Transient current
    - Expressed as percentage of maximum current
- Target impedance is a function of frequency if
  - Tolerance is a function of frequency
  - Transient current is a function of frequency

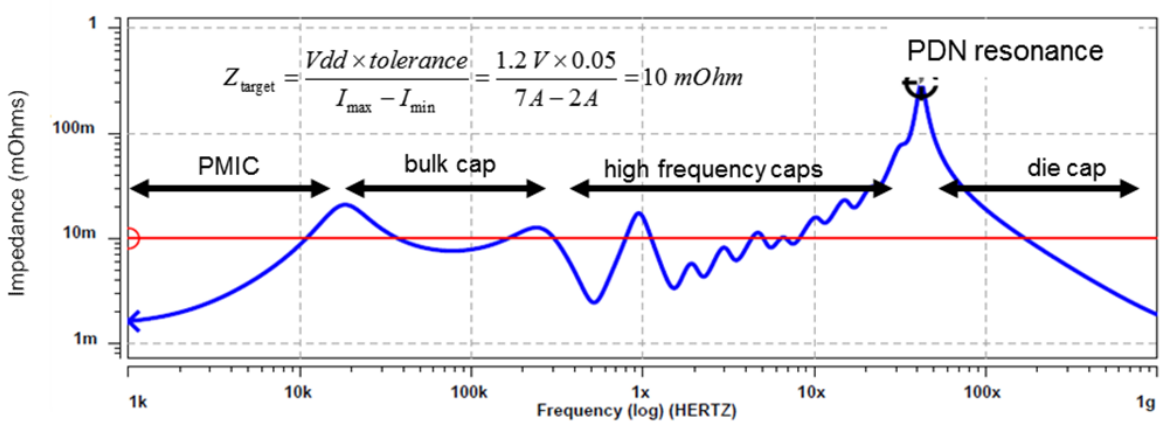


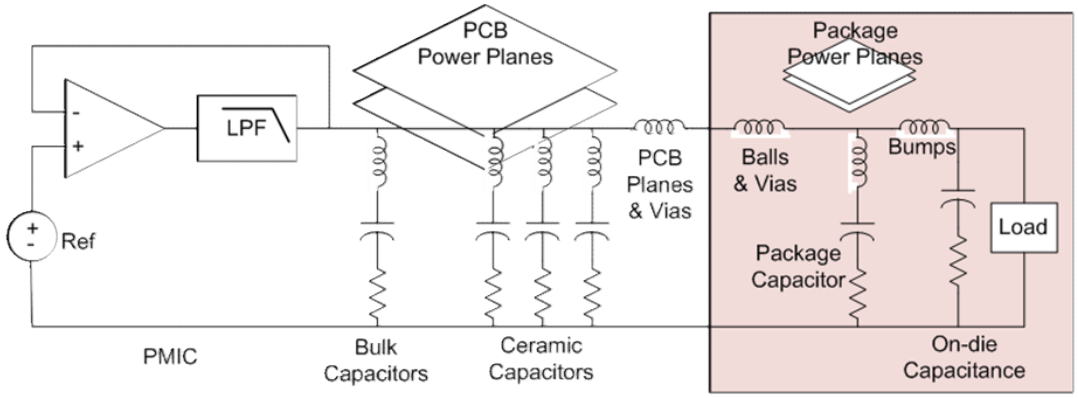
$$Z_{target} = \frac{Vdd \times tolerance}{I_{max} - I_{min}} = \frac{1.2\,V \times 0.05}{7\,A - 2\,A} = 10\,mOhm$$

Supply that meets Z_{target} almost certainly will not exceed specified voltage tolerance with given transient current

… but that can be expensive …

Components for Power Distribution Network (PDN)



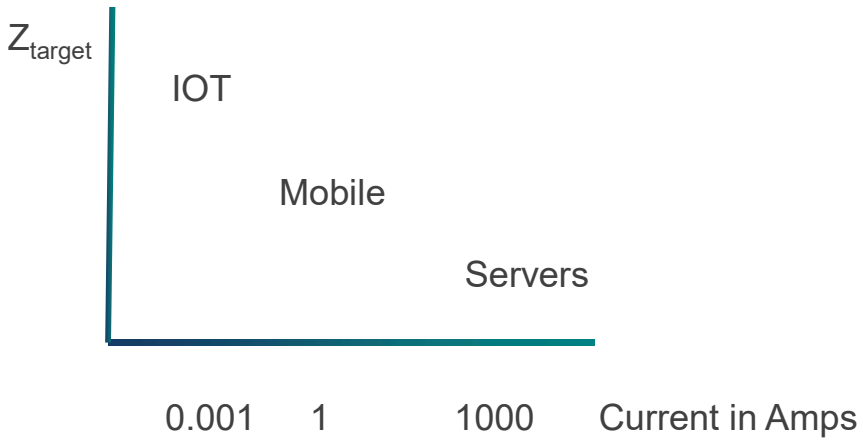


PDN Space: Very Low Currents to Very High Currents

PDN principles are still the same: Manage the PDN impedance

- Target Impedance Scales
- It is just a version of Ohms Law

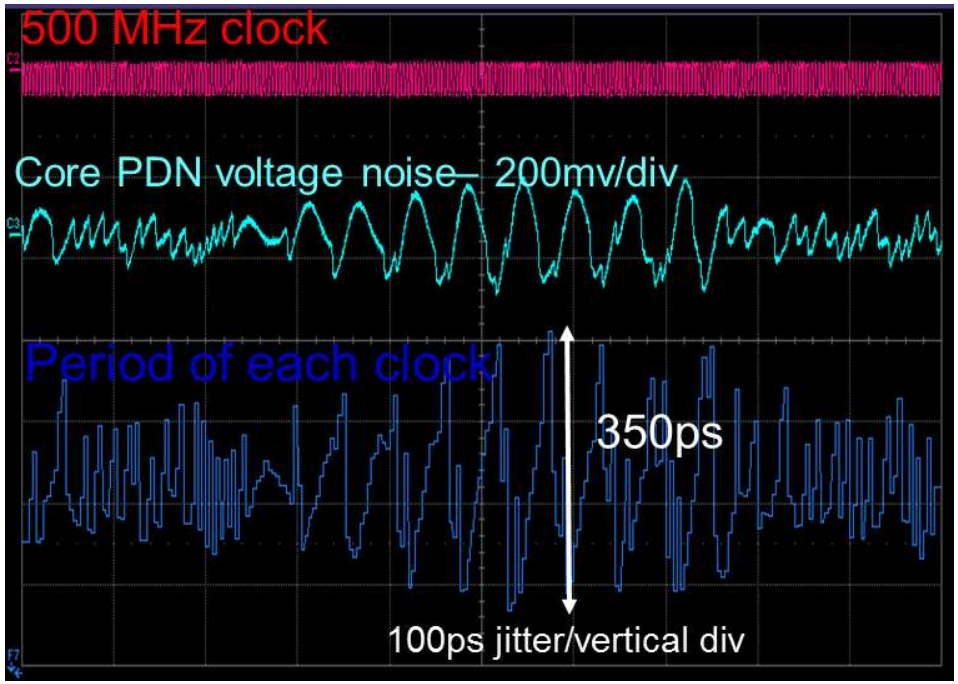
Product	Current	Z_{target}
Internet of Things	mA	Ω
Mobile Computing	Amps	mΩ
Servers	100's of amps	μΩ



$$Z_{target} = \frac{Vdd \times tolerance}{I_{max} - I_{min}} = \frac{1.2\,V \times 0.05}{7\,A - 2\,A} = 10\,mOhm$$

Jitter Is Important for IO and Serdes Applications

- Voltage droops are important for ***logic cores***
  - Determines Fmax – maximum clock frequency
  - Determines Vmin – minimum functional voltage
- ***IO and Serdes*** Applications
  - Sensitive to dV/dt
  - PDN induced Jitter
- PRBS Clock gating
  - Creates PDN current at resonant frequency
  - Excessive PDN noise: 300 mV p-p
  - 350 ps jitter correlates to PDN noise

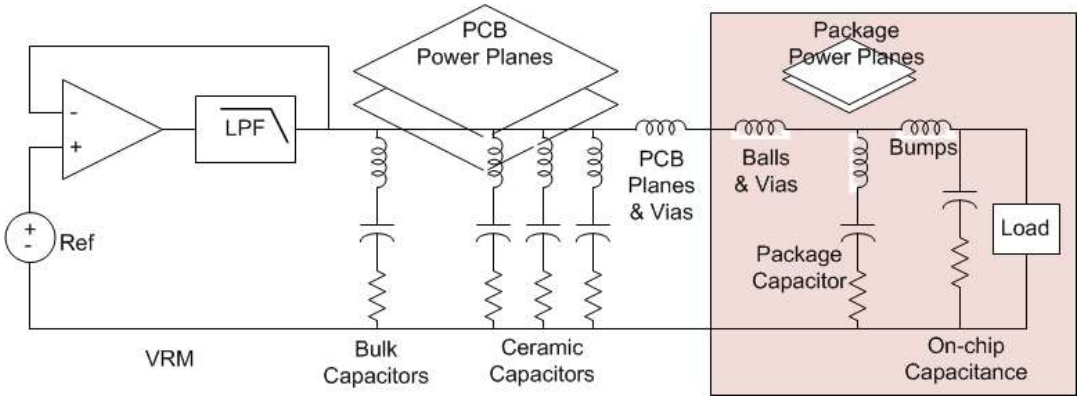


50 ns / div

PDN noise needs to be controlled for both logic cores and communications circuits

Transient Current Considerations

- Transient current paradox
  - Commonly used terminology
  - But often misunderstood…
- Examples of Transient current
  - Impulse: Clock edge current
  - Step: Burst transient
  - Resonance: Periodic burst transient
- $I_{transient} = I_{max} - I_{min} = dI$
- Current waveforms have large variation across system
  - Filtering effect of inductance and capacitance
  - Very different time constants
- Current profiles have frequency content depending on length of time, dT
  - 100's of pSec only affects die
  - Few nSec affects package
  - 10's of nSec affects PCB
  - µSec affects VRM

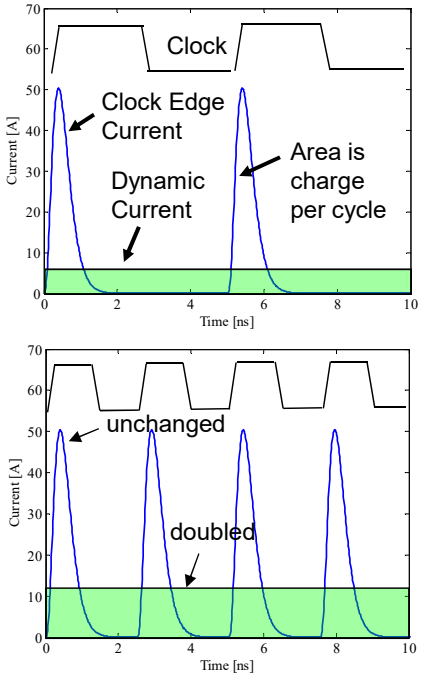


Current Definitions – On-Chip Level

- Clock edge current:
  - Instantaneous current drawn
  - by die logics at clock edges
- Charge per clock cycle:
  - Independent of clock frequency

$$Q = \int_0^T i_{clk\_edge}(t) \cdot dt$$

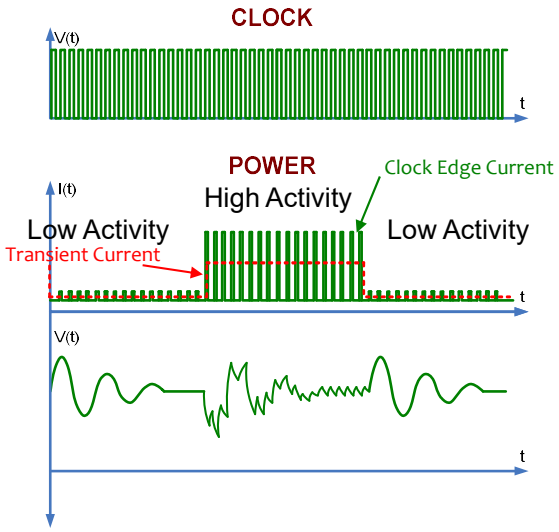
- Dynamic current:
  - Time averaged clock edge current
  - Comes with the clock
  - Static (leakage) current not included
  - Used for target impedance design
  - Proportional to clock frequency



$$I_{dynamic} = Q / T = \frac{1}{T}\int_0^T i_{clk\_edge}(t) \cdot dt$$

Time Average Dynamic Current

- System level current considerations
- Low Activity:
  - Clock is active but Data is Idle
- High Activity:
  - Clock and Data are active
- Transient Current:
  - high-activity current minus low-activity current
  - AKA power transient

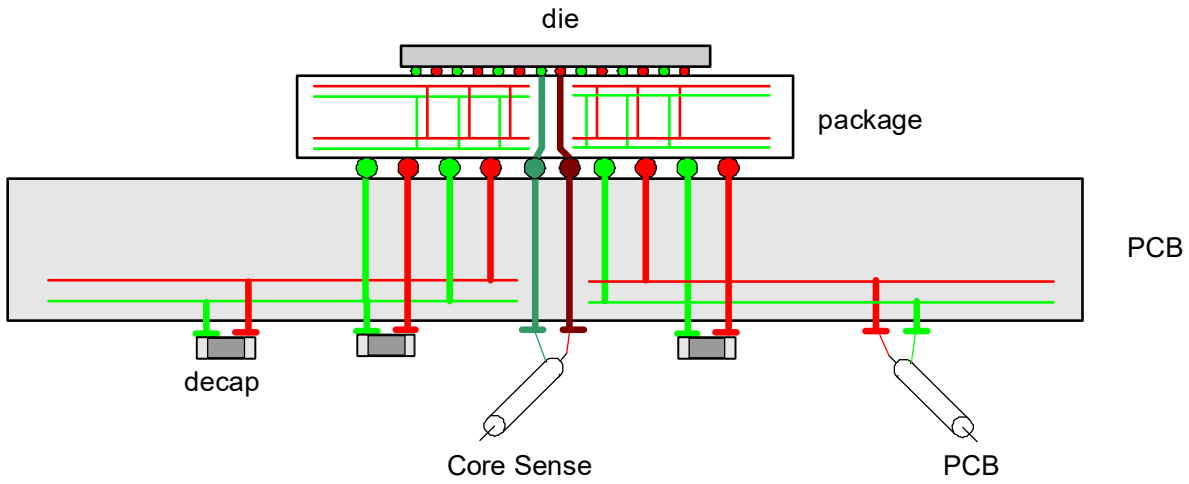


System Level PDN responds to power transients.
Clock edge currents are filtered by the package.

L, R and C in the PDN, PDN Resonance Calculator

Larry Smith

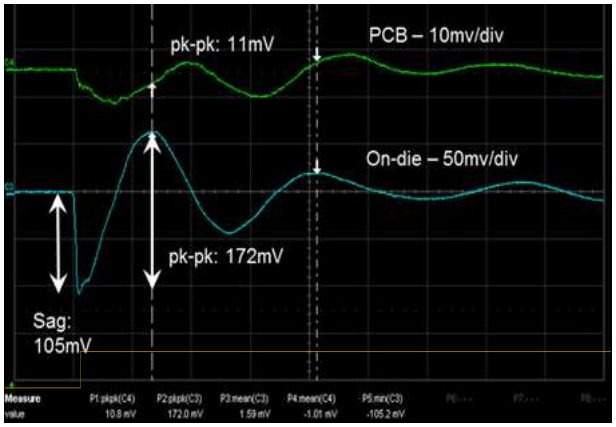
System Cross Section for Measurements



- Die on Package on PCB
- Capacitance is mostly on the die
- Inductance is mostly in the package and PCB
- Resistance is in the die, package, PCB and capacitors
- Simple RLC circuit closely represents system
- Next we will examine lab measurements for a real hardware system

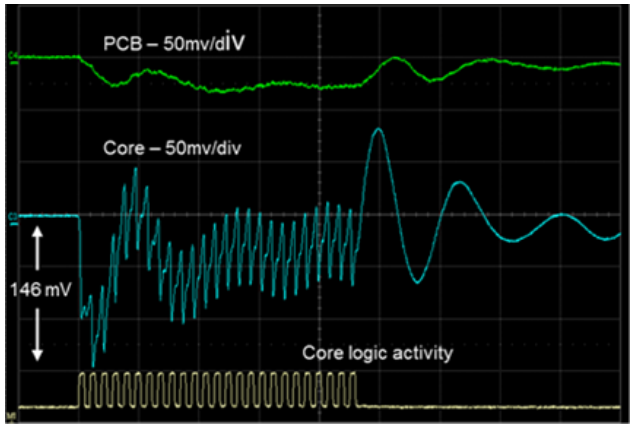
Fundamental PDN Voltage Responses

Impulse Response (Clock Edge Noise)



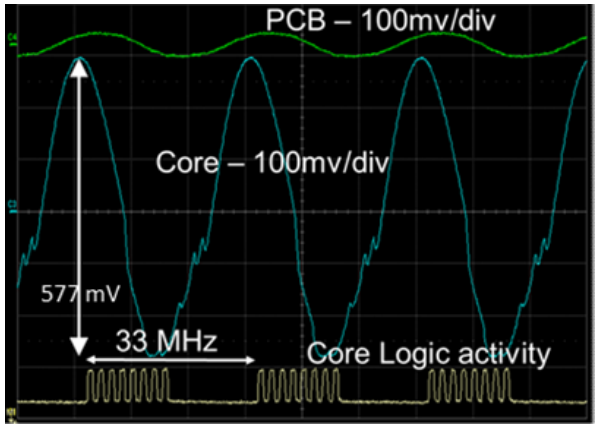
10 nS / Div

Step Response



10 nS / Div

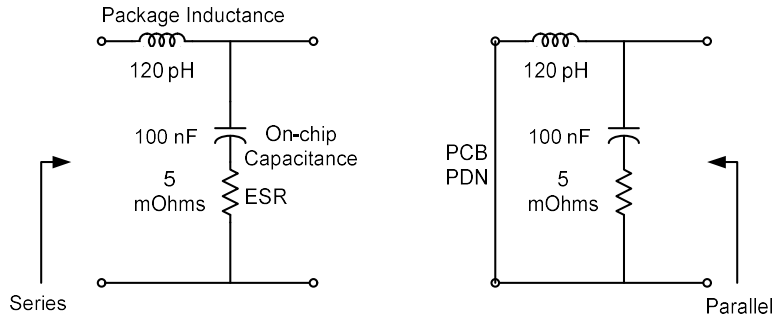
Resonance Response

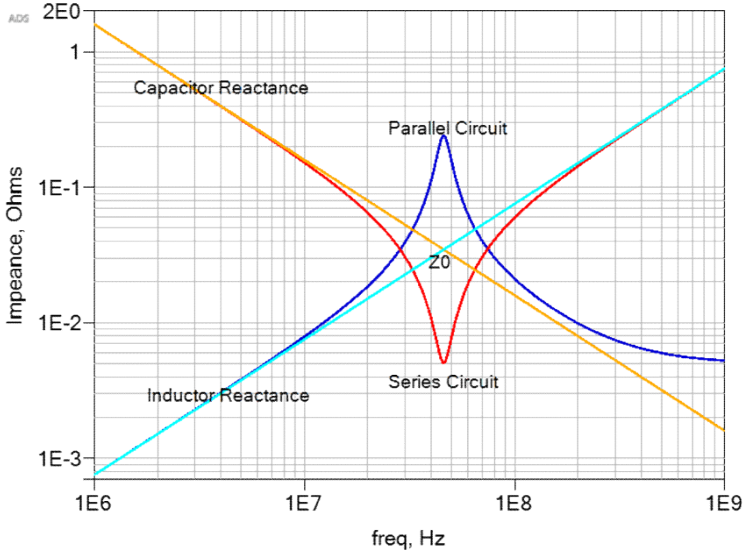


10 nS / Div

Waveforms curtesy of Altera. On-Chip PDN Noise Characterization and Modeling, DesignCon 2010

Equations for Series and parallel circuits





- Measure series resonance from the package balls
- Stimulate parallel resonance from chip circuits
- The RLC elements are the same

Resonant frequency $$f_0 = \frac{1}{2\pi\sqrt{LC}}$$

Reactance at resonance $$X = Z_0 = \sqrt{\frac{L}{C}}$$

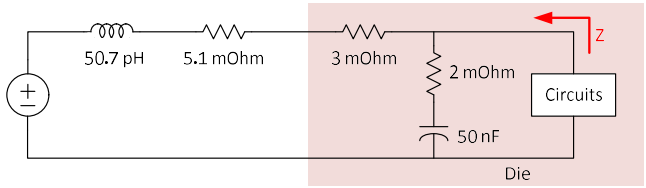
$$Q\text{-}factor = \frac{Z_0}{R} = \frac{\sqrt{L/C}}{R}$$

Estimate of impedance peak at resonance

$$Z_{peak} \doteq Z_0 \bullet Q\text{-}factor = \frac{X^2}{R} = \frac{L/C}{R}$$

The beginning of a PDN Resonant Calculator

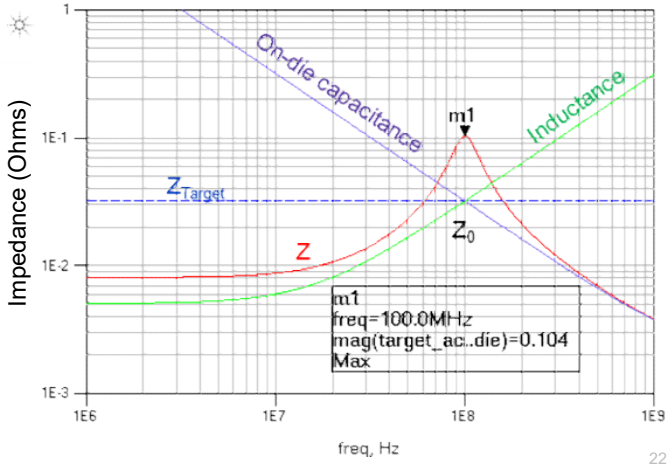
PDN Resonance Calculator – Frequency Domain



Frequency Domain		
Vdd	1	V
Core Cap	50	nF
PDN loop Inductance	50.7	pH
PDN loop resistance	10.1	mOhm
dynamic current	1.55	A
Resonant Frequency	100	MHz
PDN Z_0	32	mOhm
q-factor from PDN loop	3.15	
Expected impeance Peak	100	mOhm
Target Impedance	32	mOhm
Assumed Die resistance	5.0	mOhm
External PDN loop resistance	5.1	mOhm

- Spread Sheet for PDN parameter calculations
  - Inputs (independent parameters) are the green shaded cells
  - Results (dependent parameters) are calculated in the white cells

- Desire 100 mOhm peak at 100 MHz
  - Choose 50 nF for on-die capacitance
  - Calculate L $f_0 = 1/2\pi\left(\sqrt{LC}\right)$
  - Calculate Z0 $Z_0 = \sqrt{L/C}$
  - Calculate q-factor $q\text{-}factor = Z_0 / R = \sqrt{L/C}/R$
  - Choose R for 100mOhm peak $Z_{peak} \doteq Z_0 \bullet q\text{-}factor = \dfrac{L/C}{R}$



PDN Parameter Calculations – Time Domain

- Average clock cycle charge is easily calculated
  - Average bench current
  - Clock frequency
  - Assumes all clock cycles are equal

$$Q_{cycle} = \frac{I_{dynmic}}{f_{clock}} = \frac{1.55A}{1GHz} = 1.55\,nCoul$$

- Charge is consumed from on-die capacitance

$$Q = CV$$
$$dQ = C \bullet dV$$

- Impulse response (droop) from single clock cycle

$$V_{clock\,edge} = \frac{Q_{cycle}}{ODC} = \frac{I_{dynamic} / f_{clock}}{ODC} = \frac{1.55A / 1GHz}{50nF} = 31\,mV$$

- Step response (droop) from fast edge

$$V_{step} = I_{step} \times Z_0 = 1.55A \times 32\,mOhm = 49\,mV$$

- Resonance response (peak-peak) from repeating steps

$$P\text{-}P_{resonance} = \frac{4}{\pi} I_{tran} Z_{peak} = \frac{4}{\pi} \times 1.55A \times 100\ m\Omega = 198\ mV$$

Frequency Domain		
Vdd	1	V
Core Cap	50	nF
PDN loop Inductance	50.7	pH
PDN loop resistance	10.1	mOhm
dynamic current	1.55	A
Resonant Frequency	100	MHz
PDN Z_0	32	mOhm
q-factor from PDN loop	3.15	
Expected impeance Peak	100	mOhm
Target Impedance	32	mOhm
Assumed Die resistance	5.0	mOhm
External PDN loop resistance	5.1	mOhm
Time Domain		
f_{clock}	1	GHz
charge per clock cycle (Q_{cycle})	1.55	nCoul
Expected clock edge droop (impulse)	31	mV
Expected step response droop	49	mV
Expected peak-peak noise at resonance	198	mV

$$PDN\ Z_0 = \sqrt{\frac{L}{C}}$$

Capacitance, Inductance, Resistance and the PDN Ecology

Eric Bogatin

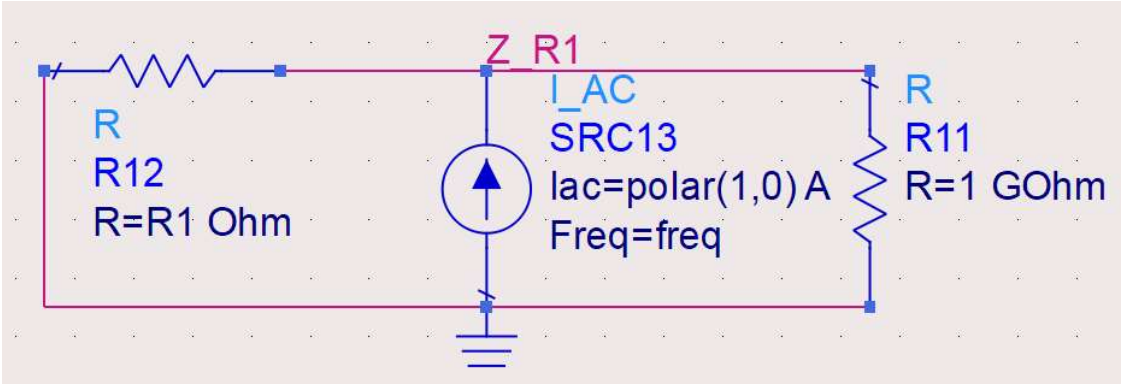
Simulating Impedance with SPICE

V(f) = Z(f) x I(f)

If I(f) = constant current source, I0 = 1 Amp, then

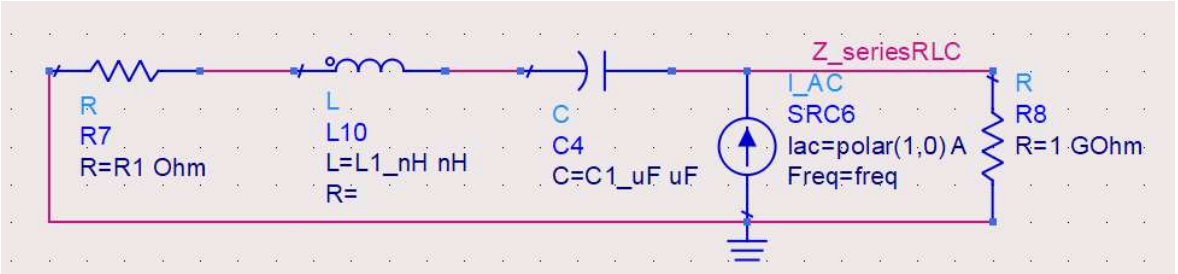
V(f) = Z(f)

Sim voltage, it is numerically the impedance



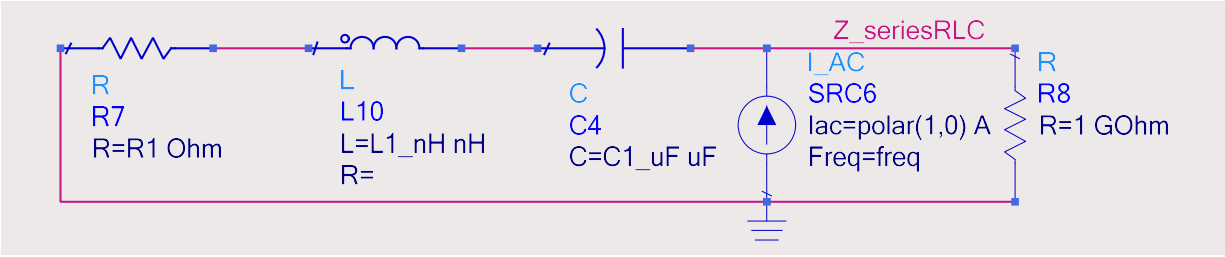
Series RLC Circuits

Series circuit
Equations
Figures of Merit



Series RLC Circuits

Figures of merit



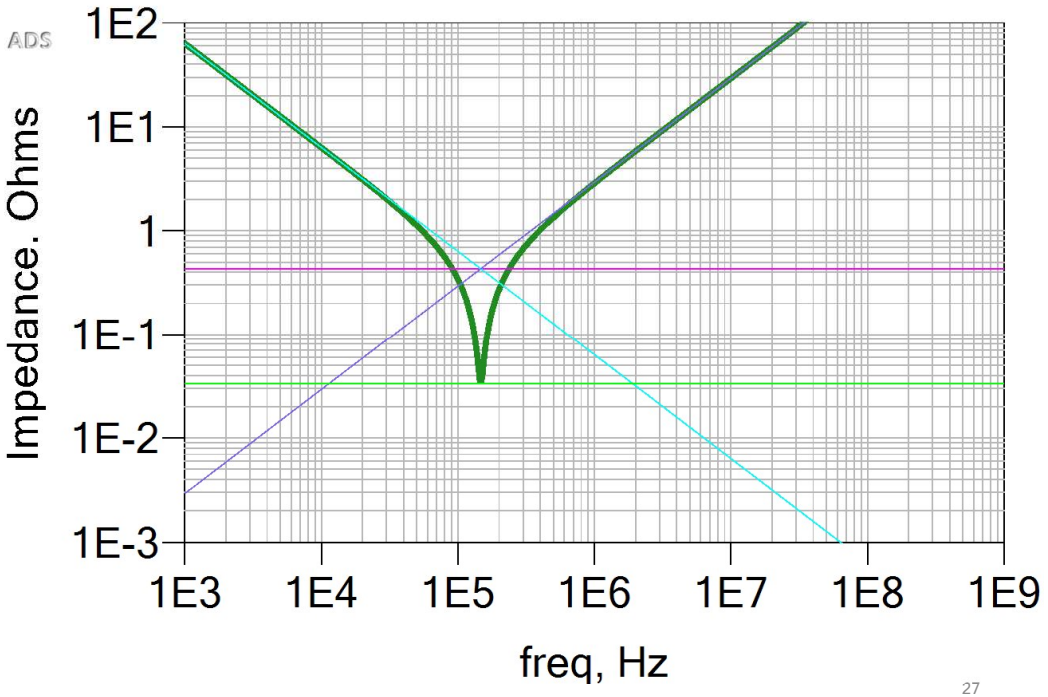
$$f_0 = 1/2\pi\left(\sqrt{LC}\right)$$

$$Z_0 = \sqrt{L/C}$$ Impedance at which $Z_L = Z_C$

$$q\text{-}factor = Z_0 / R = \sqrt{L/C}/R$$

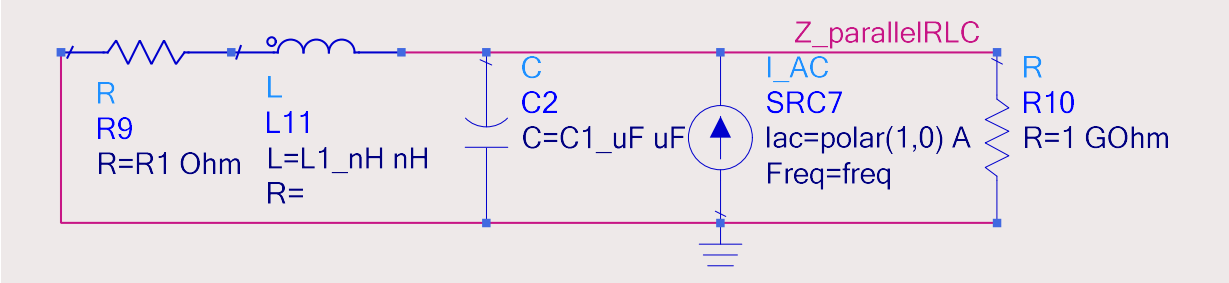
$$Z_{dip} \doteq \frac{Z_0}{q\text{-}factor} = \frac{RZ_0}{Z_0} = R$$

If C increases?
If L increases?
If R increases?
Why do I care about the dip?



Parallel Circuits

Figures of merit



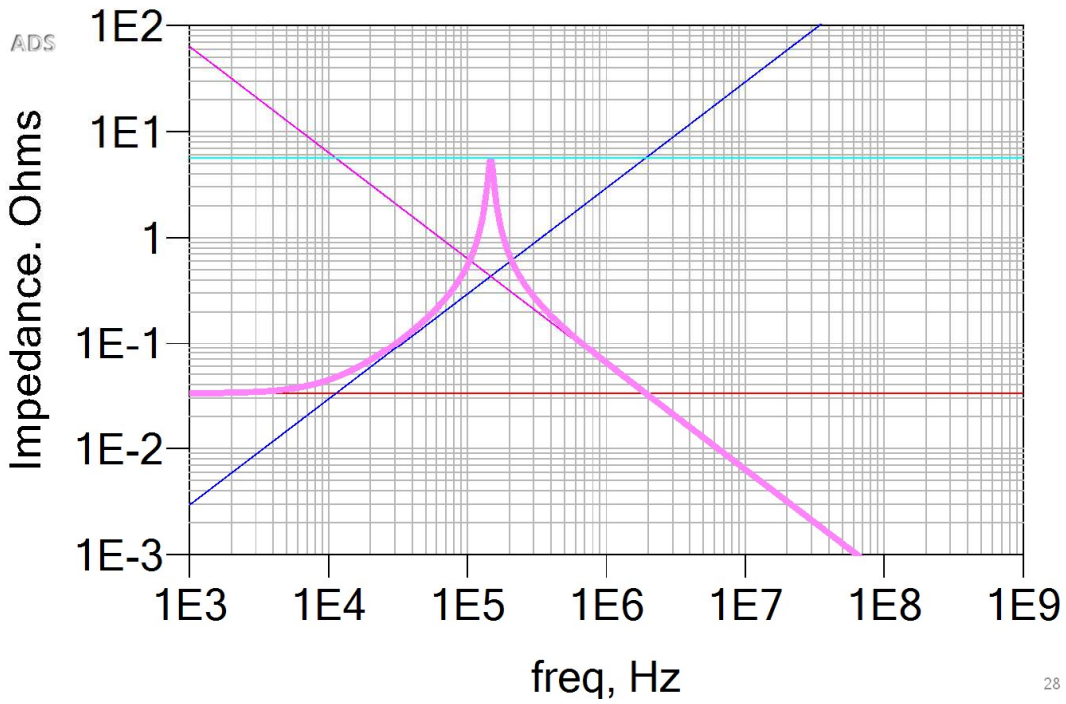
$f_0 = 1/2\pi\left(\sqrt{LC}\right)$

$Z_0 = \sqrt{L/C}$ Impedance at which $Z_L = Z_C$

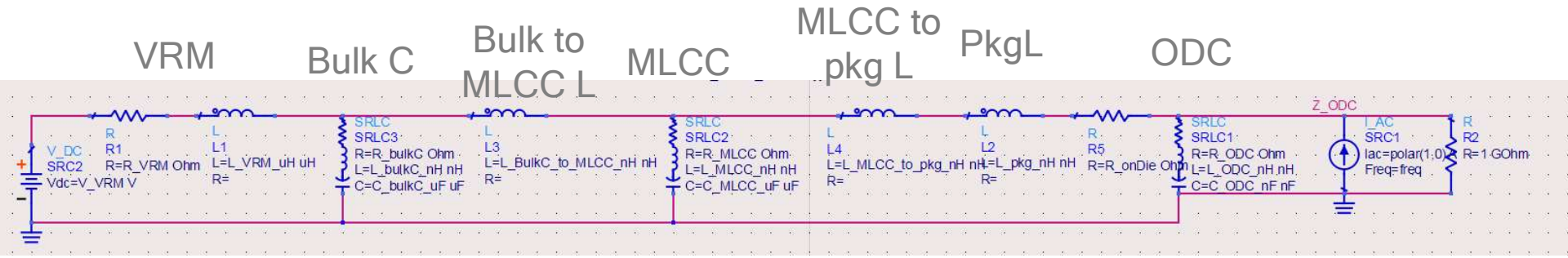
$q\text{-}factor = Z_0 / R = \sqrt{L/C}/R$

$Z_{peak} \doteq Z_0 \times q\text{-}factor$

If C increases?
If L increases?
If R increases?
How to decrease the peak?
Optimized R is ~ target impedance



The PDN Ecology



Bandini Mountain

Up is and L, down is a C

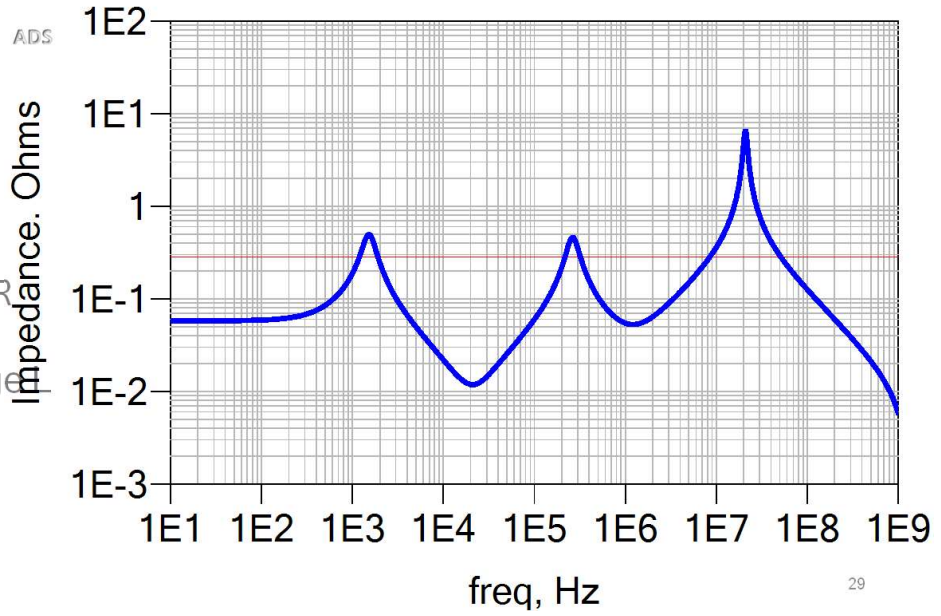
Peaks are local- depend on the local L and C

Reduce any peak with higher C, lower L and optimized R

Always a benefit making MLCC L comparable to package L

No point making MLCC L << package L

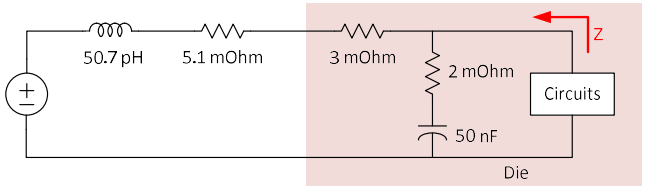
A larger C will hide the lower frequency L



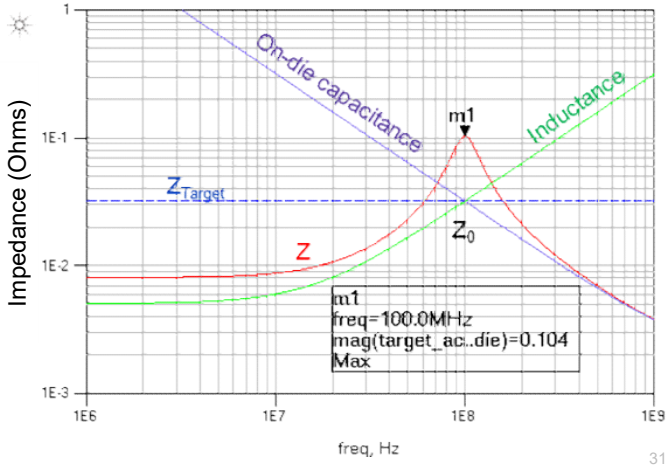
PDN Resonant Calculator Transient Currents Inductors and Capacitors

Larry Smith

PDN Resonance Calculator – Frequency Domain



Frequency Domain		
Vdd	1	V
Core Cap	50	nF
PDN loop Inductance	50.7	pH
PDN loop resistance	10.1	mOhm
dynamic current	1.55	A
Resonant Frequency	100	MHz
PDN Z_0	32	mOhm
q-factor from PDN loop	3.15	
Expected impeance Peak	100	mOhm
Target Impedance	32	mOhm
Assumed Die resistance	5.0	mOhm
External PDN loop resistance	5.1	mOhm



- Spread Sheet for PDN parameter calculations
  - Inputs (independent parameters) are the green shaded cells
  - Results (dependent parameters) are calculated in the white cells

- Desire 100 mOhm peak at 100 MHz
  - Choose 50 nF for on-die capacitance
  - Calculate L $f_0 = 1/2\pi\left(\sqrt{LC}\right)$
  - Calculate Z0 $Z_0 = \sqrt{L/C}$
  - Calculate q-factor $q\text{-}factor = Z_0 / R = \sqrt{L/C}/R$
  - Choose R for 100mOhm peak $Z_{peak} \doteq Z_0 \bullet q\text{-}factor = \frac{L/C}{R}$

PDN Parameter Calculations – Time Domain

- Average clock cycle charge is easily calculated
  - Average bench current
  - Clock frequency
  - Assumes all clock cycles are equal

$$Q_{cycle} = \frac{I_{dynmic}}{f_{clock}} = \frac{1.55A}{1GHz} = 1.55\,nCoul$$

- Charge is consumed from on-die capacitance

$$Q = CV$$
$$dQ = C \bullet dV$$

- Impulse response (droop) from single clock cycle

$$V_{clock\,edge} = \frac{Q_{cycle}}{ODC} = \frac{I_{dynamic} / f_{clock}}{ODC} = \frac{1.55A / 1GHz}{50nF} = 31\,mV$$

- Step response (droop) from fast edge

$$V_{step} = I_{step} \times Z_0 = 1.55A \times 32\,mOhm = 49\,mV$$

- Resonance response (peak-peak) from repeating steps

$$P\text{-}P_{resonance} = \frac{4}{\pi} I_{tran} Z_{peak} = \frac{4}{\pi} \times 1.55A \times 100\ m\Omega = 198\ mV$$

Frequency Domain		
Vdd	1	V
Core Cap	50	nF
PDN loop Inductance	50.7	pH
PDN loop resistance	10.1	mOhm
dynamic current	1.55	A
Resonant Frequency	100	MHz
PDN Z_0	32	mOhm
q-factor from PDN loop	3.15	
Expected impeance Peak	100	mOhm
Target Impedance	32	mOhm
Assumed Die resistance	5.0	mOhm
External PDN loop resistance	5.1	mOhm
Time Domain		
f_{clock}	1	GHz
charge per clock cycle (Q_{cycle})	1.55	nCoul
Expected clock edge droop (impulse)	31	mV
Expected step response droop	49	mV
Expected peak-peak noise at resonance	198	mV

$$PDN\ Z_0 = \sqrt{\frac{L}{C}}$$

Impulse Response – PWL Current Source

- Impulse of charge is consumed from PDN

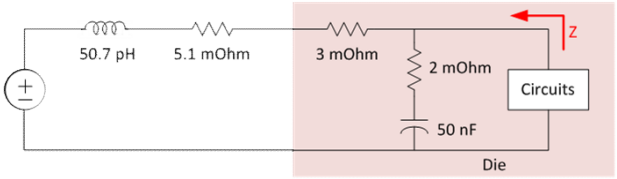
$$Q = \frac{I_{dynamic}}{f_{clock}}$$

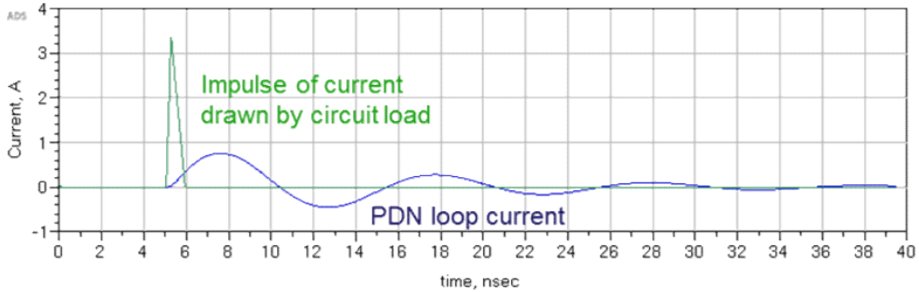
- Happens in less than 1 clock cycle
- Calculate droop from Q=CV

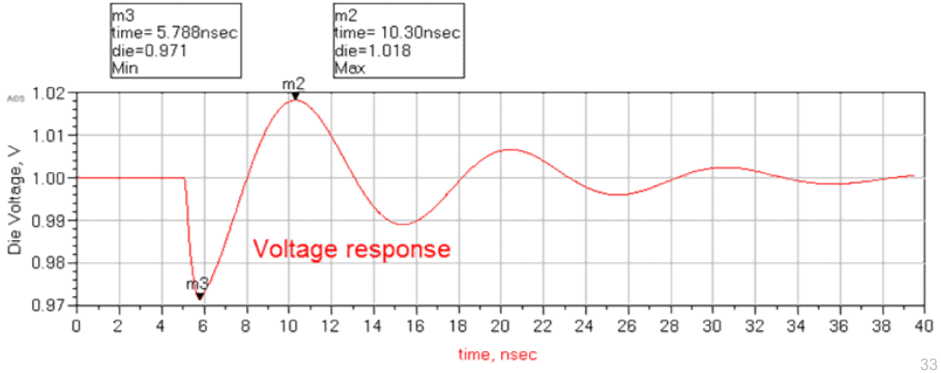
$$V_{droop} = \frac{I_{dynamic} / f_{clock}}{ODC} = \frac{1.55A / 1GHz}{50nF} = 31mV$$

- Simulated impulse droop
  - 29 mV
  - Some current came in during impulse

- Impulse droop is determined by on-die capacitance
  - Inductance has no effect
  - Impedance peak has no effect







Step Response and Characteristic Impedance - Transient

- PDN parameters chosen so that

$$Z_{target} = Z_0 = \sqrt{L/C}$$

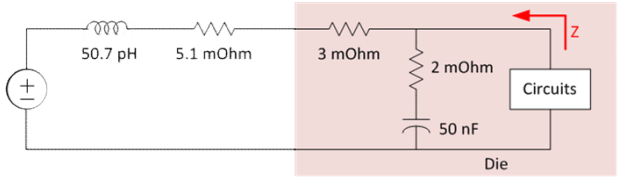
- PDN Parameters
  - Vdd=1V
  - $I_{transient}$=1.55A
  - Tolerance=5%
  - Cap = 50 nF
  - Inductance = 50.7 pH

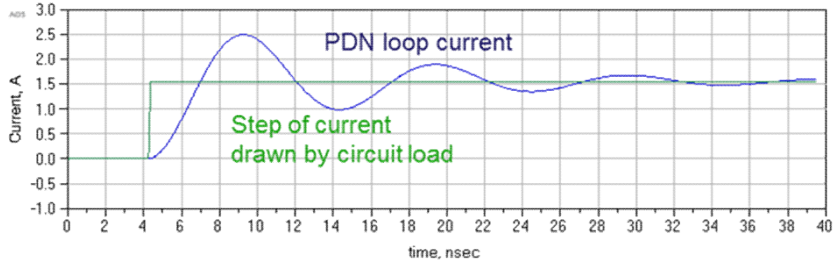
$$Z_{target} = \frac{Vdd \times tolerance}{I_{transient}} = \frac{1 \times 5\%}{1.55} = 32\ mOhm$$

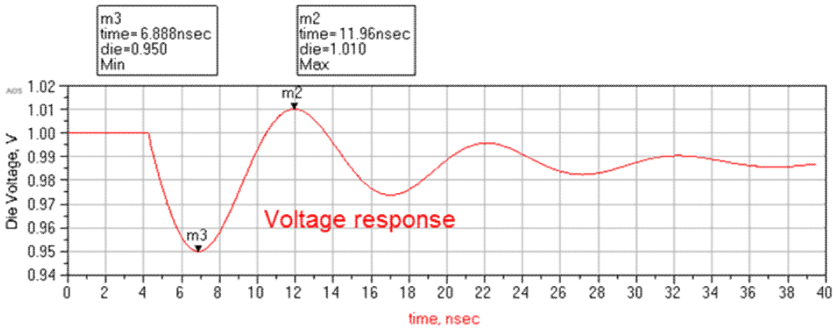
- Step Response Droop
  - 50 mV
  - Same as 5% tolerance

$$Z0 = \sqrt{\frac{L}{C}} = \sqrt{\frac{50.7\,pH}{50nF}} = 32\,mOhm$$

$$V_{step} = I_{step} \times Z_0 = 1.55A \times 32\,mA = 50\,mV$$







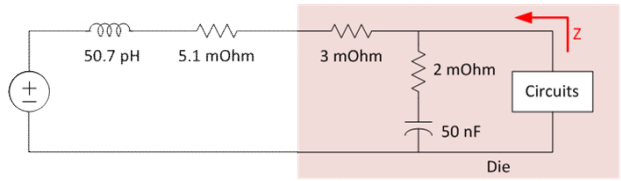
Design Z_0 = Z_{target} in order to have step response droop = tolerance

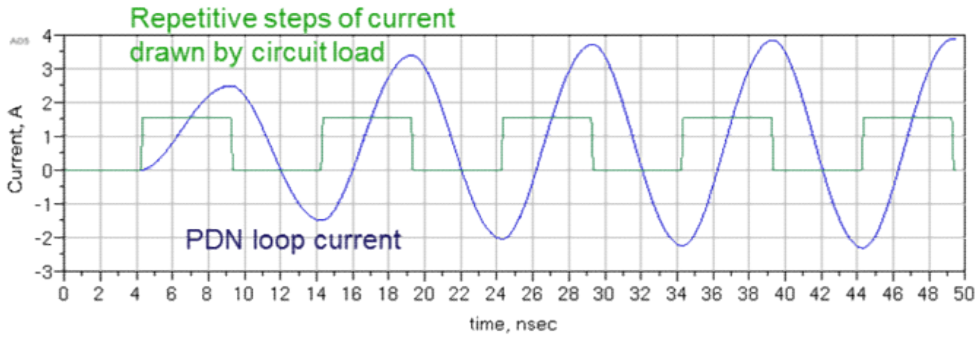
Resonance Response

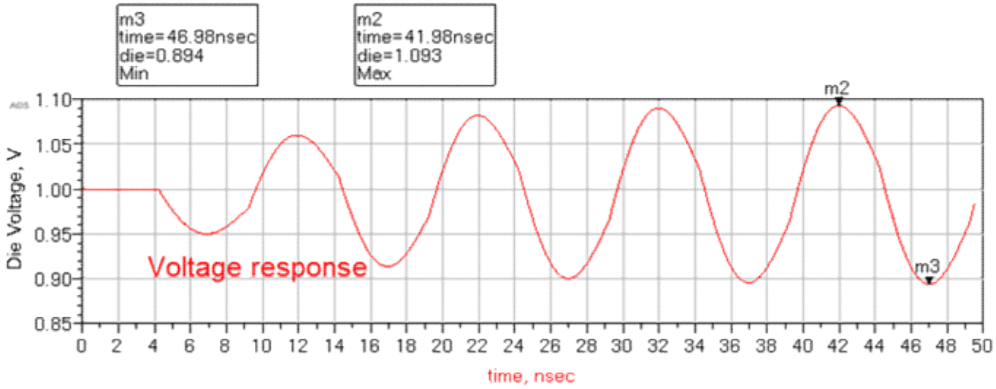
- Estimate P-P noise
  - Z_{peak} is 103 mOhms
  - I_{tran} = 1.55A pulses for 5 nSec

$$PP_{resonance} = \frac{4}{\pi} I_{tran} Z_{peak}$$
$$= \frac{4}{\pi} 1.55A \times 103m\Omega$$
$$= 203mV$$

  - The 4/π comes from Fourier transform of square wave
- Simulated P-P noise
  - 201 mV
- Mitigate resonant peak by
  - Reducing L
  - Increasing C
  - Increasing R (damping)







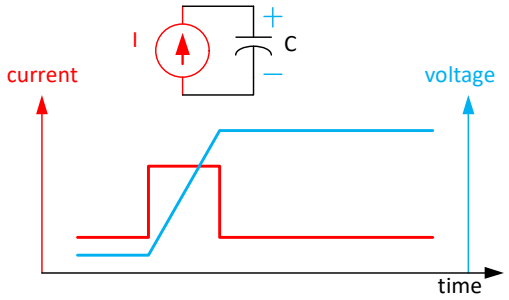
Current, Voltage and Time for Reactive Components

Which comes first, voltage or current?

- Capacitor
- Voltage lags behind current
  - Current into capacitor changes voltage

$$\frac{dv}{dt} = \frac{I}{C} \qquad V = \frac{1}{C}\int I \bullet dt$$

  - I/C is the forcing function
  - dv/dt is the result

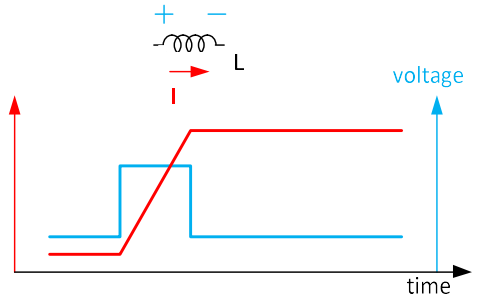


On-die cap protects circuits from ground bounce

- Inductor
- Voltage leads current
  - Voltage across inductor changes current

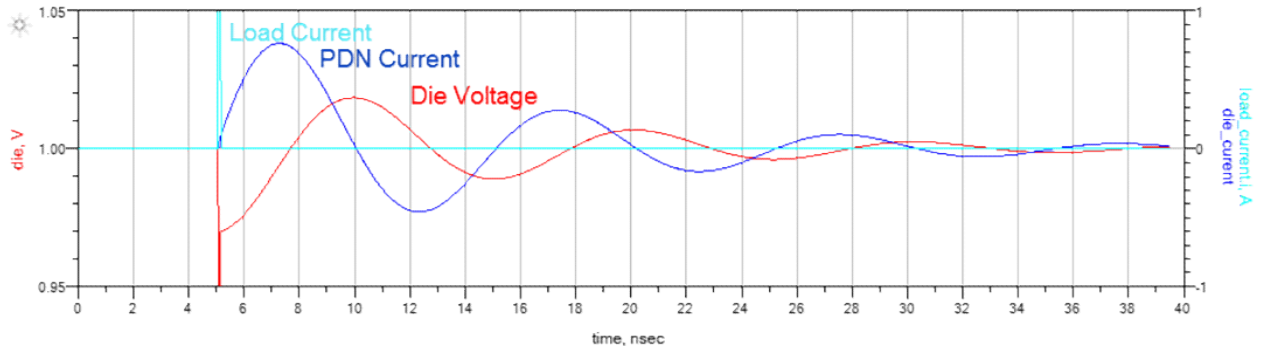
$$\frac{di}{dt} = \frac{V}{L} \qquad I = \frac{1}{L}\int V \bullet dt$$

  - V/L is the forcing function
  - di/dt is the result

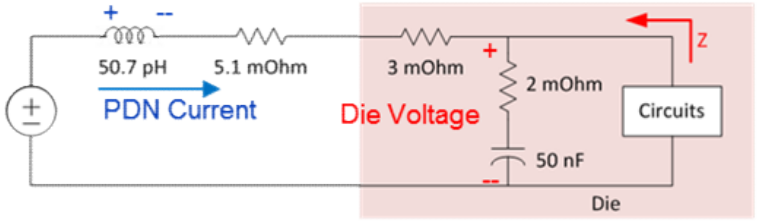


On-die cap voltage has to droop to draw in outside current

Voltage and Current in Time – Impulse Response



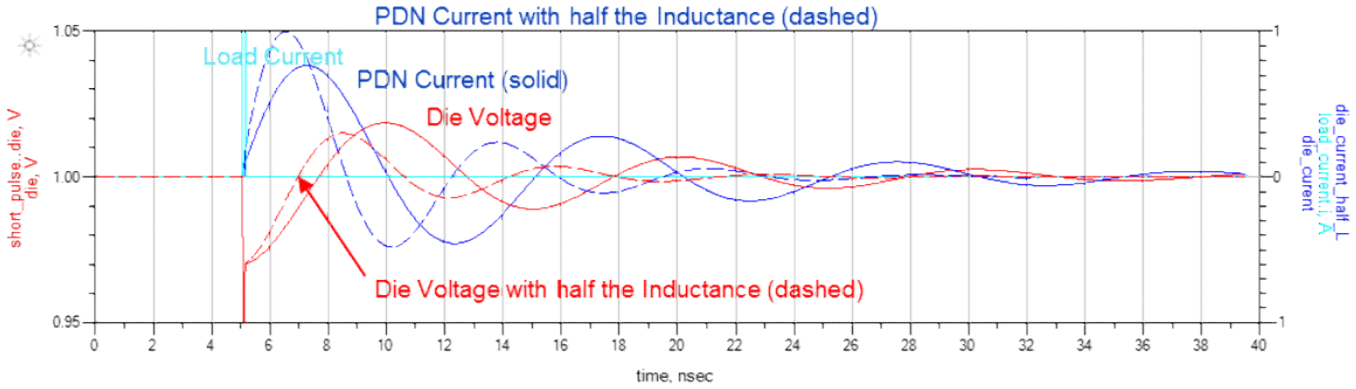
- Single clock edge creates impulse
- Sequence of Events
  - Circuits consume die current (charge)
  - Die voltage droops
  - Current comes in from outside inductor
    - Brings voltage back to nominal
  - Current diminishes as die voltage rises above nominal
- Inductor current ramps up until die voltage returns
- Current into die capacitance leads die voltage



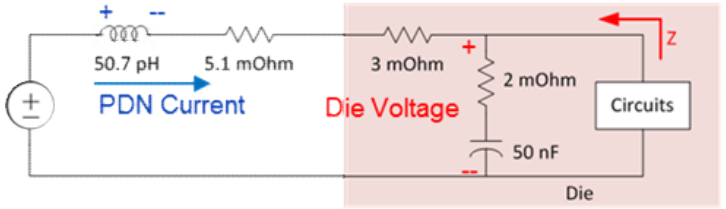
Inductor current responds to voltage across it (voltage leads current)

Die capacitor voltage lags behind inductor current

Half the Inductance Doubles the di/dt



- Cut PDN inductance in half
  - 25.35 pH
    - down from 50.7 pH
- Charge consumed from die is constant
- Inductor di/dt doubles
  - Slope is twice as steep
  - Current ramps up faster
- Initial droop is the same
  - Resonant frequency is higher
  - q-factor is lower

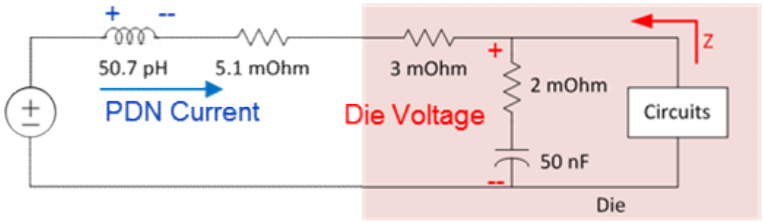


di/dt is the inductor response to V/L

Key Concepts for PDN on-die capacitance and inductor

- The on-die voltage can only be changed by passing current through the capacitance
- The root cause of PDN voltage noise is charge drawn from the on-die capacitance
  - On-die voltage noise is inversely proportional to C
  - Voltage noise during the clock cycle is determined by the charge (integral I x dt)

$$V = \frac{1}{C}\int I \bullet dt$$



- Inductor current does not come in from the outside world until the die voltage drops
  - Current through the inductor remains constant until a voltage appears across it
  - A smaller inductor makes a higher di/dt and brings current in faster (this is good)

$$\frac{di}{dt} = \frac{V}{L}$$

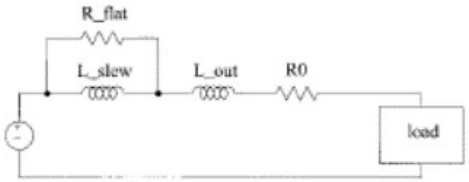
$$I = \frac{1}{L}\int V \bullet dt$$

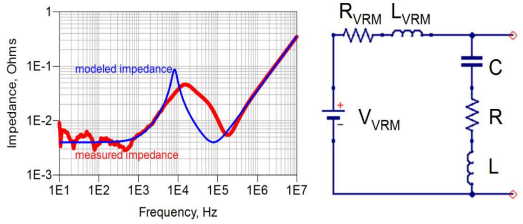
VRM Model - Ideal Voltage Source Isolation

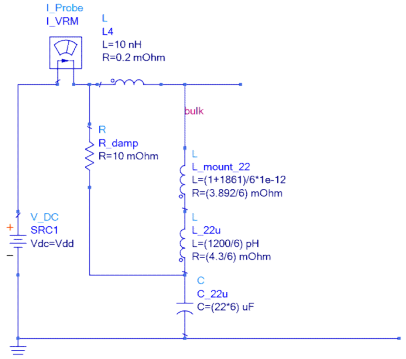
Larry Smith

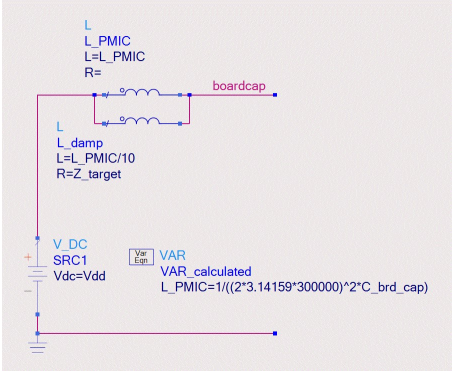
Evolution of Larry's VRM Model for PDN Simulations

- Historical VRM Models
  - 4 element LRLR
    - for PC silver box
  - Simple RL
    - Is underdamped
  - 3 element LRL
    - Has damping
    - Doesn't work well with cap models
  - 4 element LLRR
    - Has damping
    - Works with cap models
    - Blocks high frequency current
- Goal of VRM model for PDN simulations
  - Enable simulation of board caps, package and die
  - Don't short out PDN components with ideal voltage source



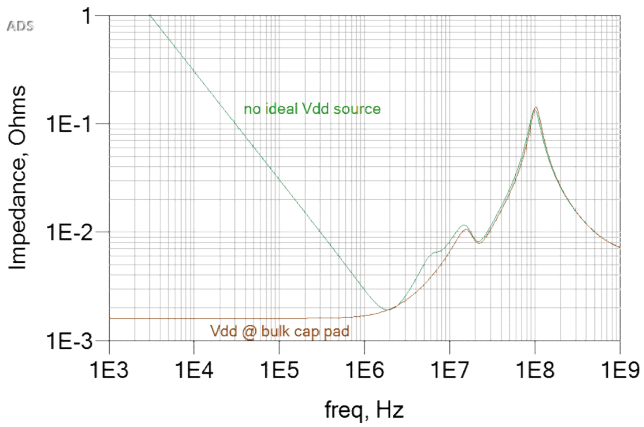


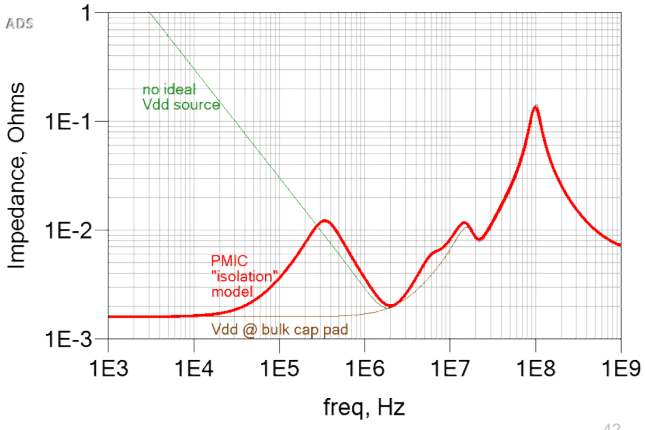




Poor VRM model – an Ideal Voltage Source

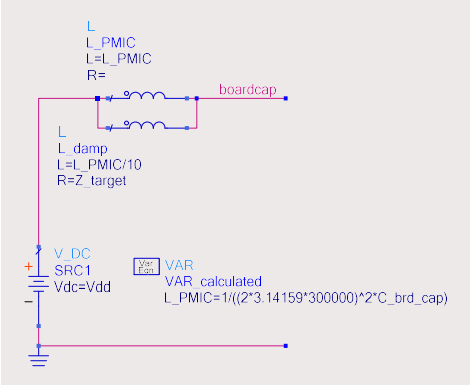
- An ideal voltage source is zero impedance
  - It shorts out anything in parallel with it
  - Common mistake is to attach ideal voltage source to extracted port on PCB
  - Bulk caps are effectively removed from simulation
- A good VRM model forms an impedance peak
  - About 1/10 to ½ of the bulk cap SRF
- Bulk caps are now on board with high frequency caps
  - We want to simulate properties of bulk caps
- The VRM model is not the same as an SMPS inductor
  - It is an equivalent model that forms an impedance peak at the right place

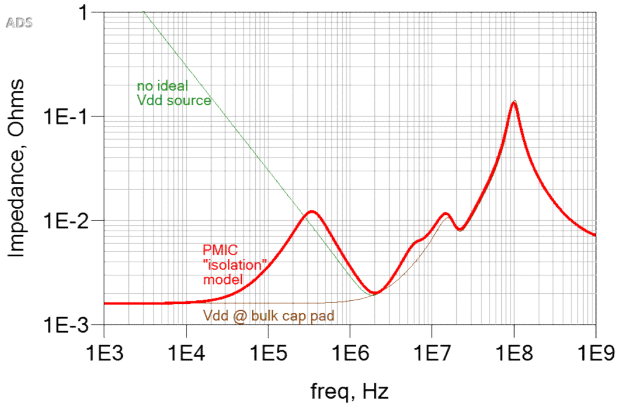


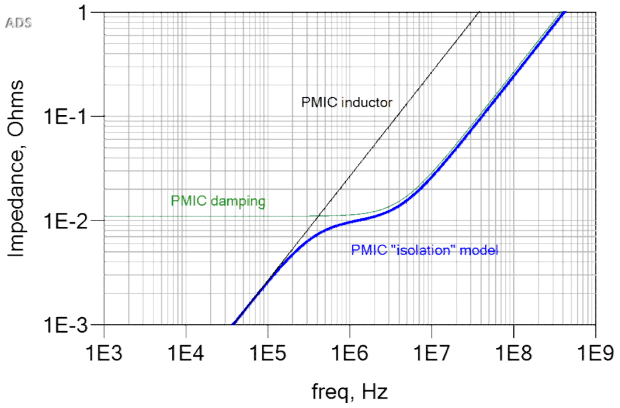


Frequency Domain Simulations for VRM Models

- Must prevent ideal voltage source from shorting out bulk caps
  - Have impedance peak at some low frequency
    - 10 kHz to 1 MHz for board VRMs
    - 10's of MHz for integrated voltage regulators (IVR)
- Must have proper damping for bulk capacitance
- Must be high impedance at high frequency
  - Should not deliver significant current at 1 GHz







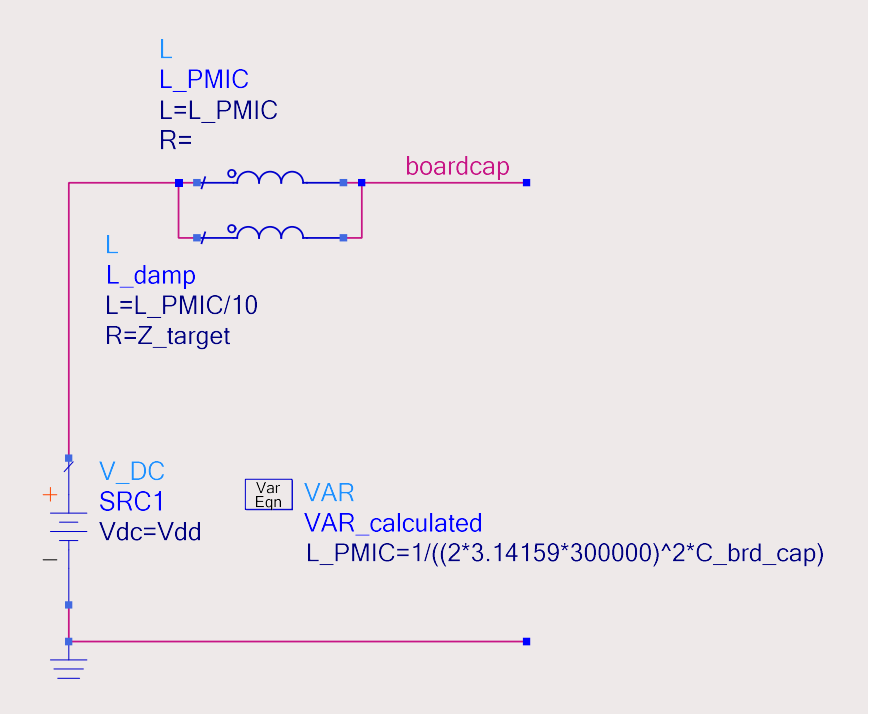
Model Topology

Passive inductor and resistor components and calculations

- We desire an impedance peak at about 300kHz
  - Choose inductance value from: $f_0 = \frac{1}{2\pi\sqrt{LC}}$
  - Inductor calculation example:

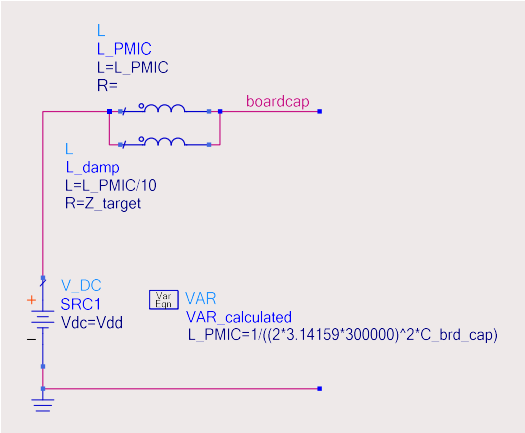
$$L_{PMIC} = \frac{1}{(2\pi f_{PMIC})^2 C_{board}} = \frac{1}{(2\pi 300\,kHz)^2 66\,\mu F} = 4.26\,nH$$

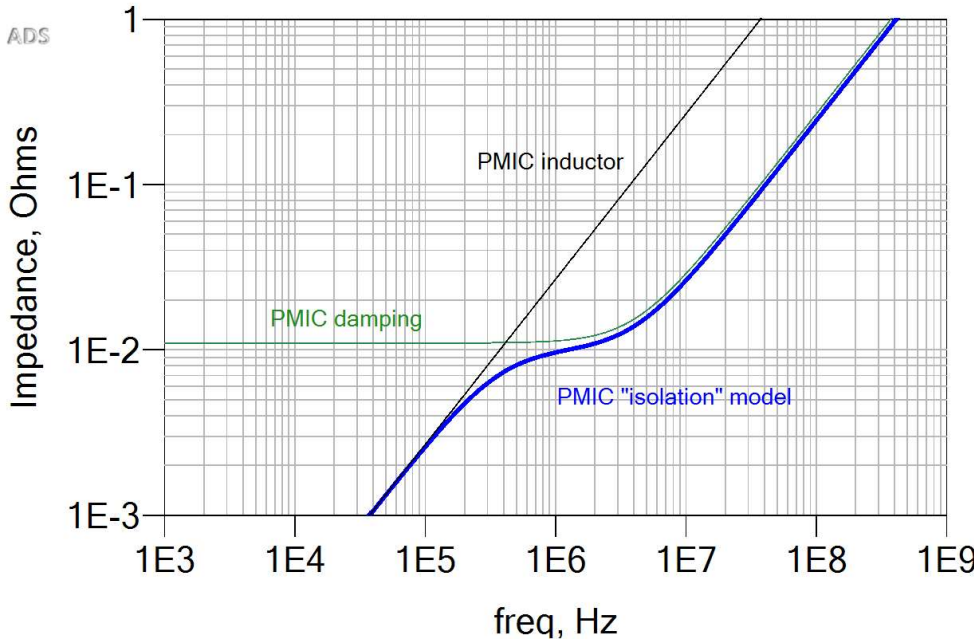
  - This is not the PMIC inductor
    - It is an inductance that causes a 300 kHz peak when combined with 66 uF board cap
- Damping Resistance $Z_{target} = \frac{V_{dd} \times Tol}{I_{dynamic}}$
  - Use R=Z_{target} for damping resistor
- Isolate PMIC with inductance:
- Connect isolation model to board caps at PMIC inductor location $L_{damp} = L_{PMIC} / 10$



Ideal Source Isolation - Parameter Curves

- PMIC inductor by itself has no damping
  - Leads to excessively high Q peak
- “Damping Inductor” provides two functions
  - Resistor parallel to PMIC inductance for loss
  - Inductance to block high frequency current
    - Inductance is 1/10 PMIC inductance

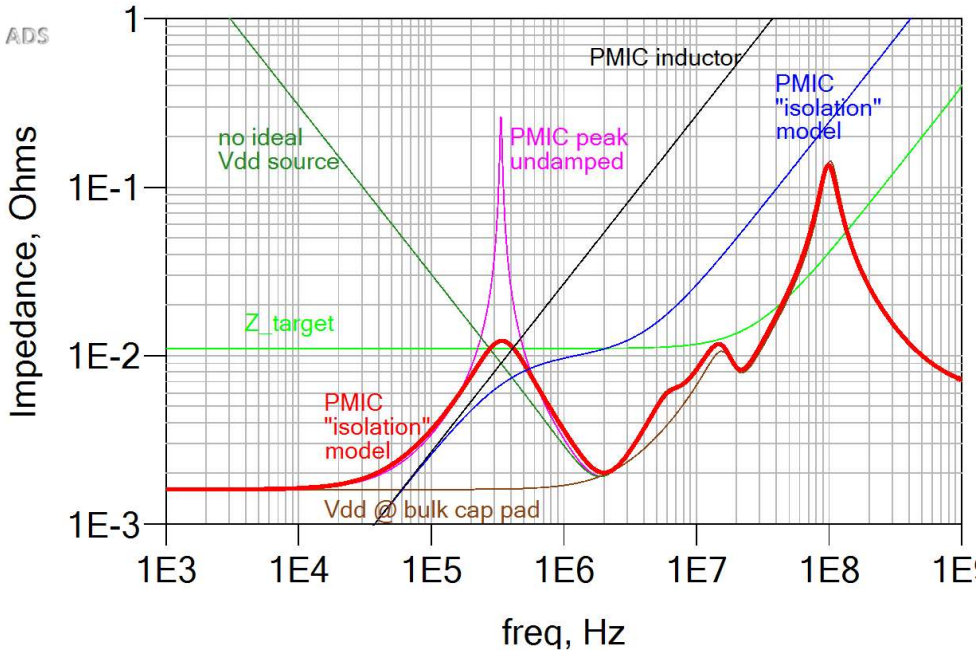




Complete Frequency Domain View of PDN

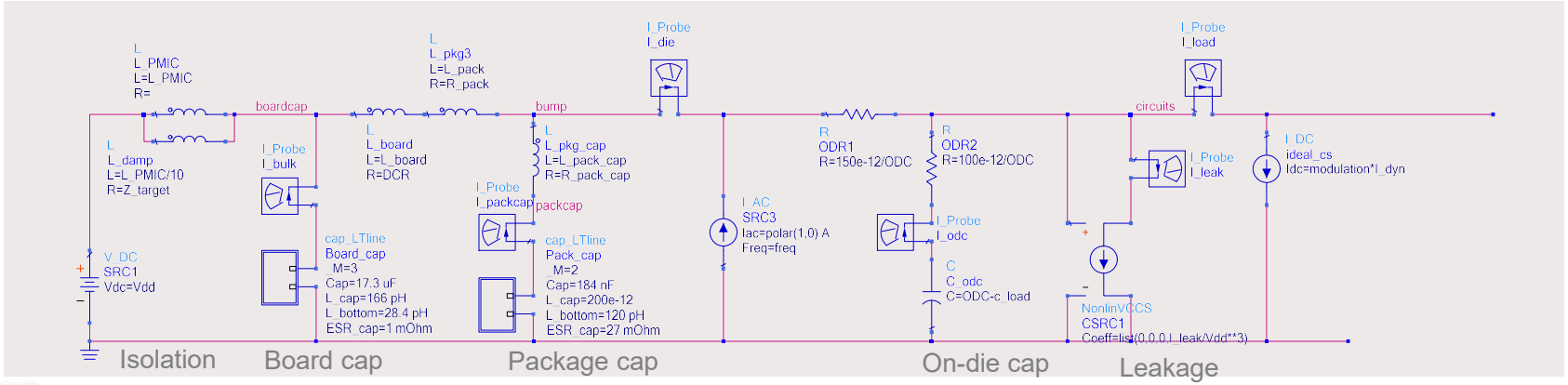
Ideal source isolation model provides peak at ~300kHz

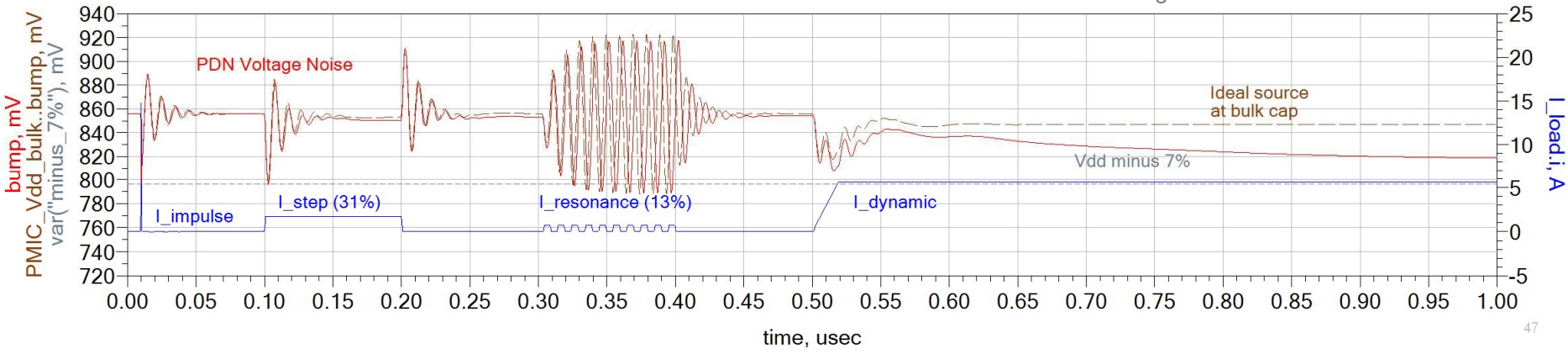
- PMIC inductance and Bulk capacitance cross at 300 kHz (characteristic impedance)
- Lack of damping is problem for PMIC L
  - Must include R=Z_{target} for losses
    - Isolation model peaks just above target impedance
  - Block high frequency current from isolation resistor with small inductance, $L_{PMIC}/10$
- PDN capacitors are fully present and not shorted out
  - Package cap
  - Board 3T caps and any high frequency caps



ADS Lumped Parameter Model for PDN and PRC Sim

Isolated source and board source give similar droops. Bulk cap charge is used up.

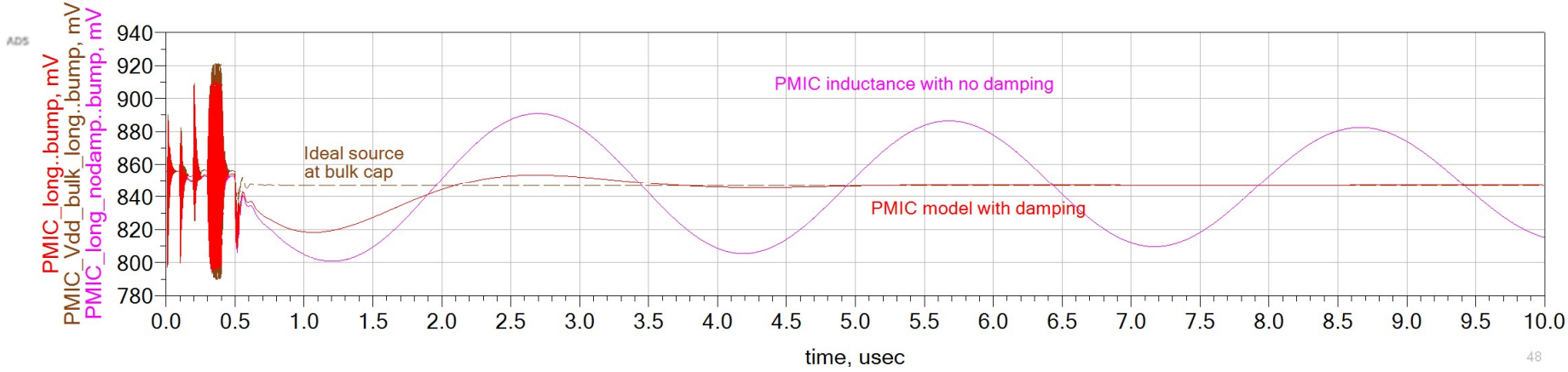




Isolation Model with and without Damping

High Q factor resonances ring forever in the time domain

- Simulation lasts for 10 uSec, 10 x longer than simulation on previous slide
- PRC waveforms are bunched up in first 500 nSec
- PMIC droop occurs at about 1 uSec
  - Damped out nicely with loss resistor (red)
  - Rings for a long time without damping (pink)
  - Ideal source on board has no PMIC droop (brown)

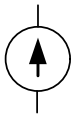


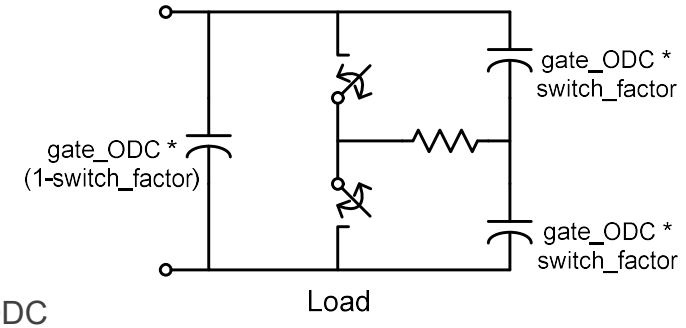
Switched Capacitor Load

Larry Smith

Time Domain Load Circuit for PDN Simulation

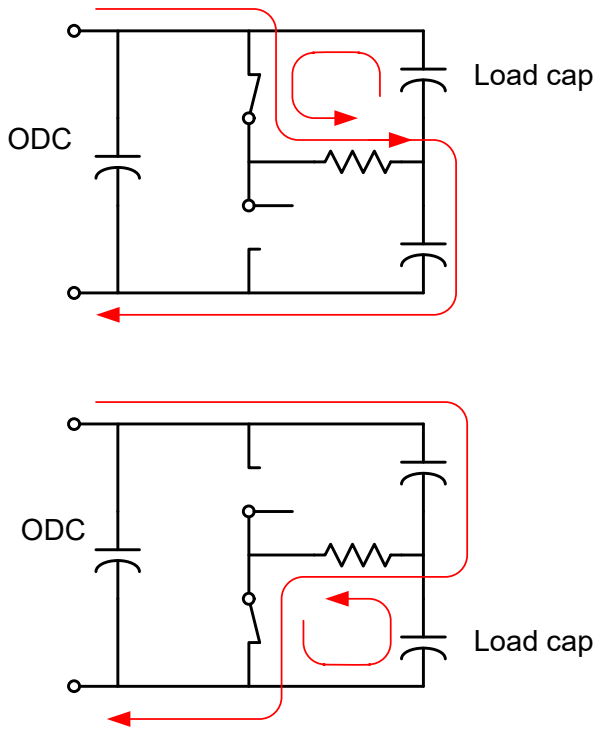
- Previous Loads
  - Current source
    - Current is independent of voltage
    - Provides no damping
  - Time varying resistor
    - Current diminishes with less voltage
    - Provides damping
- New Load Circuit – Switched Capacitor Load
  - Operates the same way as CMOS circuits
    - Current is proportional to voltage
    - Provides damping
  - Portion of the ODC is switched
    - Switch factor
  - Easily handles power transients
    - Load capacitance changes with time
    - Take some capacitance from the load and put it back into ODC





Load Operation

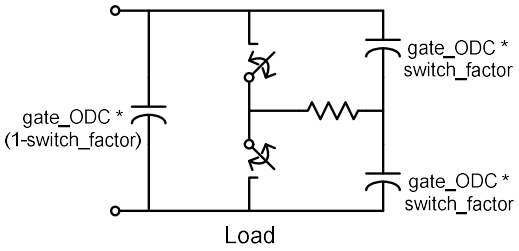
- Switch low-to-high
  - Current charges lower cap
  - Upper cap discharges
- Switch high-to-low
  - Current charges upper cap
  - Lower cap discharges
- Resistor sets time constant
  - 2x current for each edge
  - Reverses direction for each edge
  - 1x current drawn from ODC for each edge
- Switch factor
  - Calculated in spread sheet
  - Draws dynamic current from package
  - Expressed as percentage of ODC
- Transient current
  - Load capacitance varies with time
  - Example: draw 8 amps at 500 MHz (max current)
    - 10% of ODC is placed in load cap position
    - A 50% current transient is desired (draw 4 amps)
    - Load cap is reduced by half to 5% of ODC
    - Clock frequency remains the same but 4 amp transient has occurred
- Real CMOS circuits operate this way

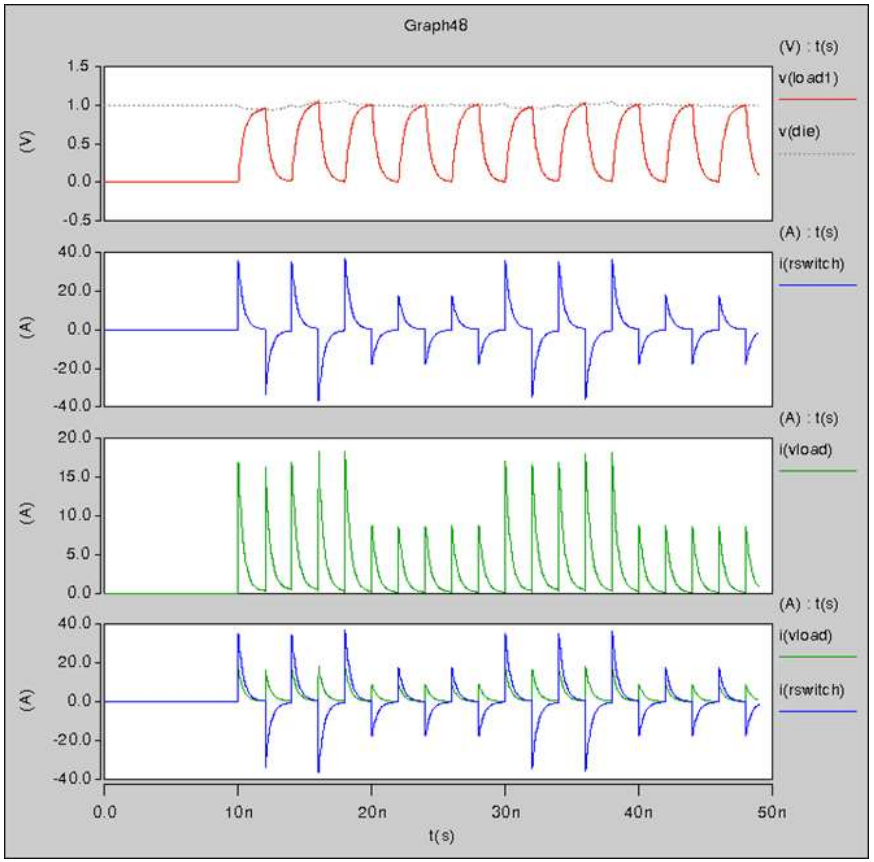


Consume ODC current on both rising and falling edges

Load Waveforms

- Load voltage alternates between 0V and 1V
  - red
- 2x Current is drawn through resistor both directions
  - blue
- 1x Current is drawn from ODC on each edge
  - green
- Events
  - 10nSec: load starts
  - 20nSec: load drops in half
  - 30nSec: back to full load
    - 10% switching factor
  - 40nSec: half load
    - 5% switching factor
- Load capacitance changes with time
- Time constant is set with resistor





Calculate Switch Activity from Q=CV

- One Clock Edge
  - PDN Impulse Response
- Initial voltage sag:

$$\Delta V = q_{clock\_edge} / C_{odc}$$

- Calculate average clock edge charge

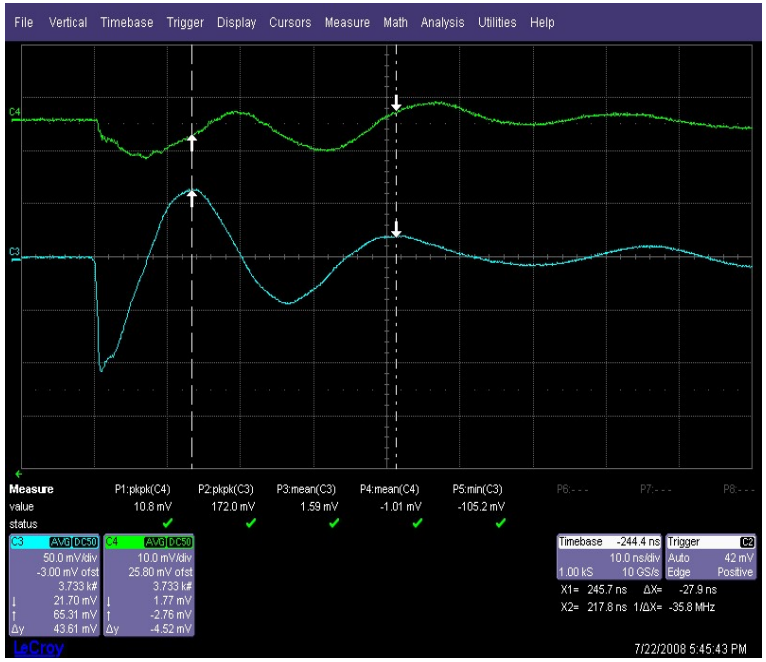
$$q_{clock\_edge} = \frac{current}{frequency} = \frac{10\,\text{amp}}{533\,\text{MHz}} = 18.8\,\text{nCoul}$$

- Calculate the capacitance that must have switched

$$C_{switched} = \frac{q}{V} = \frac{18.8\,\text{nCoul}}{1.1\text{V}} = 17.1\,\text{nF}$$

- Calculate the switch factor given the on-die capacitance

$$S.F. = \frac{q_{switched}}{ODC} = \frac{17.1\,\text{nCoul}}{300\,\text{nCoul}} = 0.057 = 5.7\%$$



Voltage	volts	1.10
Dynamic AVG current per channel or bank*	amps	10.0
clock frequency	MHz	533
charge per cycle	nCoul/cycle	18.8
load capactiance that switched	nF	17.1
switch factor	%	5.7
Die		
ODC (on-die capacitance)	nF	300

Impulse Response – PWL Current Source

- Impulse of charge is consumed from PDN

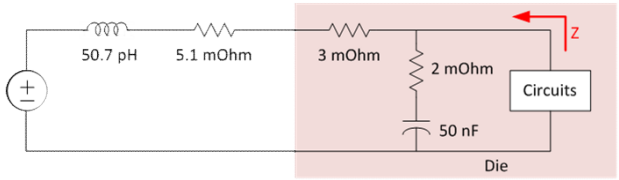
$$Q = \frac{I_{dynamic}}{f_{clock}}$$

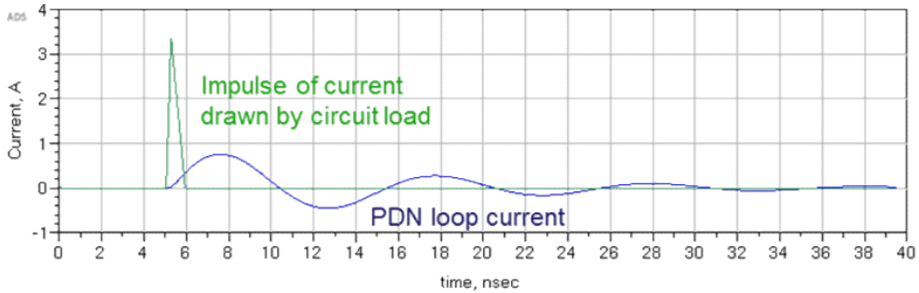
- Happens in less than 1 clock cycle
- Calculate droop from Q=CV

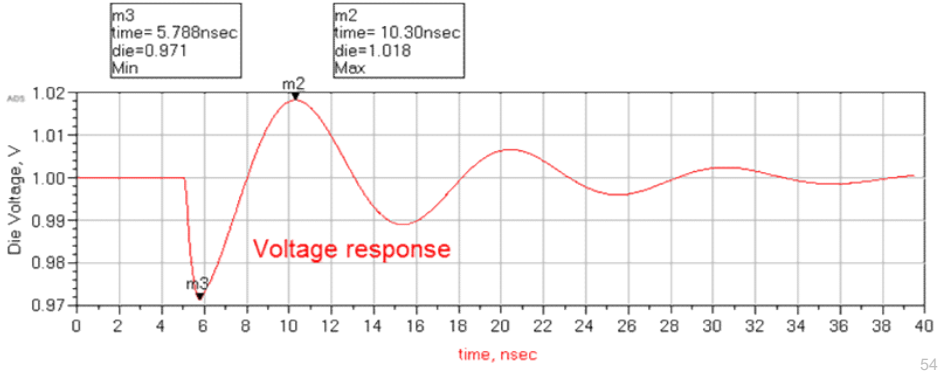
$$V_{droop} = \frac{I_{dynamic} / f_{clock}}{ODC} = \frac{1.55A / 1GHz}{50nF} = 31mV$$

- Simulated Droop
  - 29 mV
  - Some current came in during impulse

- Droop is determined by on-die capacitance
  - Inductance has no effect
  - Impedance peak has no effect





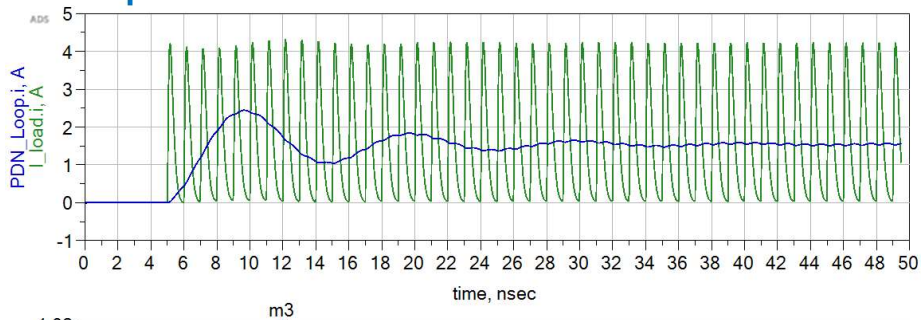


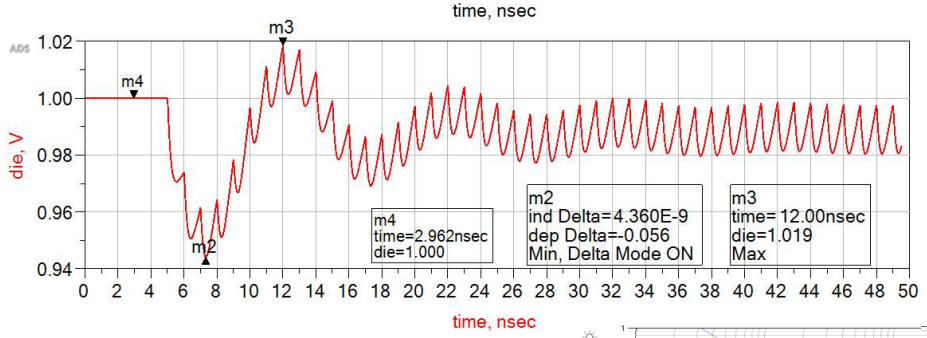
Step Response and Characteristic Impedance - Transient

- PDN parameters chosen so that

$$Z_{target} = Z_0 = \sqrt{L/C}$$

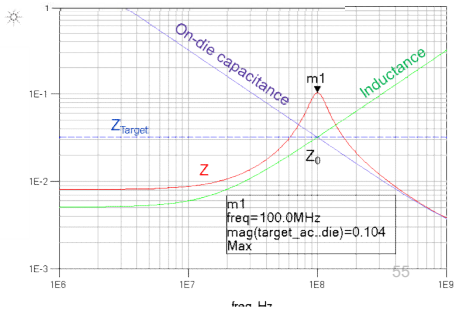
- PDN Parameters
  - Vdd=1V
  - $I_{transient}$=1.55A
  - Tolerance=5%
  - Cap = 50 nF
  - Inductance = 50.7 pH
- Step Response Droop
  - 56 mV
  - Nearly same as 5% tolerance
  - Includes clock edge noise





$$Z_{target} = \frac{Vdd \times tolerance}{I_{transient}} = \frac{1 \times 5\%}{1.55} = 32\ mOhm$$

$$Z0 = \sqrt{\frac{L}{C}} = \sqrt{\frac{50.7\,pH}{50nF}} = 32\,mOhm$$



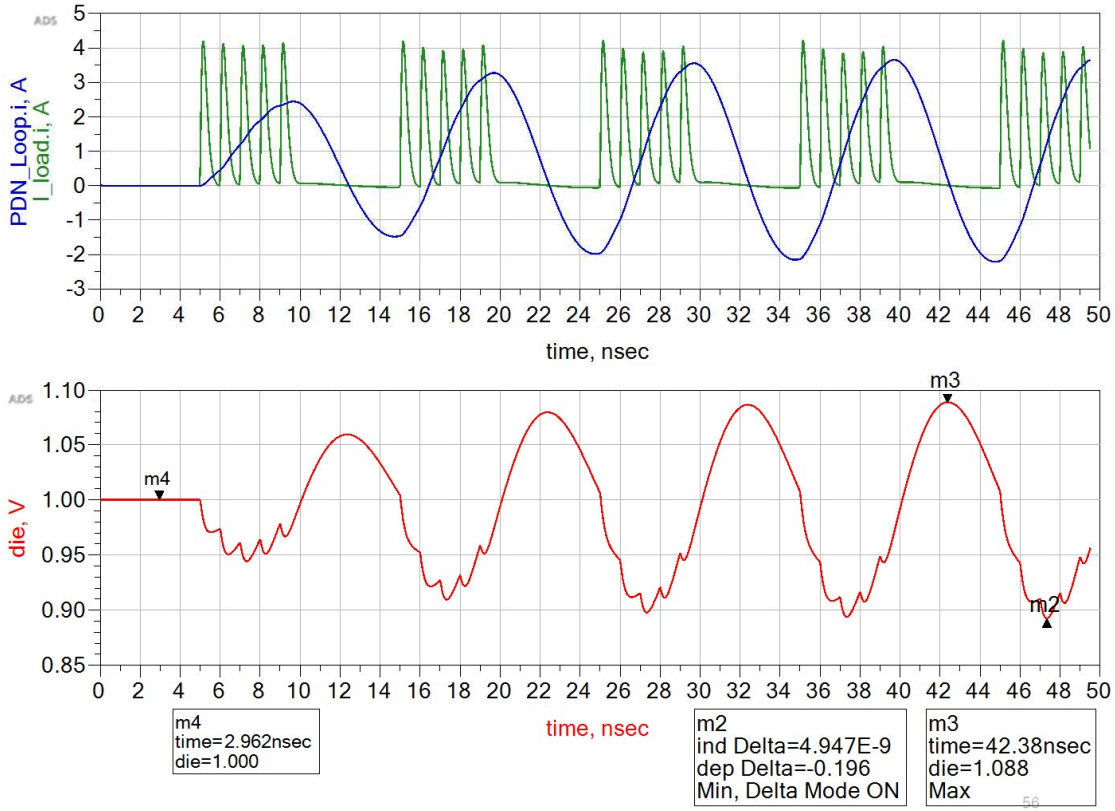
To have step response droop = tolerance, make Z_0=Z_{target}

Resonance Response – Switched Capacitor Load

- Estimate P-P noise
  - Z_{peak} is 103 mOhms
  - I_{tran} = 1.55A pulses for 5 nSec

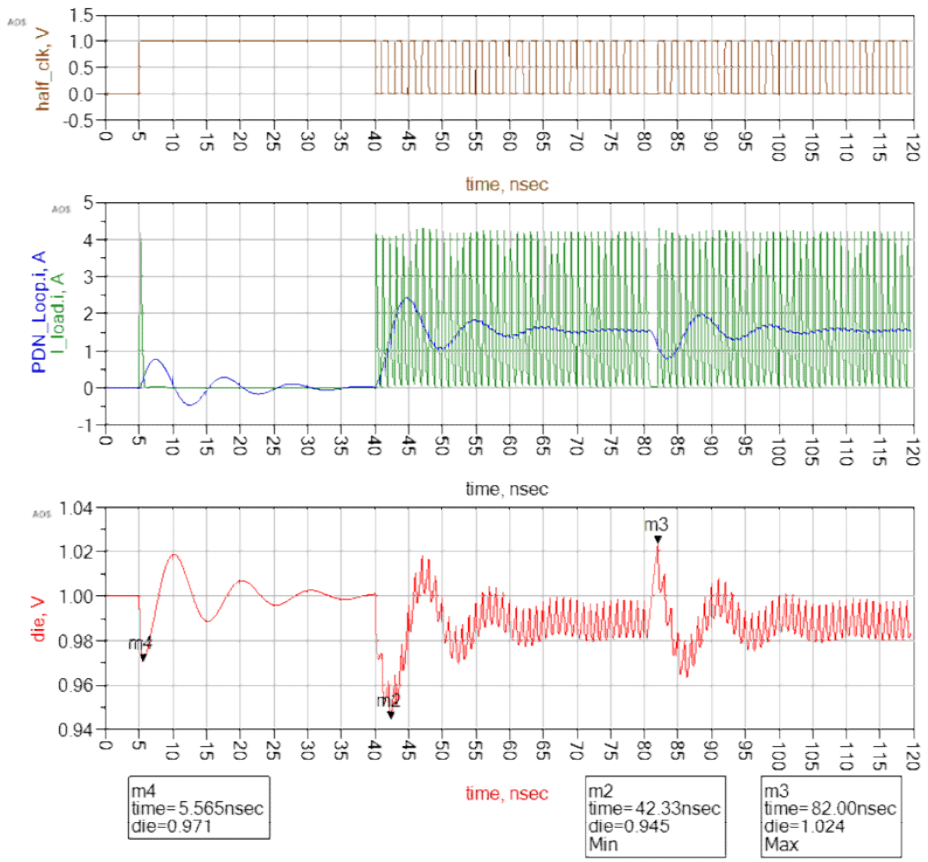
$$PP_{resonance} = \frac{4}{\pi} I_{tran} Z_{peak}$$
$$= \frac{4}{\pi} 1.55A \times 103m\Omega$$
$$= 203mV$$

  - The 4/π comes from Fourier transform of square wave
- Simulated P-P noise
  - 196 mV
- Mitigate resonant peak by
  - Reducing L
  - Increasing C
  - Increasing R (damping)



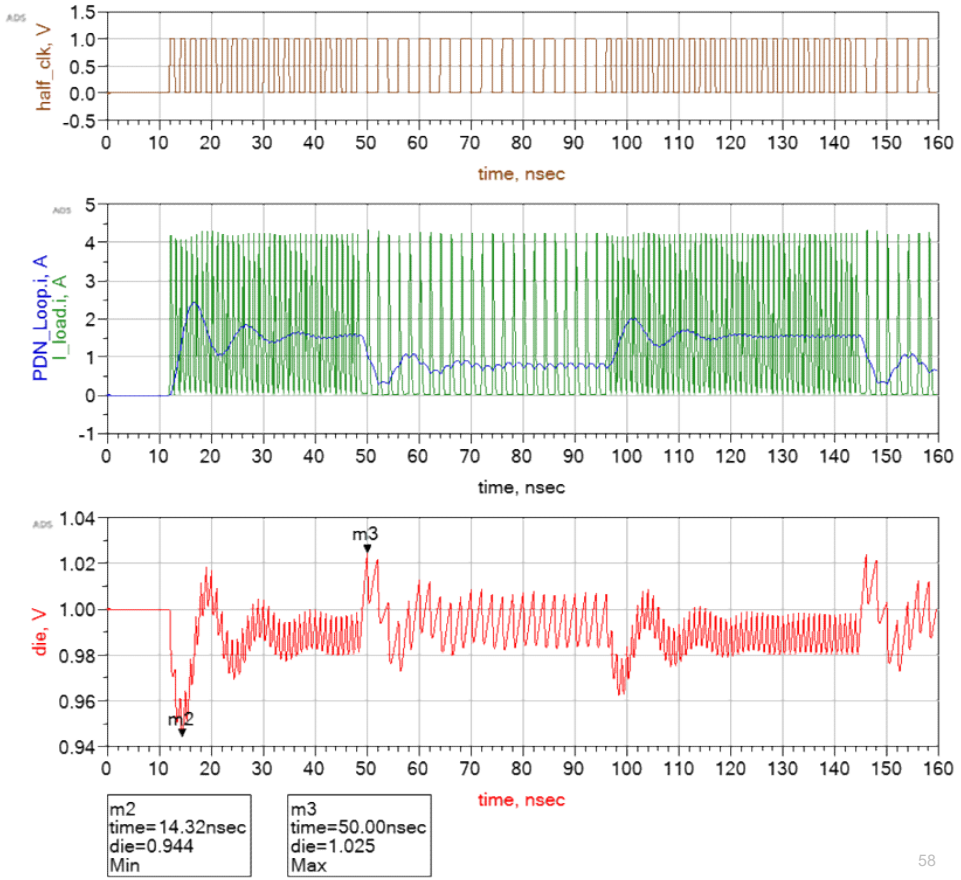
Compare Impulse, Anti-Impulse and Step Responses

- Anti-impulse is one missing pulse
  - AKA Pulse swallowing
  - Signature is nearly opposite that of impulse
  - Creates much PDN noise
- Compare droops
  - Impulse
    - 29 mV
  - Step
    - 55 mV
  - Anti-impulse
    - 36 mV
- Mitigation
  - Only C helps impulses
  - Both L and C help step response



Clock Manipulations – full, half, full

- Full clock begins abruptly
  - 56 mV droop
- Clock frequency drops in half
  - 25 mV spike
- Full clock frequency returns
  - 38 mV droop



FPGA PDN Correlation

Larry Smith

FPGA Model to Hardware Correlation

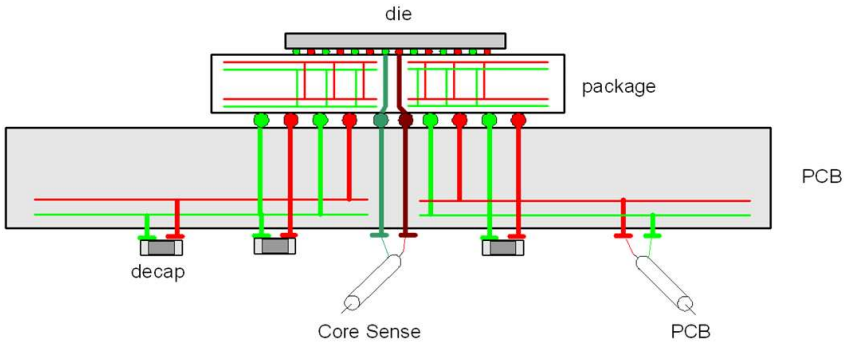
Use measurements to figure out what the PDN parameters must have been

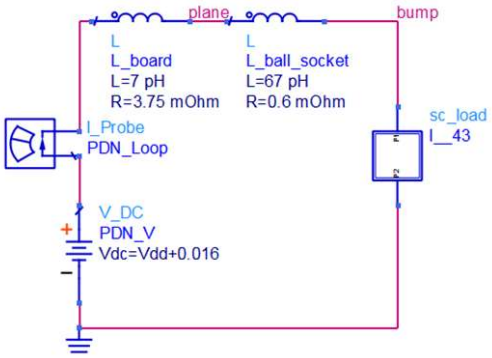
- Use PDN Resonant Calculator Concepts
- Start with basic measured values
- Calculate major PDN parameters
  - On-die capacitance
  - PDN loop inductance
  - Damping losses and q-factor
- Compare measured and simulated results
  - Graphically
  - Quantitatively

	FPGA PDN Example	Inputs	Calculations	Simulated	Units
1	Vdd	1.1			V
2	leakage current	3			A
3	Total current at 266 MHz	11			A
4	Total current at 533 MHz	19			A
5	f_{clock}	533			MHz
6	Clock edge noise (impulse response)	105		104	mV
7	Resonant Frequency	33		33.11	MHz
8	100 nsec droop on board, fclk=266 MHz	30			mV
9	Dynamic current @ 266 MHz		8		A
10	Dynamic current @ 533 MHz		16		A
11	Charge per clock cycle (q_{cycle})		30		nC
12	Capacitance that switched		27		nF
13	Capacitance that did not switch		286		nF
14	On-die capacitance		313		nF
15	Switch Factor		9%		
16	PDN loop Inductance		74		pH
17	PDN Z_0		15.4	15.4	mΩ
18	Board loop resistance		3.75		mΩ
19	Ball/socket resitance	0.6			mΩ
20	Bump loop resistance		4.35		mΩ
21	Effective resistance from leakage @ Vdd0		122		mΩ
22	Load resistance for 16A resonance		138		mΩ
23	Die resistance		0.80		mΩ
24	q-factor from bump loop		3.54	3.05	
25	q-factor from leakage		7.9	7.5	
26	q-factor from load		8.9	8.8	
27	q-factor from ODR		19.3	20.7	
28	Combined q-factor		1.75	1.68	
29	Impedance peak		26.9	25.9	mΩ
30	Z_target for 266 MHz		6.9		mΩ
31	Z_target for 533 MHz		3.4		mΩ
32	Step response droop		123	150	mV
33	Resonance peak-peak noise		548	584	mV

FPGA model to hardware correlation

- Measurement Fixture
  - Die on package on board
  - Bump sense lines from backside of board
    - Do not carry PDN current
  - Board sense points at cap pads
- Bandini Mountain Impedance peak
  - Inductance is on board and package
  - Resistance is on die, package and board
  - Capacitance is on-die
- Top level schematic
  - Die represented by switched capacitor load





Simulated and Measured Impulse Response

- A single clock cycle draws an impulse of current
- Calculate charge per clock cycle
  - F_{clk} = 533 MHz
  - $I_{dynamic}$ =16 A
  - Charge per cycle = 30 nCoul
- Capacitance
  - that switched = 27 nF
  - that did not switch = 286 nF
  - total on-die capacitance = 313 nF
- Inductance
  - Resonant frequency = 33 MHz
  - PDN loop inductance = 74 pH

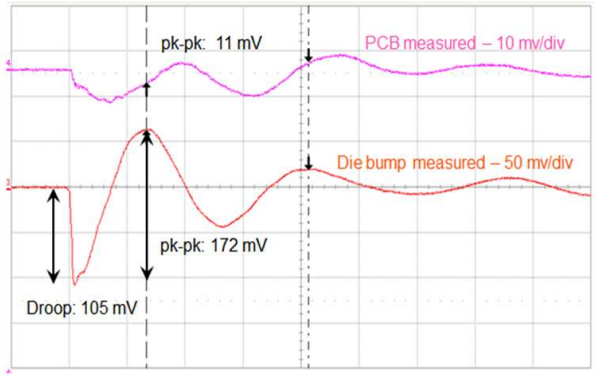
$$q_{cycle} = \frac{I_{dynamic}}{f_{clk}} = \frac{16A}{0.533\ GHz} = 30\ nC/cycle$$

$$C_{switched} = \frac{q_{switched}}{Vdd} = \frac{30\ nCoul}{1.1\ V} = 27\ nF$$

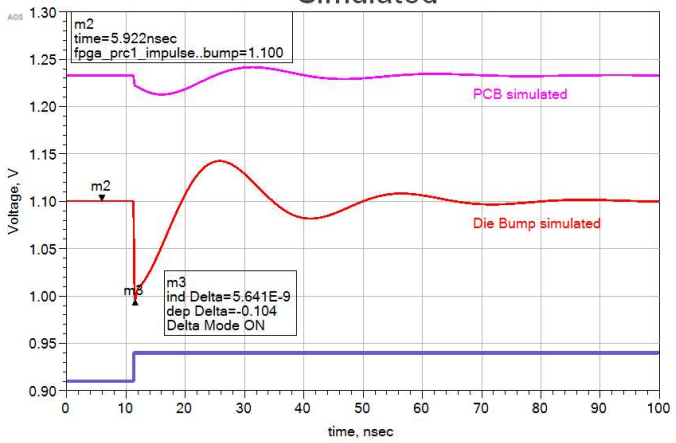
$$C_{ODC\_ns} = \frac{dq}{dV} = \frac{q_{switched}}{V_{droop}} = \frac{30\ nCoul}{0.105\ V} = 286\ nF$$

$$f_0 = \frac{1}{2\pi\sqrt{L_{loop}C_{ODC}}} = \frac{1}{period}$$

Measured



Simulated

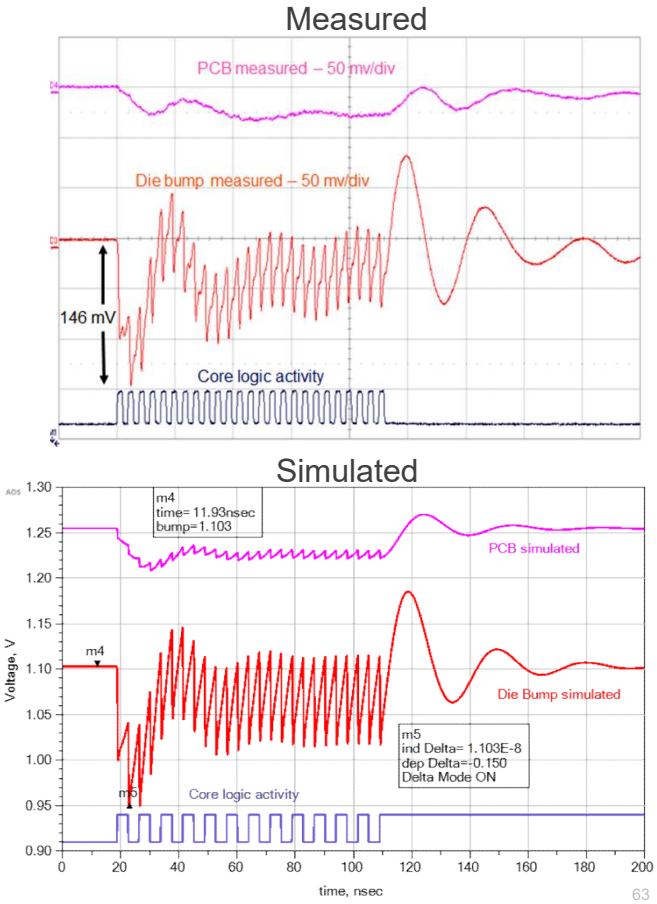


Simulated and Measured Step Response

- Step load is drawn from PDN
  - About 25 clock cycles delivered to lab FPGA
  - Switched capacitor load draws current on both edges
- Step signatures on both current attack and release
  - PDN voltage droop on current attack
  - PDN voltage spike on current release
  - No adaptive voltage positioning was used
- Obtain board resistance from board measurement

$$R_{board} = \frac{30mV}{8A} = 3.75m\Omega$$

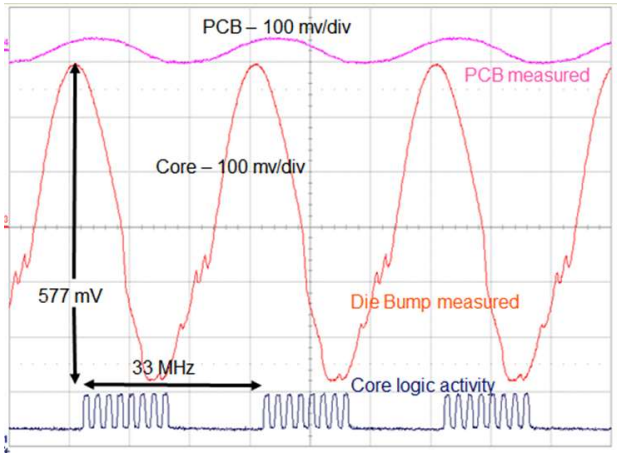
- Good Model to hardware correlation for step response
  - Used loop inductance and on-die capacitance from impulse response calculations



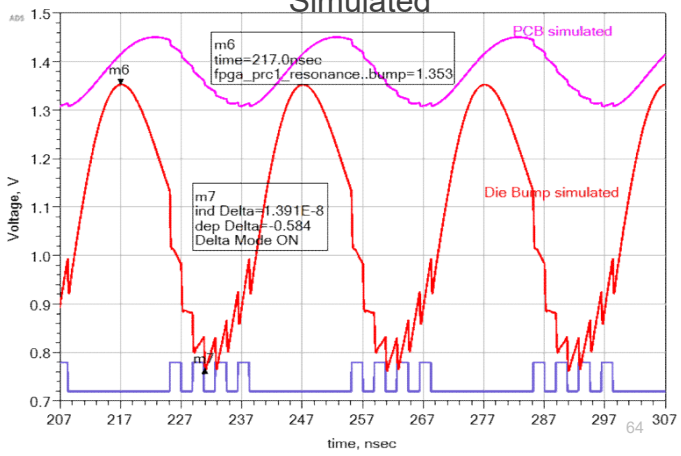
Simulated and Measured Resonance Response

- Resonance load is drawn from PDN
  - 8 clock cycles at 533 MHz
  - No clock cycles for same time period
  - Repeat
- Excellent model to hardware correlation
  - 577 mV p-p measured
  - 584 mV p-p simulated
- Impulse response parameters
  - on-die capacitance = 313 pH
  - loop inductance = 74 pH
- Qfactor and loss contributions from
  - bump loop resistance
  - on-die capacitance ESR
  - leakage
  - load

Measured

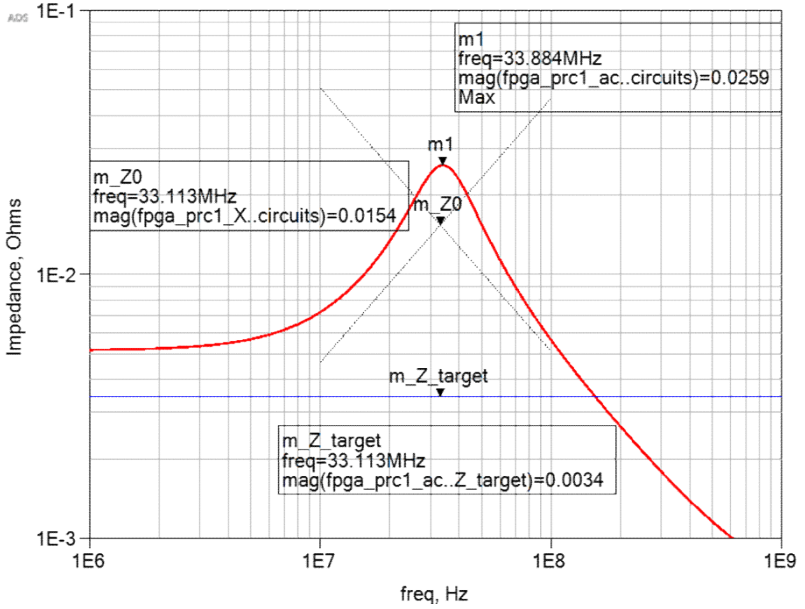


Simulated



Frequency Domain Simulation of FPGA PDN parameters

- Bandini Mountain PDN parameters
  - On-die capacitance = 313 nF
  - Bump loop resistance = 74 pH
  - Z0 = 15.4 mOhms
  - Impedance peak = 25.9 mOhms
  - Q-factor = 25.9/15.4 = 1.68
- Target impedance
  - Far below Z_0 and Z_{peak}
  - FPGA was pushed far harder than it should have been when operated as a product
  - This is why PDN voltage noise is so high
- PDNs can deliver much more current than what is indicated by target impedance
  - Consequence is excessive voltage droop
  - Far exceeds voltage tolerance

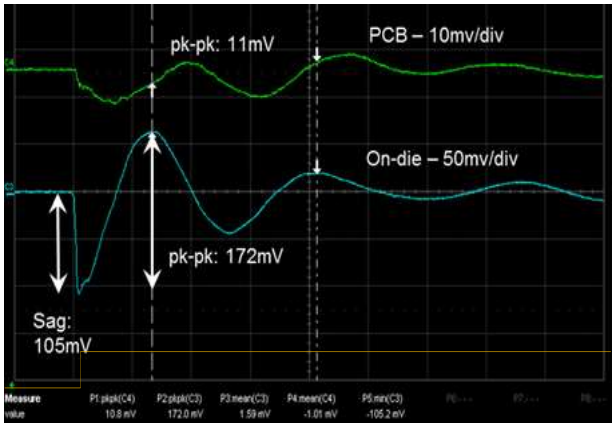


$$Z_{target} = \frac{V_{dd} \times tolerance}{I_{transient}}$$

Basic PDN Voltage Responses Shown in Introduction

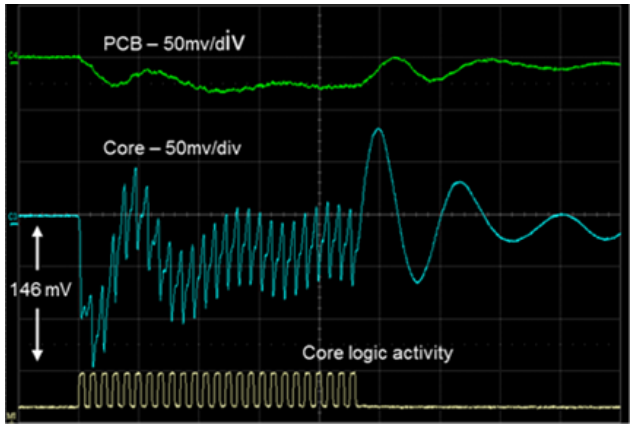
These are the waveforms that were correlated with extracted PDN parameters

Impulse Response (Clock Edge Noise)



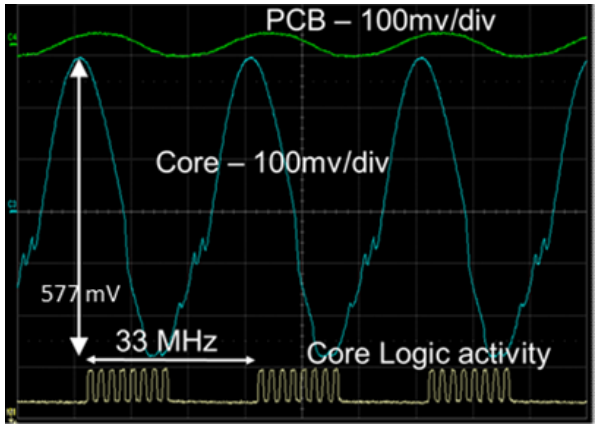
10 nS / Div

Step Response



10 nS / Div

Resonance Response



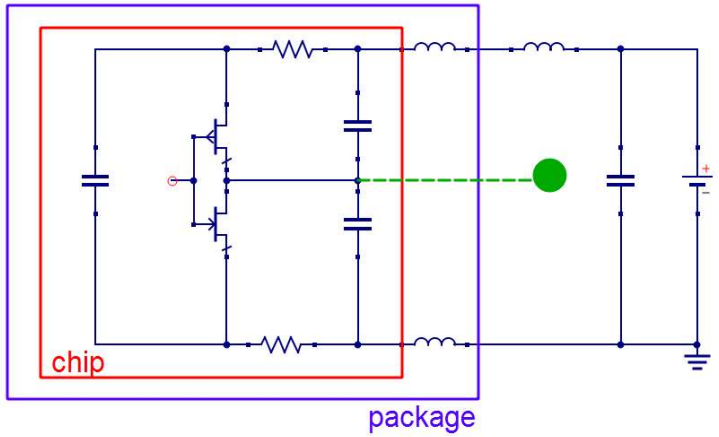
10 nS / Div

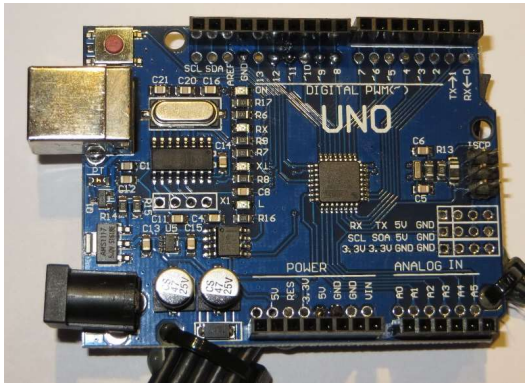
Waveforms curtesy of Altera. On-Chip PDN Noise Characterization and Modeling, DesignCon 2010

Measurements Controller

Eric Bogatin

Another Trick When the Vcc, Vdd rails are shared on-die





Use an I/O line as a sense line:

- Quiet Hi
- Quiet Lo

Features:

- On-die capacitance
- On-die resistance
- A bunch of gates than toggle
- Capacitive load: ref to Vdd and Vss
- Package lead inductance
- On board inductance
- VRM

Instrumented Board: Using 6 Channels

Toggle pin 8 as trigger at start of operation (450 Ohm series with cable)

Toggle 9, 10, w, wo 50 Ohm load (use scope to load)

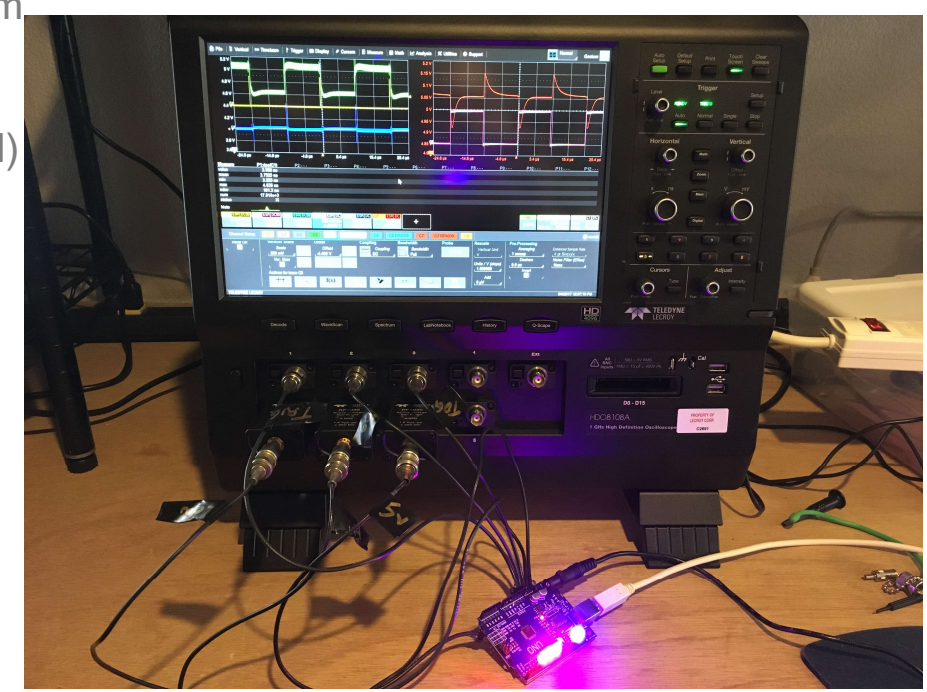
Set pin 11 LOW, measure Vss with RP4030

Set pin 12 HIGH, measure Vcc with RP4030

Measure board level 5 V with RP4030

Toggle pin 13 with LED load (~ 40 mA)

Toggle pins 7, 5, 3 with LED load (~ 30 mA each)



When I/Os Toggle

I/O driving 50 Ohms rise time ~ 15 nsec

I/O on for 2 cycles

On-die Vcc drops 300 mV when on (probably IR drop)

Board level Vcc drop < 50 mV (low duty cycle)

When I/O switches from HIGH → LO, on-die Vss bounces 200 mV

Take-Aways

- Increase the die capacitance to reduce the voltage noise
  - Fast PDN noise droops are proportional to 1/C
- Reduce the system inductance to bring current (charge) into the die faster
  - Incoming current reduces the charge delivered by the on-die capacitance
- Both of these are costly
  - But you get what you pay for

Summary

- PDNs are best analyzed and designed in the frequency Domain
  - Resistive and reactive components: R, L and C
- PDN time domain voltage is the only thing that matters to the product
  - Impulse, Step, Resonance responses must be managed
- The Target Impedance is the reference level to evaluate the PDN impedance
  - The step response will stay within tolerance if Z0 = Ztarget
  - The p-p resonance response is determined by Zpeak
- CMOS dynamic current comes from a series of current (charge) impulses
  - Logic activity draws an impulse of charge at each clock edge
  - Average clock cycle charge is calculated from bench current and frequency
  - On-die voltage droop from single impulse is calculated from Q=CV
- The voltage on-die must droop to draw current in from outside world
  - Capacitor dv/dt = I/C
  - Inductor di/dt = V/L
  - Large signal transient current is very important
  - Small signal di/dt (slope) is not very important
- Switch capacitor loads behave like CMOS
  - Current source loads have no damping
- PDN time domain noise is mitigated by:
  - Capacitance for clock edge impulse response
  - Capacitance and inductance for step response
  - Capacitance, inductance and resistance (q-factor) for resonance response

$$Z_{target} = \frac{Vdd \times tolerance}{I_{transient}}$$

$$Z_0 = \sqrt{L / C}$$

$$Z_{peak} \doteq X \bullet Q = \frac{X^2}{R} = \frac{L / C}{R}$$

$$Q\_factor = \frac{Z_{peak}}{Z_0} = \frac{Z_0}{R_{loop}}$$

$$Q_{cycle} = I_{dynamic} / \mathrm{f}_{clock}$$

$$V_{clock\ edge\ droop} = \frac{Q_{cycle}}{C} = \frac{I_{dynamic} / f_{clock}}{ODC}$$

$$V_{step\ droop} = I_{step} \times Z_0$$

$$V_{P\text{-}P\ \ resonance} = \frac{4}{\pi} I_{tran} Z_{peak}$$

Thank you

PDN Tutorial contents were drawn from these publications

- L. D. Smith, R. E. Anderson, D. W. Forehand, T. J. Pelc, T. Roy, "Power Distribution System Design Methodology and Capacitor Selection for Modern CMOS Technology," IEEE Transactions on Advanced Packaging, Vol.22, No.3, P284, August 1999.

- L.D. Smith, S. Sun, P. Boyle, B. Krsnik, "System Power Distribution Network Theory and Performance with Various Noise Current Stimuli Including Impacts on Chip Level Timing," Proc. Custom Integrated Circuits Conference, September 2009.

- S. Sun, L. D. Smith, P. Boyle, B. Krsnik, "On-Chip PDN Noise Characterization and Modeling," Santa Clara, CA, DesignCon 2010.

- L.D. Smith, M. Sarmiento, Y. Tretiakov, S.Sun, Z. Li, S. Chandra, "PDN Resonance Calculator for Chip, Package and Board, Santa Clara, CA, DesignCon 2012.

- L. D. Smith, E. Bogatin, *Principles of Power Integrity for PDN Design*, Prentice-Hall, 2017.