Power Integrity Behavior for Various Packaging Environments

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***Abstract*— Power integrity design has become a critical issue in digital electronic systems, as advanced CMOS LSIs operate at higher clock frequency and at lower supply voltage. Power supply fluctuation excited by core circuits or I/O buffer circuits induces logic instability and electromagnetic radiation. Therefore, total impedance of power distribution network (PDN) must be taking into consideration in the chip-package-board co-design. Especially, anti-resonance peaks in the PDN created by the parallel combination of on-chip capacitance and package inductance induce the unwanted power supply fluctuation, and results in the degradation of signal integrity and electromagnetic interference (EMI). In this paper, effects of critical damping condition for the total PDN impedance on power supply noise has been studied by adding different RC circuit to the intrinsic on-die RC circuit of chip. Three test chips were assumed to be designed on-chip PDN properties. The measurement and analysis of power supply noises for the three test chips showed typical characteristics of oscillatory region and damped regions the critical damping condition against the anti-resonance peak has been proved to be effective to suppress the power supply noise on the chip. Furthermore QFP and BGA are used for a package and the effect of anti-resonance and power supply noise control by the total impedance of a chip package board are verified from the difference in inductance.**

Keywords—Power integrity; Anti-resonance peak; co-design; total PDN impedance;

I. INTRODUCTION

As CMOS LSI systems operate at higher clock frequency and at lower supply voltage, power integrity is becoming a critical issue to maintain digital electronic systems more stable. Therefore, the power integrity design must be taken into consideration from the chip-package co-design point of view, because so called, chip-package parallel resonance in the power distribution network (PDN) occurs due to the parallel combination of on-die capacitance and package inductance. To estimate the anti-resonance frequency and the peak level exactly, on-chip PDN must be designed along with package design.

Simultaneous switching output buffers (SSO) noise and power supply noise on the core circuits have been almost studied from the time domain. A total PDN impedance which consisted of chip PDN, package PDN, and board PDN has become an important approach from the frequency domain to understand the noise phenomena more clearly and optimize the PDN characteristics properly [1]-[3]. Furthermore, this anti-resonance peak is normally difficult to observe directly by the conventional methods. Then, on-chip noise monitoring circuits are expected to play an important role to measure the power supply fluctuation inside a chip [4]-[5].

In this paper, three test chips with different on-die PDN have been assumed. Then, the effects of PDN impedance for the core circuits on the power supply noise were examined to obtain the resonant free PDN by establishing critical damped PDN.

II. PARALLEL RESONANCE OF TOTAL PDN

Fig.1 shows a simplified PDN model which consisted of chip, package and board. In this model, switching current flows through on-die capacitance (C_{die}),on-die resistance (R_{die}), board impedance (Z_{pcb}), and package inductance (L_{pkg}). Because the board impedance (Z_{pcb}) is normally smaller than the package inductance (L_{pkg}) for the conventional board with several decoupling capacitors, anti-resonance peak occurs at around the cross point between package inductance and on-die capacitance as shown in Fig.2.

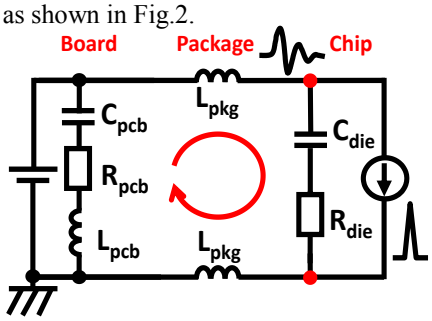

Fig.1. Simplited total PDN model consisted of chip, package and board

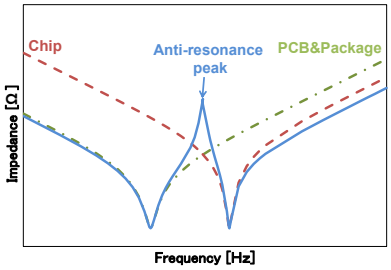

Fig.2. Anti-resonance peak caused by parallel resonance between PDNs in chip and package

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III. TEST CHIP DESIGN

Fig.3 shows a detailed equivalent circuit model of on-chip PDN. Simplified PDN model consisted of R_{die} and C_{die} was divided into the intrinsic PDN parameters and the added PDN parameters. The intrinsic capacitance (C_{itr}) consists of the well-capacitance of MOS transistor and the mutual capacitance among the power/ground grid lines of the chip, and the intrinsic resistance (R_{itr}) consists of the trace resistance of the power/ground grid lines. The R_{itr} is dependent on the physical layout of on-chip PDN. Intentionally added C_{add} and R_{add}, were assumed to be fabricated by using MIM (metal-insulator-metal) capacitance and thin-film process, respectively. These added C_{add} and R_{add} were serially connected each other, and they were connected to the intrinsic PDN in parallel.

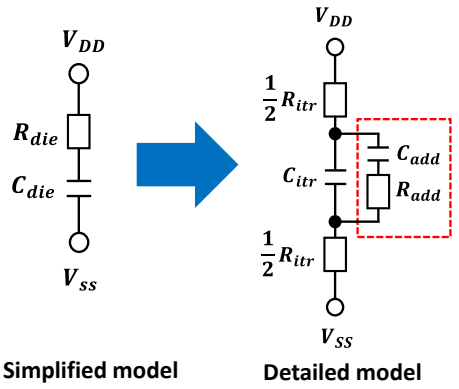

Fig.3. Detailed on-chip PDN model

Three test chip were desined to have the same noise generating circuits in the different on-chip PDN properties as shown in Fig.4. The size of the test chips was 2.5 by 2.5 mm. The PDN of the chip A was designed to have just intrinsic PDN of the test chip without any intentionally added decoupling capacitance (C_{add}) of 580 pF was assumed to be intentionally added in parallel to the intrinsic PDN of the chip. For the chip C, both on-die capacitance (C_{add}) and on-die resistance (R_{add}) were intentionally added. The value of C_{add} was the same as the chip B, and R_{add} was assumed to be 1.33 ohms.

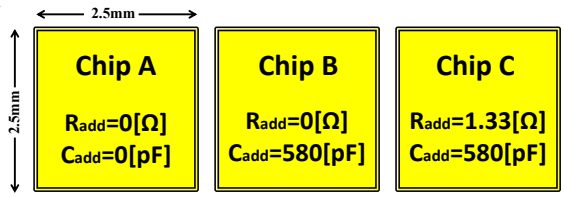

Fig.4. Three test chip design with different PDN

Three test chip with different on-chip PDN properties were designed as shown in Fig.5. Each test chip was designed to have both noise generating circuits noise generating circuits and on-chip noise monitoring circuits Fig.6 shows a noise generating circuit using shoot-through current (STNG: shoot-through noise generator) with different current dribabilities by changing the number of CMOS inverter stages. Noise monitoring circuits were designed utilizing CMOS output buffer circuits. They were located at the four corners of each chip. Power supply noise was observed by fixing the signal output at the high level, and ground noise was observed by fixing it at the low level.

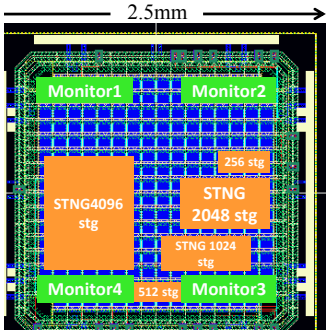

Fig.5. Basic chip layout with noise generators and monitoring circuit

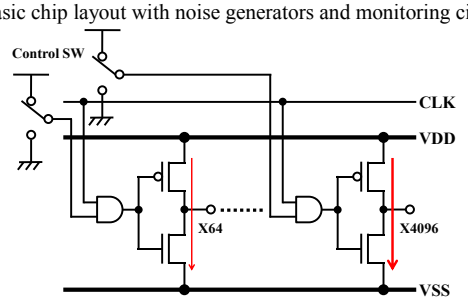

Fig.6. CMOS shoot-through noise generating circuit

IV. MESUREMENT OF POWER SUPPLY NOISES

Fig.7 to 9 shows measured power supply noises when the STNG with the macimum strength of 1024 was excited at a frequency of 10MHz. Fig.7 showed typical oscillatory waveforms for the chip A without any intentional on-die capacitance and resistance. The large ringing noises were excited for chip A, and the peak to peak nose level were largest among three test chip. Fig.8 also showed oscillatory waveforms for the chip B. The noise amplitude was decreased by the intentional on-die decoupling capacitance, but it still showed an oscillatory property. Fig.9 showed critical damped waveforms for the chip C. The peak-to-peak noise amplitude was suppressed to the almost same level of the chip B. The settling time was the shortest among the three test chip. Therefore, the chip C is the most effective for a noise reduction effect. Furthermore, as for the fluctuation of the power supply voltage of BGA package, the ringing waveform have been suppressed in comparison with QFP package.

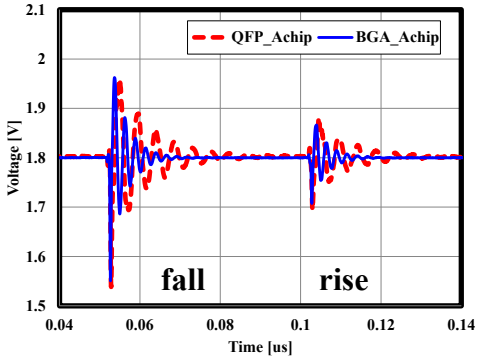

Fig.7. Measured power supply noises for chip A

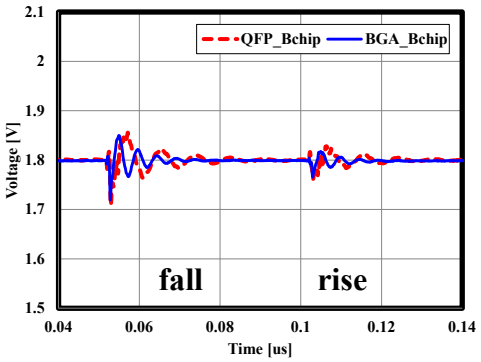

Fig.8. Measured power supply noises for chip B

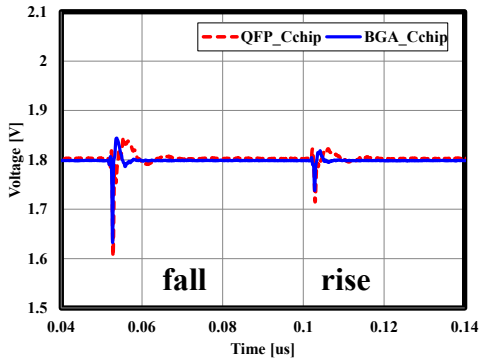

Fig.9. Measured power supply noises for chip C

V. SIMULATION OF POWER SUPPLY NOISE

The following shows chip-package-board total modeling and simulation step. Power supply line of chip was simulated by the commercially available software, Totem (Apache Design Solution). The simulation by the Totem is basically separated by three steps. The first step was an extracting step of the current supply line. The second step was a mapping step of the extracted current waveforms to the physical information though GDS file of the test chip. The power supply fluctuations inside the chip were obtained in the final step.

Then, power supply line of package was modeled by the commercially available software, Q3D Extractor (ANSYS corp). Fig.10 shows QFP package model by Q3D Extractor. Material of the lead frame was set to copper. And the material of wire bonding was gold.Fig.11 shows BGA package model by Q3D Extractor. Power supply line of board was modeled by commercially available software, SIwave (ANSYS corp).

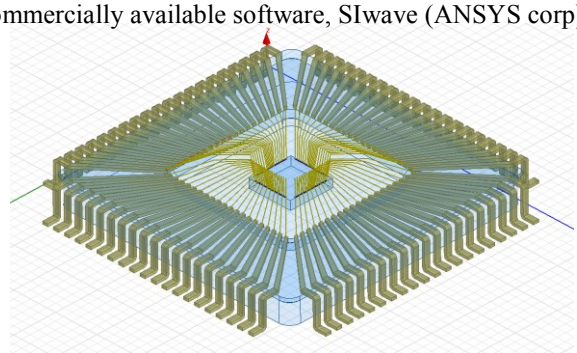

Fig.10. QFP model

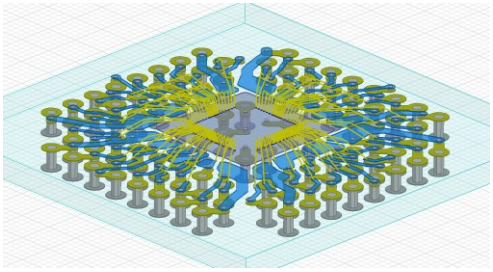

Fig.11. BGA model

Fig.12 shows evaluation board model by SIwave. Board design data was used by converting Gerber format made by EAGLE (Cad soft corp).

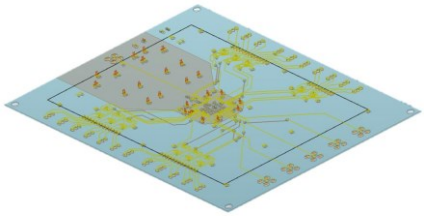

Fig.12. Board model

Total PDN model has been established by connecting SPICE models of the chip, package and board as shown in Fig13. Each PDN model was extracted by using previous softwares. Fig.14 to 16 show simulated power supply noises of both QFP and BGA package for A, B, and C chips respectively. Driving circuit was the shoot-through current noise generating circuit with 1024-stage CMOS inverters switched at a frequency of 10 MHz. Simulated waveforms shows good agreement with measured ones. Fig.17 shows comparison data of the peak-to-peak noise level and the settling time among three test chips. Here, the settling time was defined to be the period that the noise fluctuation becomes within 1 percent of the supply voltage of 1.8V.

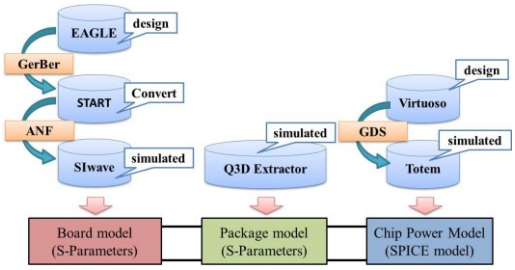

Fig.13. Chip-Package-Board co-analysis flow

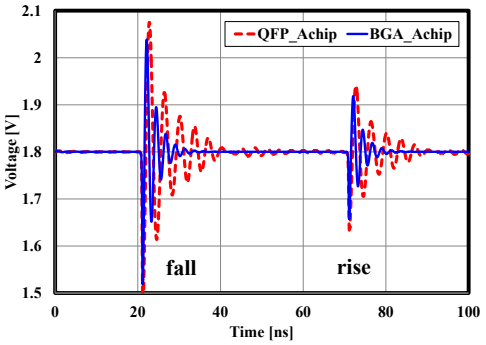

Fig.14. Simulated power supply noise for chip A

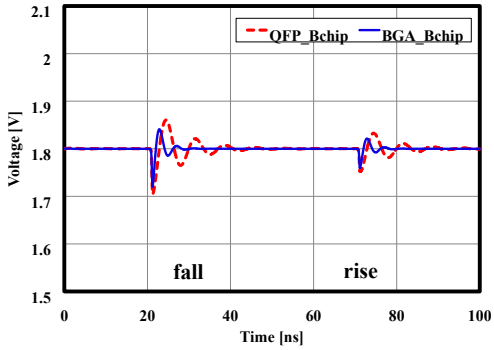

Fig.15. Simulated power supply noise for chip B

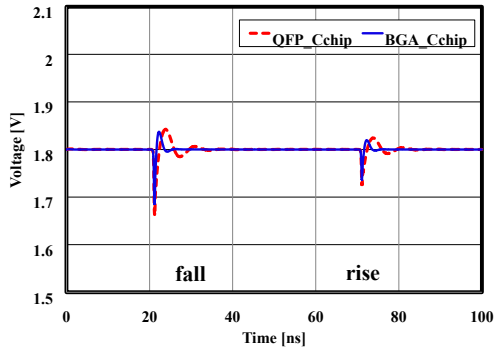

Fig.16. Simulated power supply noise for chip C

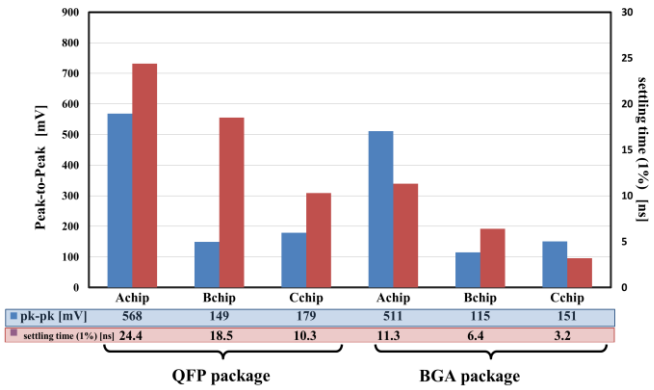

Fig.17. Comparison of peak-to-peak noise and settling time

VI. SIMULATED TOTAL PDN IMPEDANCE

Fig.18 shows the synthesized total PDN impedances for the three test chips under the bias condition of 1.8V. Anti-resonace peak for the chip A was the biggest compared to the other two chips. Anti-resonance peak for the chip B was considerablyl suppressed than the chip A. Anti-resonance peak for the chip C is the lowest among the three chips. Large ringing noises for the chip A was excited by the high anti-resonance peak in total PDN. Judging from the total PDN impedance, it has been proved that suppression of the anti-resonance peak is an effective way to reduce power supply noise. Furthermore, because the package inductance of BGA is smaller than that of QFP, anti-resonance peak was shifted to higher frequency range by the low inductance BGA. This causes the period of ringing waveform became shorter than for the cases of BGA .

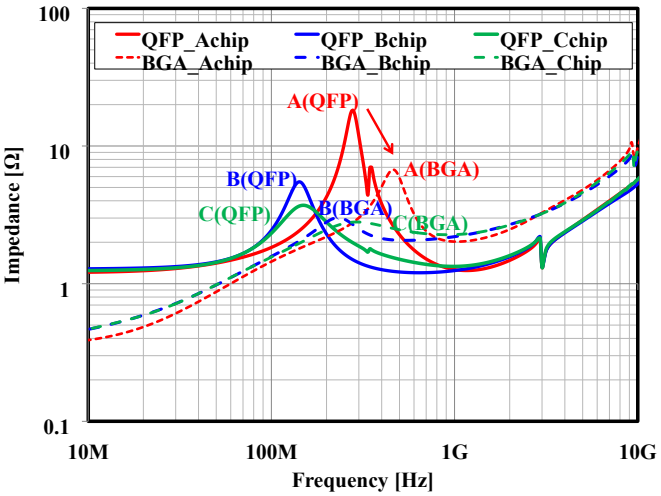

Fig.18. Comparison of simulated anti-resonance peaks for three chips and two packages

VII. SUMMARY

Three test chips with different PDN properties were designed so as to examine the effect of the total PDN peak which arises from the parallel combination of the package inductance and the chip capacitance. Typical power supply noises of chip A showed ringing waveform. The addition of on-die capacitance and resistance to the intrinsic on-chip PDN property well contributed to reduce power supply noise and ringing waveform.

Finally, anti-resonance peak suppression in total PDN reduced power supply noise, and resulting ringing waveforms was suppressed by adding proper capacitance and resistance in the on-die PDN along with low inductance BGA.

Acknowledgments

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