Layout Parameter Optimization Based Power and Signal Integrity Performance Improvement of High-Speed Interfaces of Wirebond Packages

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Abstract

The purpose of this paper is to present layout parameter optimization based power and signal integrity performance improvement investigation of high-speed interfaces in wirebond packages. Effects of different sections of signal nets, wirebond diameter, material and other stackup parameters on the noise performance of the package system is discussed in detail. The methodology developed in this paper, based on different sections of power and signal nets and supported by simulation results, provides design guidelines for the efficient and cost-effective wirebond IC-package systems development.

1. Introduction

High-speed data signals from I/O drivers of IC-chip, placed on an IC-package, are transmitted through signal nets to the receivers placed on the board side of the IC-package. The noise generated by fast switching signals through the parasitic of these signal nets adversely affect the quality and timing of data at I/O receivers. In practice, characteristic impedance is used as a figure-of-merit to characterize the effect of the parasitics associated with different sections of signal nets routed in IC-packages. The cross-sectional dimensions for single-ended and differential signal nets are defined based on the specified characteristic impedance and differential impedance. In order to minimize the discontinuities between different sections of a signal net, causing reflections and distortions in the signals, the signal nets in an IC-package are designed with uniform characteristic impedance. Also, the single-ended and mixed mode S-parameters are used to characterize the noise performance of coupled single-ended and differential signal nets. More specifically, return losses and insertion losses are used as the figure of merits for the performance evaluation of differential signal nets in an IC- package.

In general, signal nets routed in an IC-package are not considered as the infinitely long continuous transmission lines due to discontinuities created by wirebonds, vias, balls and other interconnects. In order to develop an effective design procedure to improve the signal quality and the overall noise performance of the IC-package, it is important to understand the effect of these discontinuities. Therefore, it is critical to accurately characterize each section and component of a signal net in an IC-package.

The purpose of this paper is to present modeling, simulation and analysis methodology for characterizing the effect of discontinuities between different sections of high-speed signal nets in a wirebond IC-package. The effect of discontinuities between different sections of a signal nets in a wirebond IC-package are considered in terms of (i) wirebond, signal traces, vias and solder balls, individually, (ii) wirebond plus trace, (iii) wirebond plus trace plus via and (iv) wirebond plus trace plus via plus solder balls. The paper presents an efficient process for computing key electrical parameters for different sections of signal nets in a wirebond IC-package. The process discussed in the paper provides insight to optimize each section of a signal net to improve the overall power and signal integrity performance of wirebond IC-packages.

Next, the effects of diameter and material of the wirebond on the key electrical parameters used for evaluating the power and signal integrity performance of the high-speed interface are discussed. Finally, stackup parameters, such as dielectric thickness between a signal layer and its reference or between the power and ground layers on the characteristic impedances and other electrical parameters of signal nets are discussed. The layout parameter optimization methodology for noise performance improvement, supported by extensive simulation results, is discussed considering a real multilayer wirebond IC-package as an example.

2. Layout Parameter Optimization Based Wirebond Package Modeling Process

A wirebond-package, with Silicon-DIE/IC-Chip placed on a PCB is shown in Figure 1. The wirebonds for signals and power/ground pins on the IC-chip, respectively, are connected to signal traces on the signal layer and power/ground rings on the package. The signal traces for high-speed interfaces on the signal layers are routed with reference to power/ground planes, needed for signal return current path. These signal and power/ground nets terminate through respective vias to the array of solder balls/C5s/ball-grid arrays (BGAs) attached to pads on the bottom layer of the package, as shown in Figure 1. The solder balls cover the entire area on the bottom layer of the package. Typically, the solder ball pitch is used in the range of 0.7 mm to 1.27 mm, depending on the number of signal, power and ground pins, used in the silicon-die. Finally, the signals, powers and ground BGAs are connected to the copper pads on a multilayer printed circuit board. (PCB).

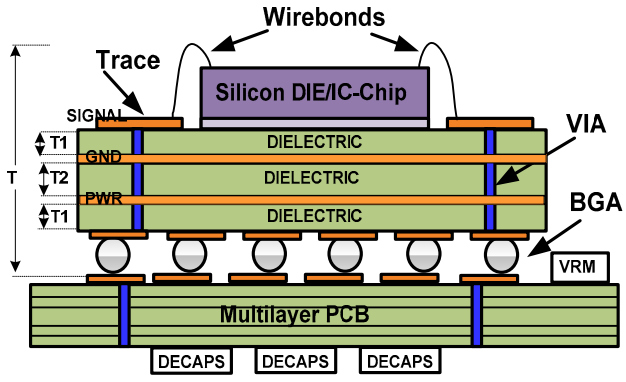

Figure 1

The paper presents an efficient methodology, supported by simulation results, using a real wirebond IC-package as an example to illustrate and evaluate the effect of layout parameters on the power and signal integrity performance of high-speed signal interfaces. The 3D view of a multilayer wirebond IC-package with a coupled differential-pair signal nets on the signal layer of the package, with respective vias and wirebonds is shown in Figure 2.

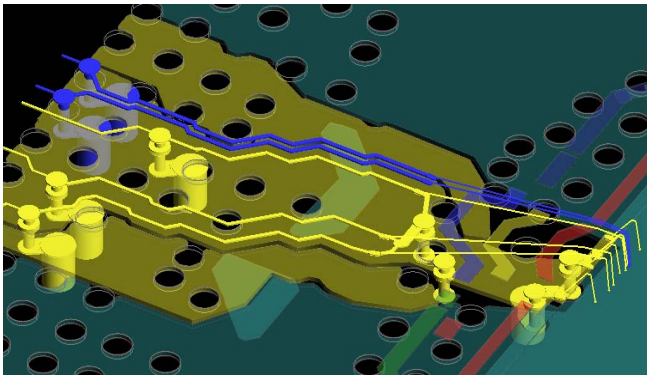

Figure2

A simplified model of the wirebond IC-package of Figure 2 is shown in Figure 3.

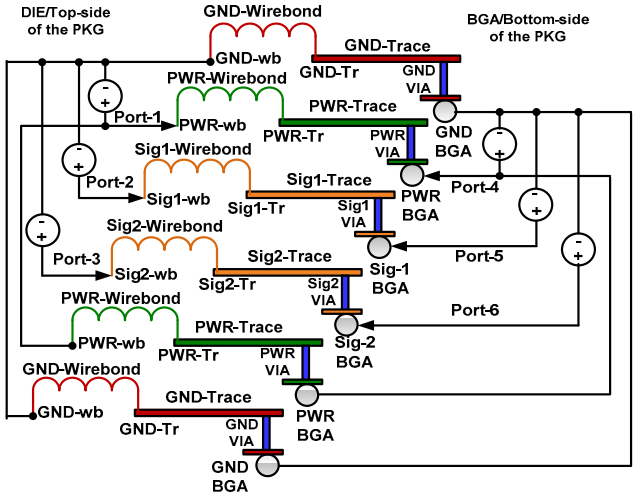

Figure 3

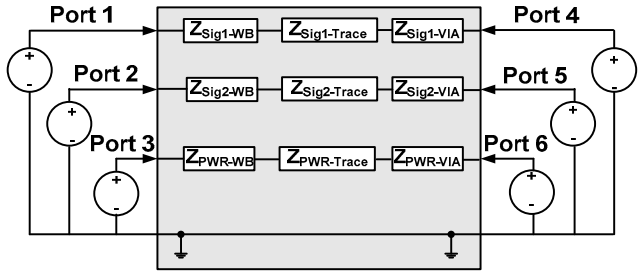

Figure 4

In order to extract the electrical model of the signal nets and power nets, electrical ports are connected on the die-side and the BGA-side of the package, as shown in Figure 3. Thus, another simplified electrical model of the package, with wirebonds, signal traces and vias including BGAs, represented in terms of the respective impedances, is shown in Figure 4.

In general, in order to evaluate the power and signal integrity performance of an IC-package, signal interfaces and power-nets are modeled in terms of standard multiport S-parameters [1]. These standard S-parameters are converted into mixed-mode parameters for the noise performance evaluation of differential signals [2]. Figure 5 illustrates the modeling and simulation process for generating standard S-parameter model of signal and power nets of an wirebond IC-package, using a commercially available field solver [3a].

2.1 Electrical Parameters for Sections of Signal Nets

In order to identify the noise contribution by different sections of a signal and power nets, frequency-domain simulations can be performed for the following cases:

Case-1: Wirebonds(WB)+Trace+VIA+BGA,

Case-2: Trace + VIA + BGA, Case-3: VIA + BGA,

Case-4: VIA only and Case-5: BGA only

The ports connections for Case-1 to Case-3 are illustrated in the flow diagram shown in Figure 5. The wirebonds or trace or VIAs can be turned off easily in most of the commercially available field solver.

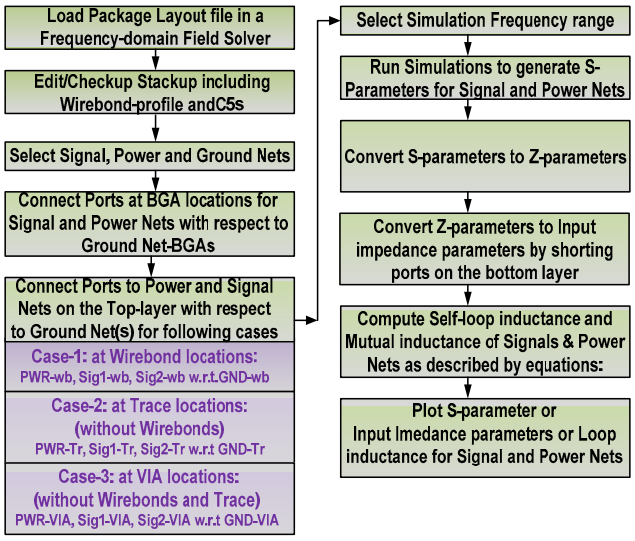

Figure 5

The field solver generated S-parameters for signal and power nets can be converted to impedance/admittance matrices using

$$[Z] = Z_o([I]+[S])([I]-[S])^{-1},\ [Y] = Z_o^{-1}([I]-[S])([I]+[S])^{-1}$$

where, Z_o is the characteristic impedance and I is the identity matrix.

Note that the input impedance looking from the die-side can be computed from the Z-parameters, with ports on the BGA-side shorted or opened. The input impedance, with ports on the BGA side shorted is defined as input-loop-impedance.

Thus, input-loop-impedances for Case-1, Case-2 and Case-3, for a single-ended signal net of a closely coupled differential-pair of a wirebond package, defined as $Z_{in\_(WB+Trace+VIA+BGA)}$, $Z_{in\_(Trace+VIA+BGA)}$ and $Z_{in\_(VIA+BGA)}$

respectively, can be computed from the field solver generated S-parameters for each of these cases.

Next, the input-loop-impedances for wirebonds, trace and (wirebond + trace) sections of the signal net, can be computed as follows:

Case-6: $Z_{in\_WB} = Z_{in\_(WB+Trace+VIA+BGA)} - Z_{in\_(Trace+VIA+BGA)}$

Case-7: $Z_{in\_Trace} = Z_{in\_(Trace+VIA+BGA)} - Z_{in\_(VIA+BGA)}$

Case-8: $Z_{in\_(WB + Trace)} = Z_{in\_(WB + Trace+VIA+BGA)} - Z_{in\_(VIA+BGA)}$

Finally, the input-loop-impedance, Zin-loop, typically inductive in nature, can be expressed as $Z_{in\text{-}loop} = R_{ac,loop} + j\omega L_{loop}$, where $R_{ac,loop}$ is defined as the frequency-dependent loop ac-resistance and L_{loop} is defined as the self-loop-inductance. Therefore, the loop ac-resistance and self-loop-inductance can be computed using

$$R_{ac,loop} = Real(Z_{in-loop}) \text{ and } L_{loop} = \frac{Imaginary(Z_{in-loop})}{\omega}$$

2.2 Simulation Results for Sections of a Signal Net

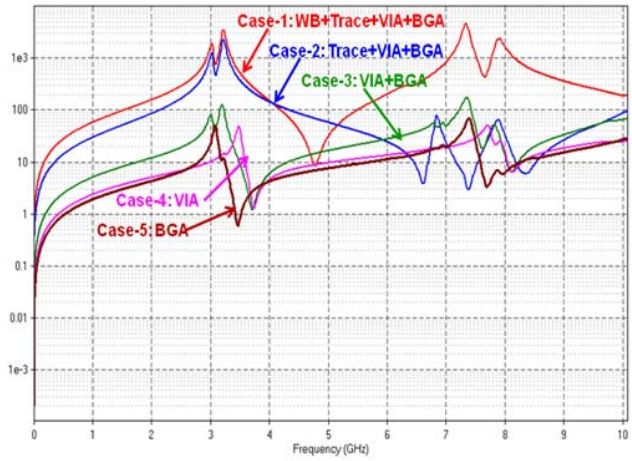

Figure 6

Figure 6 shows the input impedances $Z_{in\_(WB+Trace+VIA+BGA)}$, $Z_{in\_(Trace+VIA+BGA)}$ and $Z_{in\_(VIA+BGA)}$ respectively, computed from the field solver generated S-parameters for Case-1, Case-2 and Case-3 of a single-ended signal net of the differential-pair of the wirebond IC- package.

The total self-loop-inductance, ac-resistance and capacitance for Case-1(WB+Trace+VIA+BGA) of the single-ended signal net with wirebond of Gold and Copper material and diameter values of 0.8 mil, 0.96 mil, 1.0 mil and 1.2 mil are shown in Figure 7, 8 and 9 respectively.

Note that the loop inductance of the signal net with copper wirebond decreases by 0.6% -0.8% as compared to that of the gold wirebond. The loop inductance of the signal net with gold/copper wirebond reduces by 2.5%, when the wirebond diameter is increased from 0.8 mil to 0.96 mil. Also, the ac resistance for signal net with copper wirebond decreases in the range of 13%-18%, as compared to that of the gold wirebond. However, the change in ac resistance with wirebond diameter remains almost same for wirebond material as gold or copper.

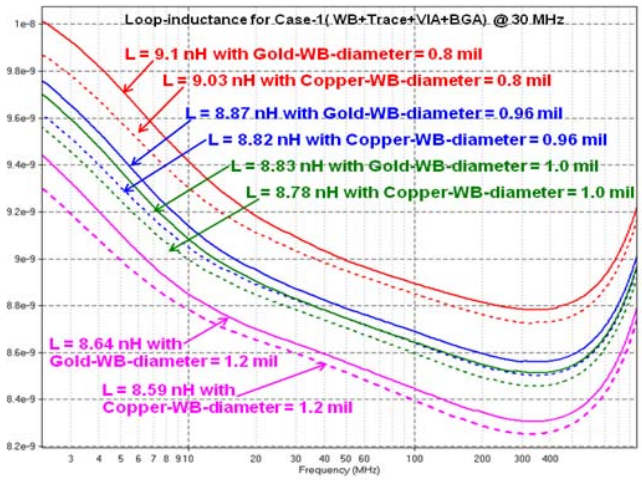

Figure 7

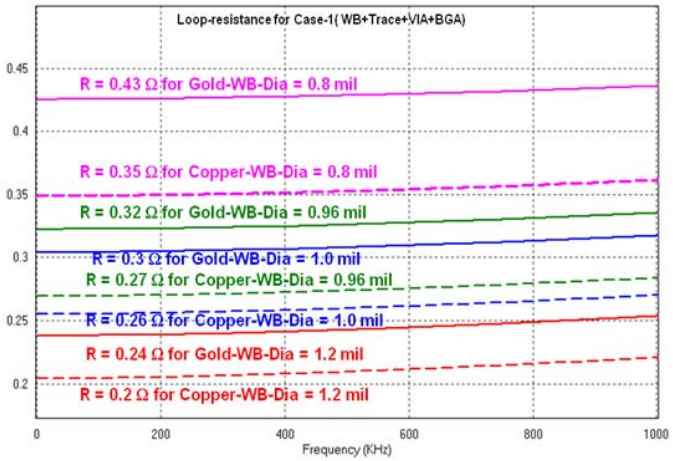

Figure 8

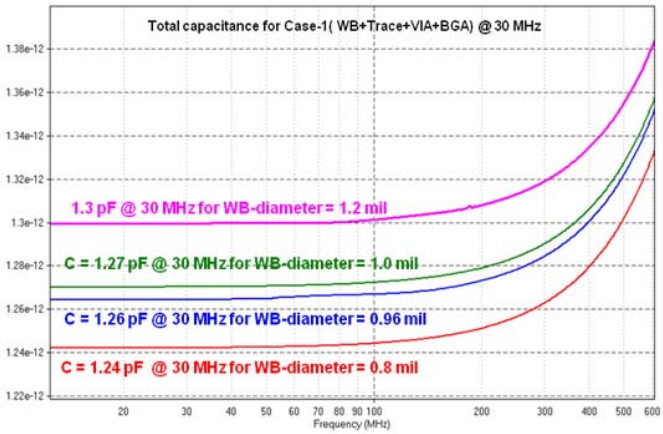

Figure 9

The dc resistance for Case-1(WB+Trace+VIA+BGA) of a single-ended signal net with gold and copper wirebond of diameter 0.8 mil, 0.96 mil, 1.0 mil and 1.2 mil, are shown in Figure 10.

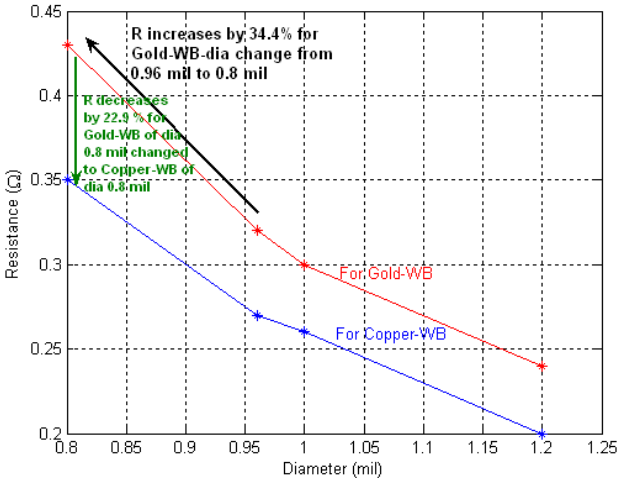

Figure 10

Next, the input impedances for the wirebond(WB), Trace and (WB+Trace) sections of a single-ended signal net, computed using expressions for Case 6, Case 7 and Case8, are shown in Figure 11.

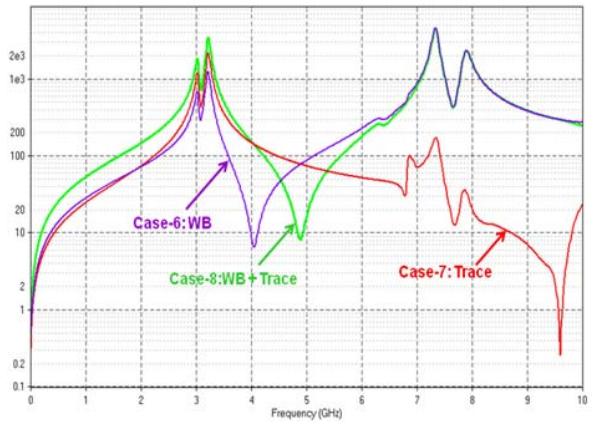

Figure 11

The self-loop inductances of the wirebond section (Case-6) of the single-ended signal net for wirebond-diameter values of 0.8 mil, 0.96 mil, 1.0 mil and 1.2 mil are shown in Figure 12.

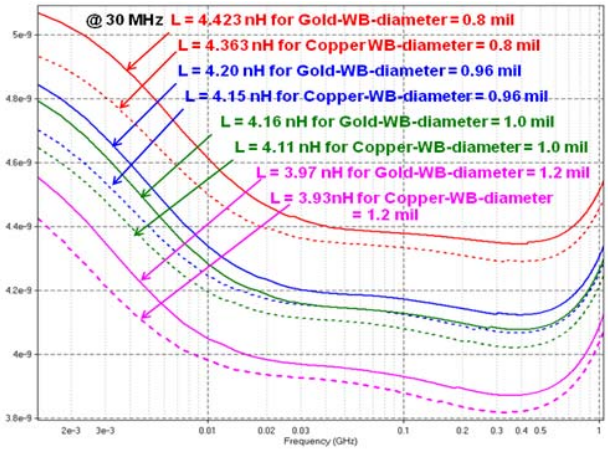

Figure 12

The variation of the total self-loop inductance at 30 MHz for Case-1 and Case-6 with wirebond-diameter is shown in Figure 13. It can be noted that the loop-inductance of the wirebond is almost 50% of the total self-loop inductance of the signal net.

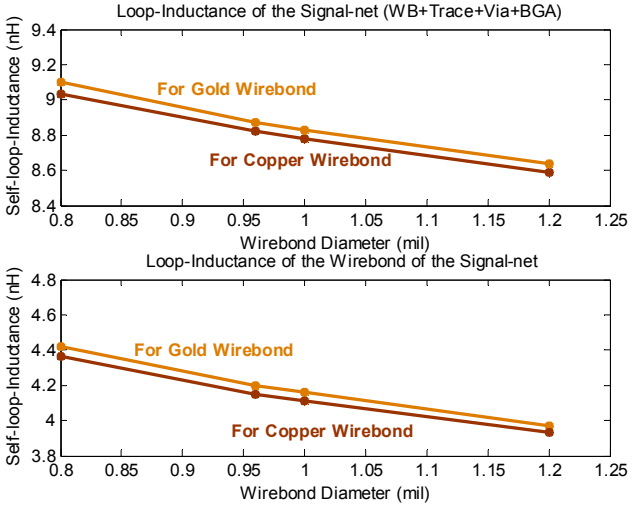

Figure 13

The loop inductance of the signal net for Case-1, Case-2 and Case-3 is compared in Figure 14.

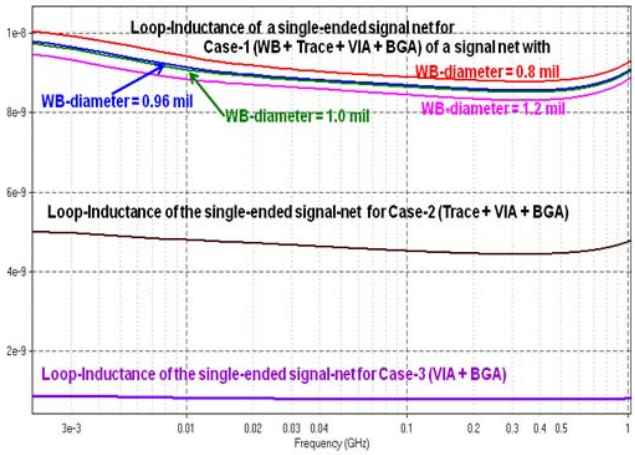

Figure 14

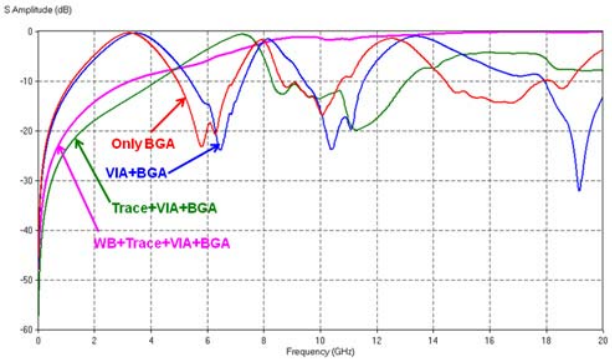

Figure 15

Figure 15 shows the differential return loss for Case-1, Case-2 and Case-3 for the differential pair of signals, obtained by from the mixed-mode S-parameters.

The input impedance magnitude of the power delivery network (PDN) is illustrated in Figure 16.

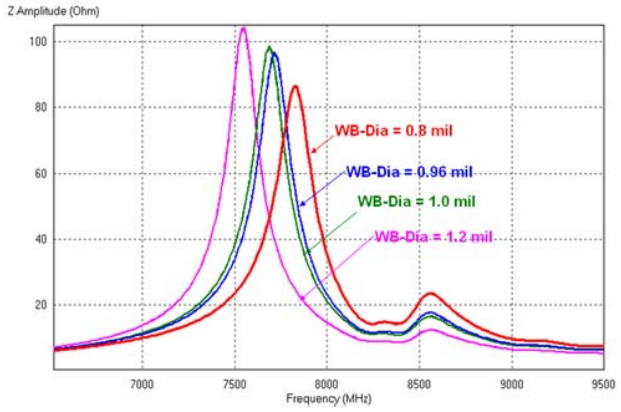

Figure 16

Note that, the peak amplitude of input impedance of the PDN increases with the decreasing value of the wirebond diameter, due to decreasing value of the resistance. Figure 17, shows the voltage at the 25W IC-Chip terminal, due to its triangular current switching at 1.5GHz through the PDN connected with the 1.5 Volt power supply.

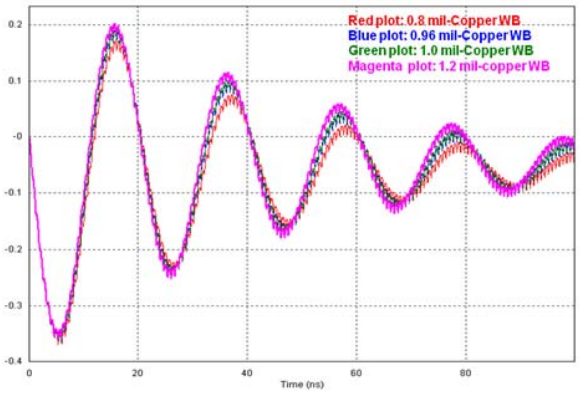

Figure 17

The voltage waveforms in Figure 14 are more damped, due to increased value of resistance of the power delivery net with smaller values of wirebond diameter.

3 Effect of Stackup/Dielectric Thickness Change

The effects of dielectric thicknesses T1 and T2, as shown in Figure 1, on the key electrical parameters affecting the power and signal integrity performance of high-speed signal interfaces and power nets are discussed in this section. The effect of dielectric thickness between (a) a signal layer and its power/ground reference (T1) or (b) a power and a ground layer (T2), or (c) the combination of (a) and (b) on the characteristic impedances and the package electrical model parameters of signal and power nets are investigates for the values of T1 and T2, as shown in Table-1.

Table-1

	T1 (um)	T2(um)	T (mm)
Option-1	**110**	**100**	**1.45**
Option-2	**80**	**100**	**1.35**
Option-3	**130**	**60**	**1.45**
Option-4	**130**	**100**	**1.48**
Option-5	**80**	**180**	**1.46**

The total package thickness (T) includes thicknesses of soldermask, dielectrics between signal and power/ground reference, power/ground planes and solder balls.

The input impedances shown in Figure 18 are obtained from the frequency domain simulations process for Case-1, as described in Figure 5. Note that dielectric thicknesses (T1 and T2) considered in option-3 produce the input impedance of least magnitude and resonant peaks. However, the dielectric thicknesses of option-2 produces the input impedance of smaller magnitude over a wide frequency range.

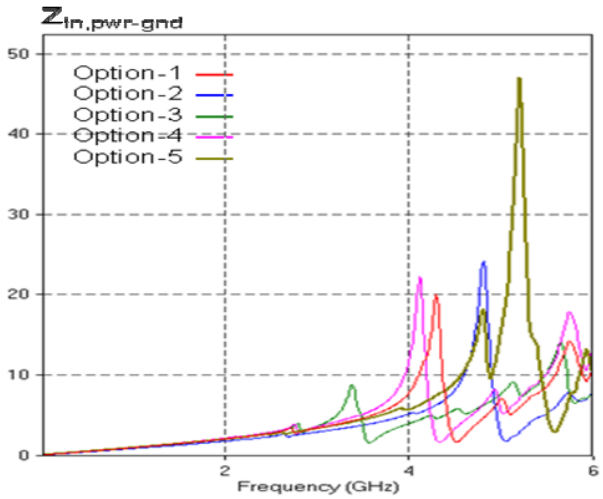

Figure 18

Next, considering dielectric thickness options illustrated in Table-1, a single section R-L-C model, as shown in Figure 19, for the power delivery networks and each of the signal nets of the wirebond package, including mutual coupling coefficients, is generated using a commercially available field solver [3b]. Note that the R-L-C model at a specific frequency can be extracted from the field-solver generated S-parameters [4].

Figure 20 shows the loop resistance (R), loop inductance (L), and total capacitance (C) values for the PDN extracted at frequency 30 MHz.

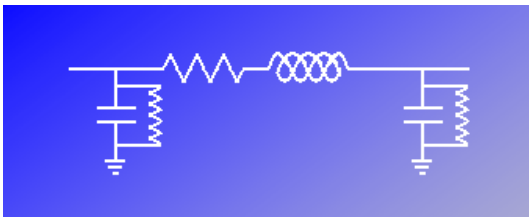

Figure 19

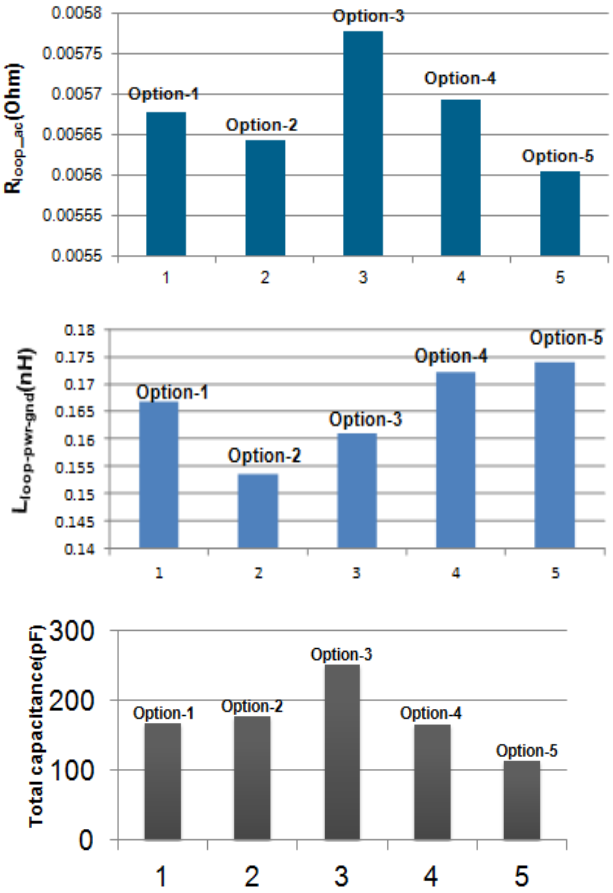

Figure 20

It can be noted, as illustrated in Figure 19(b), that decreasing only T1 (Option-2) or increasing only T1 (Option-4), with respect to its value in Option-1, decreases/increases the total loop inductance of the PDN, mainly due to the inductance contributed by the wirebond. Similarly, the increased loop-inductance of the PDN for Option-5, as compared to Option-2 mainly corresponds to increased value of T2 in the substrate. However, the change in the total loop inductance of the power net, when both T1 and T2 are changed, as in Option-5 with respect to Option-1, can be predicted accurately only by simulations. Finally, the characteristic impedances of a group of signal nets of the parallel interface, obtained for Option-1 to Option-5, are shown in Figure 21. The characteristic impedances for Option-2 and Option-5 are reduced due to the reduced value of thickness (T1) between the signal layer and the closest reference (GND) plane.

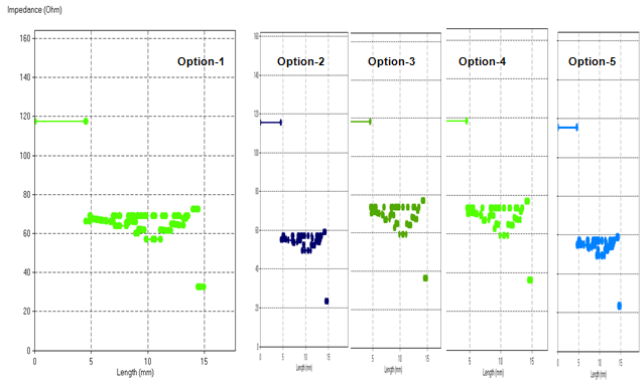

Figure 21

4. Conclusion

An efficient modeling, simulation and analysis methodology of characterizing the PDN and high-speed signal interfaces in a wirebond IC-package, considering discontinuities due to wirebonds, traces, vias and BGAs is described in this paper. Effects of wirebond diameter and material on the key electrical parameters, commonly used for evaluating and optimizing the power and signal integrity performance of the high-speed interface of the wirebond IC-package are discussed in detail. In addition, the effect of layout/stackup parameters on the key electrical parameters of the wirebond IC-package systems is illustrated in detail. The methodology presented in this paper, quantifies the key electrical parameters associated with each section of the signal and power nets, which in turn provides layout parameter optimization based design guidelines for efficient and cost-effective high-performance wirebond IC-package systems development.

5. Reference

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