Agenda

- **Power integrity challenges and solution**

- **New PI features in R14.5**

- **Power integrity case study**

        July 24, 2019

Power Integrity Challenges and Solution

Trends Requiring Chip Aware System Design

The die-to-die system is extremely complex:

- **Silicon driver/receiver**
- **3D component interconnect**
- **Chip to package**
- **Package to daughter card**
- **Daughter card to backplane**
- **Power delivery network effects**

Complex problems

- **High risk**
  - **New unfamiliar phenomena?**
- **High cost of design errors**

**Solving them is requiring new strategies and simulation tools.**
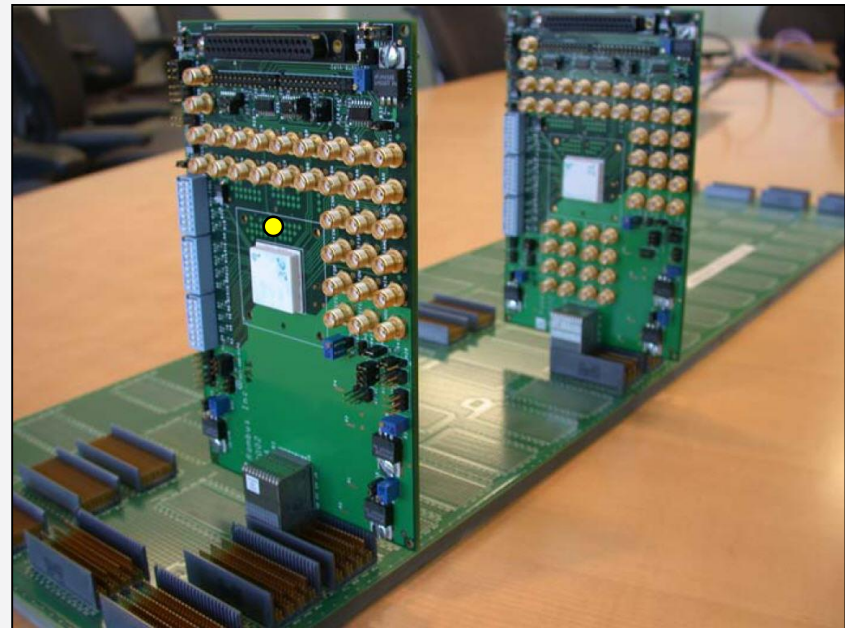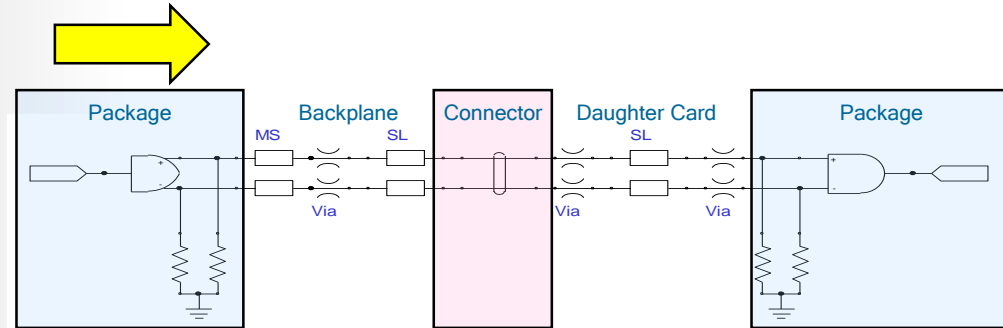
What is a Power Distribution Network (PDN)?

Complex multi-stage network supplying power to all devices in a system.

For typical products the PDN includes:

- **Voltage regulator module (VRM)**

- **Board power/ground planes and decoupling capacitors**

- **Package power/ground planes and decoupling capacitors**
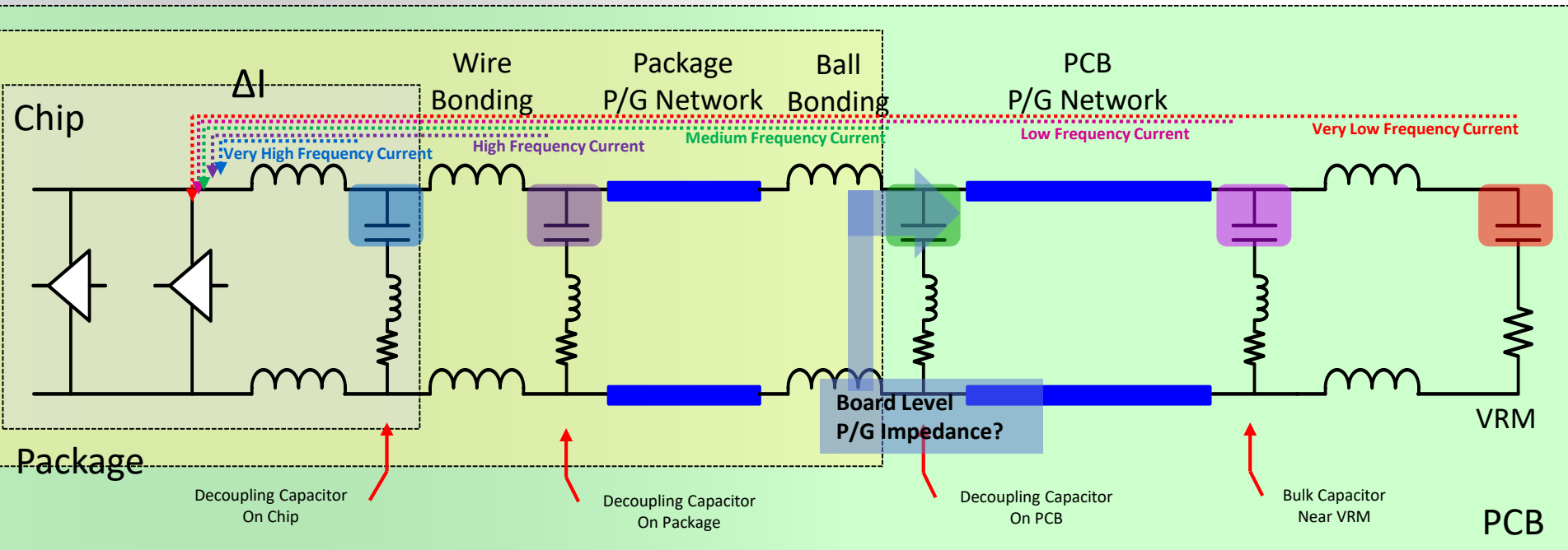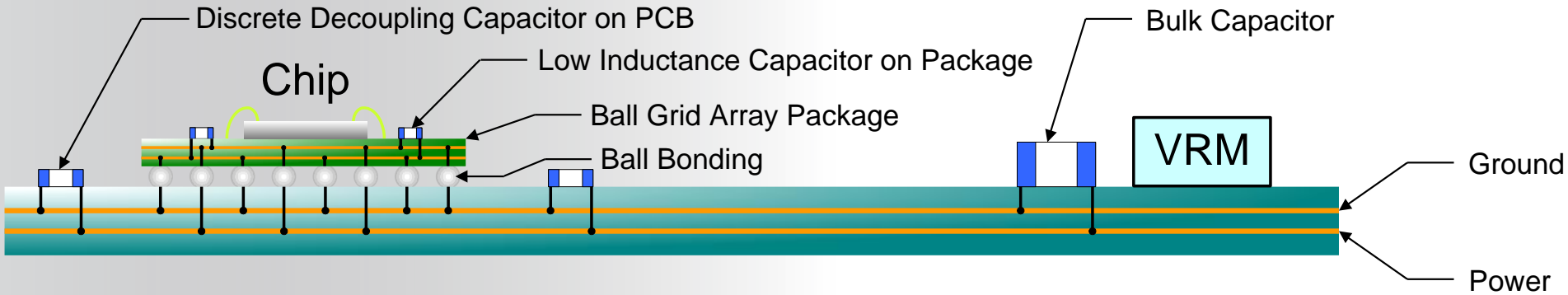
- **Chip power/ground structures and capacitance**
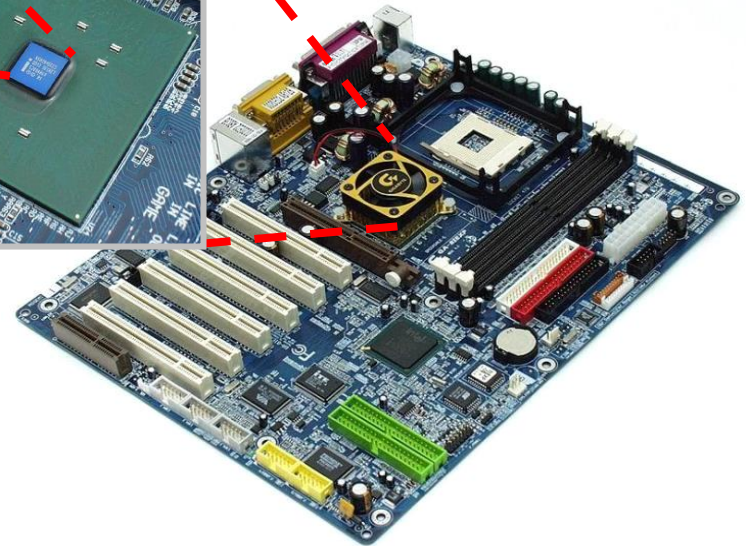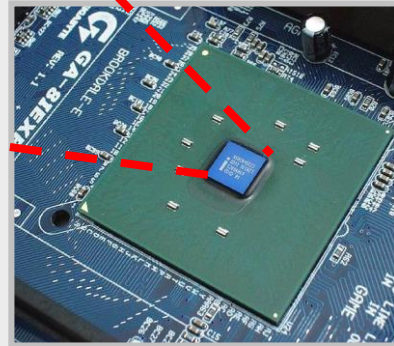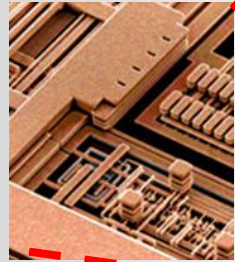
PDN Requirements:

- **Must deliver clean power to the ICs**

- **Must provide low impedance, low noise reference path for signals**
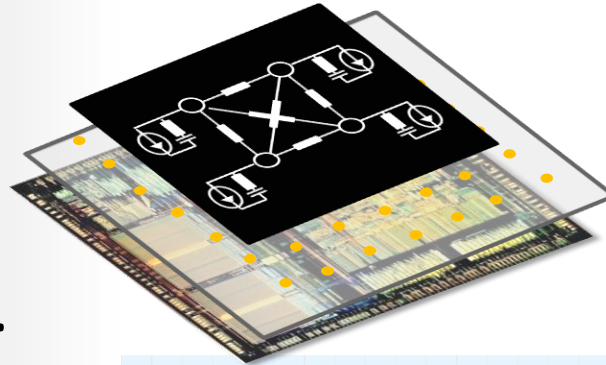
- **Must not contribute excessive EMI**

Board Level Power Integrity?

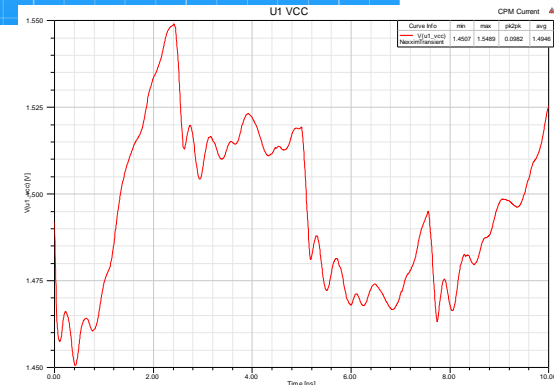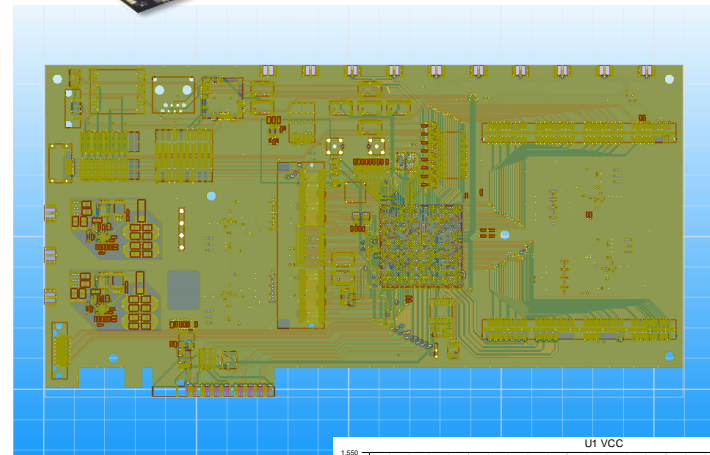**Full PDN**

ANSYS Chip-Aware PDN Solution

Redhawk generates a chip power model (CPM) including chip PDN parasitics and switching currents.

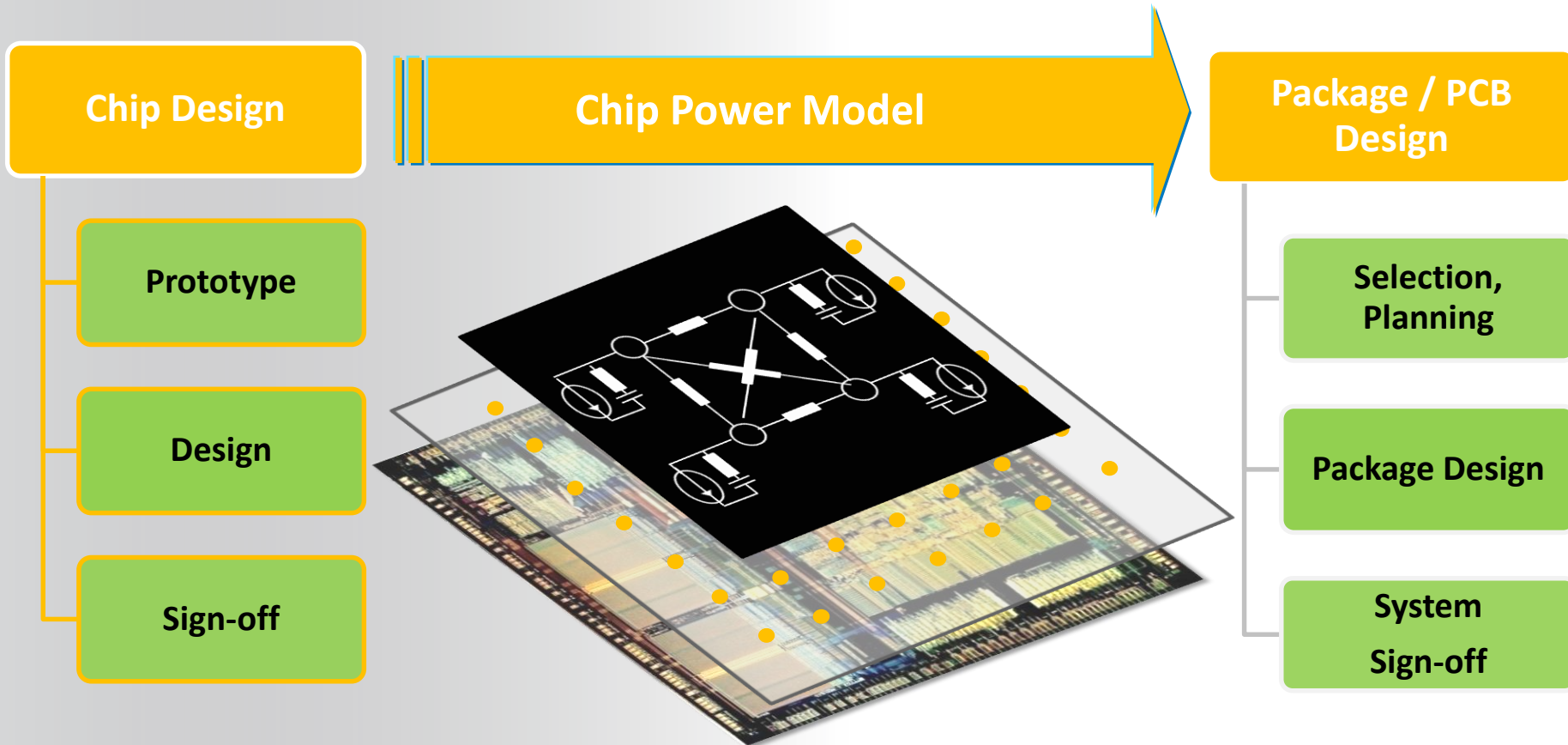**PSI and SIwave provide robust extraction of IC packages and boards with broadband S-parameter models.**

PI Advisor optimizes decoupling capacitor selection to meet a target impedance.

Designer SI simulates power noise in the time domain.
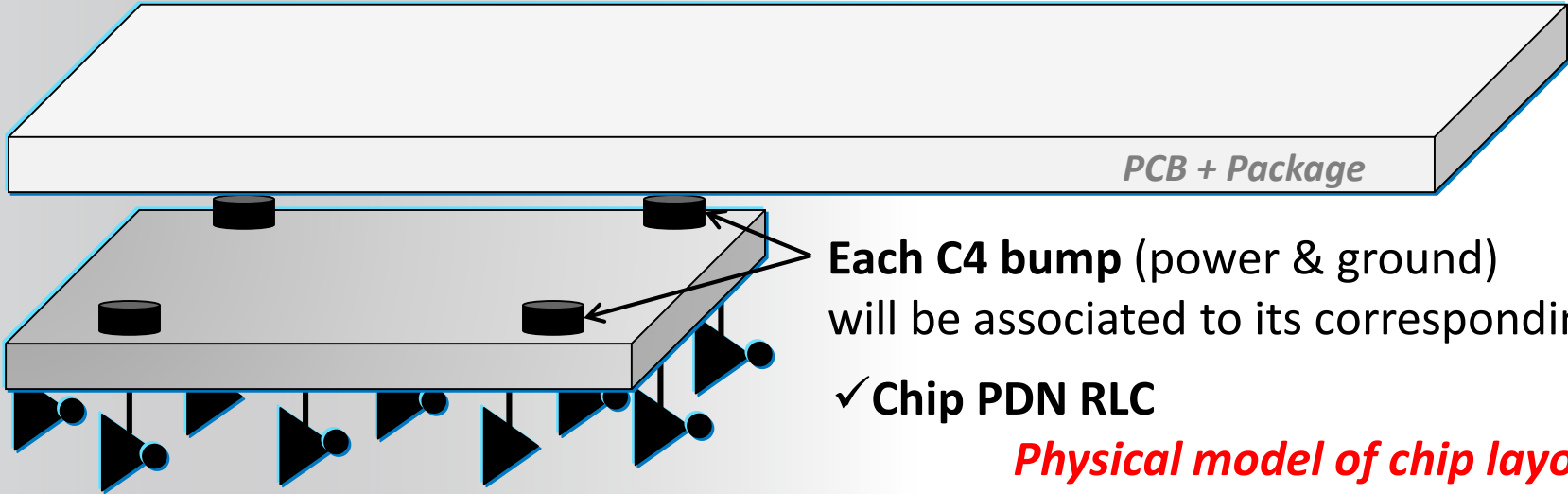
Chip Power Model (CPM)

July 24, 2019

CPS Convergence Using CPM

Chip Design
- Prototype
- Design
- Sign-off

Chip Power Model

Package / PCB Design
- Selection, Planning
- Package Design
- System Sign-off

July 24, 2019

What's in a CPM?

PCB + Package

Each C4 bump (power & ground)
will be associated to its corresponding:

✓**Chip PDN RLC**
  Physical model of chip layout

✓**Transistor/cell current /cap/ESR**
  Electrical model of chip layout

**CPM is topological,
physical and activity based**

```
.SUBCKT PowerModel p1 p2
*****************************************************
* Apache RedHawk Chip Power Model [Accurate RC reduction]
**********  *****************************************
          * Apache RedHawk Chip Power Model [ Ver 1.00 ]
          * Version: 10.2    Linux32e3 (Jan 20 00:31:13 2011)
* Pad name *****************************************
* DPOWER21 .INCLUDE "PowerModel.sp.inc"
* DGROUND20
          * Begin Chip Package Protocol --->
* No connec * die_area 0 0 4920.62 5000.36
C0_1 p1 p2 * Start Units
R_1_1 p1 n3 *   Length um
C_1_1 n3 p2 * End Units
R_2_1 p1 n4 * DPOWER21    :    (4905.000000 3279.000000)  :  p1  = PAR_0_0_VDD
C_2_1 n4 p2 * DGROUND20   :    (4880.000000 3219.000000)  :  p2  = PAR_0_0_VSS
R_3_1 p1 n5 * End Chip Package Protocol <---
C_3_1 n5 p2
R_4_1 p1 n6 .subckt adsPowerModel p1 p2
C_4_1 n6 p2
.ENDS       Xpdn  p1 p2 PowerModel

            Icursig1 p1 p2 pwl(
            + 0.000000ps 0.589435
            + 150.000000ps 0.854897
            + 240.000000ps 0.867186
            + 330.000000ps 0.827372
```

© 2011 ANSYS, Inc.   July 24, 2019

Benefits of CPM

Chip Current

Traditional die model	Apache CPM

Simplifying assumption of all gates switching at same time

Apache CPM: supports both static and dynamic models

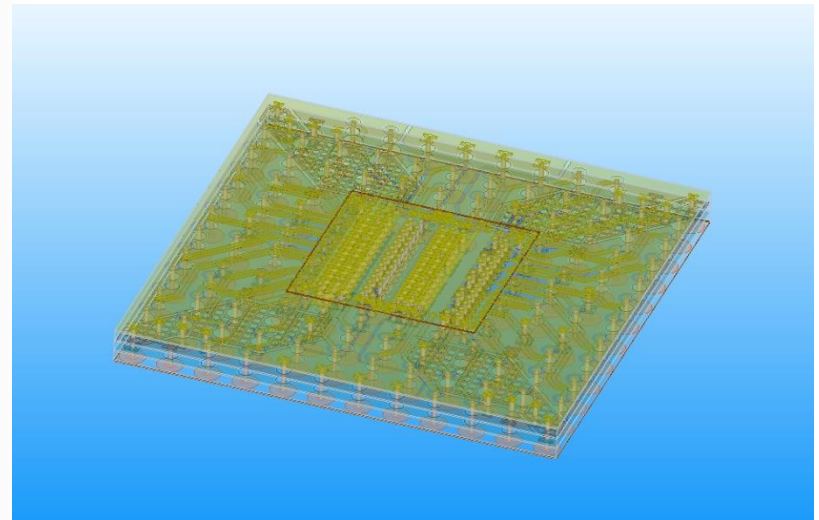**Chip Parasitics**

Estimated Cdie
Missing Rdie, Ldie

Single Lumped Model
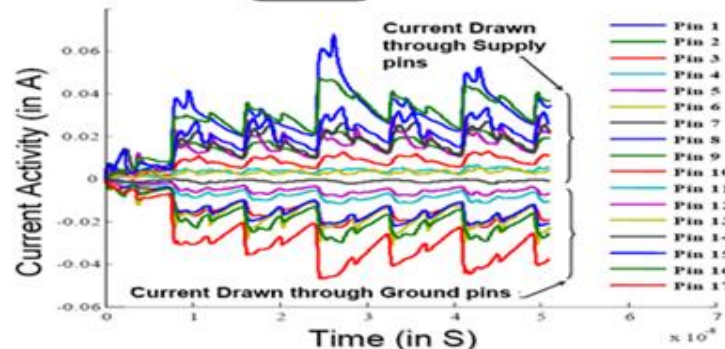
CPM includes all die parasitics

Power-grid RLC
Intrinsic De-cap
Intentional De-cap
Instance Load Capacitance
Well Capacitance

July 24, 2019

SIwave CPM Integration
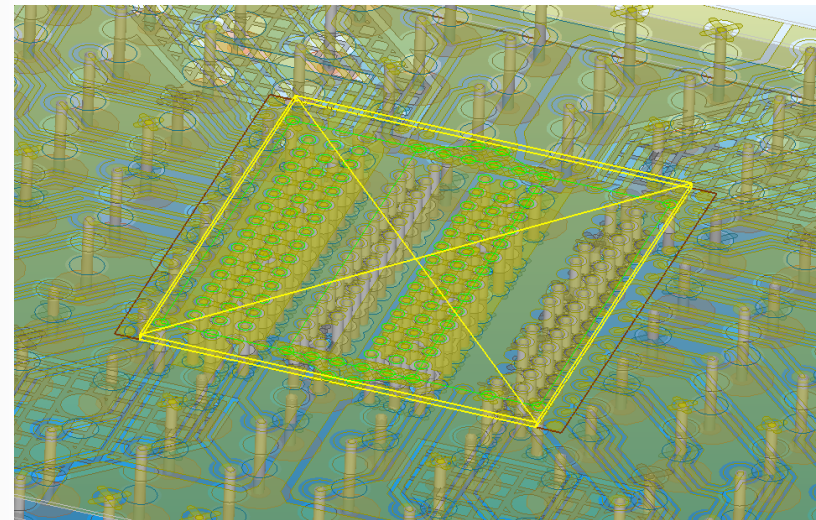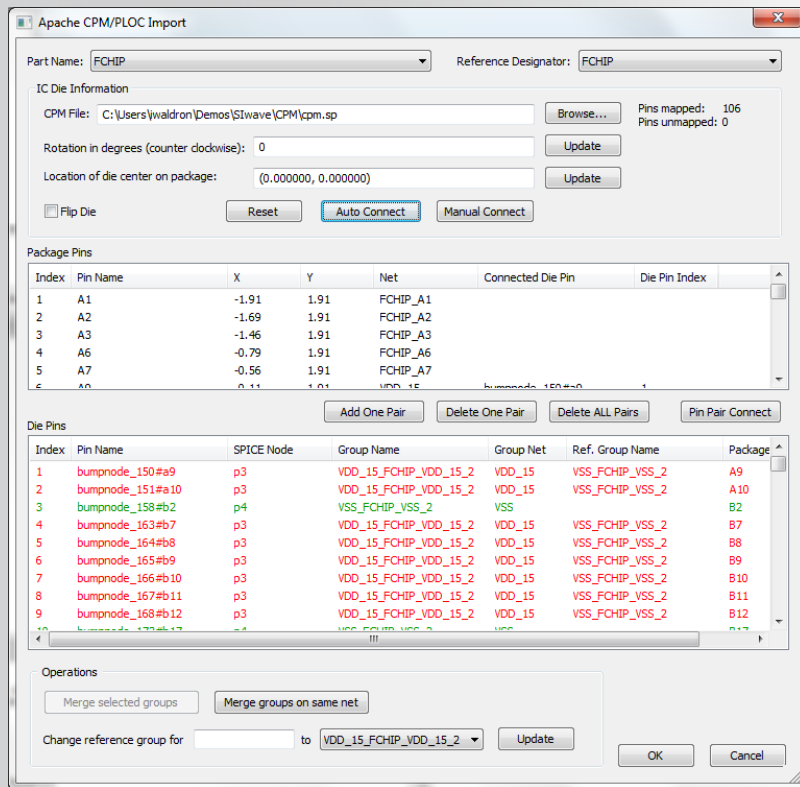
SIwave CPM integration includes the following:

- **Import of die PDN for inclusion in frequency-domain extractions**
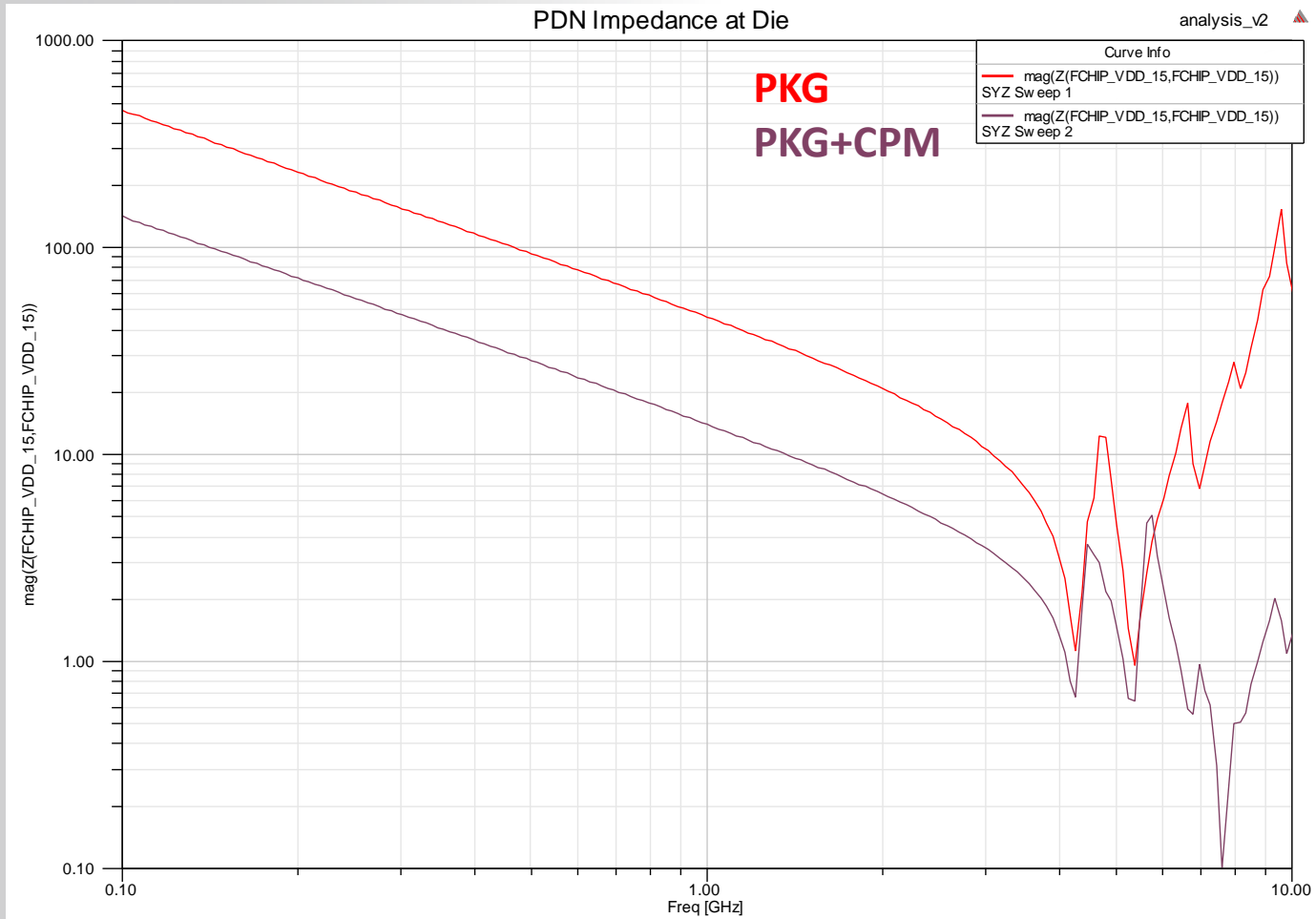
- **Automatic matching of die pin to CPM pin locations**

SIwave CPM Setup

© 2011 ANSYS, Inc.   July 24, 2019

CPM Impedance Effect

© 2011 ANSYS, Inc.   July 24, 2019

Sentinel PSI

July 24, 2019
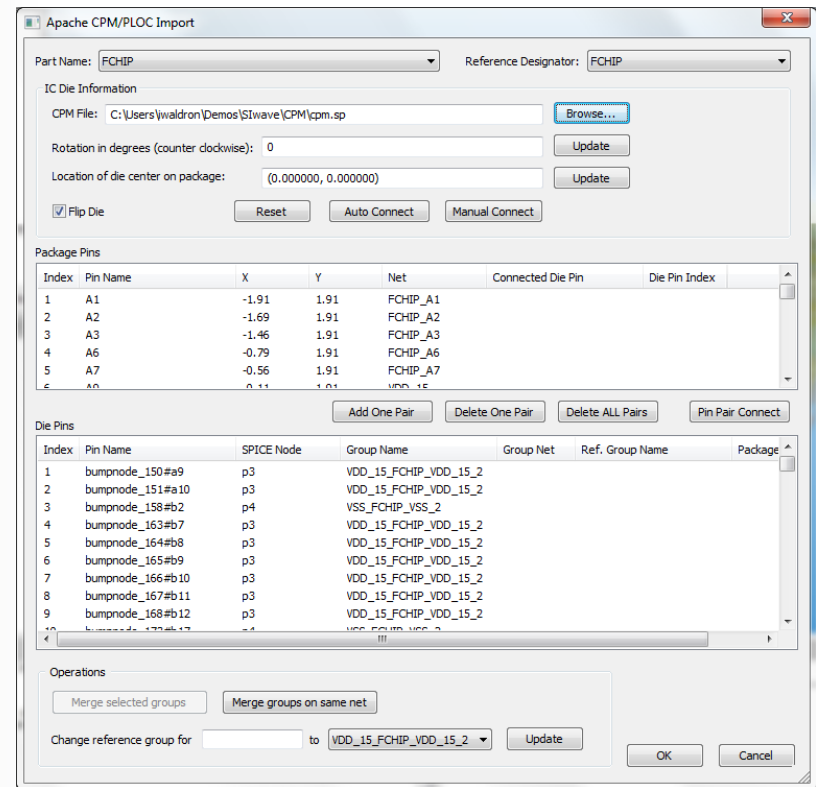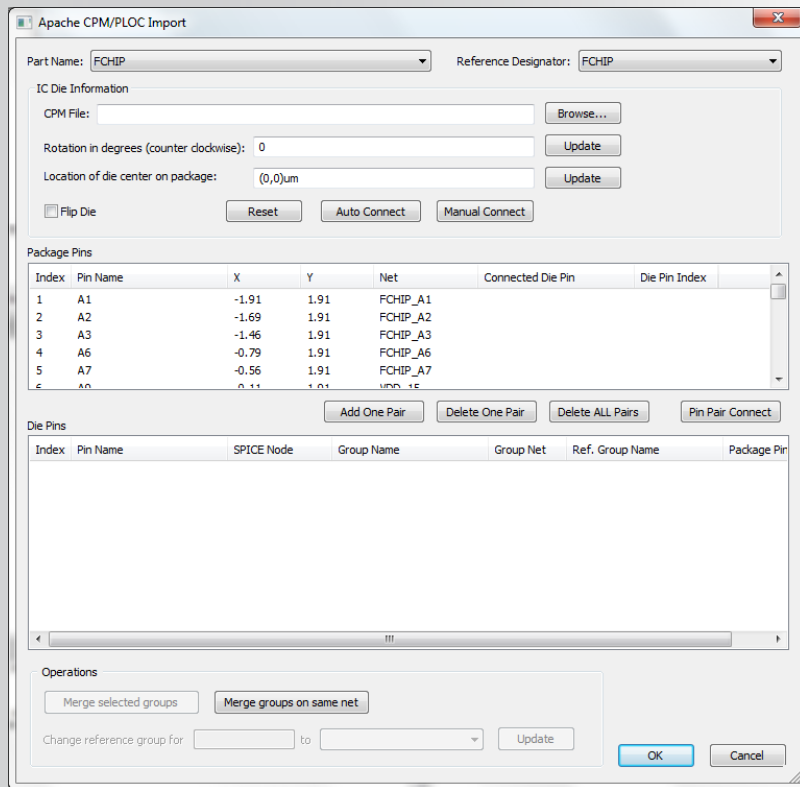
ANSYS Package/Board Solvers

3D full-wave   Hybrid full-wave   **SPEED**

Sentinel-PSI

SIwave
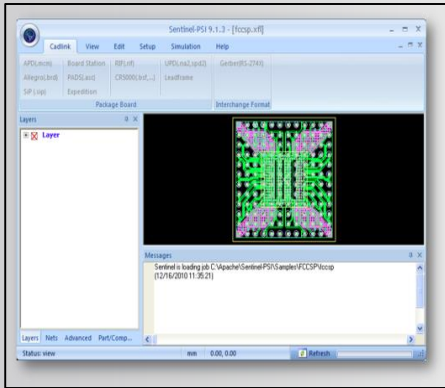
• Fast FEM using prism elements
• Tailored for PI package analysis

• FAST Hybrid method for PKG/BRD
• Handles many, but not all 3D effects

**Trade-off speed for 3D accuracy**

Fast

Package/PCB structures Containing

- **Highly perforated metal planes**
  - **Swiss Cheese PWR/GND planes**
  - **Hatched PWR/GND planes**
- **Two layer PCBs without reference layers**
- **Transmission lines over non-ideal ground**
- **Ports with unreferenced terminals**
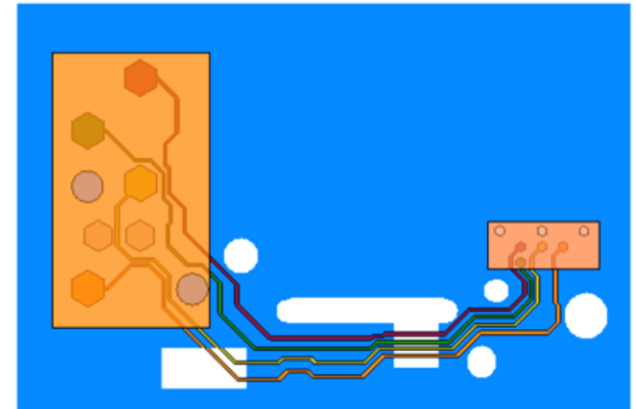- **Visualization of PWR/GND AC currents**
- **Vias with large anti-pads**
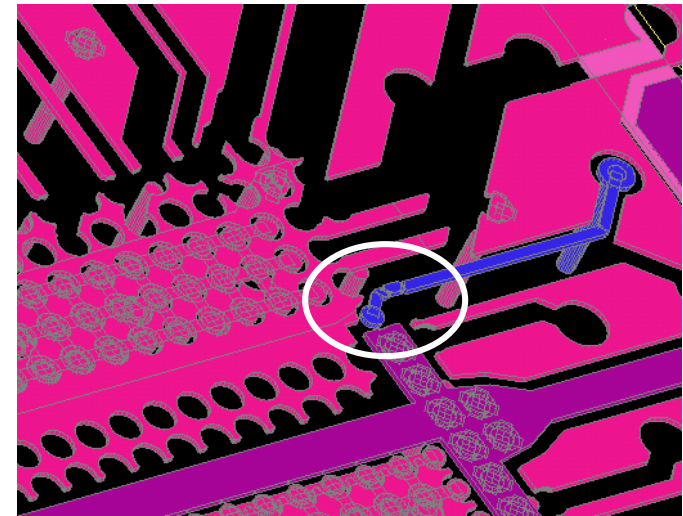
Port With Unreferenced Terminal

Large continuous anti-pads
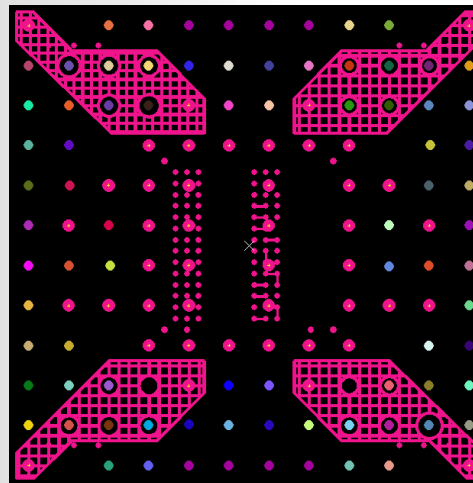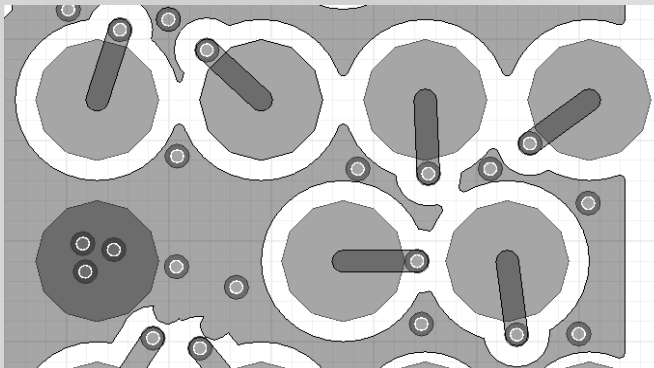
Typical Hatched Plane



Lines over non-ideal ground cutouts

PI Advisor

PI Advisor is an addon for Siwave that automatically optimizes capacitor selection to meet a target impedance:

Inputs:

- **Capacitor locations**

- **Candidate capacitors**

Outputs:

- **Capacitor schemes that indicate which candidate, if any, to populate at each location.**

- **Impedance versus target for each scheme.**

               July 24, 2019

Target Impedance

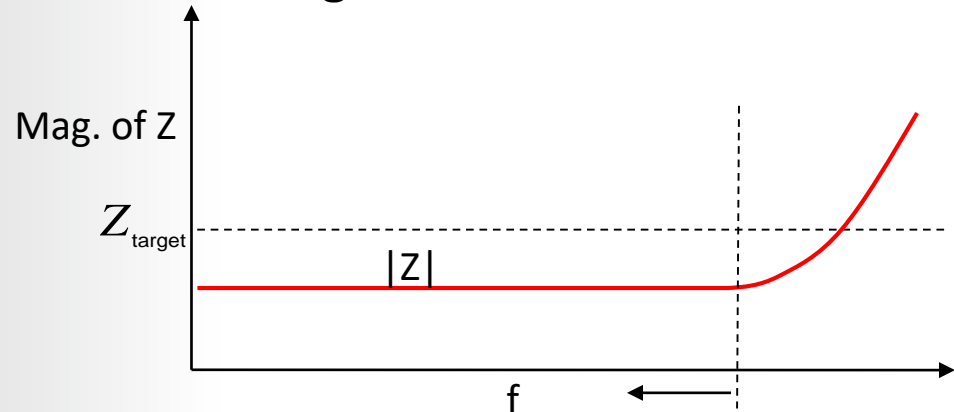July 24, 2019
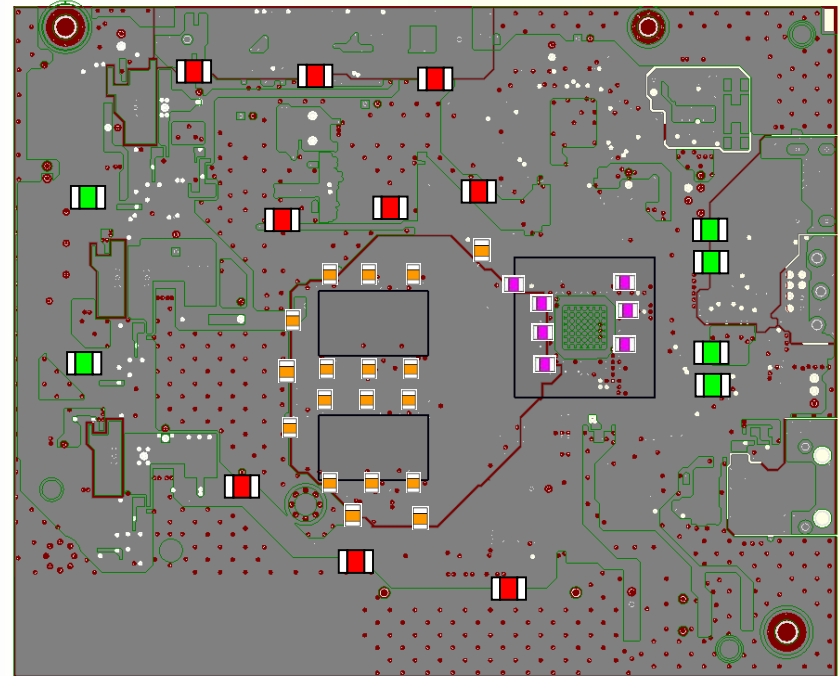
Target Impedance

- **Designing for power integrity often involves a target impedance**
  - Maximum allowable impedance magnitude over frequency which will result in acceptable voltage noise
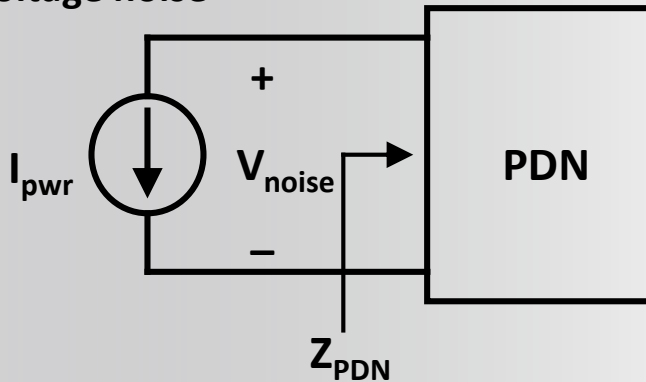
$$V_{noise} = I_{pwr} Z_{PDN}$$

(Quantities are phasors)

- **Several technical references contain something like**

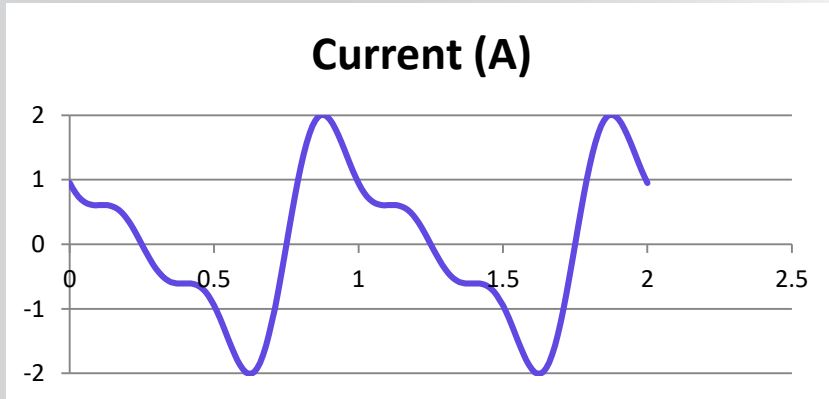$$Z_{target} = \frac{V_{noise(max)}}{I_{pwr(ACpeak)}}$$

- **An example can illustrate the complexities with this approach…**

        July 24, 2019

A Simple Target Impedance Example

- **Suppose we have a power current with the periodic AC component shown below (peak amplitude of 2A):**

Current (A)

$$I(t) = |I_1| \cos(2\pi t + \theta_{I1})$$
$$+|I_2| \cos(4\pi t + \theta_{I2})$$
$$+|I_3| \cos(6\pi t + \theta_{I3})$$

- **Suppose we have a maximum allowable voltage amplitude of 1V**
- **The simple approach suggests a max Z$_{PDN}$ of 0.5Ω over the frequency components contained in the current will satisfy the noise requirement**
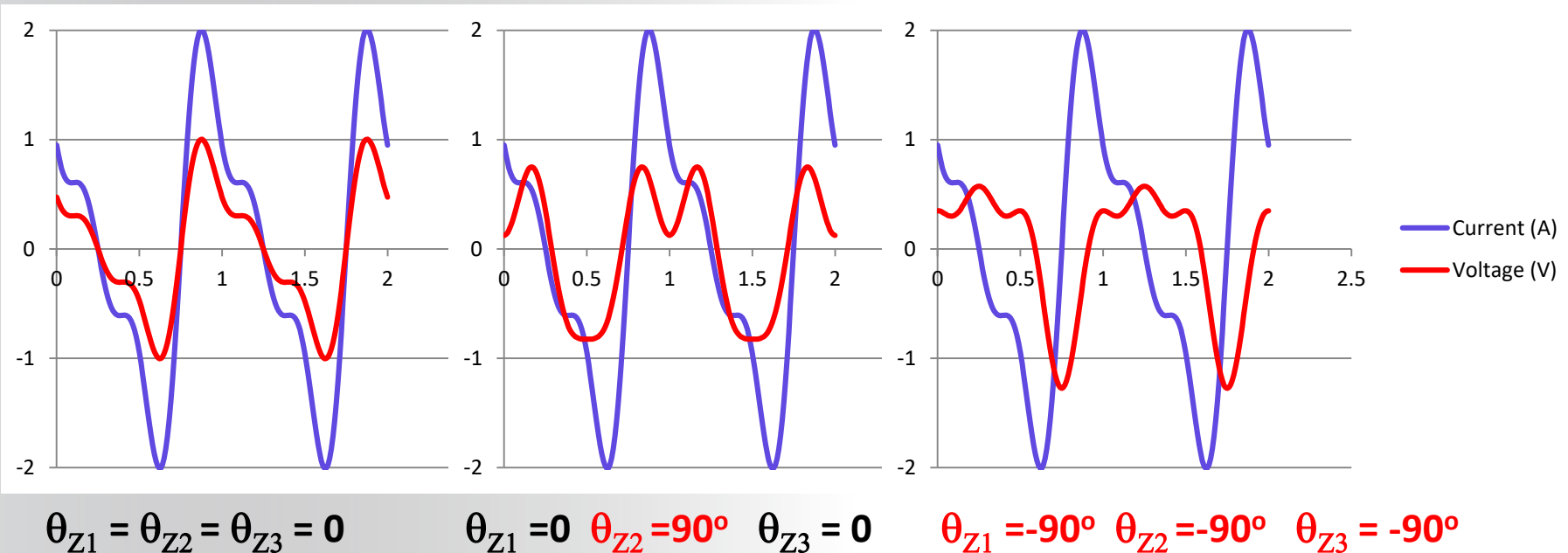
$$\left|Z_{PDN}\right|$$

0.5Ω
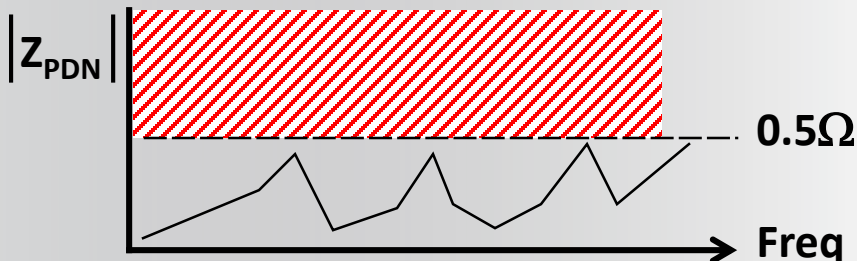
Freq

$$V_f(t) = \left|I_f\right| \cdot \left|Z_f\right| \cos\left(2\pi f t + \theta_{If} + \theta_{Zf}\right)$$

But our impedance tolerance does not specify phase

     July 24, 2019

Effects of Different Impedance Phases

- **Assume our PDN impedance just satisfies the requirement at each frequency: $|Z_1| = |Z_2| = |Z_3| = 0.5\Omega$, but vary the impedance phase assumptions**

$\theta_{Z1} = \theta_{Z2} = \theta_{Z3} = 0$ $\theta_{Z1} = 0$ $\theta_{Z2} = 90°$ $\theta_{Z3} = 0$ $\theta_{Z1} = -90°$ $\theta_{Z2} = -90°$ $\theta_{Z3} = -90°$

Simple approaches to calculating target impedance can provide a useful guide, but results should be verified with time-domain simulation

     July 24, 2019

Target Impedance Notes

Reliance on a purely resistive target impedance may not bound the resulting time-domain voltage waveform to the desired amplitude.

Target impedance calculations should take into account the impedance phase as well as magnitude, but the current state-of-the-art does not.

More to come from ANSYS on this topic...

          July 24, 2019

Power Integrity Case Study

        July 24, 2019

PDN Under Test

1.5V power supply for FPGA on board.

Chip included as Apache CPM.

Package included as static S-parameters.

Board extracted with SIwave 7.

Simulation includes:

- GND

- VCC_1V5

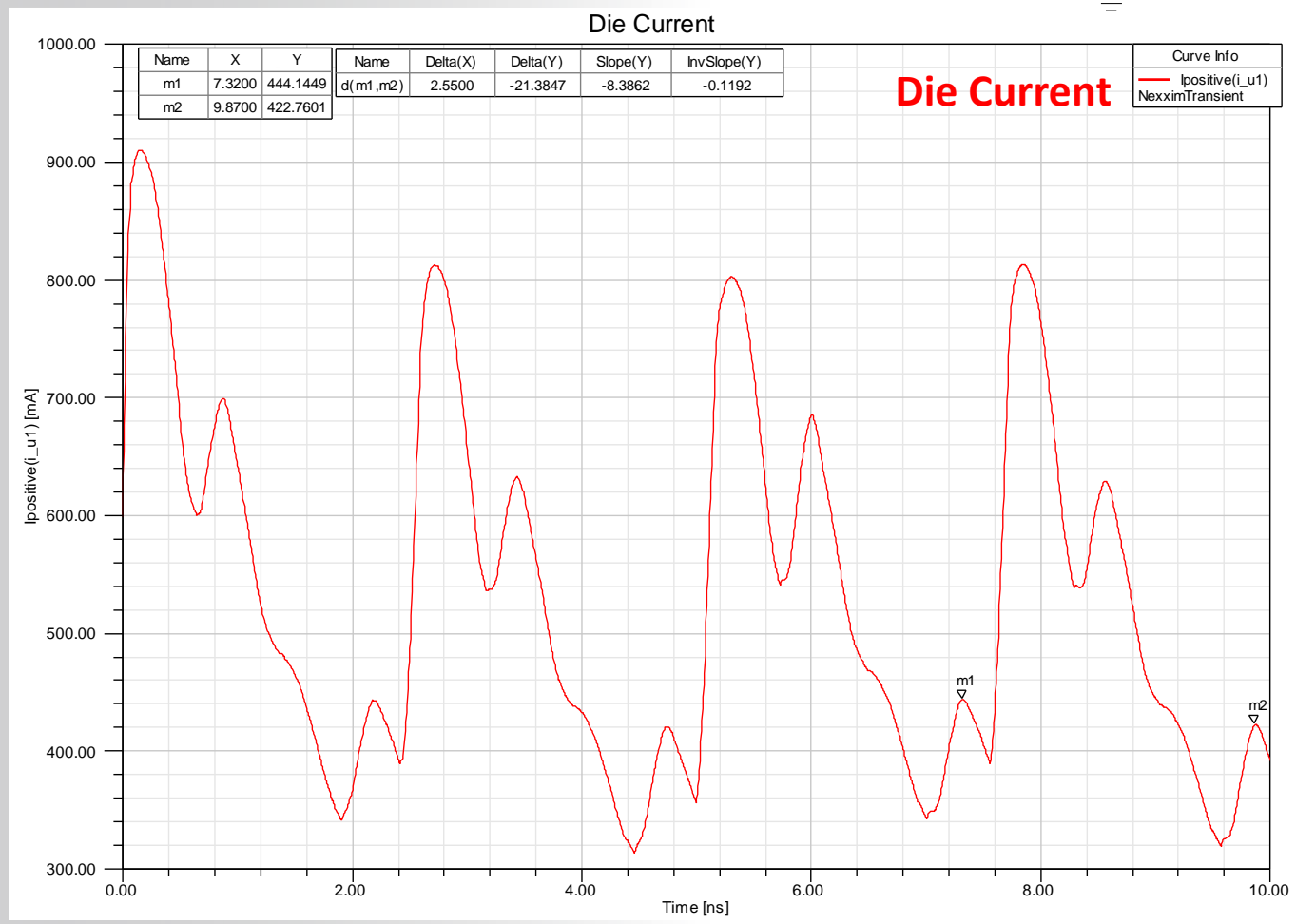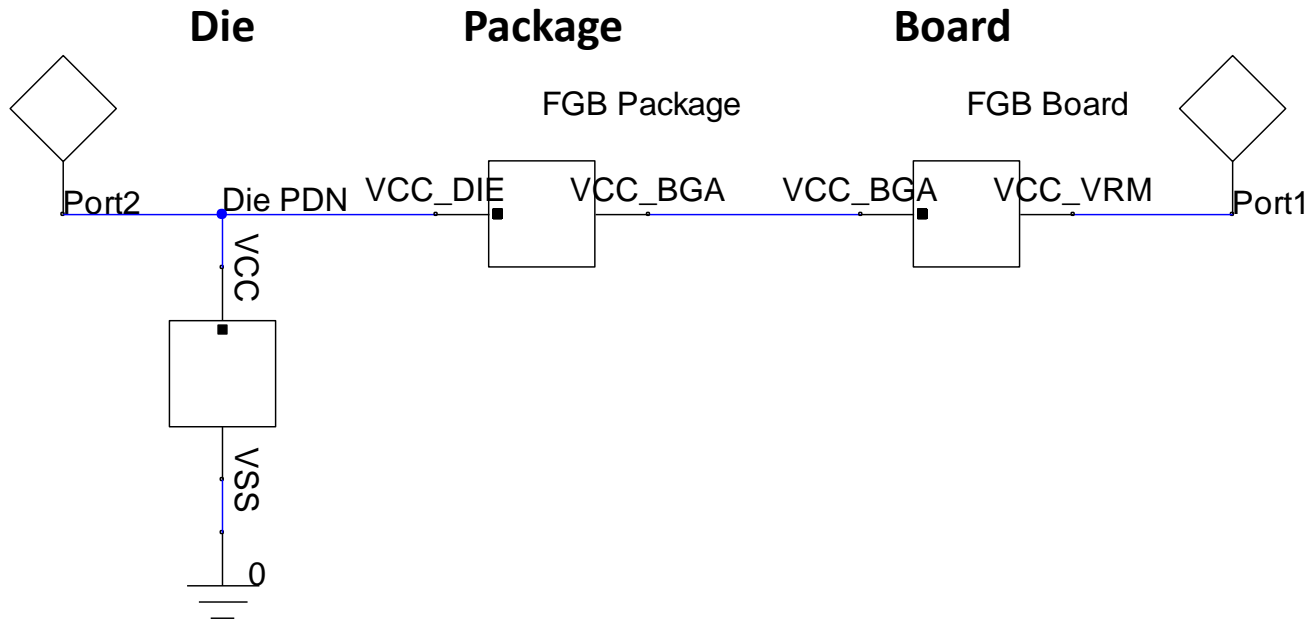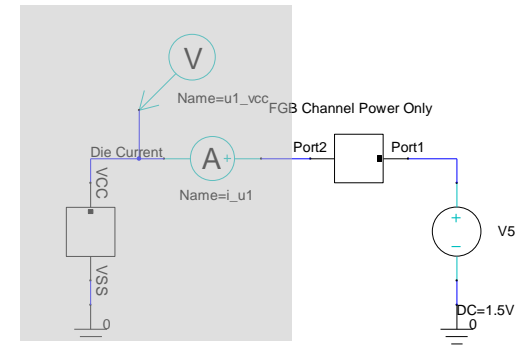System excited by CPM currents.

July 24, 2019

Die Current

PDN Channel

Die   **Package**   **Board**

FGB Package   FGB Board

Port2   Die PDN   VCC_DIE   VCC_BGA   VCC_BGA   VCC_VRM   Port1

VCC

VSS

0
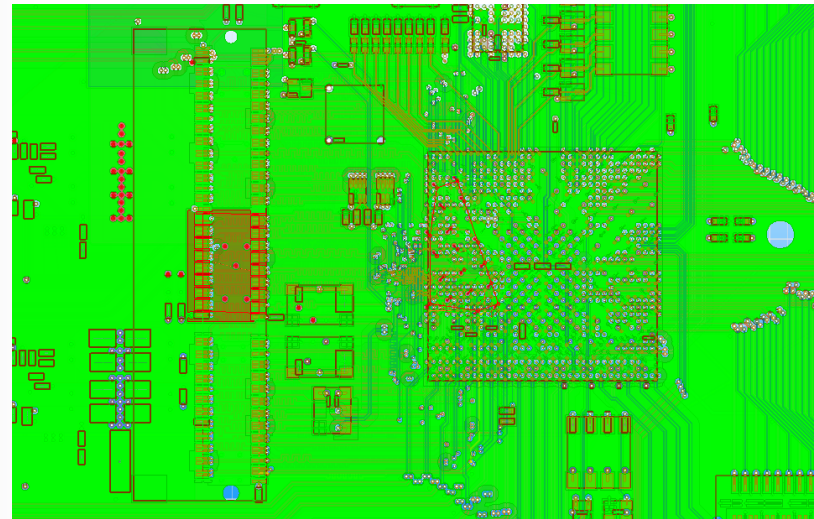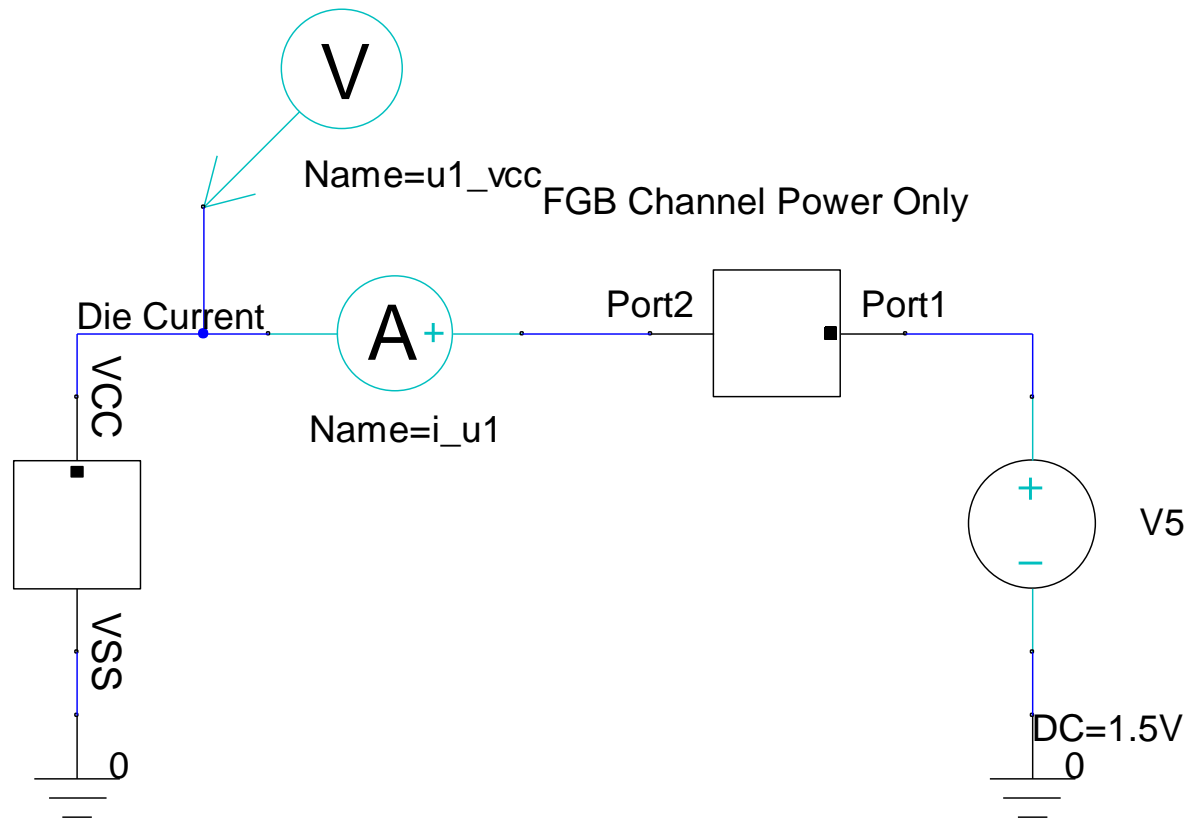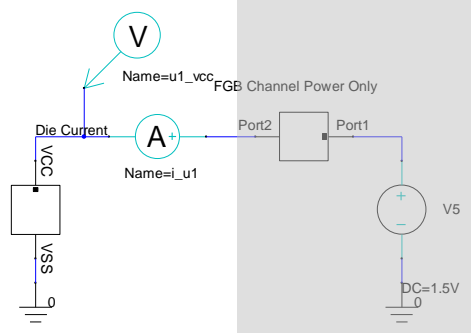
PDN Impedance Components

Full PDN Impedance

© 2011 ANSYS, Inc.   July 24, 2019
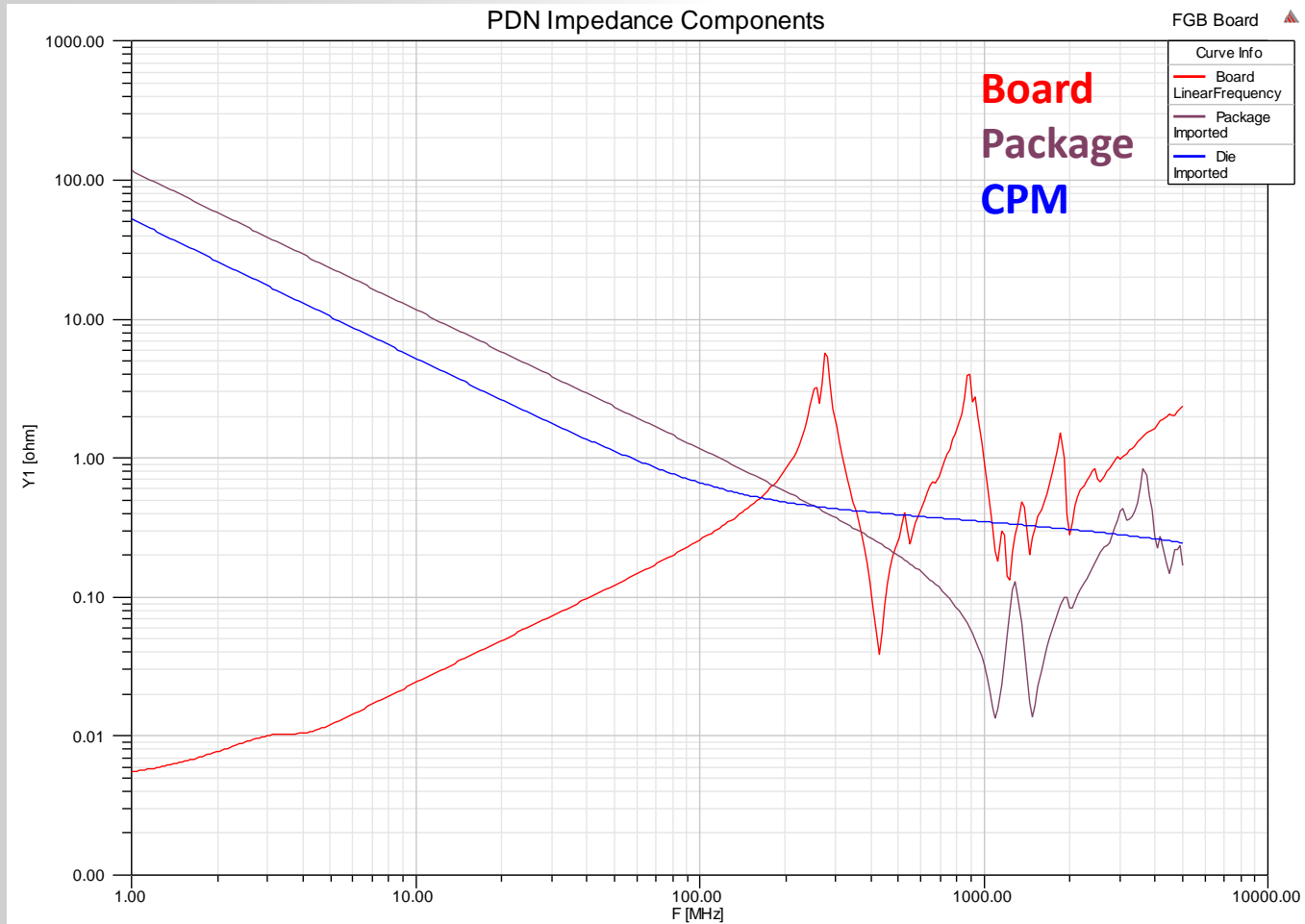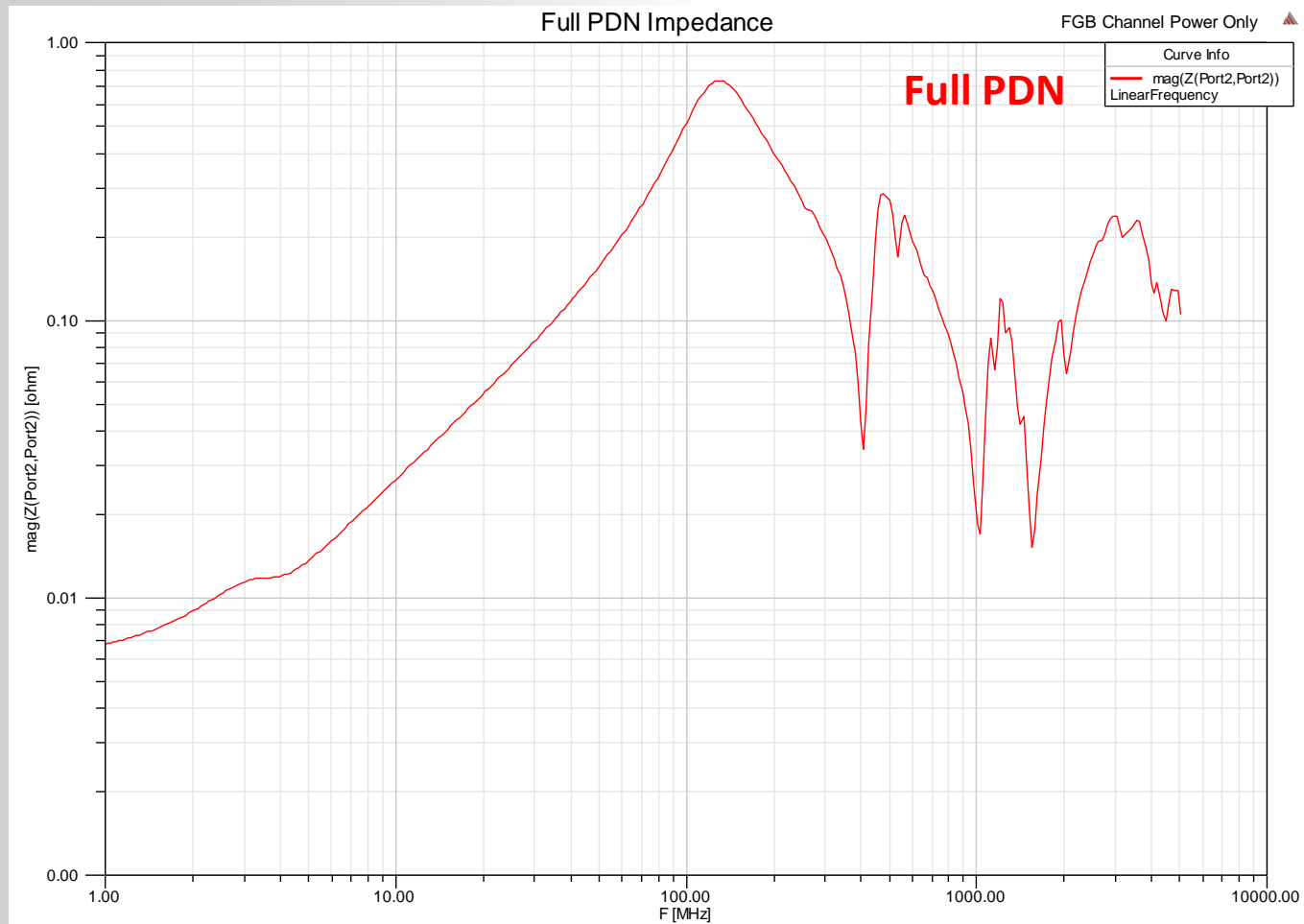
Package Model Fit

Package Model Fit

© 2011 ANSYS, Inc.   July 24, 2019

Die Model Fit

Port1

C55

3 nF

3e-009farad

R54

0.3 ohm

0.3

0

Die Model Fit

© 2011 ANSYS, Inc.   July 24, 2019
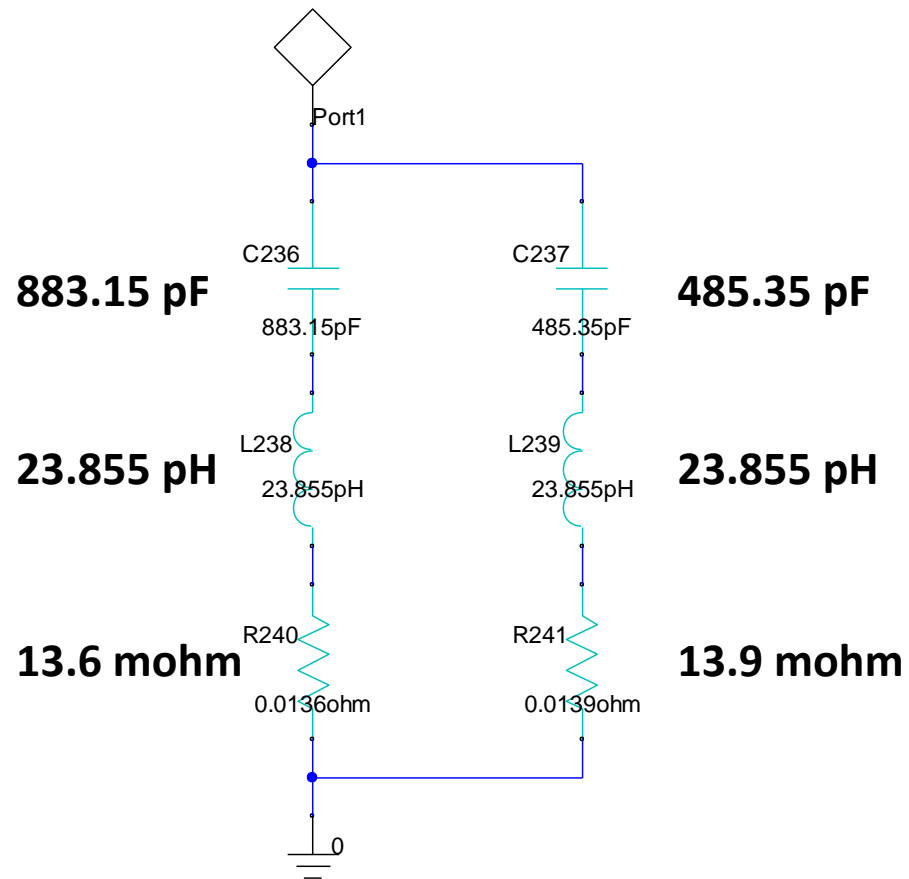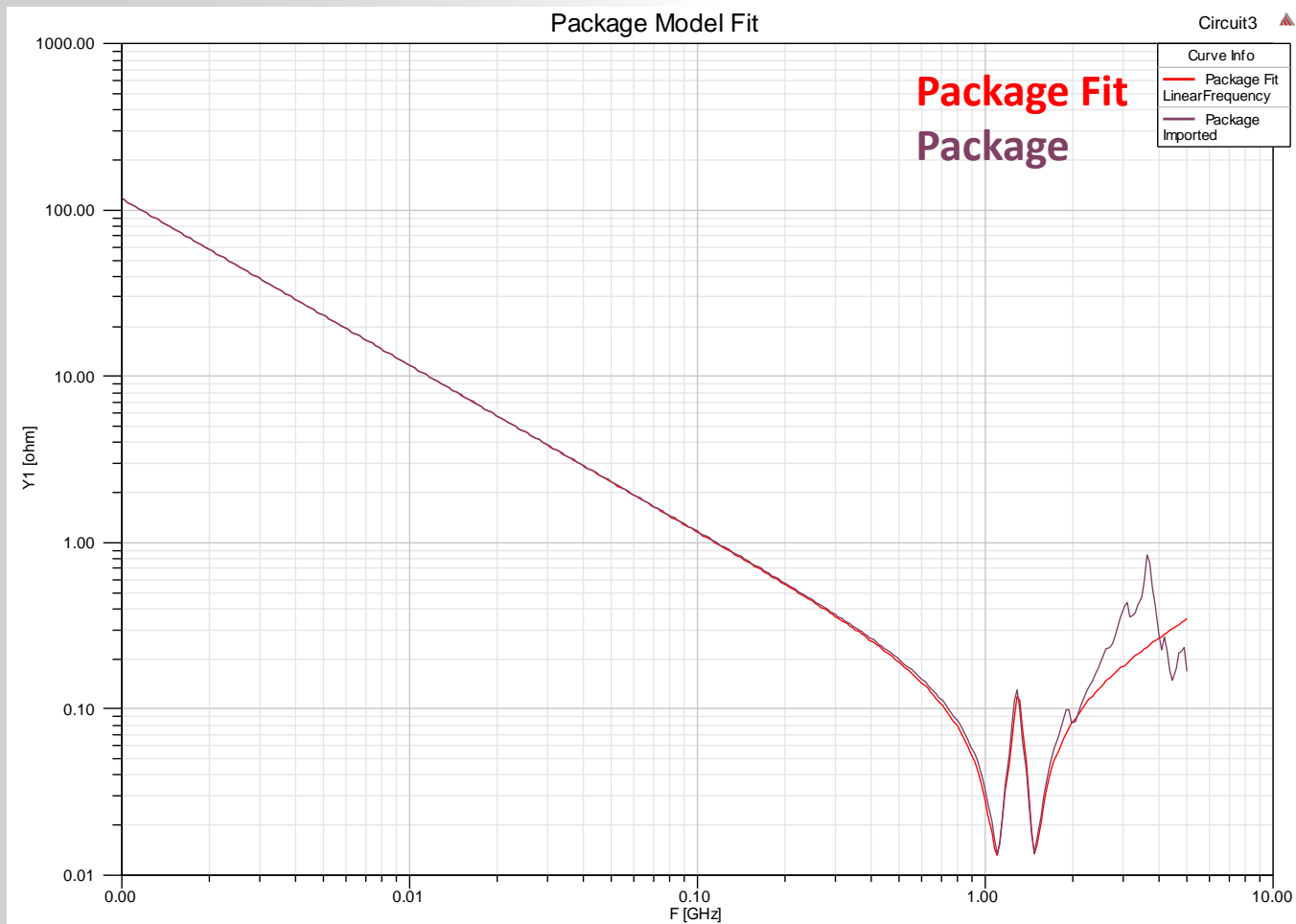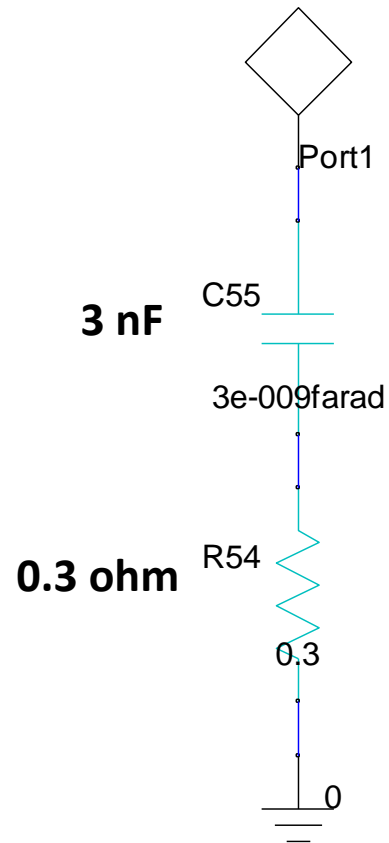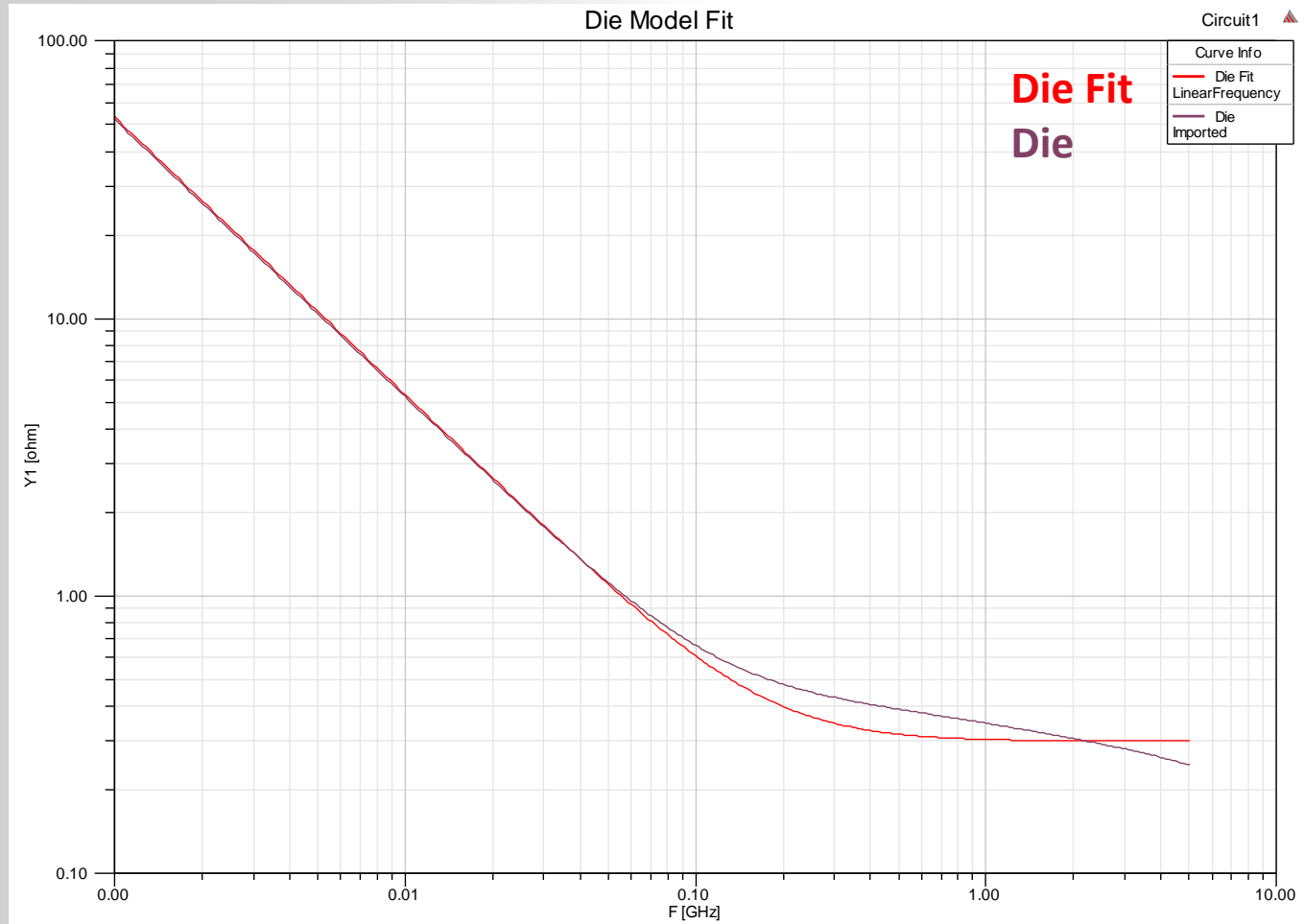
Board with Package/Die Fits

© 2011 ANSYS, Inc.   July 24, 2019
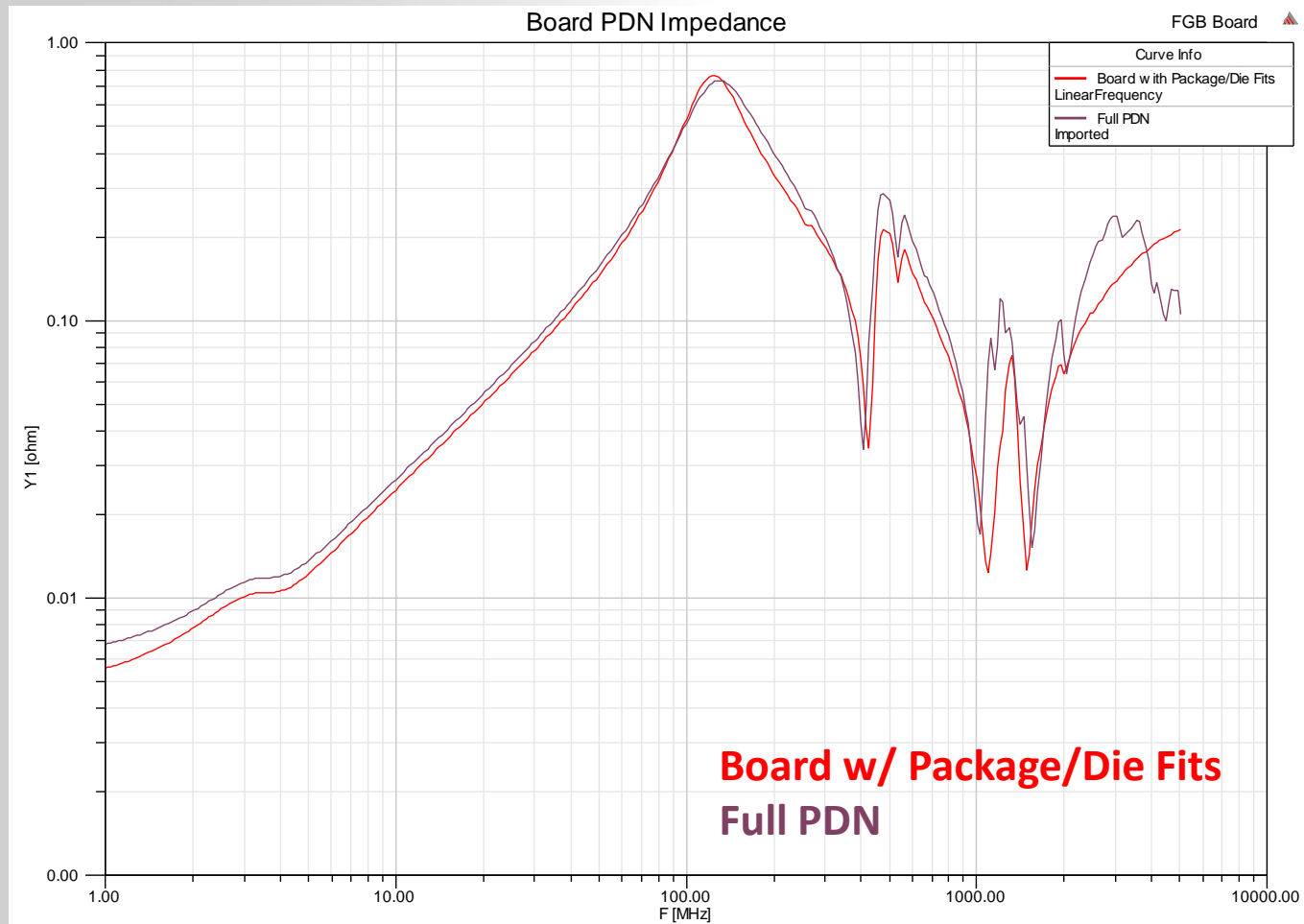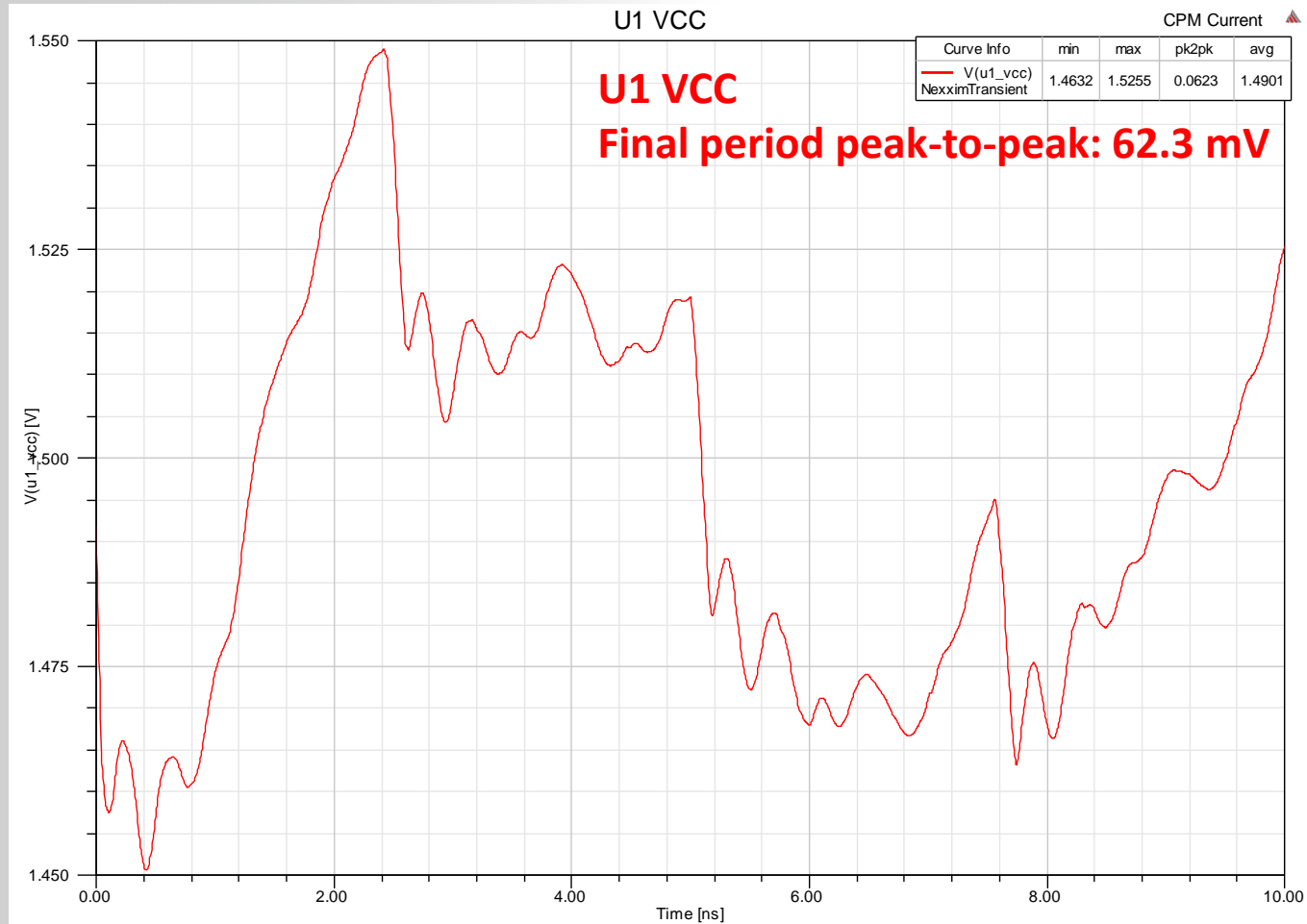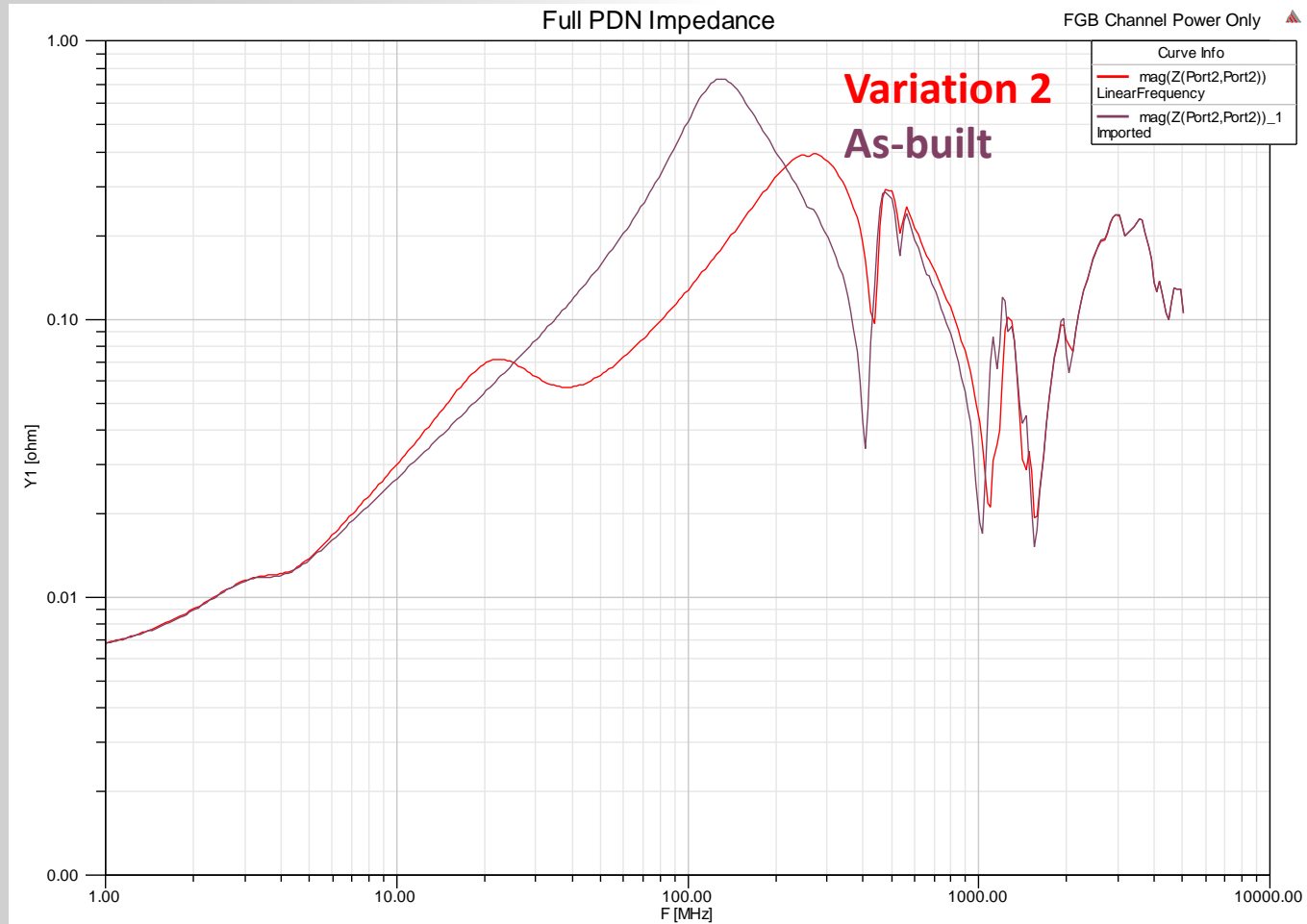
Board Variations Analyzed

1. **As initially designed.**

   – **Eight 100 uF bulk capacitors at VRM output, two 10 uF capacitors, and two 1 uF capacitors.**

2. **With added high-frequency capacitors.**

   – **12 0.01 uF capacitors placed on bottom layer below FPGA**

3. **With PI Advisor-optimized capacitor solution.**

   – **Target impedance: 0.3 ohms up to 1 GHz**

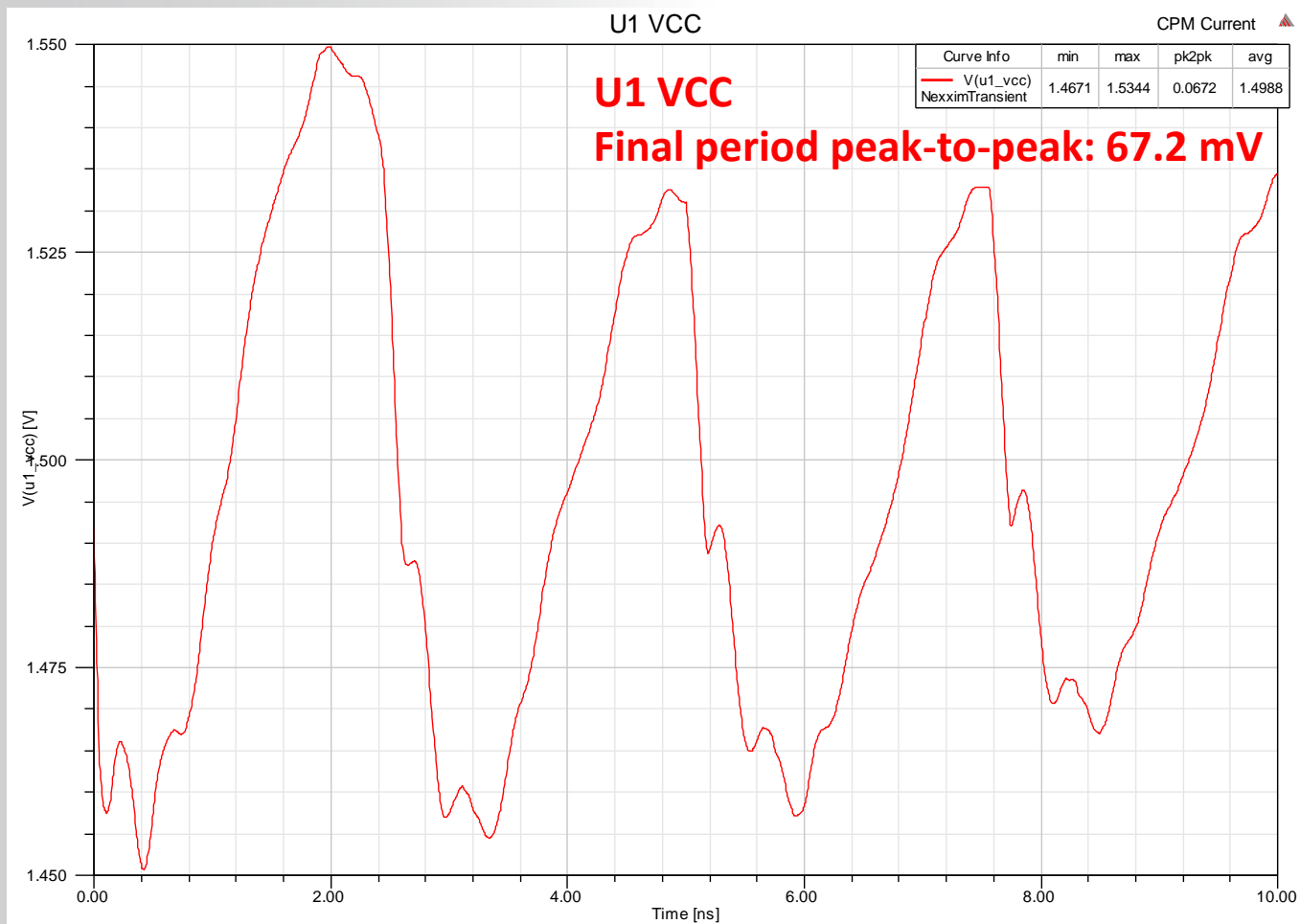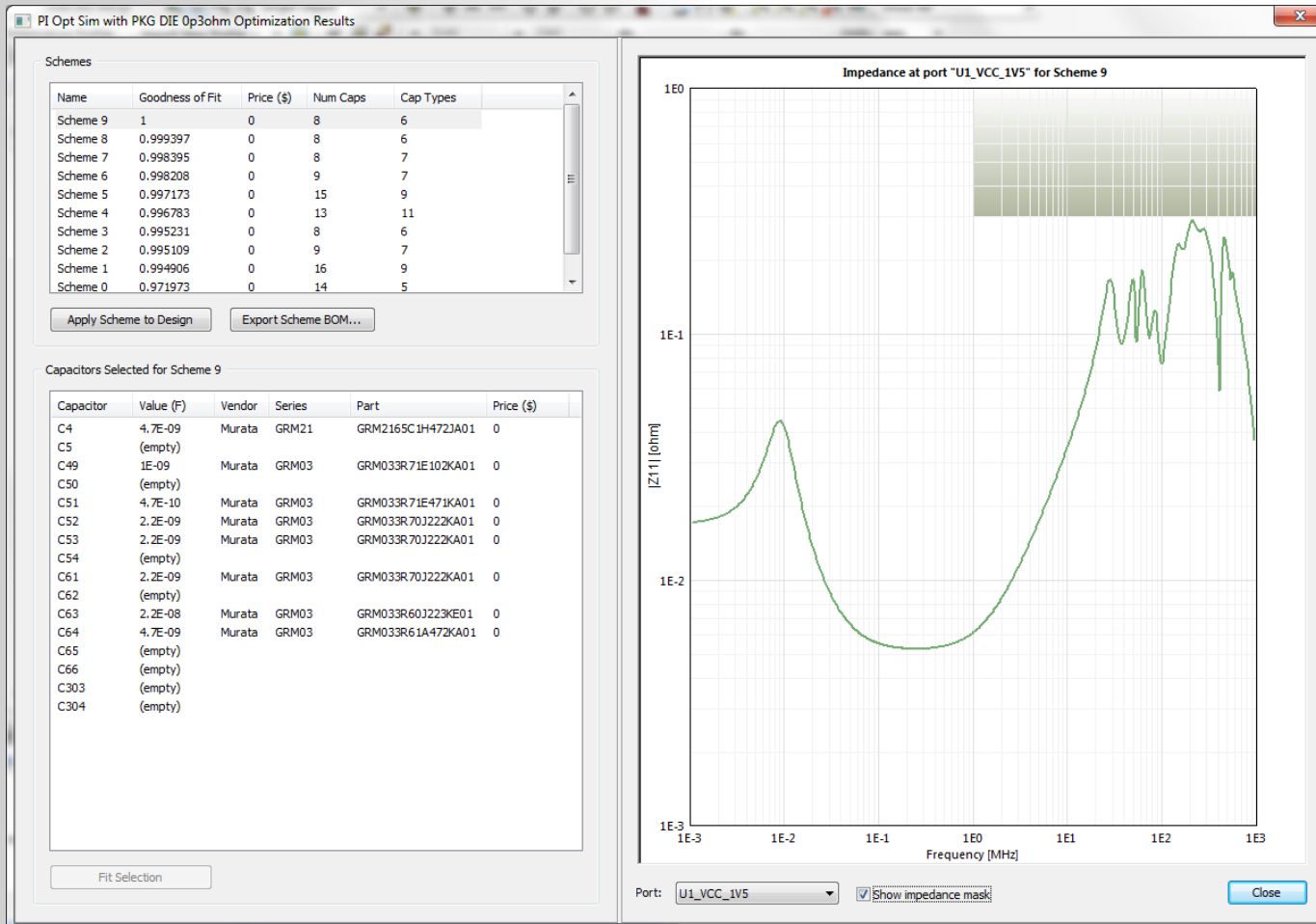   – **Package RLC fit and die RC fit included at board FPGA footprint**

           July 24, 2019

Variation 2: Added Capacitors
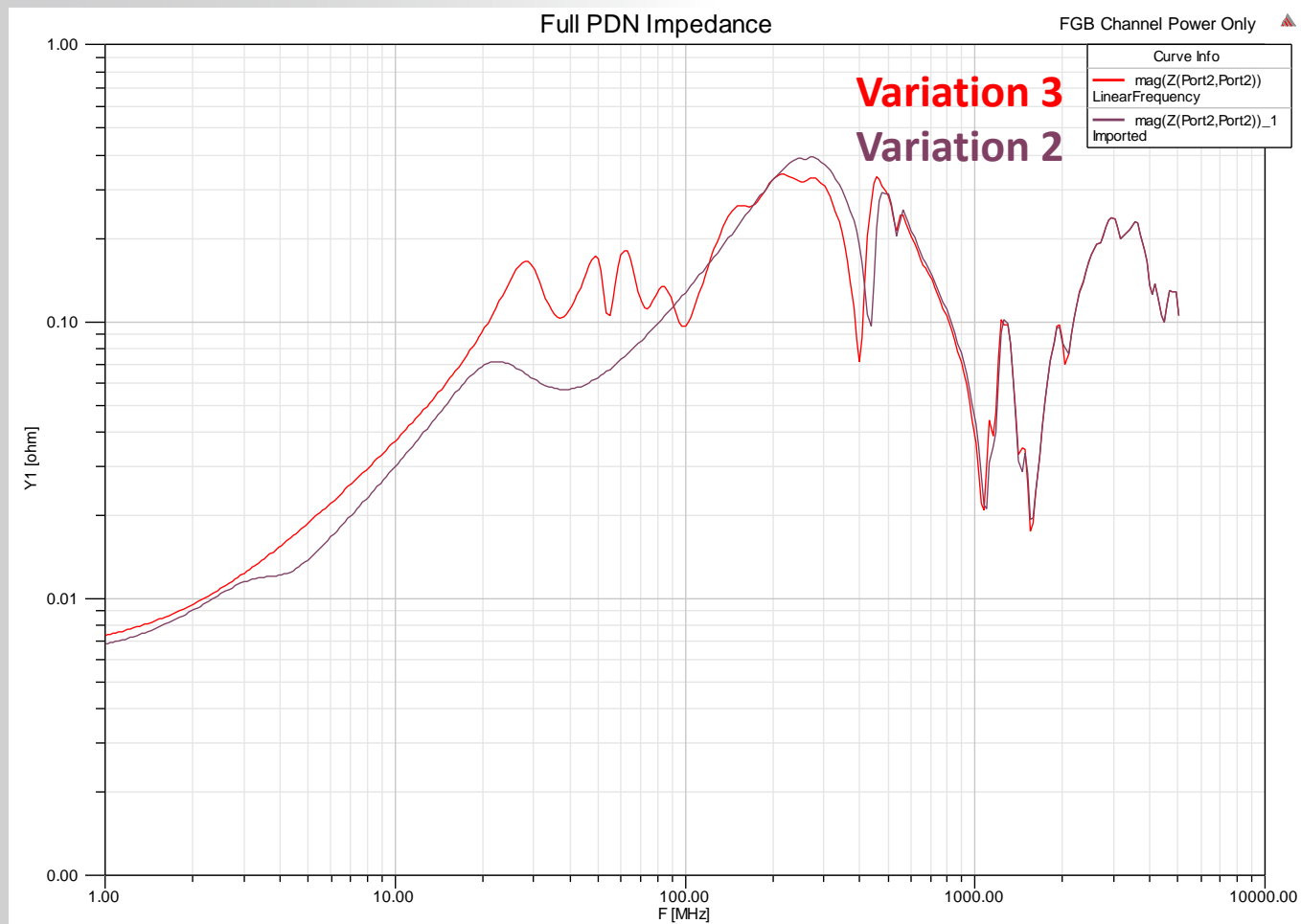

© 2011 ANSYS, Inc.   July 24, 2019

Variation 2: Added Capacitors

© 2011 ANSYS, Inc.   July 24, 2019

Variation 3: PI Advisor

Variation 3: PI Advisor

© 2011 ANSYS, Inc.   July 24, 2019

Variation 3: PI Advisor

© 2011 ANSYS, Inc.   July 24, 2019

Conclusion
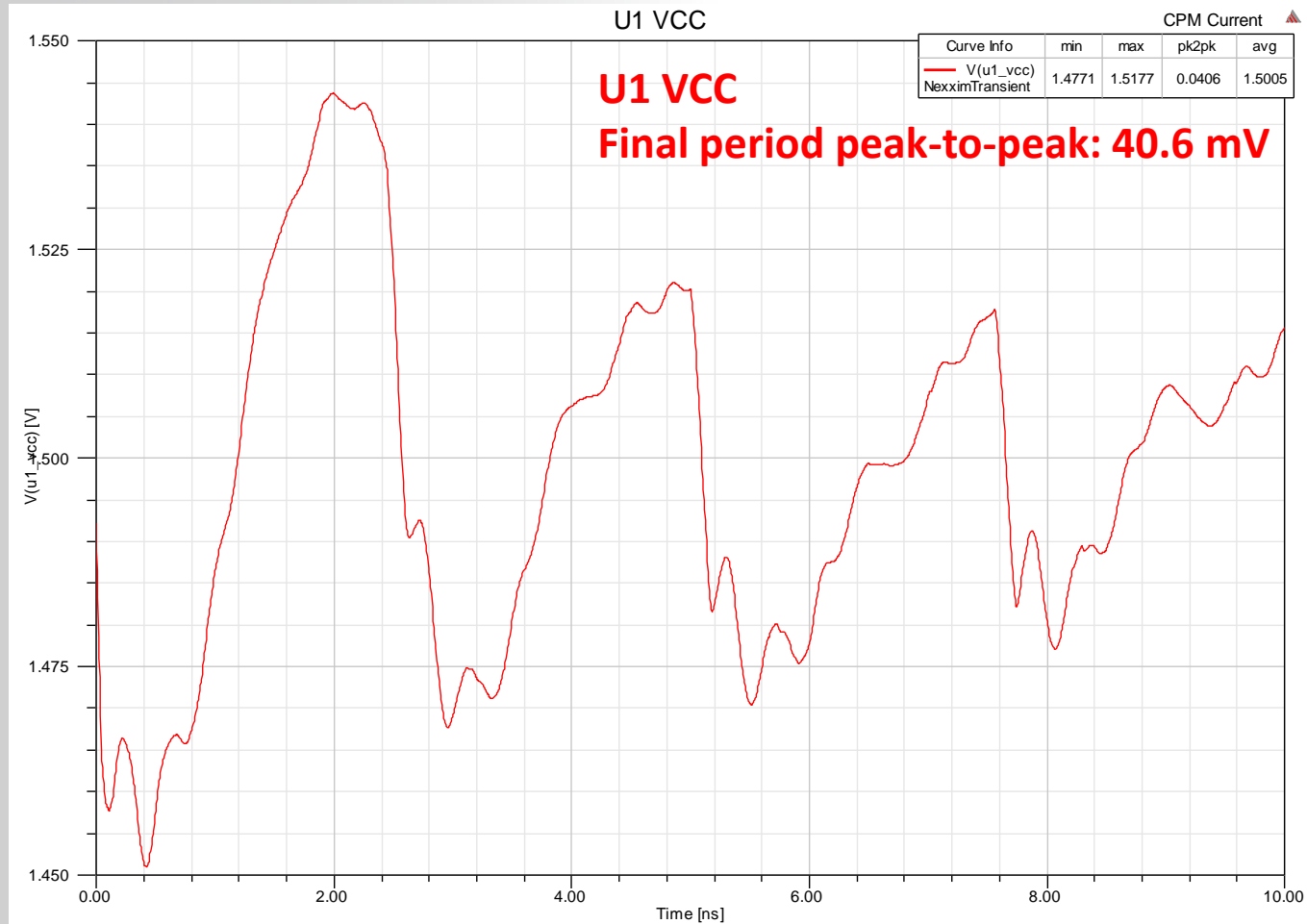
Power integrity simulation requires accurate package and chip PDN models to ensure correct designs.

The ANSYS chip-package-system technologies provide full coverage for PI simulation needs:

- **CPM: chip PDN and current draw**

- **SIwave and PSI: package PDN**

- **SIwave: board PDN**

- **Designer: frequency- and time-domain simulation for full PDN**

        July 24, 2019