

Chip-Aware Power Integrity

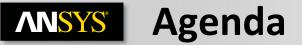
Fluid Dynamics

Structural Mechanics

Electromagnetics

Systems and Multiphysics

Greg Pitner Isaac Waldron



- Power integrity challenges and solution
- New PI features in R14.5
- Power integrity case study



Power Integrity Challenges and Solution

ANSYS Trends Requiring Chip Aware System Design

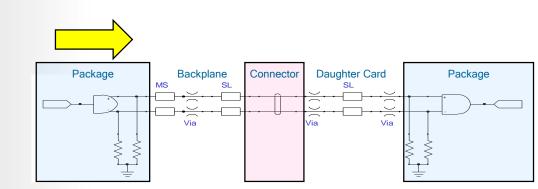
The die-to-die system is extremely complex:

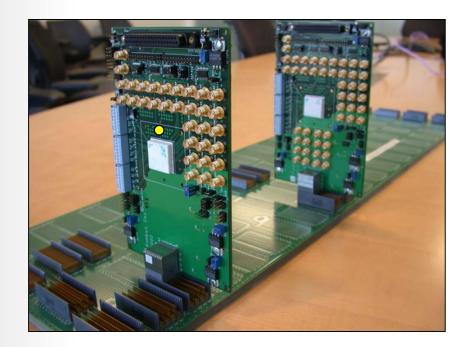
- Silicon driver/receiver
- 3D component interconnect
- Chip to package
- Package to daughter card
- Daughter card to backplane
- Power delivery network effects

Complex problems

- High risk
 - New unfamiliar phenomena?
- High cost of design errors

Solving them is requiring new strategies and simulation tools.





ANSYS What is a Power Distribution Network (PDN)?

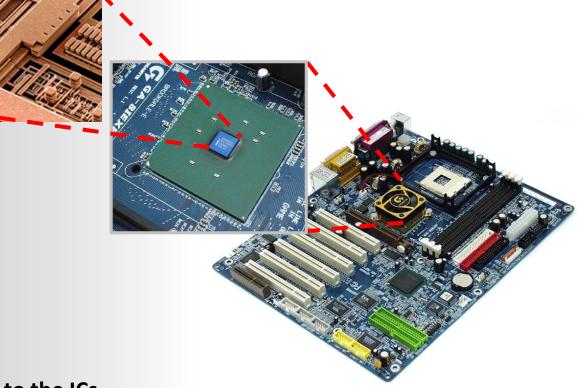
Complex multi-stage network supplying power to all devices in a system.

For typical products the PDN includes:

- Voltage regulator module (VRM)
- Board power/ground planes and decoupling capacitors
- Package power/ground planes and decoupling capacitors
- Chip power/ground structures and capacitance

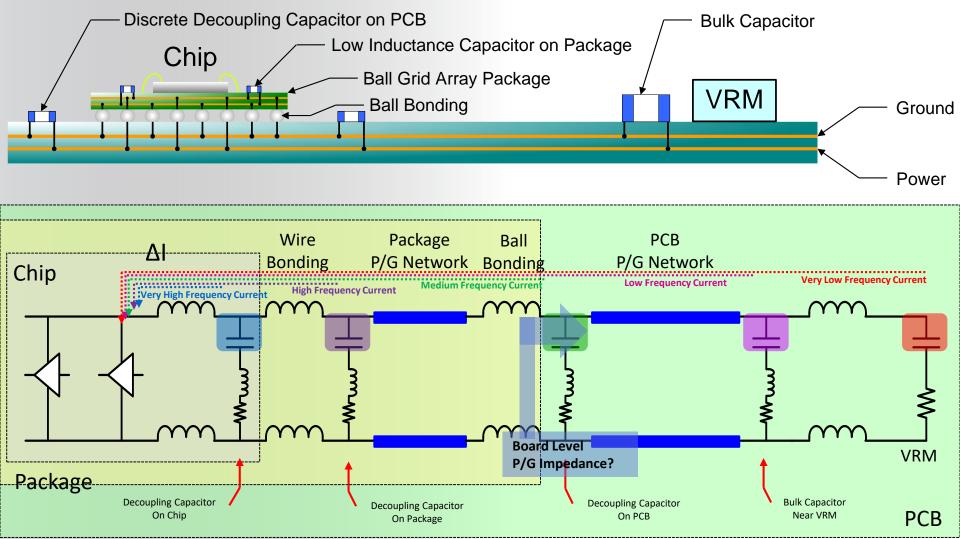
PDN Requirements:

- Must deliver clean power to the ICs
- Must provide low impedance, low noise reference path for signals
- Must not contribute excessive EMI



ANSYS Board Level Power Integrity?

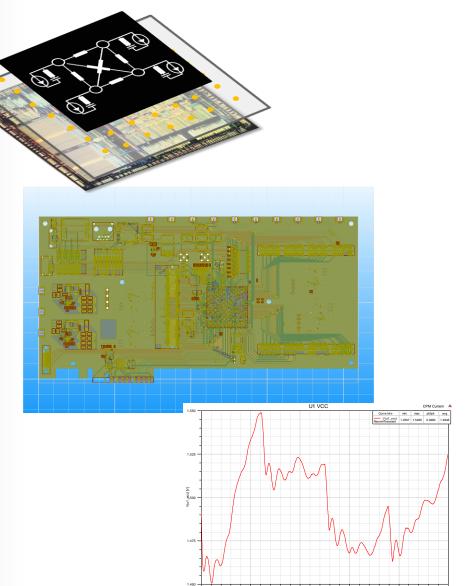
Full PDN



ANSYS ANSYS Chip-Aware PDN Solution

Redhawk generates a chip power model (CPM) including chip PDN parasitics and switching currents.

- PSI and SIwave provide robust extraction of IC packages and boards with broadband Sparameter models.
- PI Advisor optimizes decoupling capacitor selection to meet a target impedance.
- Designer SI simulates power noise in the time domain.

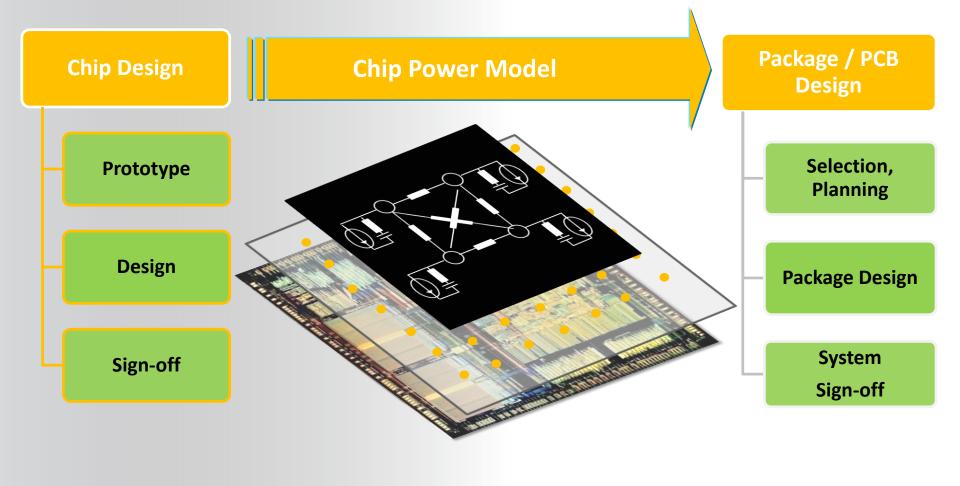




Chip Power Model (CPM)

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ANSYS CPS Convergence Using CPM



ANSYS What's in a CPM?

PCB + Package



Each C4 bump (power & ground) will be associated to its corresponding:

✓ Chip PDN RLC

Physical model of chip layout

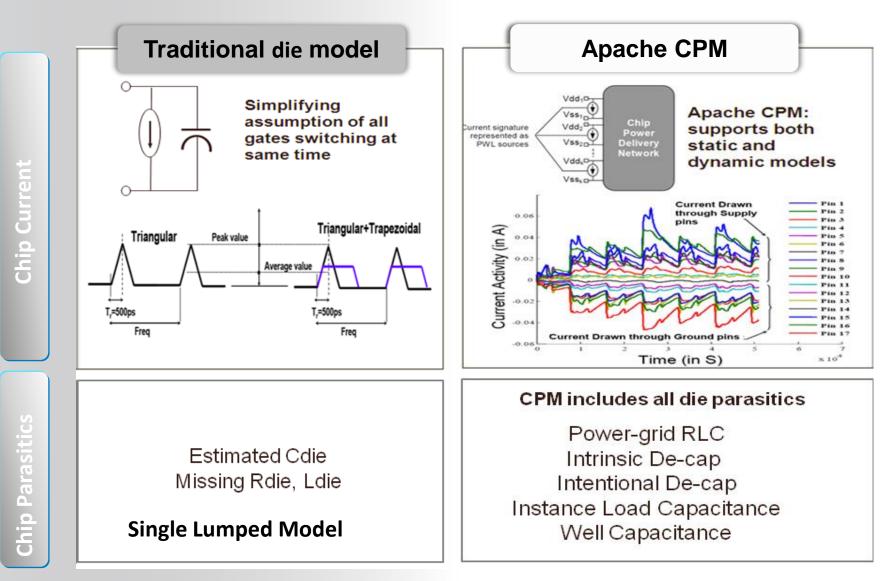
✓ Transistor/cell current /cap/ESR
Electrical model of chip layout

CPM is topological, physical and activity based

SUBCKT PowerModel p1 p2 * Apache RedHawk Chip Power Model [Accurate RC reduction] ********* Apache RedHawk Chip Power Model [Ver 1.00] Version: 10.2 Linux32e3 (Jan 20 00:31:13 2011) * Pad name DPOWER21 INCLUDE "PowerModel.sp.inc" DGROUND20 * Begin Chip Package Protocol ---> * No connec * die_area 0 0 4920.62 5000.36 CO 1 p1 p2 * Start Units Length um R_1_1 p1 n3 * End Units C_1_1 n3 p2 (4905.000000 3279.000000) (4880.000000 3219.000000) * DPOWER21 p1 = PAR 0 0 VDD R_2_1 p1 n4 p2 * DGROUND20 = PAR 0 0 VSS C_2_1 n4 p2 R_3_1 p1 n5 * End Chip Package Protocol <---</p> C_3_1 n5 p2 .subckt adsPowerModel p1 p2 R 4 1 p1 n6 C_4_1 n6 p2 Xpdn p1 p2 PowerModel ENDS Icursig1 p1 p2 pw1(+ 0.000000ps 0.589435 + 150.000000ps 0.854897 + 240.000000ps 0.867186 + 330.00000ps 0.827372 July 24, 2019 © 2011 ANSYS, Inc.

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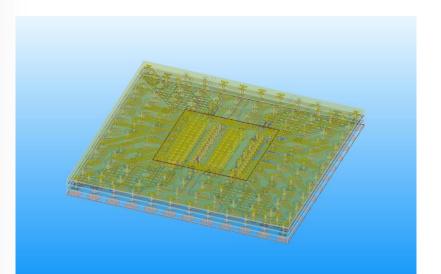




ANSYS Slwave CPM Integration

Slwave CPM integration includes the following:

- Import of die PDN for inclusion in frequency-domain extractions
- Automatic matching of die pin to CPM pin locations



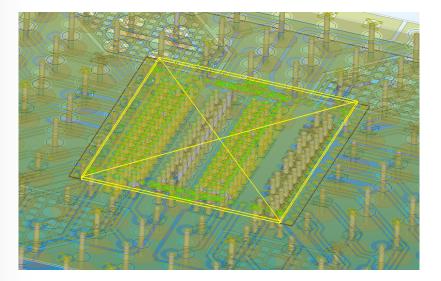


	ne: FCHIP			•	Reference Design	ator: FCHIP		
IC Die I	Information							
CPM F	File:					Browse		
Detet	tion in degrees (counter cloci	(mine), 0				Update		
Locati	ion of die center on package	e: (0,0)un	1			Update		
📰 Flip	p Die	Reset		Auto Connect	Manual Connect			
ickage i	Pins							
ndex	Pin Name	x	Y	Net	Connected D	ie Pin	Die Pin Index	
	A1	-1.91	1.91					
	A2	-1.69	1.91					
	A3	-1.46	1.91 1.91	_				
				FCHIP_A6				
	A6	-0.79						
	A6 A7	-0.79	1.91	FCHIP_A7				
e Pins	A7	-0.56	1.91	FCHIP_A7	Delete One Pair	Delete ALL Pa		ir Connect
e Pins	A7	-0.56	1.91	FCHIP_A7				
e Pins	A7	-0.56	1.91	FCHIP_A7	Delete One Pair Group Net			
e Pins	A7	-0.56	1.91	FCHIP_A7				
e Pins Index	A7 Pin Name	-0.56	1.91	FCHIP_A7				air Connect
e Pins ndex	A7 Pin Name	-0.56	1.91	Add One Pair Group Name III				

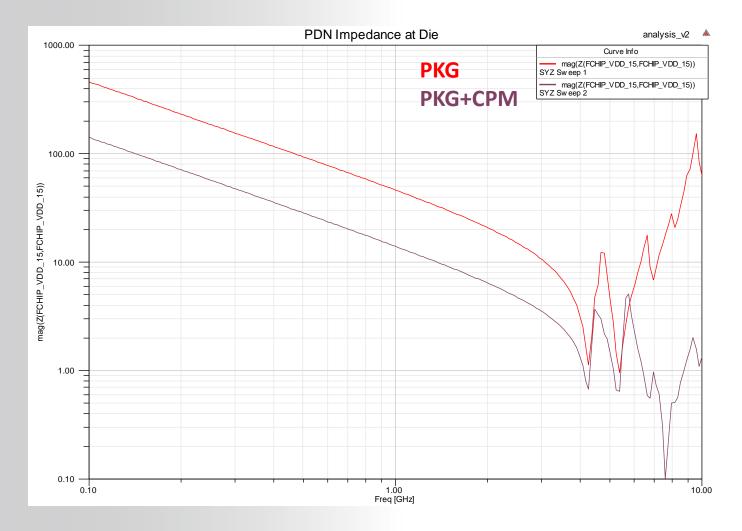
	ne: FCHIP			▼ F	Reference Designator:	FCHIP		•
IC Die	Information							
CPM I	File: C:\Users\iwaldron\Demo	s\SIwave\CPM	\cpm.s)	Bro	owse		
Rotat	tion in degrees (counter clockwi	ise): 0			U	Ipdate		
Locat	ion of die center on package:	(0.0000	00.00	00000)		Iodate		
Locut	ion of the center on publicager	(0.0000				puate		
V Fli	p Die	Reset		Auto Connect Mar	nual Connect			
ackage	Pins							
index	Pin Name	x	Y	Net	Connected Die Pir	n	Die Pin Index	*
1	A1	-1.91	1.91	FCHIP_A1				
2	A2	-1.69	1.91	FCHIP_A2				
3	A3	-1.46	1.91	FCHIP_A3				
ŧ	A6	-0.79	1.91	FCHIP_A6				
5	A7	-0.56	1.91	FCHIP_A7				
	40	0.11	1.01	VDD 1E				
e Pins				Add One Pair Del	lete One Pair De	elete ALL Pair	- Di- D-	ir Connect
	PL 41							
	Pin Name	SPICE Node		Group Name	Group Net	Ref. Group I		Package ^
1	bumpnode_150#a9	p3		VDD_15_FCHIP_VDD_15	Group Net			
1 2	bumpnode_150#a9 bumpnode_151#a10	p3 p3		VDD_15_FCHIP_VDD_15 VDD_15_FCHIP_VDD_15	Group Net			
1 2 3	bumpnode_150#a9 bumpnode_151#a10 bumpnode_158#b2	p3 p3 p4		VDD_15_FCHIP_VDD_15 VDD_15_FCHIP_VDD_15 VSS_FCHIP_VSS_2	Group Net			
1 2 3 4	bumpnode_150#a9 bumpnode_151#a10 bumpnode_158#b2 bumpnode_163#b7	p3 p3 p4 p3		VDD_15_FCHIP_VDD_15 VDD_15_FCHIP_VDD_15 VSS_FCHIP_VSS_2 VDD_15_FCHIP_VDD_15	Group Net			
1 2 3 4 5	bumpnode_150#a9 bumpnode_151#a10 bumpnode_158#b2 bumpnode_163#b7 bumpnode_164#b8	p3 p3 p4 p3 p3		VDD_15_FCHIP_VDD_15 VDD_15_FCHIP_VDD_15 VSS_FCHIP_VSS_2 VDD_15_FCHIP_VDD_15 VDD_15_FCHIP_VDD_15	Group Net			
1 2 3 4 5 5	bumpnode_150#a9 bumpnode_151#a10 bumpnode_158#b2 bumpnode_163#b7 bumpnode_164#b8 bumpnode_165#b9	p3 p3 p4 p3 p3 p3 p3		VDD_15_FCHIP_VDD_15 VDD_15_FCHIP_VDD_15 VSS_FCHIP_VSS_2 VDD_15_FCHIP_VDD_15 VDD_15_FCHIP_VDD_15 VDD_15_FCHIP_VDD_15	Group Net			
1 2 3 4 5 5 7	bumpnode_150#a9 bumpnode_151#a10 bumpnode_158#b2 bumpnode_163#b7 bumpnode_164#b8 bumpnode_165#b9 bumpnode_166#b10	p3 p3 p4 p3 p3 p3 p3 p3 p3		VDD_15_FCHIP_VDD_15 VDD_15_FCHIP_VDD_15 VSS_FCHIP_VSS_2 VDD_15_FCHIP_VDD_15 VDD_15_FCHIP_VDD_15 VDD_15_FCHIP_VDD_15 VDD_15_FCHIP_VDD_15	Group Net			
1 2 3 4 5 6 7 8	bumpnode_150 #a9 bumpnode_151#a10 bumpnode_158#b2 bumpnode_163#b7 bumpnode_164#b8 bumpnode_165#b9 bumpnode_166#b10 bumpnode_167#b11	p3 p3 p4 p3 p3 p3 p3 p3 p3 p3 p3		VDD_15_FCHIP_VDD_15 VDD_15_FCHIP_VDD_15 VSS_FCHIP_VSS_2 VDD_15_FCHIP_VDD_15 VDD_15_FCHIP_VDD_15 VDD_15_FCHIP_VDD_15 VDD_15_FCHIP_VDD_15 VDD_15_FCHIP_VDD_15	Group Net			
1 2 3 4 5 6 7 8 9	bumpnode_150#a9 bumpnode_151#a10 bumpnode_158#b2 bumpnode_164#b8 bumpnode_164#b8 bumpnode_165#b9 bumpnode_165#b10 bumpnode_167#b111 bumpnode_168#b12	p3 p3 p4 p3 p3 p3 p3 p3 p3 p3 p3 p3		VDD_15_FCHIP_VDD_15 VDD_15_FCHIP_VDD_15 VSS_FCHIP_VSS_2 VDD_15_FCHIP_VDD_15 VDD_15_FCHIP_VDD_15 VDD_15_FCHIP_VDD_15 VDD_15_FCHIP_VDD_15 VDD_15_FCHIP_VDD_15	Group Net			
Index 1 2 3 4 5 5 6 7 8 9 9	bumpnode_150 #a9 bumpnode_151#a10 bumpnode_158#b2 bumpnode_163#b7 bumpnode_164#b8 bumpnode_165#b9 bumpnode_166#b10 bumpnode_167#b11	p3 p3 p4 p3 p3 p3 p3 p3 p3 p3 p3		VDD_15_FCHIP_VDD_15 VDD_15_FCHIP_VDD_15 VSS_FCHIP_VSS_2 VDD_15_FCHIP_VDD_15 VDD_15_FCHIP_VDD_15 VDD_15_FCHIP_VDD_15 VDD_15_FCHIP_VDD_15 VDD_15_FCHIP_VDD_15	Group Net			
1 2 3 4 5 6 7 8 9	bumpnode_150#a9 bumpnode_151#a10 bumpnode_158#b2 bumpnode_163#b7 bumpnode_164#b8 bumpnode_165#b9 bumpnode_66#b10 bumpnode_167#b11 bumpnode_168#b12	p3 p3 p4 p3 p3 p3 p3 p3 p3 p3 p3 p3		VDD_15_FCHIP_VDD_15 VDD_15_FCHIP_VDD_15 VSS_FCHIP_VSS_2 VDD_15_FCHIP_VDD_15 VDD_15_FCHIP_VDD_15 VDD_15_FCHIP_VDD_15 VDD_15_FCHIP_VDD_15 VDD_15_FCHIP_VDD_15 VDD_15_FCHIP_VDD_15	Group Net			
1 2 3 4 5 6 6 7 8 9 0 0 9 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	bumpnode_150#a9 bumpnode_151#a10 bumpnode_158#b2 bumpnode_163#b7 bumpnode_164#b8 bumpnode_165#b9 bumpnode_165#b10 bumpnode_165#b11 bumpnode_168#b12 bumpnode_168#b12	p3 p3 p4 p3 p3 p3 p3 p3 p3 p3 p3 p3	on sam	VDD_15_FCHIP_VDD_15 VDD_15_FCHIP_VDD_15 VSS_FCHIP_VSD_2 VDD_15_FCHIP_VDD_15 VDD_15_FCHIP_VDD_15 VDD_15_FCHIP_VDD_15 VDD_15_FCHIP_VDD_15 VDD_15_FCHIP_VDD_15 VDD_15_FCHIP_VDD_15 VDD_15_FCHIP_VDD_15	Group Net			
1 2 3 4 5 5 6 7 8 9 9 0 0 pera	bumpnode_150#a9 bumpnode_151#a10 bumpnode_158#b2 bumpnode_163#b7 bumpnode_164#b8 bumpnode_165#b9 bumpnode_165#b10 bumpnode_165#b11 bumpnode_168#b12 bumpnode_168#b12	p3 p3 p4 p3 p3 p3 p3 p3 p3 p3		VDD_15_FCHIP_VDD_15 VDD_15_FCHIP_VDD_15 VSS_FCHIP_VSD_2 VDD_15_FCHIP_VDD_15 VDD_15_FCHIP_VDD_15 VDD_15_FCHIP_VDD_15 VDD_15_FCHIP_VDD_15 VDD_15_FCHIP_VDD_15 VDD_15_FCHIP_VDD_15 VDD_15_FCHIP_VDD_15	Group Net 2 2 2 2 2 2 2 2 2 2 2 2 2			



art Nar	me: FCHIP		▼ Re	eference Designat	or: FCHIP	
IC Die	Information			-		
		1			Pins ma	pped: 106
CPM	File: C:\Users\iwaldron\D	emos (SIwave (CPM)	(cpm.sp			mapped: 0
Rota	ition in degrees (counter clo	ckwise): 0			Update	
Local	tion of die center on packag	· · · · · · · · · · · · · · · · · · ·	00, 0.000000)		Update	
LUCU	aon of the center of packag	(0.0000	00, 0.000000)		opdate	
F	lip Die	Reset	Auto Connect Manu	ual Connect		
ockage	e Pins					
Index	Pin Name	x	Y Net	Connected Die	Pin Die Pin	Index
1	A1	-1.91	1.91 FCHIP_A1			
2	A2	-1.69	1.91 FCHIP_A2			
8	A3	-1.46	1.91 FCHIP_A3			
ŧ.	A6	-0.79	1.91 FCHIP_A6			
i	A7	-0.56	1.91 FCHIP_A7			
e	A0	0.11	1.01 UDD 1E	humphada 15	n#-n 1	
e Pins		0.11			Delete ALL Pairs	Pin Pair Connect
		SPICE Node				Pin Pair Connect Package
e Pins index			Add One Pair Dele	te One Pair	Delete ALL Pairs	
e Pins index	Pin Name	SPICE Node	Add One Pair Dele	te One Pair Group Net 2 VDD_15	Delete ALL Pairs Ref. Group Name	Package
e Pins ndex	Pin Name bumpnode_150#a9	SPICE Node p3	Add One Pair Dele Group Name VDD_15_FCHIP_VDD_15_	te One Pair Group Net 2 VDD_15	Delete ALL Pairs Ref. Group Name VSS_FCHIP_VSS_2	Package A9
e Pins index	Pin Name bumpnode_150#a9 bumpnode_151#a10	SPICE Node p3 p3	Add One Pair Dele Group Name VDD_15_FCHIP_VDD_15_ VDD_15_FCHIP_VDD_15_	te One Pair Group Net 2 VDD_15 2 VDD_15 VSS	Delete ALL Pairs Ref. Group Name VSS_FCHIP_VSS_2	Package A9 A10
e Pins ndex	Pin Name bumpnode_150#a9 bumpnode_151#a10 bumpnode_158#b2	SPICE Node p3 p3 p4	Add One Pair Delety Group Name VDD_15_FCHIP_VDD_15_ VDD_15_FCHIP_VDD_15_ VDD_15_FCHIP_VD2_15_ VSS_FCHIP_VSS_2 VSS_FCHIP_VSS_2	te One Pair Group Net 2 VDD_15 2 VDD_15 VSS 2 VDD_15	Delete ALL Pairs Ref. Group Name VSS_FCHIP_VSS_2 VSS_FCHIP_VSS_2	Package A9 A10 B2
e Pins ndex	Pin Name bumpnode_150#a9 bumpnode_151#a10 bumpnode_158#b2 bumpnode_163#b7	SPICE Node p3 p3 p4 p3	Add One Pair Delety Group Name VDD_15_FCHIP_VDD_15_ VDD_15_FCHIP_VDD_15_ VSS_FCHIP_VSS_2 VDD_15_FCHIP_VDD_15_FCHIP_VDD_15_ VDD_15_FCHIP_VDD_15_	Group Net 2 VDD_15 2 VDD_15 VSS 2 VDD_15 2 VDD_15 2 VDD_15 2 VDD_15	Delete ALL Pairs Ref. Group Name VSS_FCHIP_VSS_2 VSS_FCHIP_VSS_2 VSS_FCHIP_VSS_2	Package A9 A10 B2 B7
e Pins index	Pin Name bumpnode_150#a9 bumpnode_151#a10 bumpnode_158#b2 bumpnode_163#b7 bumpnode_164#b8	SPICE Node p3 p3 p4 p3 p3 p3	Add One Pair Delety Group Name VDD_15_FCHIP_VDD_15_ VDD_15_FCHIP_VDD_15_ VSS_FCHIP_VSS_2 VDD_15_FCHIP_VDD_15_ VDD_15_FCHIP_VDD_15_ VDD_15_FCHIP_VDD_15_ VDD_15_FCHIP_VDD_15_	te One Pair Group Net 2 VDD_15	Delete ALL Pairs Ref. Group Name VSS_FCHIP_VSS_2 VSS_FCHIP_VSS_2 VSS_FCHIP_VSS_2 VSS_FCHIP_VSS_2 VSS_FCHIP_VSS_2	Package A9 A10 B2 B7 B8
e Pins ndex	Pin Name bumpnode_150 #a9 bumpnode_151 #a10 bumpnode_158 #b2 bumpnode_163 #b7 bumpnode_164 #b8 bumpnode_165 #b9	SPICE Node p3 p3 p4 p3 p3 p3 p3	Add One Pair Delety Group Name VDD_15_FCHIP_VDD_15_ VDD_15_FCHIP_VDD_15_ VSS_FCHIP_VSS_2 VDD_15_FCHIP_VDD_15_ VDD_15_FCHIP_VDD_15_ VDD_15_FCHIP_VDD_15_ VDD_15_FCHIP_VDD_15_	te One Pair Group Net 2 VDD_15	Delete ALL Pairs Ref. Group Name VSS_FCHIP_VSS_2 VSS_FCHIP_V	Package A9 A10 B2 B7 B8 B9
e Pins ndex	Pin Name bumpnode_150##9 bumpnode_151##10 bumpnode_163#b7 bumpnode_163#b7 bumpnode_163#b9 bumpnode_165#b10 bumpnode_165#b12	SPICE Node p3 p3 p4 p3 p3 p3 p3 p3 p3 p3	Add One Pair Delety Group Name VDD_15_FCHIP_VDD_15_ VDD_15_FCHIP_VDD_15_ VSS_FCHIP_VSS_2 VDD_15_FCHIP_VDD_15_ VDD_15_FCHIP_VDD_15_ VDD_15_FCHIP_VDD_15_ VDD_15_FCHIP_VDD_15_ VDD_15_FCHIP_VDD_15_ VDD_15_FCHIP_VDD_15_ VDD_15_FCHIP_VDD_15_ VDD_15_FCHIP_VDD_15_ VDD_15_FCHIP_VDD_15_ VDD_15_FCHIP_VDD_15_	te One Pair Group Net 2 VDD_15 2 VDD_15	Delete ALL Pairs Ref. Group Name VSS_FCHIP_VSS_2 VSS_FCHIP_V	A9 A10 B2 B7 B8 B9 B10 B11 B12
e Pins ndex	Pin Name bumpnode_150#a9 bumpnode_151#a10 bumpnode_153#b2 bumpnode_163#b7 bumpnode_165#b9 bumpnode_165#b10 bumpnode_165#b11	SPICE Node p3 p4 p3 p3 p3 p3 p3 p3 p3 p3 p3 p3	Add One Pair Delete Group Name VDD_15_FCHIP_VDD_15_ VDD_15_FCHIP_VDD_15_ VDS_FCHIP_VSD_215_ VDD_15_FCHIP_VDD_15_ VDD_15_FCHIP_VDD_15_ VDD_15_FCHIP_VDD_15_ VDD_15_FCHIP_VDD_15_ VDD_15_FCHIP_VDD_15_ VDD_15_FCHIP_VDD_15_ VDD_15_FCHIP_VDD_15_ VDD_15_FCHIP_VDD_15_	Group Net 2 VDD_15	Delete ALL Pairs Ref. Group Name VSS_FCHIP_VSS_2 VSS_FCHIP_VSS_2 VSS_FCHIP_VSS_2 VSS_FCHIP_VSS_2 VSS_FCHIP_VSS_2 VSS_FCHIP_VSS_2 VSS_FCHIP_VSS_2 VSS_FCHIP_VSS_2	Package A9 A10 B2 B7 B8 B9 B10 B11 B12 B12
e Pins index	Pin Name bumpnode_150##9 bumpnode_151##10 bumpnode_163#b7 bumpnode_163#b7 bumpnode_163#b9 bumpnode_165#b10 bumpnode_165#b12	SPICE Node p3 p4 p3 p3 p3 p3 p3 p3 p3 p3 p3 p3	Add One Pair Delety Group Name VDD_15_FCHIP_VDD_15_ VDD_15_FCHIP_VDD_15_ VSS_FCHIP_VSS_2 VDD_15_FCHIP_VDD_15_ VDD_15_FCHIP_VDD_15_ VDD_15_FCHIP_VDD_15_ VDD_15_FCHIP_VDD_15_ VDD_15_FCHIP_VDD_15_ VDD_15_FCHIP_VDD_15_ VDD_15_FCHIP_VDD_15_ VDD_15_FCHIP_VDD_15_ VDD_15_FCHIP_VDD_15_ VDD_15_FCHIP_VDD_15_	te One Pair Group Net 2 VDD_15 2 VDD_15	Delete ALL Pairs Ref. Group Name VSS_FCHIP_VSS_2 VSS_FCHIP_VSS_2 VSS_FCHIP_VSS_2 VSS_FCHIP_VSS_2 VSS_FCHIP_VSS_2 VSS_FCHIP_VSS_2 VSS_FCHIP_VSS_2 VSS_FCHIP_VSS_2	Package A9 A10 B2 B7 B8 B9 B10 B11 B12
e Pins index 1 2 3 4 4 5 5 5 7 3 9	Pin Name bumpnode_150##9 bumpnode_151##10 bumpnode_163#b7 bumpnode_163#b7 bumpnode_163#b9 bumpnode_165#b10 bumpnode_165#b12	SPICE Node p3 p4 p3 p3 p3 p3 p3 p3 p3 p3 p3 p3	Add One Pair Delete Group Name VDD_15_FCHIP_VDD_15_ VDD_15_FCHIP_VDD_15_ VDS_FCHIP_VSD_215_ VDD_15_FCHIP_VDD_15_ VDD_15_FCHIP_VDD_15_ VDD_15_FCHIP_VDD_15_ VDD_15_FCHIP_VDD_15_ VDD_15_FCHIP_VDD_15_ VDD_15_FCHIP_VDD_15_ VDD_15_FCHIP_VDD_15_ VDD_15_FCHIP_VDD_15_	te One Pair Group Net 2 VDD_15 2 VDD_15	Delete ALL Pairs Ref. Group Name VSS_FCHIP_VSS_2 VSS_FCHIP_VSS_2 VSS_FCHIP_VSS_2 VSS_FCHIP_VSS_2 VSS_FCHIP_VSS_2 VSS_FCHIP_VSS_2 VSS_FCHIP_VSS_2 VSS_FCHIP_VSS_2	Package A9 A10 B2 B7 B8 B9 B10 B11 B12 B17
e Pins index 1 2 3 4 5 5 5 7 8 9 0 0per	Pin Name bumpnode_150#89 bumpnode_151#810 bumpnode_153#b2 bumpnode_163#b7 bumpnode_165#b9 bumpnode_165#b10 bumpnode_165#b11 bumpnode_163#b12	SPICE Node p3 p4 p3 p3 p3 p3 p3 p3 p3 p3 p3 p3	Add One Pair Delete Group Name VDD_15_FCHIP_VDD_15_ VDD_15_FCHIP_VDD_15_ VDD_15_FCHIP_VDD_15_ VDD_15_FCHIP_VDD_15_ VDD_15_FCHIP_VDD_15_ VDD_15_FCHIP_VDD_15_ VDD_15_FCHIP_VDD_15_ VDD_15_FCHIP_VDD_15_ VDD_15_FCHIP_VDD_15_ VDD_15_FCHIP_VDD_15_ VDD_15_FCHIP_VDD_15_ VDD_15_FCHIP_VDD_15_ VDD_15_FCHIP_VDD_15_	te One Pair Group Net 2 VDD_15 2 VDD_15	Delete ALL Pairs Ref. Group Name VSS_FCHIP_VSS_2 VSS_FCHIP_VSS_2 VSS_FCHIP_VSS_2 VSS_FCHIP_VSS_2 VSS_FCHIP_VSS_2 VSS_FCHIP_VSS_2 VSS_FCHIP_VSS_2 VSS_FCHIP_VSS_2	Package A9 A10 B2 B7 B8 B9 B10 B11 B12 B17



ANSYS CPM Impedance Effect

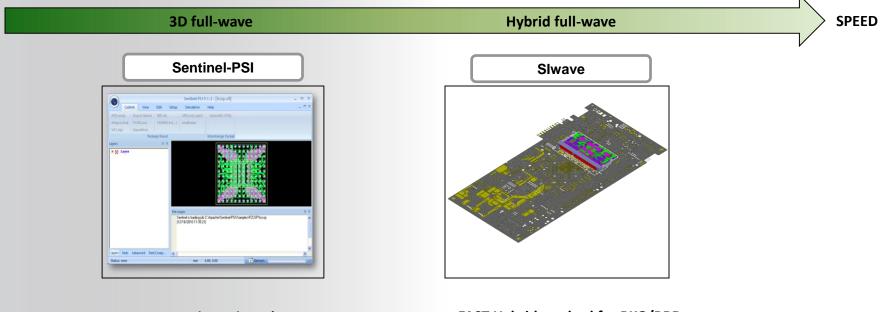




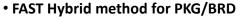
Sentinel PSI

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ANSYS ANSYS Package/Board Solvers



- Fast FEM using prism elements
- Tailored for PI package analysis



• Handles many, but not all 3D effects

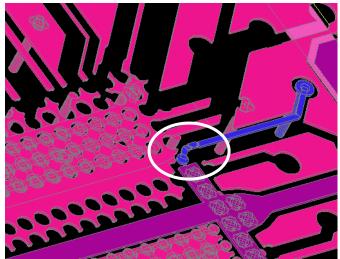
Trade-off speed for 3D accuracy



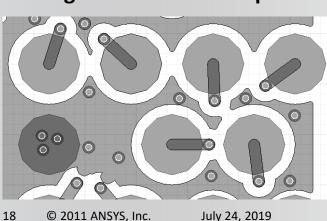
ANSYS Sentinel PSI Strengths

Package/PCB structures Containing

- **Highly perforated metal planes**
 - Swiss Cheese PWR/GND planes
 - Hatched PWR/GND planes
- **Two layer PCBs without reference layers**
- Transmission lines over non-ideal ground
- Ports with unreferenced terminals
- Visualization of PWR/GND AC currents
- Vias with large anti-pads



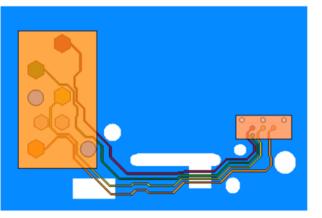
Port With Unreferenced Terminal



Large continuous anti-pads



Typical Hatched Plane



Lines over non-ideal ground cutouts



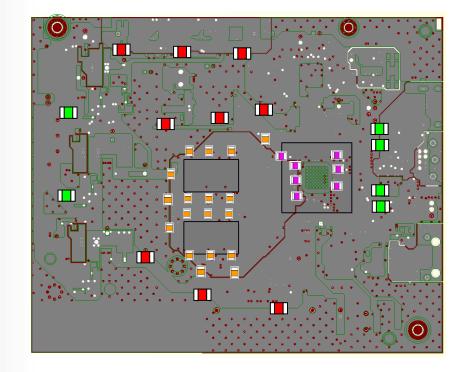
PI Advisor is an addon for Siwave that automatically optimizes capacitor selection to meet a target impedance:

Inputs:

- Capacitor locations
- Candidate capacitors

Outputs:

- Capacitor schemes that indicate which candidate, if any, to populate at each location.
- Impedance versus target for each scheme.

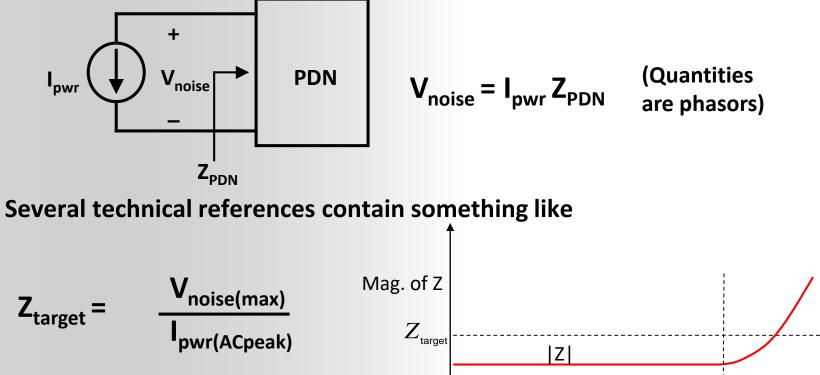




Target Impedance



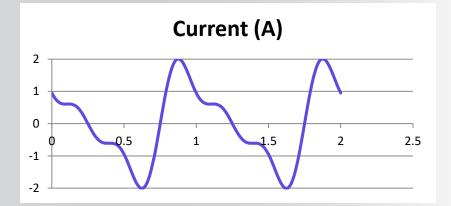
- Designing for power integrity often involves a target impedance
 - Maximum allowable impedance magnitude over frequency which will result in acceptable voltage noise



• An example can illustrate the complexities with this approach...

ANSYS A Simple Target Impedance Example

• Suppose we have a power current with the periodic AC component shown below (peak amplitude of 2A):



$$I(t) = |I_1| \cos(2\pi t + \theta_{I1}) + |I_2| \cos(4\pi t + \theta_{I2})$$

 $+|I_3|\cos(6\pi t+\theta_{I3})$

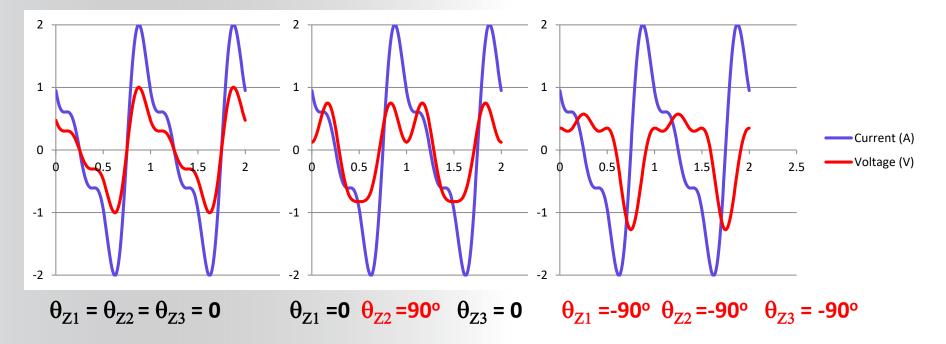
- Suppose we have a maximum allowable voltage amplitude of 1V
- The simple approach suggests a max Z_{PDN} of 0.5 Ω over the frequency components contained in the current will satisfy the noise requirement

$$V_f(t) = |I_f| \cdot |Z_f| \cos(2\pi f t + \theta_{If} + \theta_{Zf})$$

But our impedance tolerance does not specify phase

ANSYS Effects of Different Impedance Phases

• Assume our PDN impedance just satisfies the requirement at each frequency: $|Z_1| = |Z_2| = |Z_3| = 0.5\Omega$, but vary the impedance phase assumptions



Simple approaches to calculating target impedance can provide a useful guide, but results should be verified with time-domain simulation

ANSYS Target Impedance Notes

Reliance on a purely resistive target impedance may not bound the resulting time-domain voltage waveform to the desired amplitude.

Target impedance calculations should take into account the impedance phase as well as magnitude, but the current state-of-the-art does not.

More to come from ANSYS on this topic...



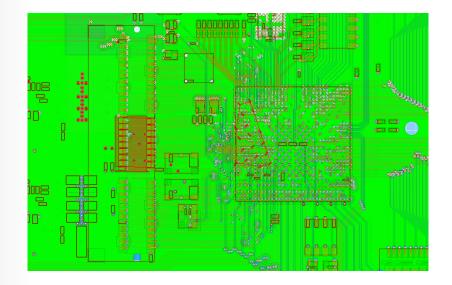
Power Integrity Case Study

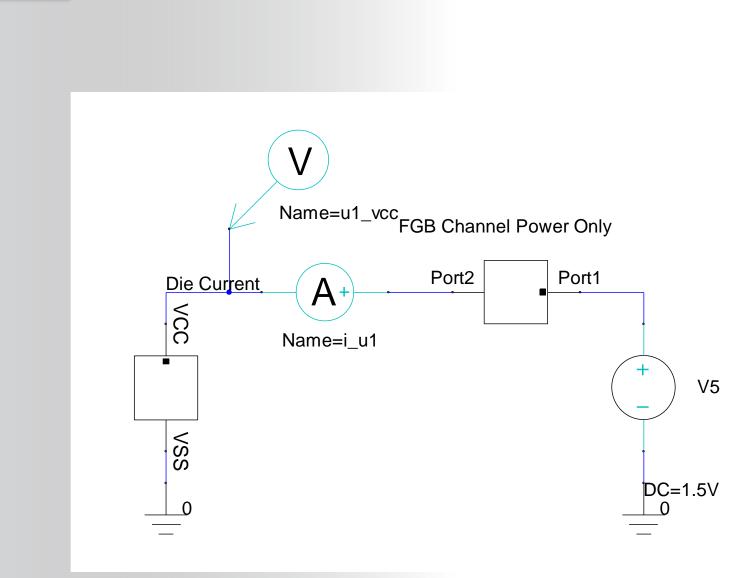
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- 1.5V power supply for FPGA on board.
- Chip included as Apache CPM.
- Package included as static Sparameters.
- **Board extracted with Slwave 7.**
- Simulation includes:
- GND
- VCC_1V5

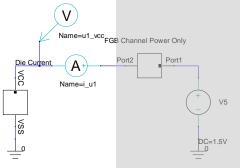
System excited by CPM currents.

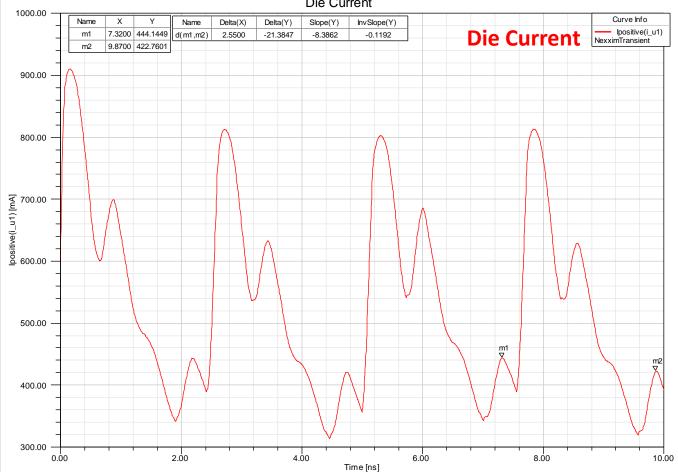




ANSYS Time Domain Circuit

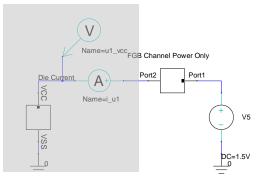


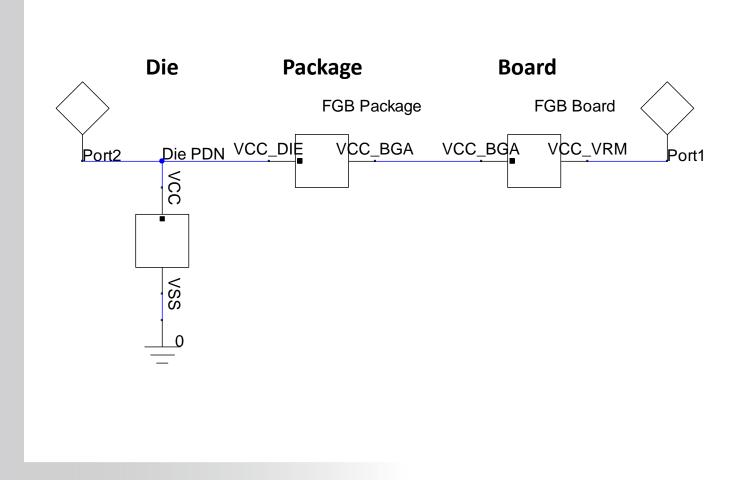




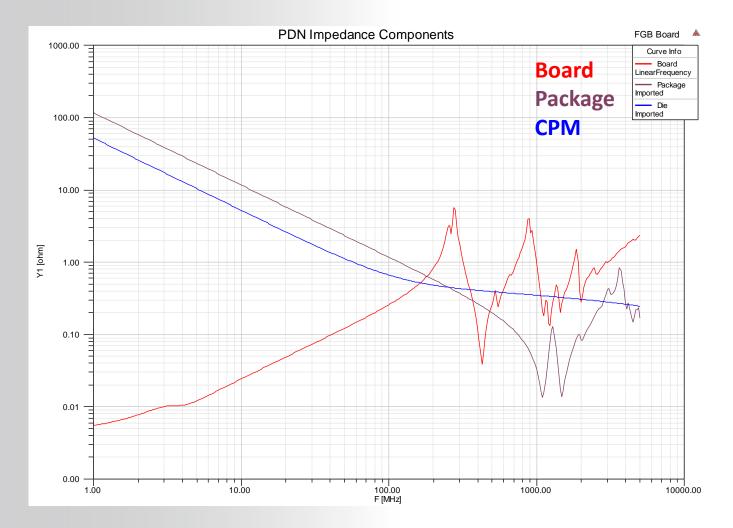
Die Current



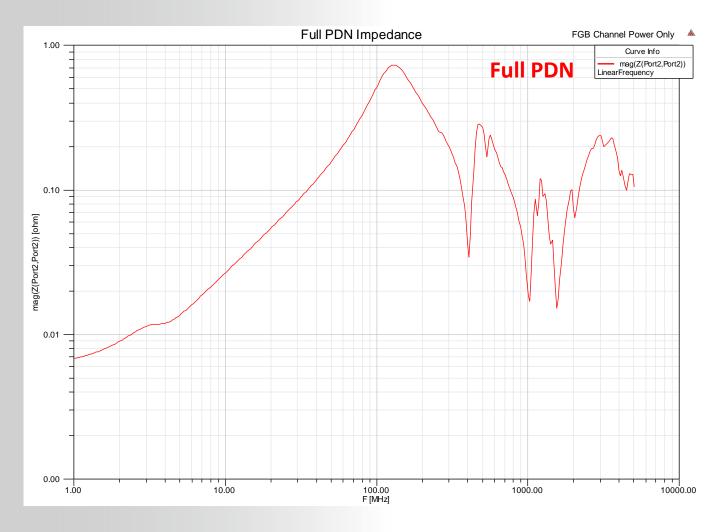


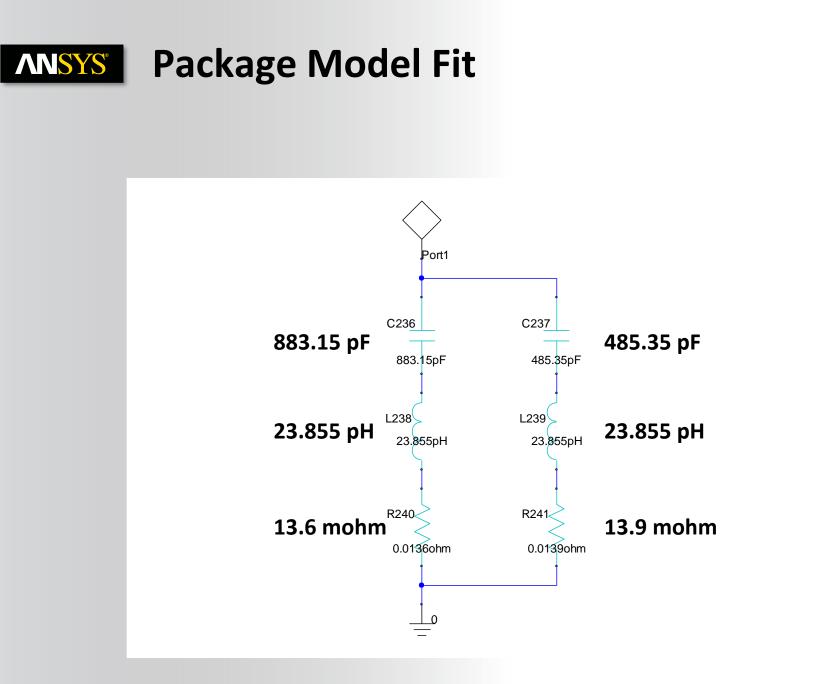


ANSYS PDN Impedance Components



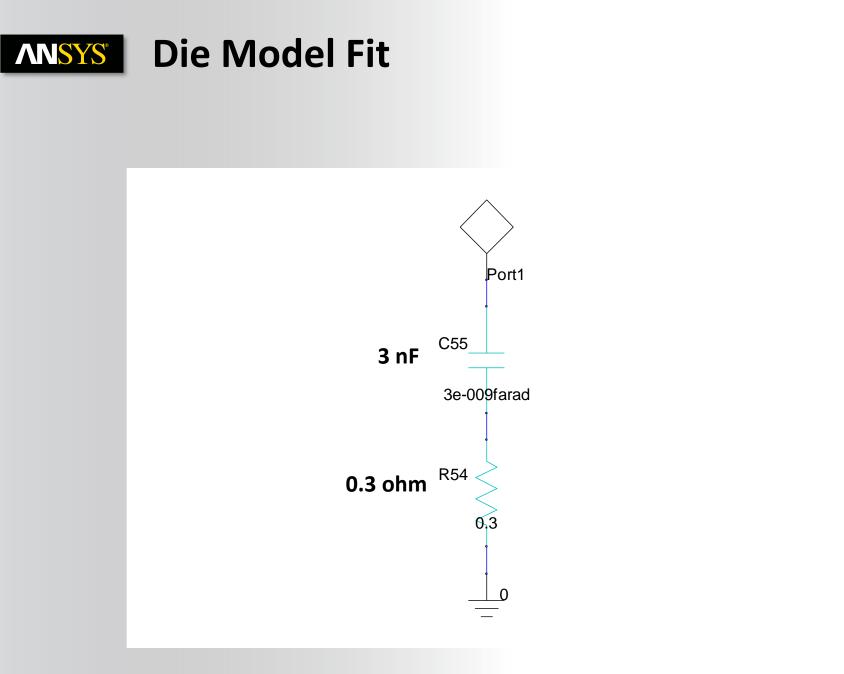
ANSYS Full PDN Impedance

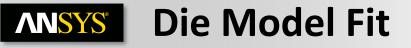


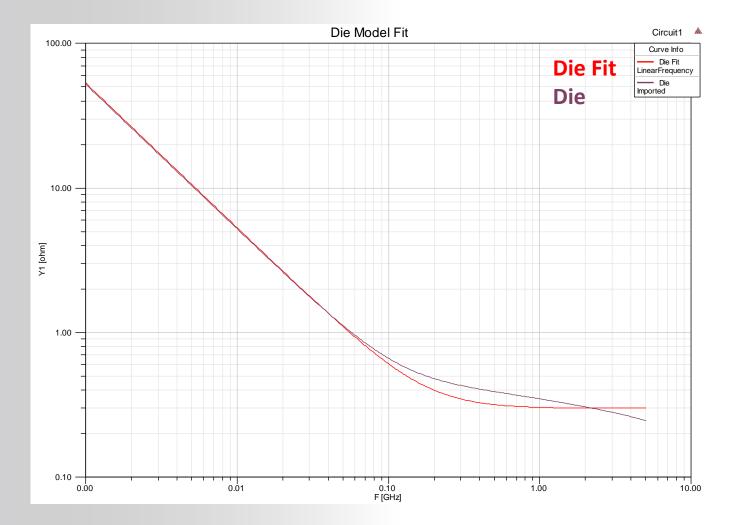


ANSYS Package Model Fit

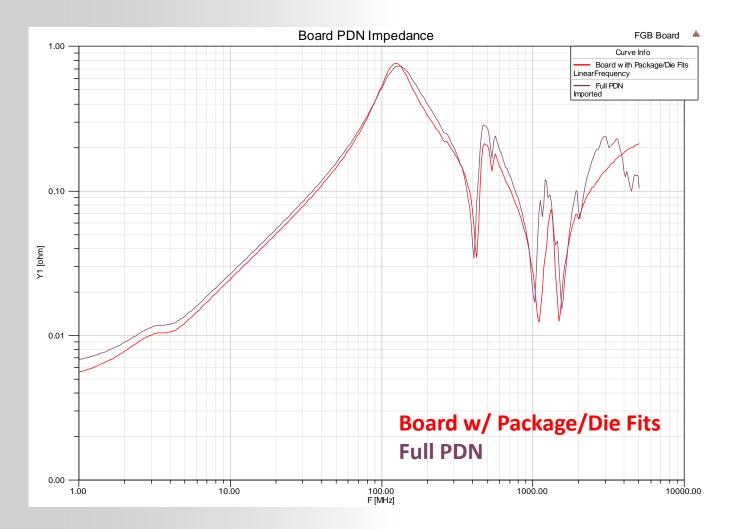








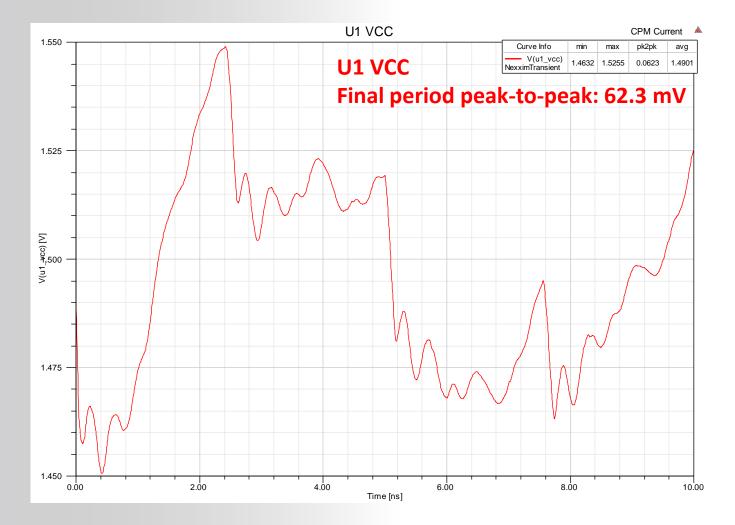
ANSYS Board with Package/Die Fits



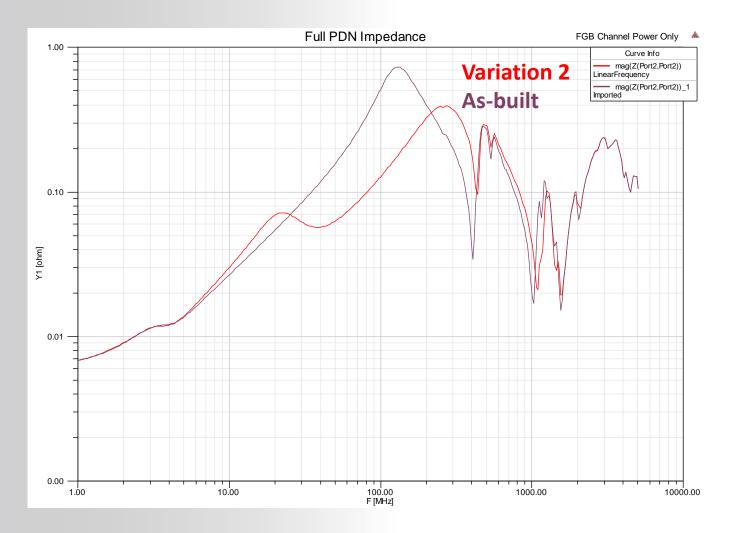
ANSYS Board Variations Analyzed

- 1. As initially designed.
 - Eight 100 uF bulk capacitors at VRM output, two 10 uF capacitors, and two 1 uF capacitors.
- 2. With added high-frequency capacitors.
 - 12 0.01 uF capacitors placed on bottom layer below FPGA
- 3. With PI Advisor-optimized capacitor solution.
 - Target impedance: 0.3 ohms up to 1 GHz
 - Package RLC fit and die RC fit included at board FPGA footprint

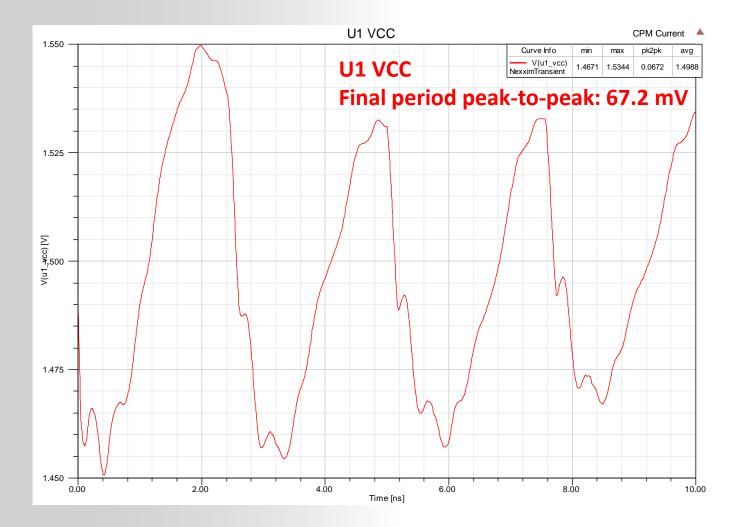
ANSYS Variation 1: As-Designed



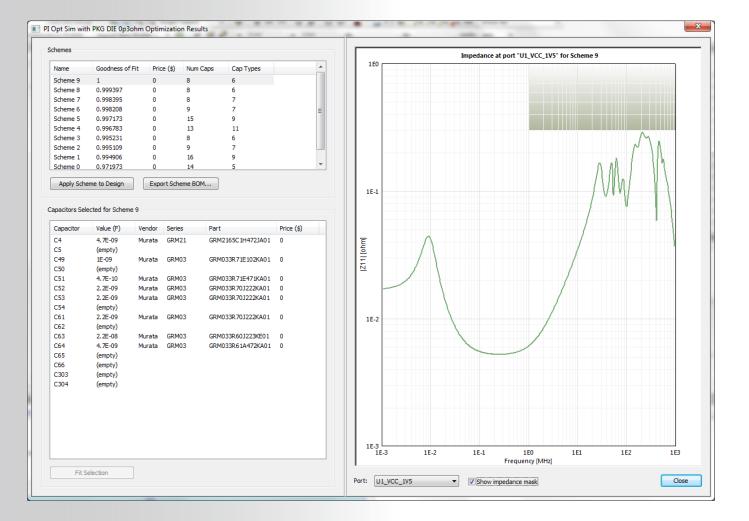
ANSYS Variation 2: Added Capacitors



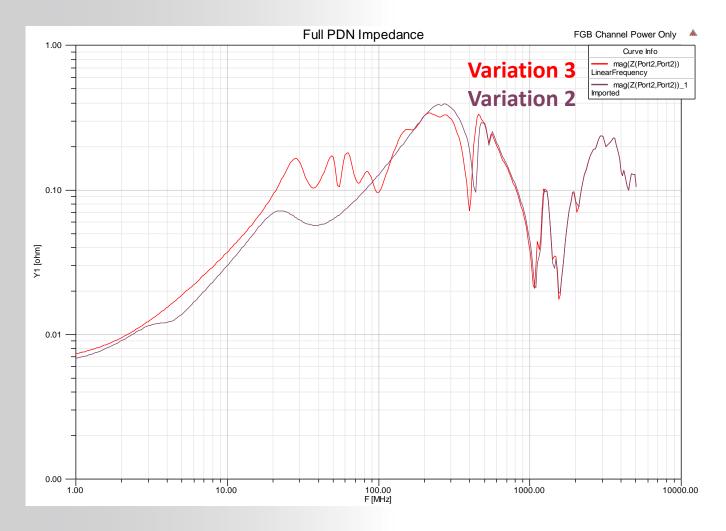
ANSYS Variation 2: Added Capacitors



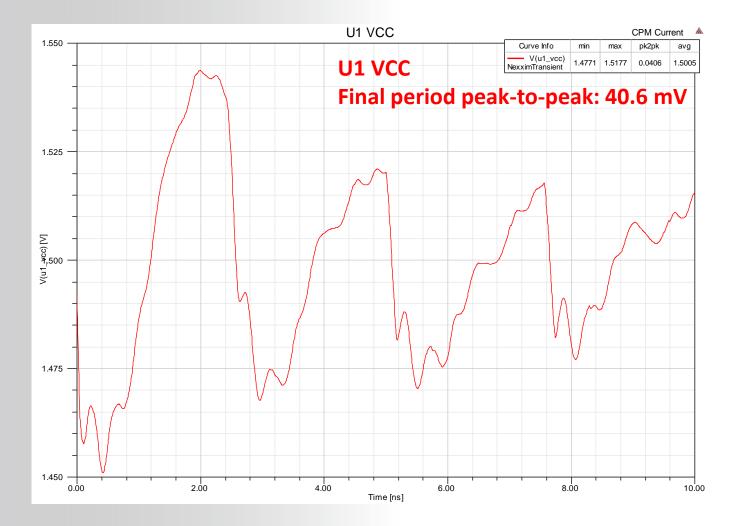
ANSYS Variation 3: PI Advisor



ANSYS Variation 3: PI Advisor



ANSYS Variation 3: PI Advisor





Power integrity simulation requires accurate package and chip PDN models to ensure correct designs.

- The ANSYS chip-package-system technologies provide full coverage for PI simulation needs:
- CPM: chip PDN and current draw
- Slwave and PSI: package PDN
- Slwave: board PDN
- Designer: frequency- and time-domain simulation for full PDN