Chip-Aware Power Integrity

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Agenda

• Power integrity challenges and solution
• New PI features in R14.5
• Power integrity case study
Power Integrity Challenges and Solution
The die-to-die system is extremely complex:

- Silicon driver/receiver
- 3D component interconnect
- Chip to package
- Package to daughter card
- Daughter card to backplane
- Power delivery network effects

Complex problems
- High risk
  - New unfamiliar phenomena?
- High cost of design errors

Solving them is requiring new strategies and simulation tools.
What is a Power Distribution Network (PDN)?

Complex multi-stage network supplying power to all devices in a system.

For typical products the PDN includes:

- Voltage regulator module (VRM)
- Board power/ground planes and decoupling capacitors
- Package power/ground planes and decoupling capacitors
- Chip power/ground structures and capacitance

PDN Requirements:
- Must deliver clean power to the ICs
- Must provide low impedance, low noise reference path for signals
- Must not contribute excessive EMI
Board Level Power Integrity?

Full PDN

- Discrete Decoupling Capacitor on PCB
- Low Inductance Capacitor on Package
- Ball Grid Array Package
- Ball Bonding
- VRM
- Bulk Capacitor
- Ground
- Power

ΔI

- Wire Bonding
- Package P/G Network
- Ball Bonding
- PCB P/G Network
- Very High Frequency Current
- High Frequency Current
- Medium Frequency Current
- Low Frequency Current
- Very Low Frequency Current

- Decoupling Capacitor On Chip
- Decoupling Capacitor On Package
- Decoupling Capacitor On PCB
- Bulk Capacitor Near VRM
Redhawk generates a chip power model (CPM) including chip PDN parasitics and switching currents.

PSI and SIwave provide robust extraction of IC packages and boards with broadband S-parameter models.

PI Advisor optimizes decoupling capacitor selection to meet a target impedance.

Designer SI simulates power noise in the time domain.
Chip Power Model (CPM)
CPS Convergence Using CPM

Chip Design
- Prototype
- Design
- Sign-off

Chip Power Model

Package / PCB Design
- Selection, Planning
- Package Design
- System Sign-off
Each C4 bump (power & ground) will be associated to its corresponding:

✓ Chip PDN RLC

Physical model of chip layout

✓ Transistor/cell current /cap/ESR

Electrical model of chip layout

CPM is topological, physical and activity based.
Benefits of CPM

Traditional die model

- Simplifying assumption of all gates switching at the same time

\[ \text{Triangular} \quad \text{Peak value} \quad \text{Triangular+Trapezoidal} \]

\[ \text{Freq} \quad T_1=500\text{ps} \quad \text{Freq} \quad T_1=500\text{ps} \]

Apache CPM

- Chip Power Delivery Network
- Supports both static and dynamic models
- Current signature represented as PWL sources

CPM includes all die parasitics

- Power-grid RLC
- Intrinsic De-cap
- Intentional De-cap
- Instance Load Capacitance
- Well Capacitance

Estimated Cdie

Missing Rdie, Ldie

Single Lumped Model
SIwave CPM Integration

SIwave CPM integration includes the following:

- Import of die PDN for inclusion in frequency-domain extractions
- Automatic matching of die pin to CPM pin locations
SIwave CPM Setup
CPM Impedance Effect

PDN Impedance at Die

Curve Info

mag(Z(FCHIP_VDD_15,FCHIP_VDD_15))

SYZ Sweep 1

PKG

PKG+CPM

mag(Z(FCHIP_VDD_15,FCHIP_VDD_15))

SYZ Sweep 2
Sentinel PSI
ANSYS Package/Board Solvers

3D full-wave

• Fast FEM using prism elements
• Tailored for PI package analysis

Trade-off speed for 3D accuracy

Hybrid full-wave

• FAST Hybrid method for PKG/BRD
• Handles many, but not all 3D effects

Fast
Sentinel PSI Strengths

Package/PCB structures Containing

• Highly perforated metal planes
  – Swiss Cheese PWR/GND planes
  – Hatched PWR/GND planes
• Two layer PCBs without reference layers
• Transmission lines over non-ideal ground
• Ports with unreferenced terminals
• Visualization of PWR/GND AC currents
• Vias with large anti-pads

Large continuous anti-pads

Port With Unreferenced Terminal

Typical Hatched Plane

Lines over non-ideal ground cutouts
PI Advisor is an addon for Siwave that automatically optimizes capacitor selection to meet a target impedance:

**Inputs:**
- Capacitor locations
- Candidate capacitors

**Outputs:**
- Capacitor schemes that indicate which candidate, if any, to populate at each location.
- Impedance versus target for each scheme.
Target Impedance
Target Impedance

• Designing for power integrity often involves a target impedance
  – Maximum allowable impedance magnitude over frequency which will result in acceptable voltage noise

\[ V_{\text{noise}} = I_{\text{pwr}} Z_{\text{PDN}} \]

• Several technical references contain something like

\[ Z_{\text{target}} = \frac{V_{\text{noise(max)}}}{I_{\text{pwr(A)peak}}} \]

• An example can illustrate the complexities with this approach...
A Simple Target Impedance Example

• Suppose we have a power current with the periodic AC component shown below (peak amplitude of 2A):

\[ I(t) = |I_1| \cos(2\pi t + \theta_{I1}) + |I_2| \cos(4\pi t + \theta_{I2}) + |I_3| \cos(6\pi t + \theta_{I3}) \]

• Suppose we have a maximum allowable voltage amplitude of 1V

• The simple approach suggests a max \( Z_{\text{PDN}} \) of 0.5\( \Omega \) over the frequency components contained in the current will satisfy the noise requirement

\[ V_f(t) = |I_f| \cdot |Z_f| \cos(2\pi f t + \theta_{I_f} + \theta_{Z_f}) \]

But our impedance tolerance does not specify phase
Effects of Different Impedance Phases

- Assume our PDN impedance just satisfies the requirement at each frequency: $|Z_1| = |Z_2| = |Z_3| = 0.5 \Omega$, but vary the impedance phase assumptions.

Simple approaches to calculating target impedance can provide a useful guide, but results should be verified with time-domain simulation.
Target Impedance Notes

Reliance on a purely resistive target impedance may not bound the resulting time-domain voltage waveform to the desired amplitude.

Target impedance calculations should take into account the impedance phase as well as magnitude, but the current state-of-the-art does not.

More to come from ANSYS on this topic...
Power Integrity Case Study
1.5V power supply for FPGA on board.

Chip included as Apache CPM.

Package included as static S-parameters.

Board extracted with SIwave 7.

Simulation includes:

- GND
- VCC_1V5

System excited by CPM currents.
Time Domain Circuit

Die Current

V
Name=u1_vcc
FGB Channel Power Only

A+
Name=i_u1

Port1
Port2

VCC
VSS

0

V

0

DC=1.5V

V5
Die Current

<table>
<thead>
<tr>
<th>Name</th>
<th>X</th>
<th>Y</th>
</tr>
</thead>
<tbody>
<tr>
<td>m1</td>
<td>7.3200</td>
<td>444.1449</td>
</tr>
<tr>
<td>m2</td>
<td>9.8700</td>
<td>422.7601</td>
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</tbody>
</table>

Die Current

<table>
<thead>
<tr>
<th>Name</th>
<th>Delta(X)</th>
<th>Delta(Y)</th>
<th>Slope(Y)</th>
<th>InvSlope(Y)</th>
</tr>
</thead>
<tbody>
<tr>
<td>d(m1,m2)</td>
<td>2.5500</td>
<td>-21.3847</td>
<td>-8.3862</td>
<td>-0.1192</td>
</tr>
</tbody>
</table>

Die Current

Curve Info

NexximTransient
PDN Impedance Components
Full PDN Impedance
Package Model Fit

- Port 1
- C236: 883.15 pF
- C237: 485.35 pF
- L238: 23.855 pH
- L239: 23.855 pH
- R240: 0.0136 ohm
- R241: 0.0139 ohm

883.15 pF
883.15 pF

23.855 pH
23.855 pH

13.6 mohm
13.9 mohm
Package Model Fit

The diagram shows a graph with the frequency (F) in GHz on the x-axis and an unknown parameter (Y) on the y-axis. The graph plots a curve that appears to be a fit of some package model, as indicated by the legend. The y-axis is labeled "Y1 [ohm]." The graph includes a title "Package Model Fit" and a subtitle "Circuit3."
Die Model Fit

3 nF

C55
3e-009farad

0.3 ohm

R54
0.3
Die Model Fit

Die Fit

Die

Circuit1

0.00 0.01 0.10 1.00 10.00
F [GHz]
0.10
1.00
10.00
100.00

Y1 [ohm]
Board with Package/Die Fits

Board PDN Impedance

FGB Board

Curve Info
- Board with Package/Die Fits
- Linear Frequency
- Full PDN
- Imported

Board w/ Package/Die Fits
Full PDN
1. As initially designed.
   - Eight 100 uF bulk capacitors at VRM output, two 10 uF capacitors, and two 1 uF capacitors.

2. With added high-frequency capacitors.
   - 12 0.01 uF capacitors placed on bottom layer below FPGA

3. With PI Advisor-optimized capacitor solution.
   - Target impedance: 0.3 ohms up to 1 GHz
   - Package RLC fit and die RC fit included at board FPGA footprint
Variation 1: As-Designed

Final period peak-to-peak: 62.3 mV
Variation 2: Added Capacitors

Variation 2
As-built
Variation 2: Added Capacitors

U1 VCC

Final period peak-to-peak: 67.2 mV
Variation 3: PI Advisor
Variation 3: PI Advisor

Variation 3
Variation 2
Variation 3: PI Advisor

U1 VCC

Final period peak-to-peak: 40.6 mV
Conclusion

Power integrity simulation requires accurate package and chip PDN models to ensure correct designs.

The ANSYS chip-package-system technologies provide full coverage for PI simulation needs:

- CPM: chip PDN and current draw
- SIwave and PSI: package PDN
- SIwave: board PDN
- Designer: frequency- and time-domain simulation for full PDN