Signal/Power Integrity Modeling of High-Speed Memory Modules Using Chip-Package-Board Coanalysis

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***Abstract*—Under the platform of a high-speed double-data-rate three (DDR3) memory module, a modeling method considering all the significant effects from the chip, package, and board levels is developed to identify and investigate the critical nets affecting the signal or power integrity (SI/PI). For SI part, accurate modeling strategies for signal channels are verified by experiments on samples of address lines. The following what-if analyses of eye diagrams help to identify the discontinuities of package trace to be the bottlenecks and have great effects on the eye diagrams. For PI issues, the modeling methodologies for power distribution networks of data buses are demonstrated and validated with the results of measurement. The analysis indicates that the parasitic effects of the low-cost package structure are the most critical, depicting the importance of improved package design in the next-generation DDR memory modules.**

***Index Terms*—Double-data-rate synchronous dynamic RAM (DDR SDRAM), eye diagram, model extraction, power distribution network (PDN), power integrity (PI), signal integrity (SI).**

I. Introduction

With the continual advancement of electronics technologies, the efficiency of memory modules is becoming a critical limiting factor for extending the performance of these computer systems. Owing to the benefits of low cost and high quality, the double-data-rate synchronous dynamic RAMs (DDR SDRAMs) are currently being developed for today's high-end computers and workstation applications. Table I shows the evolution of the DDR SDRAMs from the first to the fourth generation [1]–[3]. It can be seen that the operating voltage is getting lower with increasing data rates, thus, enabling lower power consumption and higher performance. Many nonideal effects, such as crosstalk noise [4]–[6], reflection noise [7]–[12], transmission-lines losses [13], [14], and simultaneous switching noise (SSN) [16]–[22], previously regarded as negligible have become major design challenges for satisfying the requirements of signal integrity (SI) and power integrity (PI) inside the package and board levels. Thus, the chip-package-board (CPB) coanalysis methodology for SI/PI issues has become more essential and played an important role in high-speed memory module design.

TABLE I
Evolution of DDR SDRAM

Specification	DDR1	DDR2	DDR3	DDR4
Operating Voltage (V)	2.5	1.8	1.5	1.2
Data-rate (Mbps)	200/266/ 333/400	400/533/ 667/800	800/1066/ 1333/1600	1600/2133/ 2667/3200
Setup + Hold Time (ps)	900	500	305	125

Conventional SI issues for double-data-rate three (DDR3) DRAMs are regarded as the degradation of digital signal transmission through interconnects including the crosstalk noise, reflection noise, and lossy effects. The crosstalk noise mainly originates from the mutual coupling between closely spaced interconnects, and the typical one is the serpentine delay line [4]–[6]. Discontinuities such as bends [7], via transitions [8]–[10], package structures [11], [12], and so forth, may result in severe reflection noise and also need to be considered carefully. At higher data rate, the frequency-dependent losses of transmission line have a significant impact on the signal quality and timing, and thus, cause the deterioration of eye diagrams [13], [14]. Moreover, the brief SI analysis for the address lines of the DDR3 memory module has been discussed in [15], while the PI effects are totally excluded.

Furthermore, both the plane resonances [16], [17] and the parasitic effects of interconnects [18] inside the power distribution network (PDN) can be considered as two major PI concerns [19]. If the two are not appropriately controlled, SSN will be induced on the dc voltage supply level of the PDN [20]–[22]. The combined effects of both SI and PI problems may lead to a poor eye diagram [23], false switching of the active devices, and even an overall system failure, especially when the system operates at higher frequencies. Some cosimulation

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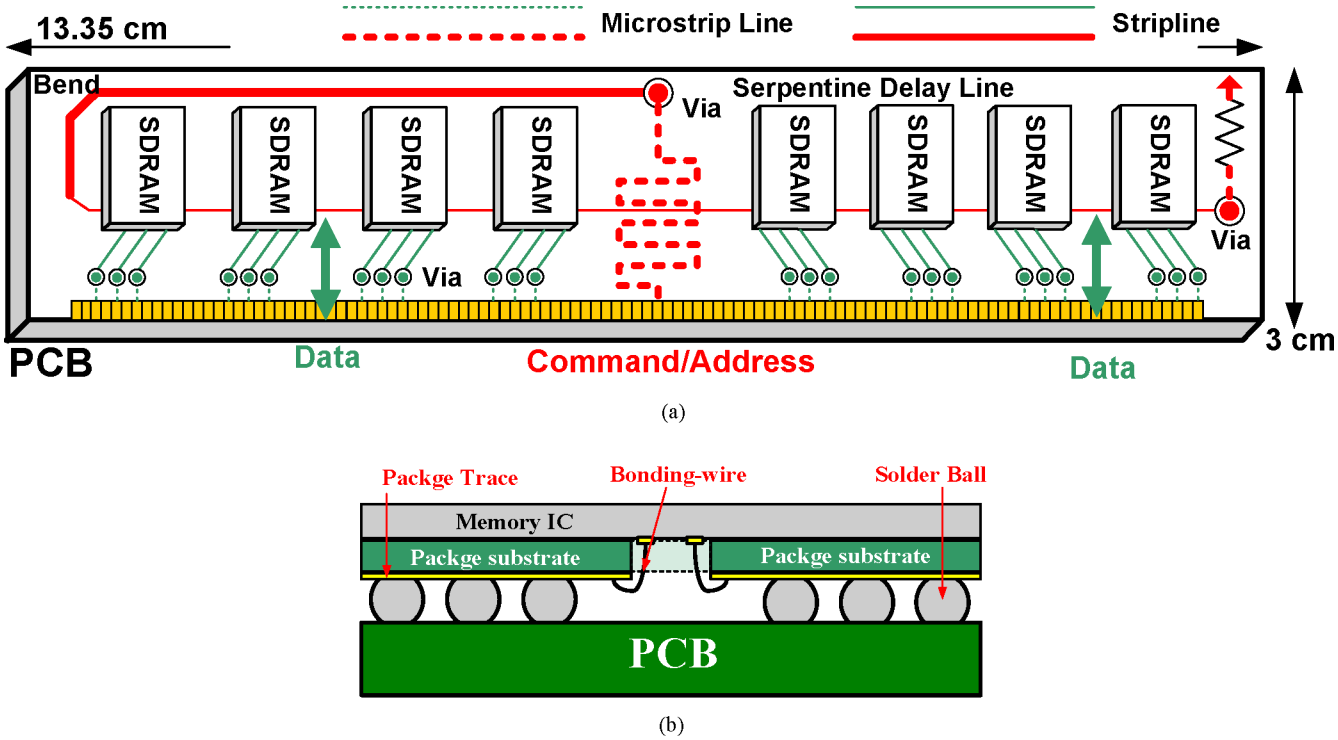


Fig. 1. Physical structure of DDR3 SDRAM memory module. (a) Top view. (b) Cross-sectional view.

techniques incorporating both the channel and PDN models have been developed for the front-side bus interface and graphic DDR system [24], [25], but it is still lacking a comprehensive study on what the bottleneck is for the extension of system performance, which serves as the major motivation for this study.

This paper focuses on the modeling of the SI/PI issues for different kinds of signal groups, i.e., command lines, address lines, clock lines, and data buses, under the platform of a high-speed DDR3 memory system. The organization is as follows. Section II describes the physical structure of the current DDR3 memory system. The modeling methods and the verification of the signal traces are presented in Section III. Then, the analysis procedure is demonstrated in Section IV to point out the influences of the most noteworthy discontinuities. For the PI issues, the modeling of PDNs among the module is verified with the results of measurement in Section V. In Section VI, what-if analysis is adopted to identify the bottlenecks for the concerns of PI inside the DDR3 memory system. Finally, some conclusion are drawn is Section VII.

II. Memory Module Overview

The DDR3 memory module, also named as dual in-line memory module, is depicted in Fig. 1(a). Usually, there are eight units of SDRAM and each of the units is composed of a memory chip with the associated package substrate. Fig. 1(b) shows the cross section of the memory module. The memory ICs are directly connected to the package with bond wires, while the package and printed circuit board (PCB) are linked by solder balls. The whole signal interconnects and the corresponding PDNs inside the DDR3 memory module can be divided into three groups, which include the clock lines, the command/address lines, and the data buses.

All signal groups, except the data buses, implement the fly-by topology [3], which sweeps long distances from the left side of PCB to the right as shown in Fig. 1(a). For long high-speed interconnects, differential lines are widely used because of their immunity to noise, crosstalk, and electromagnetic interference. Since there is an upper limit in the total number of signal interconnects, only the clock line is designed as the differential structure, while the other lines are all kept to be single-ended. As a result, the concern about SI problems for the clock lines is not so critical as compared with the other two groups.

From the PI point of view, the data buses with considerable switching currents are the most critical among the three groups. Because the off-chip drivers (OCDs) need to have a rapid current transient at their outputs, there are numerous simultaneous switching currents emerging at the power/ground nodes of OCDs. Actually, the PDN of OCDs is separated from that of other active circuits. Other signal groups thus have better immunity to the SSNs produced by the OCDs.

In summary, the significant SI issues happen to the signal groups of command/address lines, and these lines are less sensitive to the SSNs from I/O circuits. Furthermore, the data buses suffer from severe SSNs due to the connected OCDs with swift voltage transient. As the signal traces of data buses on the PCB are much shorter; the SI problems of the data buses are not serious, and are not discussed in this paper.

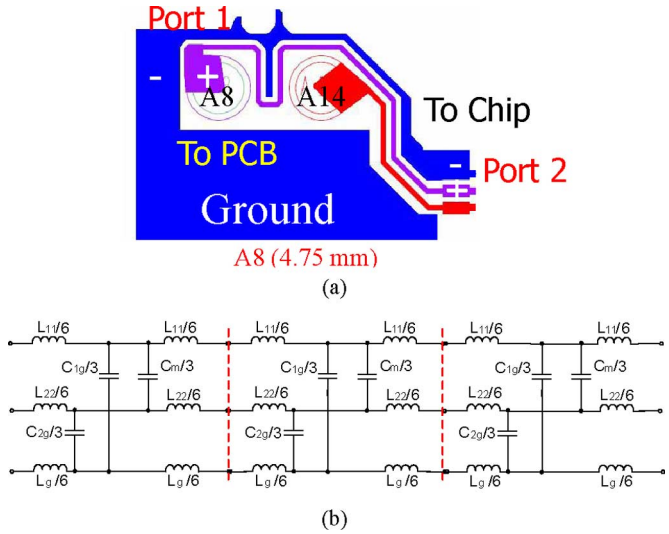
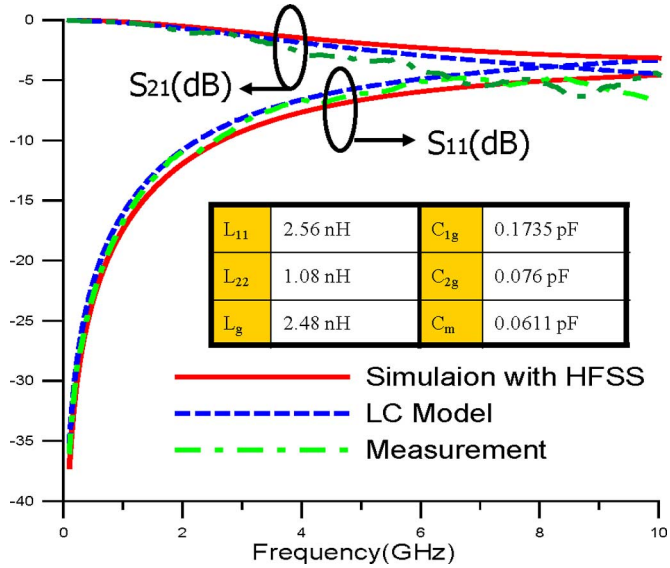


Fig. 2. Package layout of DDR3 memory module. (a) Part of an address line, and (b) corresponding equivalent model.



L_{11}	2.56 nH	C_{1g}	0.1735 pF
L_{22}	1.08 nH	C_{2g}	0.076 pF
L_g	2.48 nH	C_m	0.0611 pF

Fig. 3. Simulation and measurement results for package substrate.

III. Modeling and Verification of SI

In this section, the modeling method for the command/address line is first introduced. Since all the command and address lines have a similar physical structure, only one of the address lines is chosen for the following discussion.

The signal interconnects include two major parts, the single-layer package trace and the fly-by topology with several discontinuities on the PCB. The overall layout of the package trace includes PDNs, signal traces for the data buses as well as clock, command, and address lines. Fig. 2(a) shows the address lines of A8 and A14, which are enclosed by the ground nets in the blue region. The T-type models as depicted in Fig. 2(b) are chosen to characterize the current package design. The boundary element method is then employed to extract the capacitance and the partial inductance of the package substrate [26]. To increase the modeling accuracy at high frequencies, the package model is constructed by cascading three T-model segments as depicted in Fig. 2(b). The number of segments is determined by the criterion that the length of one segment should be smaller than one-tenth of a wavelength, depending on the highest frequency in the simulation.

As shown in Fig. 2(b), L_{11}, L_{22}, and L_g are defined as the self partial inductances of the A8, A14, and the ground trace, respectively. C_{1g} and C_{2g} represent the capacitances of the A8 and A14 line with respect to ground trace; C_m is the mutual capacitance between the A8 and A14 traces. Although not shown here, the mutual partial inductances between signal and ground traces are still introduced in the circuit simulation [27]. In Fig. 3, the accuracy of the equivalent models is verified through both the vector network analyzer (Agilent N5230 A) measurement and the 3-D electromagnetic simulator HFSS [28] from 300 kHz to 10 GHz, where the corresponding L and C values are shown in inset and the corresponding two ports are listed in Fig. 2(a).

Next, for the address lines routed in the PCB level as shown in Fig. 1(a), the profile of one sample and its equivalent model are shown in Fig. 4. The total transmission path is separated

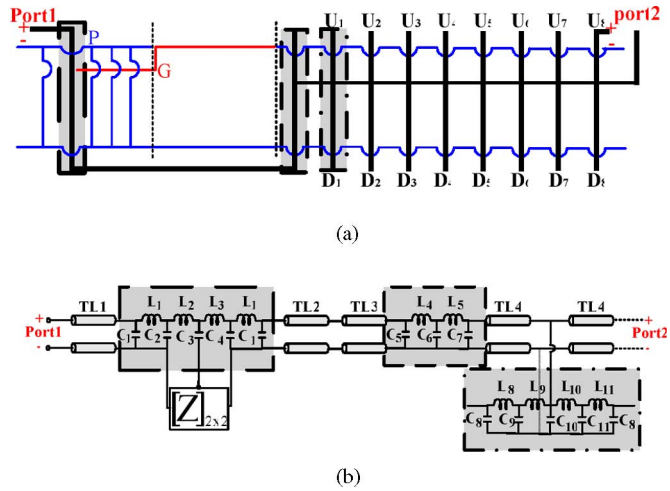


Fig. 4. PCB of memory module. (a) Profile. (b) Equivalent model.

into the transmission line sections together with three major discontinuities, which are enclosed by the dissimilar dashed lines. There are eight units of chips (U_1–U_8) placed on the upper side of PCB, while the other eight units of chips (D_1–D_8) are placed on the backside.

The TL_1 of Fig. 4(b) represents the microstrip line from the golden finger to the through-hole via on the top layer, and the TL_2 means the one in the bottom layer, which goes from the center of PCB to the left as shown in Fig. 1(a). The equivalent model of the through-hole via structure includes the multilayer ground bounce effect by appending the impedance matrix of $[Z]_{2\times2}$ extracted from the hybrid finite-element simulator [8], [19], [29]. The TL_3 is designed as a thin stripline structure with higher impedance to overcome the input capacitance of the chips. Similarly, the equivalent models of the connected via structures are also presented. According to the physical layout, the fly-by topology is thus achieved by cascading eight successive models composed of the transmission line sections and asymmetrical

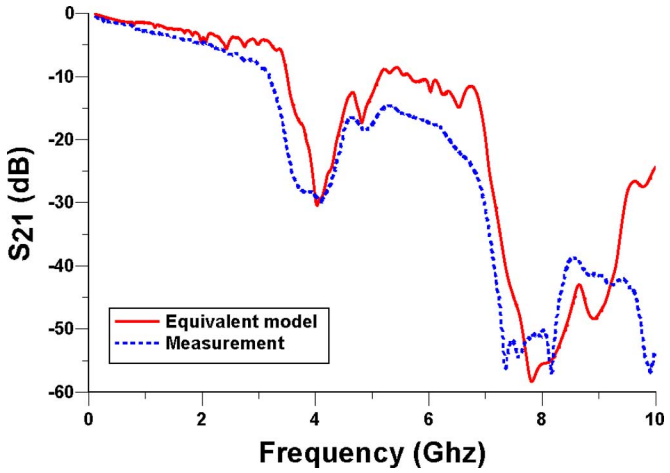


Fig. 5. Simulation and measurement results for the PCB.

via stubs. Finally, the port 2 is set at the end of the fly-by topology. Fig. 5 shows the comparisons between the simulation and measurement results, where reasonably good agreement can be noticed for the frequency range below 5 GHz. The discrepancy above 5 GHz is caused by the ignorance of the dielectric and conductor loss in the model.

IV. Analysis of SI

A. Fly-By Topology (Command/Address Line)

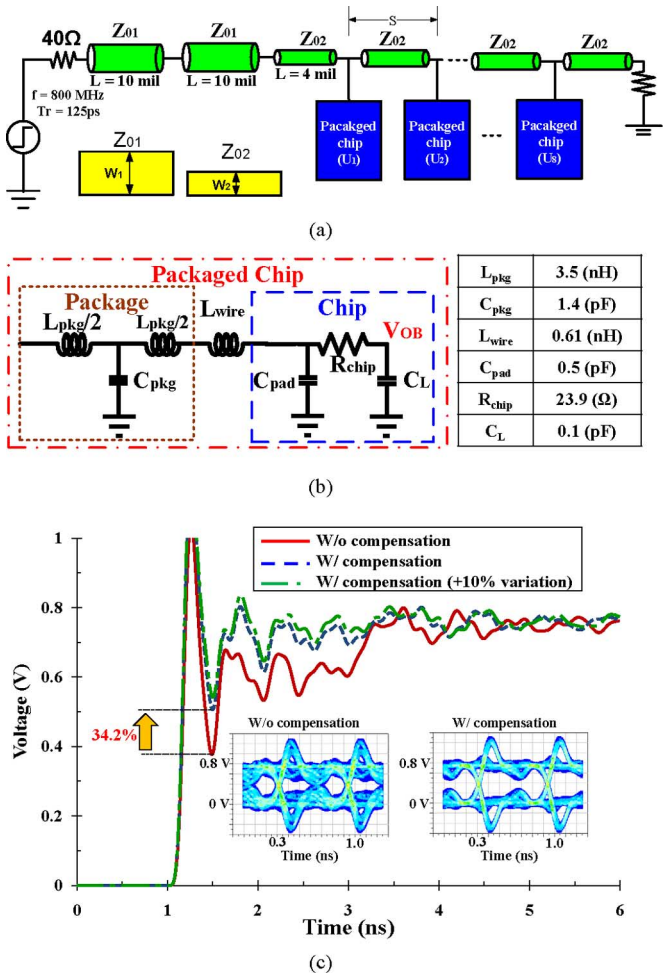
Except data buses, the other signal interconnects of the DDR3 memory module adopt the fly-by topology in order to distribute the capacitive loading of the connected memory chip, as shown in Fig. 6(a). Nevertheless, unwanted signal reflection still arises from this additional capacitive loading. Such effects can be alleviated by narrowing the connected transmission line in the vicinity, following the basic concept of impedance match employed in [30] and [31]. The total capacitance looking into the packaged chip in Fig. 6(b) is

$$C_{\mathrm{Total}} = C_{\mathrm{pkg}} + C_{\mathrm{pad}} + C_{\mathrm{L}} \tag{1a}$$

where C with subscripts pkg, pad, and L denote capacitance of the package, chip pad, and chip loading, respectively. The design uses the inductive effects of thin trace to match the overall effective impedance with the system impedance, that is,

$$Z_0 = \sqrt{\frac{L_1}{C_1}} = \sqrt{\frac{L_2}{C_2 + (C_{\mathrm{Total}}/S)}} \tag{1b}$$

where Z_0 is the system impedance, S is the distance between two chips, and L_1, C_1 and L_2, C_2 mean the per-unit-length lumped elements of the transmission lines Z_{01} and Z_{02}, respectively. Between the capacitive loading and the transmission line Z_{02}, there are always the packaged chips with the package interconnects and the corresponding chip loads. The details of the packaged chip are described in Fig. 6(b). Here, the package interconnects are one section of T-model with L_{pkg} and C_{pkg}, and then series connected with inductance of bond wire (L_{wire}) and parasitics of the chip, where the C_{pad}, R_{chip}, and C_{L} represent the capacitance of the pad, the resistance of the metal line, and the input capacitance of the chip, respectively.



L_{pkg}	3.5 (nH)
C_{pkg}	1.4 (pF)
L_{wire}	0.61 (nH)
C_{pad}	0.5 (pF)
R_{chip}	23.9 (Ω)
C_L	0.1 (pF)

Fig. 6. Influence of compensation for fly-by topology of command/address line is demonstrated. (a) Equivalent model (b) with the packaged chip parasitic and (c) simulated step responses observed at V_{OB} of (b) with corresponding eye-diagrams in the inset.

By neglecting the discontinuities of via and serpentine, Fig. 6(c) shows the simulated responses and eye diagrams at node V_{OB} within the packaged chip U_1 as marked in Fig. 6(b) with and without optimized design of the trace width. Also, in order to investigate the influences of process variations on the SI, which usually result in the change of characteristic impedance, additional waveform is shown with 10% increase of the characteristic impedance compared to the case of thin trace design. The input signal adopts the pseudorandom bit sequence (PRBS) with data rate of 1.6 Gb/s, rise time of 125 ps, and voltage amplitude of 1.5 V. Comparing the effect of design of thin traces, better impedance matching is achieved with the improvement of 34.2% in the received voltage, whereas the influence of impedance change due to process variations is not obvious. The length of the thin trace (S) can be calculated through (1). Here, the design curve is provided in Fig. 7 to facilitate the compensation design. For the present case, $Z_{01} = 40\ \Omega$ such that the original stripline width (W_1) is 10 mil wide, as well as $C_{\mathrm{Total}} = 2$ pF and the separation of memory chips is fixed at $S = 14.3$ mm. It is, thus,

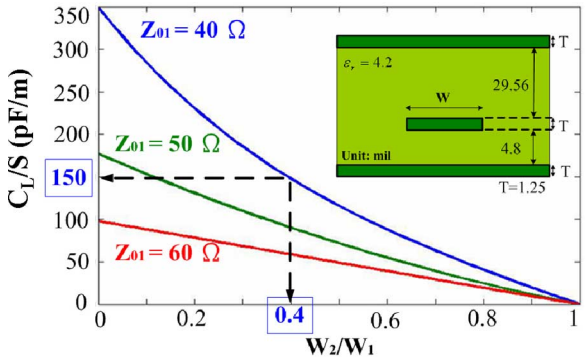


Fig. 7. Design curve for the thinner transmission line in fly-by topology.

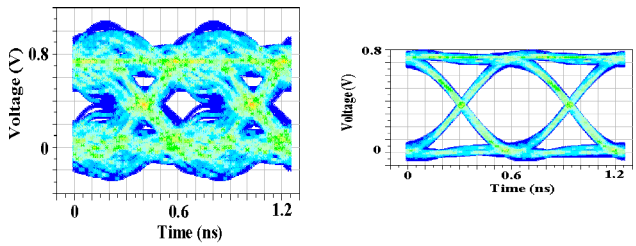


Fig. 8. Simulated eye diagrams are displayed with (a) all nonideal effects and (b) all except package. Note that the thin trace design has been included.

TABLE II
EFFECT OF EACH DISCONTINUITY ON EYE QUALITY

Degree of non-ideal effects		(v: consider x: neglect)				
Chip		V	X	V	V	V
Package		V	V	X	V	V
PCB	Via	V	V	V	X	V
	Serpentine	V	V	V	V	X
Eye-height (mV)		278	489	620	377	283
Influence (%)			75.9	123.0	35.6	1.8

deduced that the width of thin trace (W_2) should be designed to be 4 mil.

B. Effects of Other Discontinuities

Besides, the simulated eye heights in regard to all other discontinuities are observed to access their significances for the system performance. As depicted in Fig. 8, the eye diagrams considering all nonideal effects have inferior performance, while the one with the package effects excluded has best enhancement. The detailed results have been summarized in Table II. It is found that the parasitic of package has the largest significance, followed by the discontinuous effects of chip circuit, via, and serpentine in descending order. Each nonideal effect appearing in the layout of a DDR3 memory module has been thoroughly investigated through the eye diagram simulation, which would be very helpful in the package/PCB codesign for a next-generation product.

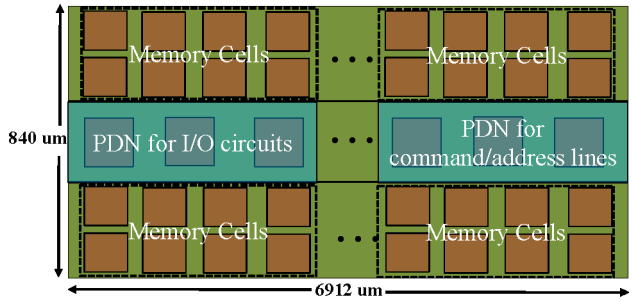


Fig. 9. Memory chip with memory cells and the PDNs.

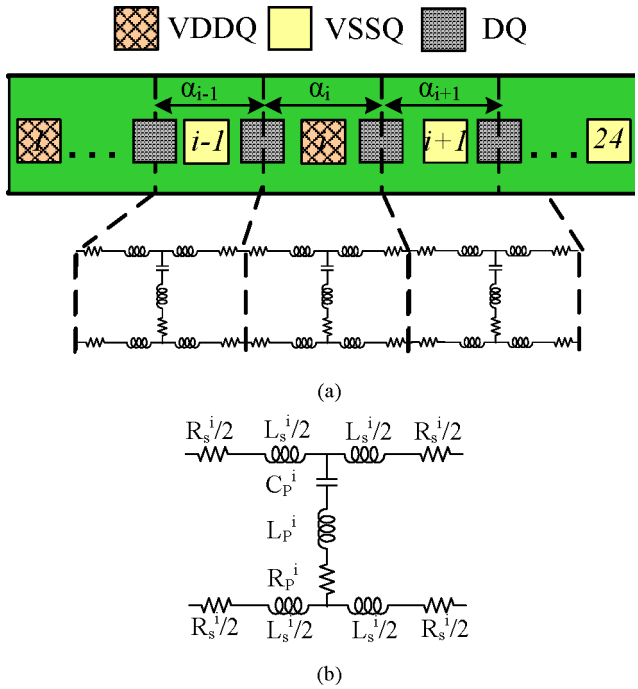


Fig. 10. PDN of I/O circuits on the chip. (a) Physical structure. (b) Equivalent model of each segment.

V. MODELING AND VERIFICATION OF PI

In this part, the modeling methodology for the PDN of data buses will be demonstrated. As mentioned earlier, the data buses are connected to the OCDs with rapid current transients so that significant SSN will be induced. As shown in Fig. 1(a), however, the signal traces of data buses are routed from the solder balls directly to the golden fingers. Thus, the models of signal traces can be simplified in the circuit simulation. The major attention could be focused on the extraction method for PDN models from the chip, package, and PCB.

The equivalent models for the PDNs inside the chip, package, and PCB are extracted in different ways. First, for the memory chip outlined in Fig. 9, it is observed that the memory cells are located in the periphery of the chip, while all the I/O and power/ground pads are placed along the center line. An example of the pad assignment of the OCD is depicted in Fig. 10(a), where the DQ, VDDQ, and VSSQ are the output, power, and ground pads of OCDs, respectively. Note that each DQ pad is arranged between the VDDQ and VSSQ pads. There are in total 12 VDDQ

and 11 VSSQ pads along the central line of the chip. The power bus model can thus be formed by cascading 23 sections of the T-models, which correspond to the total number of the VDDQ and VSSQ pads on the chip. As illustrated in Fig. 10(b), each T-section consists of an impedance $Z(\omega)$ formed by a resistance (R_S) in series with an inductance (L_S), both on the power and ground paths, and of an admittance $Y(\omega)$ formed by the series of a capacitance (C_P), an inductance (L_P), and a resistance ($R_{\rm p}$).

The *RLC* element is assumed uniformly distributed along the 1-D power/ground pads. Then, their values in *i*th section can be represented in terms of per-unit-length parameters as

$$R_S^i = \alpha_i R_S \tag{2a}$$

$$L_S^i = \alpha_i L_S \tag{2b}$$

$$R_p^i = \frac{1}{\alpha_i} R_p \tag{2c}$$

$$L_P^i = \frac{1}{\alpha_i} L_P \tag{2d}$$

$$C_P^i = \alpha_i C_P \tag{2e}$$

where

$$R_S(\omega) = \max(R_{S\rm dc}, R_{S\rm ac}\sqrt{\omega}) \tag{2f}$$

$$R_P(\omega) = \max(R_{P\rm dc}, R_{P\rm ac}\sqrt{\omega}) \tag{2g}$$

$\alpha_{\rm i}$ is the physical length of section *i* in Fig. 10(b), and R_S, L_S, R_P, L_P, and C_P are the per-unit-length parameters, respectively. The physical length α_i can be obtained in the real chip pad layout, but the seven per-unit-length parameters are unknowns that should be extracted from the results of measurements. The ABCD matrix of section *i* is

$$\begin{bmatrix} 1+ZY & (ZY+2)Z \\ \rm Y & 1+ZY \end{bmatrix} \tag{3}$$

where

$$Z(\omega) = 2j\omega L_S^i + 2R_S^i$$

$$Y(\omega) = \frac{j\omega C_P^i}{1 + j\omega C_P^i R_P^i - \omega^2 L_P^i C_P^i}.$$

The two ports are chosen at section 3 (port 1) and section 21 (port 2), the PDN on the chip can be expressed by three ABCD matrixes, $\mathbf{M}_1$, $\mathbf{M}_2$, and $\mathbf{M}_3$ as

$$\mathbf{M}_i = \begin{bmatrix} A_i & B_i \\ C_i & D_i \end{bmatrix} \tag{4}$$

where $i = 1$, 2, and 3. $\mathbf{M}_1$ stands for the network from section 1 to 3, $\mathbf{M}_2$ represents from section 4 to 21, and $\mathbf{M}_3$ represents from section 22 to final section 23. The *Y* parameters seen between port 1 and 2 can be derived as

$$Y_{11} = \frac{C_1}{D_1} + \frac{D_2}{B_2} \tag{5a}$$

$$Y_{12} = Y_{21} = -\frac{1}{B_2} \tag{5b}$$

$$Y_{22} = \frac{A_2}{B_2} + \frac{C_3}{A_3}. \tag{5c}$$

The corresponding two-port $\boldsymbol{Z}$ parameters $\boldsymbol{Z}_S$ can then be obtained by parameter transformation between $\boldsymbol{Y}$ and $\boldsymbol{Z}$ parameters.

By choosing two ports near the opposite ends of memory chip, the section 3 and 21, a two-port $\boldsymbol{Z}$ parameter $\boldsymbol{Z}_{\rm M}$ of the chip power bus is measured. The parameters $R_{S\,dc}$, $R_{S\,\rm ac}$, $R_{P\,\rm dc}$, $R_{P\,\rm ac}$, L_S, and L_P can be obtained by curve fitting. First, given the values of these parameters, the equivalent model in Fig. 10(a) is used to obtain the simulated *Z* parameters Z_{ij}^S by (3) to (5). The simulated curves of *Z* parameters versus frequency are compared with the measured data to check the model properness. Based on the Powell's method [32], these parameters can be extracted by minimizing the least square error between Z_{ij}^S and the measured *Z* parameter Z_{ij}^M, i.e.,

$$U(\Phi) = \sum_{n=1}^{1091}\sum_{i=1}^{2}\sum_{j=1}^{2} \left| Z_{ij}^S(\Phi, \omega_n) - Z_{ij}^M(\Phi, \omega_n) \right|^2. \tag{6}$$

Here, eight parts of Z_{ij}^S and Z_{ij}^M parameters are taken into account, which include real and imaginary parts of Z_{11}, Z_{12}, Z_{21}, and Z_{22}. The ω represents the radian frequency, which consists of 1091 sampled data from 300 kHz to 10 GHz, and the Φ represents the parameters to be optimized.

A real DDR3 memory chip is used as an example to extract the distributed model of the on-chip power bus. The chip size is 4074 μm $\times$ 840 μm and the memory capacity is 1 Gb. The two-port *S*-parameters are measured between section 3 (port 1) and section 21 (port 2) from 300 kHz to 10 GHz. The extracted values of $R_{S\rm dc}$, $R_{S\rm sc}$, $R_{P\rm dc}$, $R_{P\rm sc}$, L_s, L_p, and $C_{\rm de}$, are 1.211 Ω/mm, 0.708 Ω/mm/GHz$^{1/2}$, 2.048 Ω·mm, 0.882 Ω·mm/GHz$^{1/2}$, 0 pH/mm, 6.908 pH*mm, and 1.352 nF/mm, respectively. The calculated $U(\Phi)$ in (6) is 70.62, and the comparison between the results of equivalent model and measurement are shown in Fig. 11. The computing time is 809 s by the quad-core computer (Intel Core 2 Quad Q9300).

Fig. 8 presents the comparison of *Z* parameters between the vector network analyzer (Agilent N5230 A) measurement and the equivalent circuit modeling using MATLAB [33]. Good agreement is seen from 300 kHz to 10 GHz. In order to check the accuracy of the extracted model, another two-port measurement on the DDR3 chip is done between section 11 (port 1) and section 21 (port 2). The corresponding *Z* parameters predicted by the extracted models can also be obtained. The $U(\Phi)$ slightly increases to 275.19, which means that the equivalent model is still accurate enough to predict the characteristic response of the on-chip power bus up to 10 GHz.

As for the PDN of the package, the modeling method is the same as that described earlier for signal traces of the address line at the package substrate. For the PDN of the PCB, it is known that the profile of the PCB in Fig. 12(a) has eight units of packaged chip placed from the left side of PCB to the right. The layer stackup and its cross-sectional dimensions of PCB are also presented. Note that the corresponding dc voltage input VDD from the golden fingers is situated at the center of PCB. The transmission path from the dc voltage input to the most distant DRAM unit could be the critical one for PDN performance. As a result, the PDN of $\rm U_1$ is chosen to demonstrate the modeling

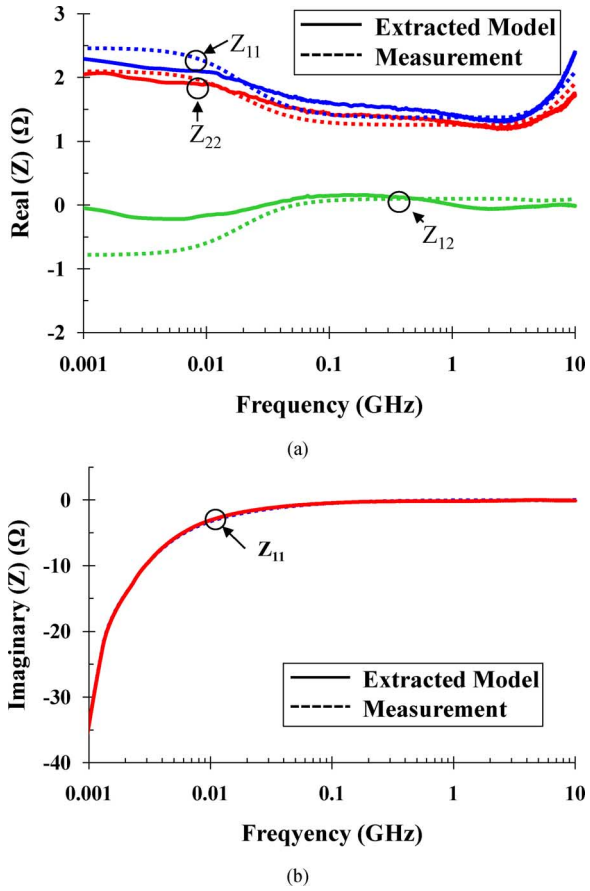


Fig. 11. Simulation and measurement results. (a) Real part of *Z* parameter. (b) Imaginary part of *Z* parameter.

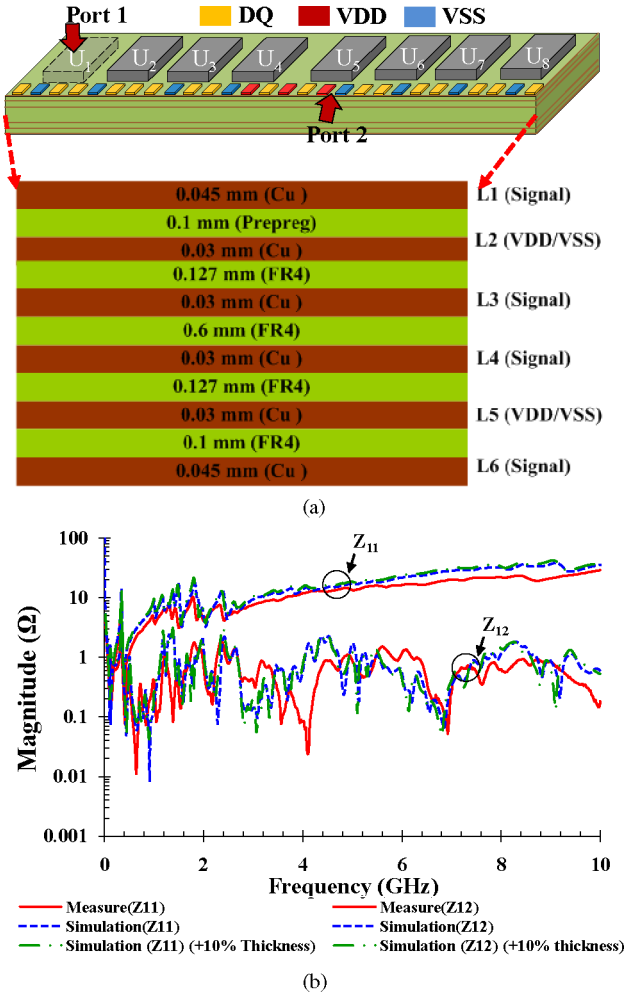


Fig. 12. Simulation setup and its results. (a) Port locations for measurement and the PCB stackup. (b) Magnitudes of Z_{11} and Z_{12}.

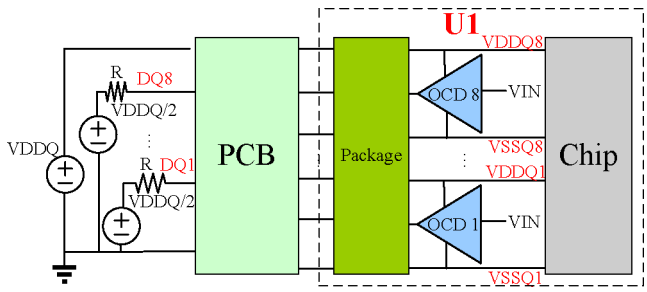


Fig. 13. Simulation setup for entire PDN of I/O interfaces.

and analysis method. Since the PCB of the memory module has six layers with hundreds of signal lines, it is complex and time-consuming to be analyzed by a full-wave simulator. Commercial software [29] using the hybrid finite element method is then utilized to construct the macromodels of PDN inside PCB. Furthermore, to consider the effect of dielectric thickness on the PI, the dielectric thickness of the PCB has been enlarged to 10% to see the influences of process variations on *Z* parameters.

The macromodels between the golden fingers of the input power/ground (VDD/VSS) and the pads connected to the solder ball on U_1 are extracted from the simulated frequency responses over 300 kHz to 10 GHz. Some measurement results are obtained to verify the modeling accuracy. One port is set at one of the voltage inputs from a golden finger, and the other is located at one of the pads connected to the solder ball on U_1. As presented in Fig. 12(b), the differences between the simulation results with and without the increasing thickness are small, and good agreements are also observed between the simulated and measured *Z* parameters. That is to say, the established macromodel can accurately predict the frequency response for the PDN of the PCB in the desired frequency band.

VI. Analysis of PI

PI problems are of great importance to the operations of I/O interconnects inside the DDR3 memory module. A simulation methodology has been established by cascading the equivalent models from different parts of memory module containing the PDNs of chip, package, and PCB. The what-if analysis is also employed to find out the bottleneck of all distinct PDNs.

As described in Section IV, eight packaged chips, each with eight OCDs, are mounted on the PCB from the left side to the right. The pads of the memory chip are placed along the central line, connected to the single-layer package by bond wires, and finally to the PCB with solder balls. Fig. 13 shows the profile of the high-speed I/O interconnects. In order to emphasize PI

TABLE III
EYE DIAGRAM PERFORMANCES VERSUS DATA RATE

Data rate (Mbps)	800	1600	2133	2667	3200
Eye width (UI)	0.974	0.902	0.934	0.723	0.685
Eye-height (mV)	792	776	655	521	412

TABLE IV
COMPARISON TABLE OF FOUR CASES OF PDNS

	Ideal	Case1	Case2	Case3	Case4
Eye-width (UI)	0.957	0.685	0.389	0.899	0.818
Eye-height (mV)	885	412	265	638	445
$\Delta VSSQ_{p\text{-}p}$ (V)	N/A	1.06	1.13	0.442	0.758
$\Delta(VDDQ\text{-}VSSQ)_{p\text{-}p}$ (V)	N/A	0.179	1.07	0.177	0.139

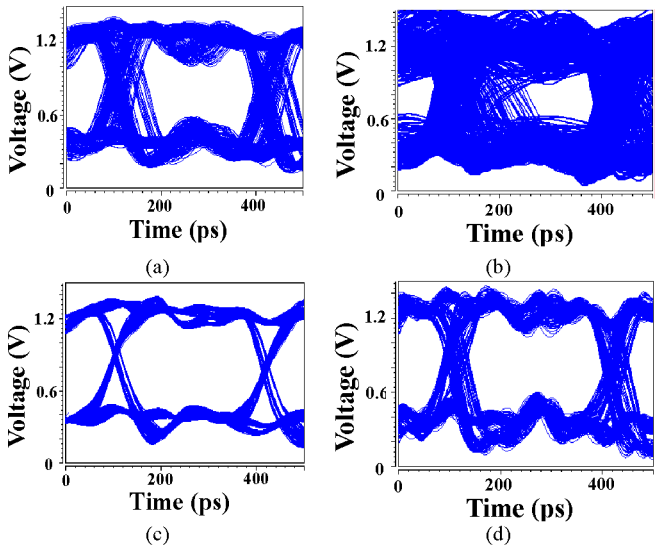


Fig. 14. Eye diagrams of Table IV. (a) Case 1. (b) Case 2. (c) Case 3. (d) Case 4.

issues of the I/O interconnects, the eight OCDs mounted on the U_1 are driven with the same PRBS to intensify SSNs. The ideal dc voltage of VDDQ with 1.5 V is set between the power and ground nets of the golden finger while the output terminations of data buses at the golden finger is a 25-Ω resistor connected to the reference voltage of half VDDQ.

As stated earlier, since the PDN linked with U_1 or U_8 is the critical path, the PDN of U_1 is selected to perform the simulation. The eight OCDs are designed to satisfy the specification of DDR3 I/O interconnects. The package model used here is constructed in accordance with the physical layout of the package structure connected to U_1. The PDN models in different regions are combined in an Hspice environment [34]. The eye diagrams of DQ_1 and the peak-to-peak voltage variations at $VDDQ_1$ and $VSSQ_1$ are of interest, as illustrated in Fig. 13. The influence of data rate on the operation of I/O circuits can also be discussed. Several data rates are chosen in the range from 800 to 3200 Mb/s, which are the possible operation speeds of a memory module from DDR2 to DDR4. The simulated eye diagram performance listed in Table III degrades dramatically as the data rate increases from 800 to 3200 Mb/s. It is imperative to find out which part of the entire PDN is the bottleneck of the memory module.

Five different cases are picked out for discussion. The ideal case means that the power nodes of all OCDs are directly connected to the VDD with the PDN excluded. Case 1 includes the entire PDN, while the cases 2, 3, and 4 remove only the PDN of the chip, package, and PCB, respectively. The corresponding eye diagram performances (DQ_1) and the peak-to-peak voltage variations at node $VSSQ_1$, $\Delta VSSQ_{p\text{-}p}$, as well as the differences between $VDDQ_1$ and $VSSQ_1$, $\Delta(VDDQ-VSSQ)_{p\text{-}p}$, for the data rate of 3200 Mb/s are listed in Table IV. All the eye diagrams except the ideal case are shown in Fig. 14, where the ideal case is to serve as a reference to evaluate the degradation for the other four cases. In order to correlate the time-domain voltage variation for each case with the power impedance profile in frequency domain, the PDN impedance between $VDDQ_1$ and $VSSQ_1$ (Z_{PDN}) and input impedance of $VSSQ_1$ (Z_{IN}) for the four cases are also shown in Fig. 15(a) and (b), respectively.

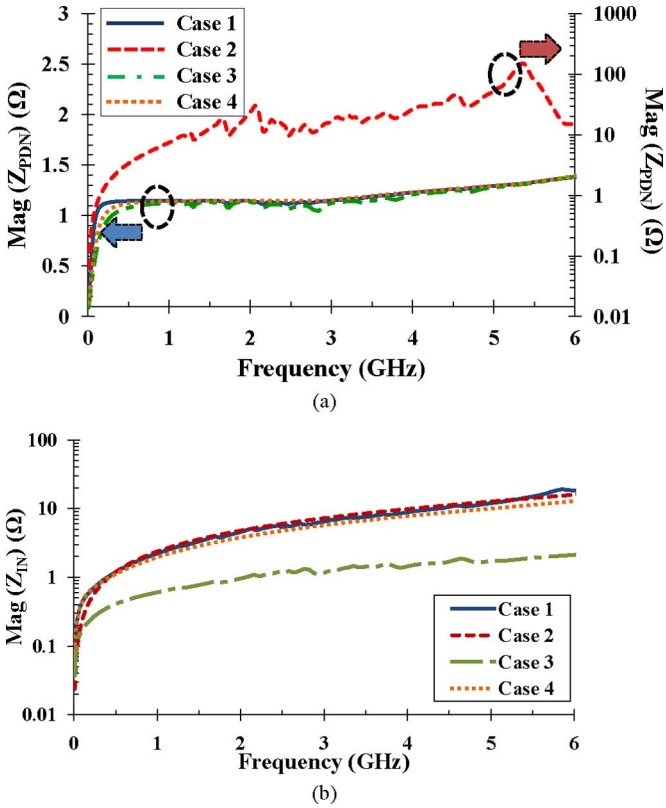


Fig. 15. Four cases of (a) PDN impedance (Z_{PDN}) between $VDDQ_1$ and $VSSQ_1$ and (b) the input impedance (Z_{IN}) at $VSSQ_1$.

Comparing the other listed results, case 2 has the worst performance among the four cases, which causes eye-width and eye-height degradation of 59.4% and 70%, respectively, as compared to those of the ideal case. The eye-diagram degradation are mostly induced by the increased voltage variation on both $\Delta VSSQ_{p\text{-}p}$ and $\Delta(VDDQ–VSSQ)_{p\text{-}p}$, which are mainly caused by the removal of the on-chip decoupling capacitors. As shown

in Fig. 15(a), without the parallel connection of on-chip decoupling capacitor, the magnitude of Z_{PDN} behaves as an inductor, and is therefore, considerably larger compared to the other cases.

As shown in Table IV, case 3 neglecting the PDN of the package has the most improvement in the eye quality. The main reason is that the voltage variation of $\Delta \mathrm{VSSQ}_{\mathrm{p\text{-}p}}$ is apparently smaller than the others. This is because the package substrate is a single-layer metal, which is the only area to place all the power, ground, and signal traces. The very thin traces on the substrate thus lead to larger self-inductance values of each trace so that considerable noise that degrades the PI/SI performance will be produced. As shown in Fig. 15(b), removing the PDN of package can have obvious decrease on the magnitude of Z_{IN} compared to the other cases.

Based on the above what-if analyses, the system bottleneck of the DDR3 memory module is identified to be the package interconnects, which is resulted from its one-layer structure with thin power and ground traces.

VII. Conclusion

An analysis methodology is proposed in this paper to investigate the system bottleneck for the current design of a DDR3 memory module. For the SI part, the characteristics of three major signal categories are clearly clarified to understand their difficult points. After that, complete modeling methods for the signal traces are discussed, and the modeling accuracy has been verified up to 10 GHz by measurements on samples of address line.

For the command/address lines, SI problems play a very important role. A thin trace design in the fly-by topology is adopted to overcome the distributed capacitive loading of packaged chip. For the present case, the time-domain simulation shows that the eye quality is improved by 34.2% with the thin trace compensation. A design curve is also given to facilitate the compensation design.

As for the data buses, the frequent and large switching currents make the PDN design significant. To consider the PI concerns, a 1-D model considering power bus of chip is extracted from the two-port measurements and good agreements are obtained to 10 GHz. Then, by combining the distributed chip model together with the package trace and extracted PCB macromodel, the overall equivalent models are analyzed for predicting the performance of eye diagrams. No matter whether for the command/address lines or data buses, the applied what-if analysis depicts that the single-layer package interconnects are the most crucial part for system performance. In other words, once the system failure occurs, the first concern for the module designers must be the package layout. The solutions for package design to solve SI and PI issues in the next generation memory module such as DDR4 are still under research in our group.

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