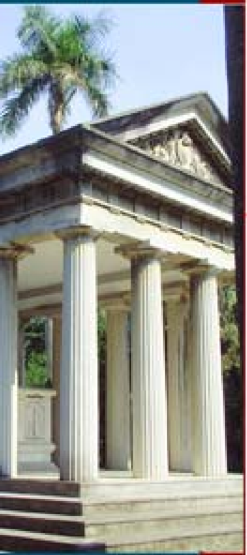

Power Integrity and EMC Design for High-speed Circuits Packages

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國立臺灣大學

NTU
National Taiwan University

Outline

- Power Distribution Network (PDN)
- Mechanism of Power Noise
- Issues and Quantification of Power Noise
- Solutions of Suppressing Power Noise
  - Decoupling Capacitors
    - Power/ground planes (PKG, PCB)
    - Surface mounted capacitor (PCB, PKG)
    - Embedded capacitor (PKG)
    - On-chip capacitor (Chip)
  - Isolation slots
  - EBG structures
    - Electromagnetic Bandgap (EBG) Power Planes
    - Photonic Crystal Power Layer (PCPL)
- Conclusion

Trends for high-performance Electronics

*Source: The International Technology Roadmap for Semiconductor (ITRS), 2007 (http://public.itrs.net)

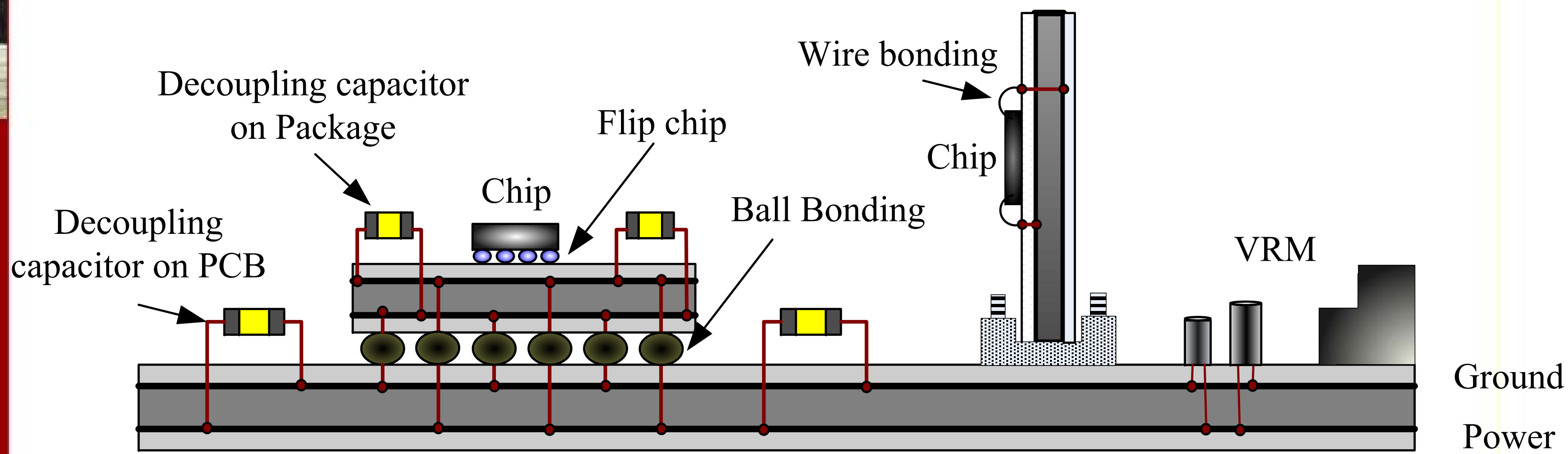
Year	Feature	V_{dd}	Chip Freq.	Power
2007	68nm	1.1V	4.70GHz	189W
2010	45nm	1.0V	5.88GHz	198W
2013	32nm	0.9V	7.34GHz	198W
2016	22nm	0.8V	9.18GHz	198W
2019	16nm	0.7V	11.48GHz	198W

Low voltage

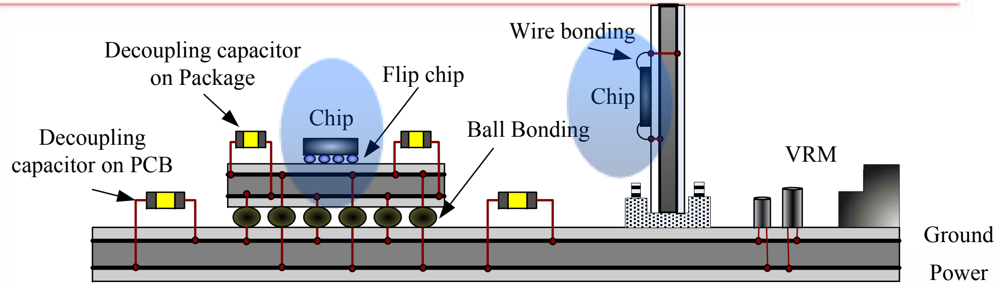
High speed

Power Distribution Network (PDN)

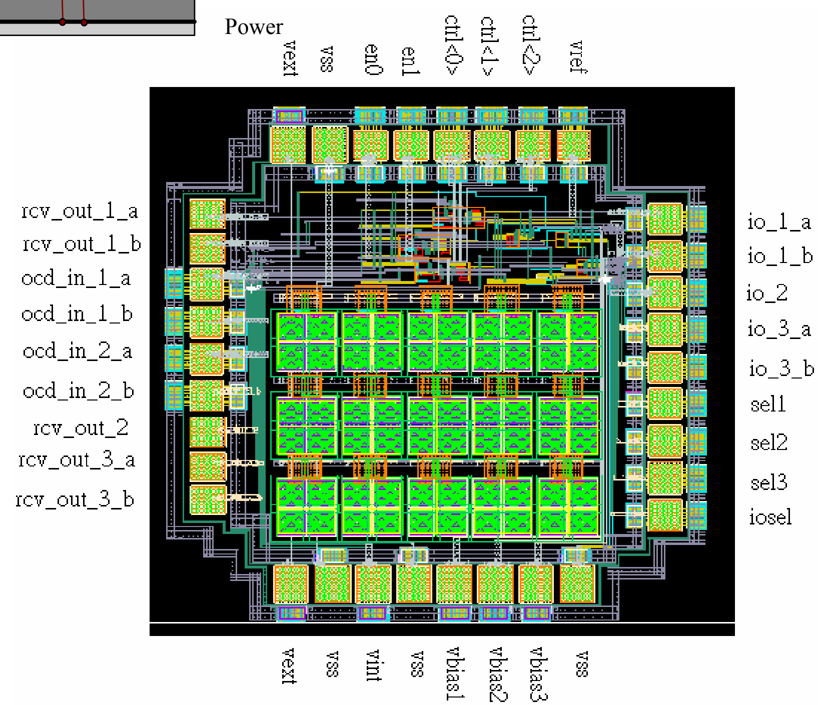
An Electronic System



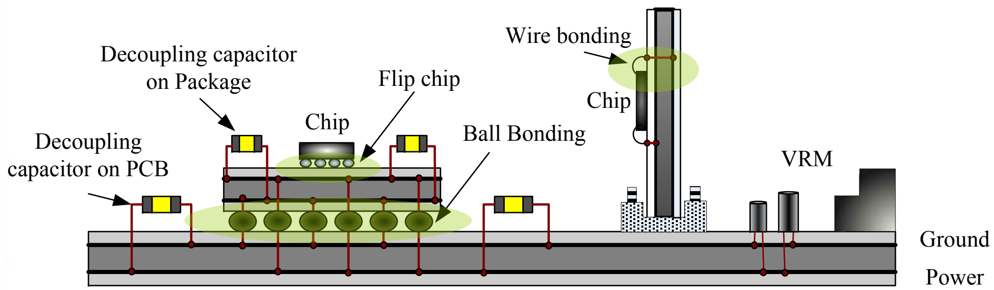
Power Distribution Network (PDN)
Chip Level



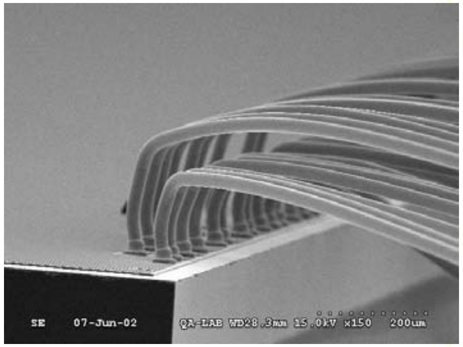
On-chip capacitor
P/G Grids
Interconnects
Pads



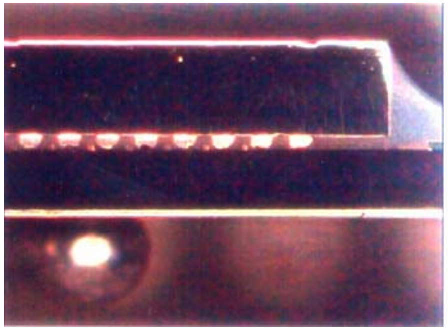
Power Distribution Network (PDN)
interconnects for Chip-PKG-PCB

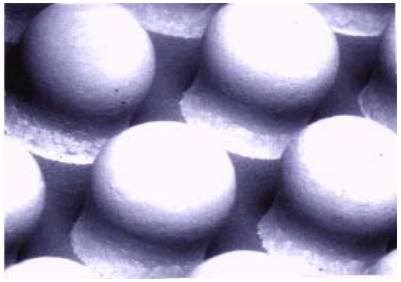


Fine pitch: 50-100um
Line length: 100-200 mil



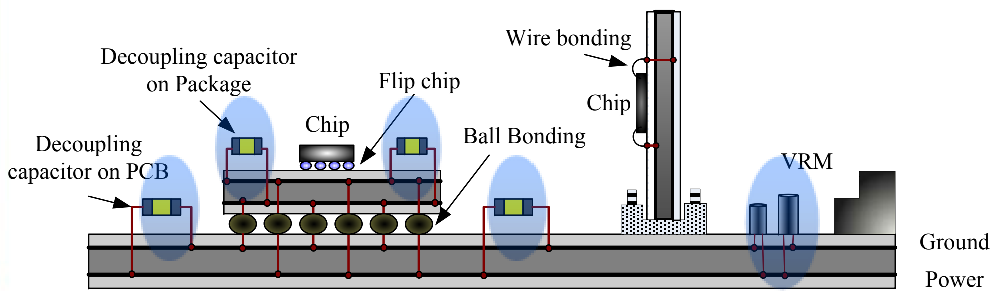
Bump pitch: 100–300um
BGA Ball pitch: 0.5mm – 1mm

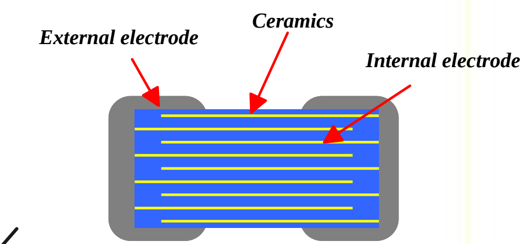




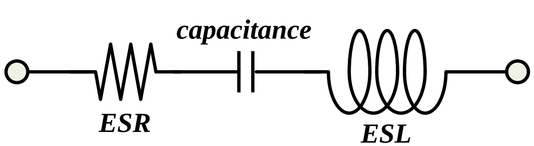
Power Distribution Network (PDN)

decoupling capacitors

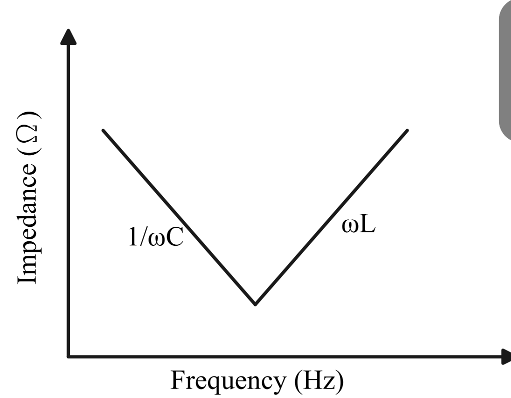




Equivalent capacitor circuit



$$\text{Impedance} = j\omega ESL + \frac{1}{j\omega C} + ESR$$



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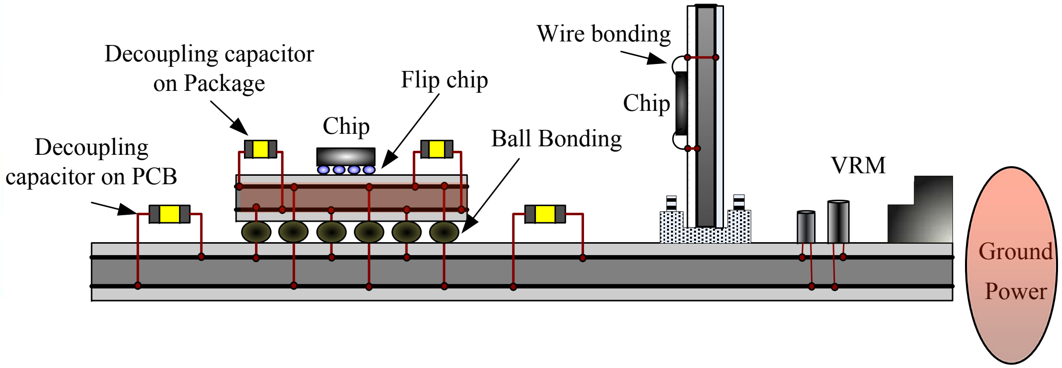
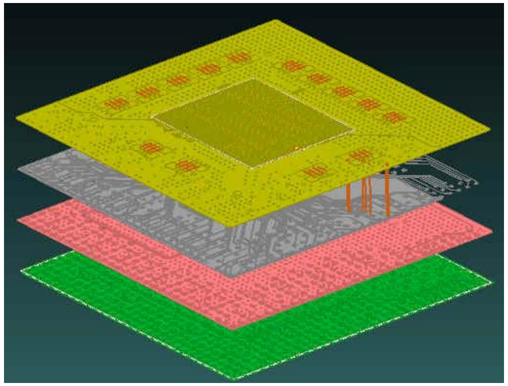
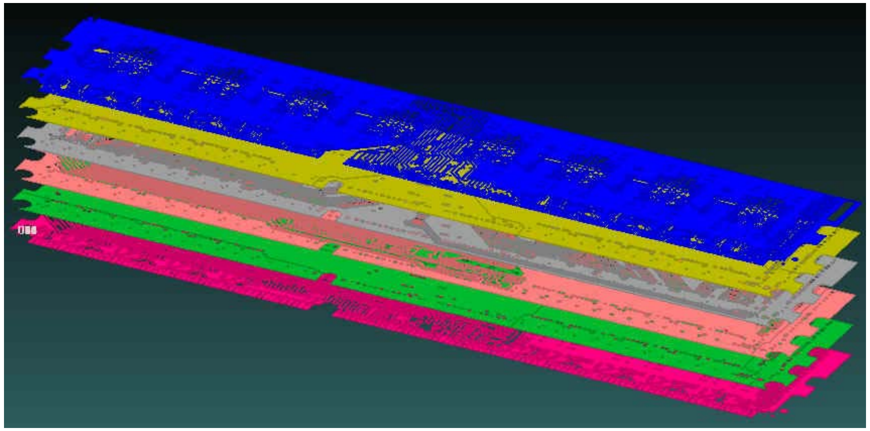
Power Distribution Network (PDN)

PWR/GND Planes

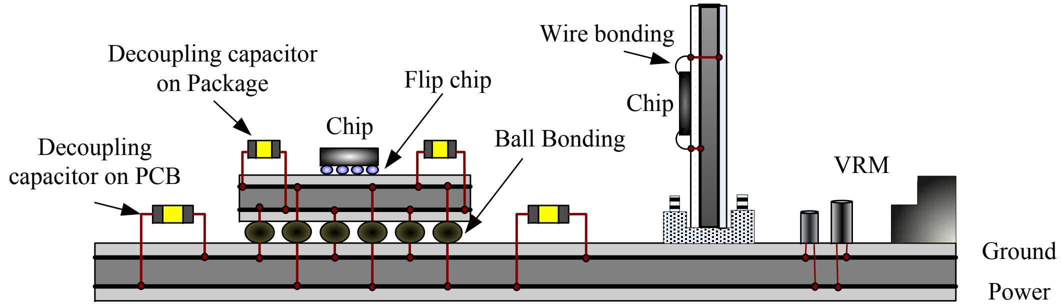


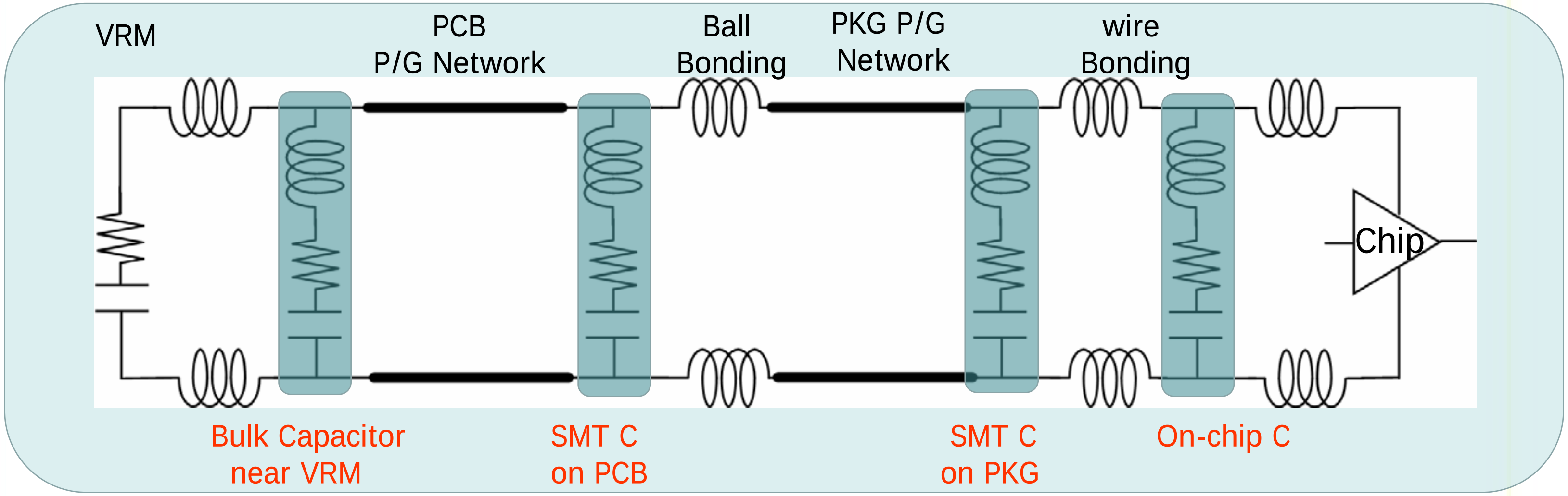




Power Distribution Network (PDN)

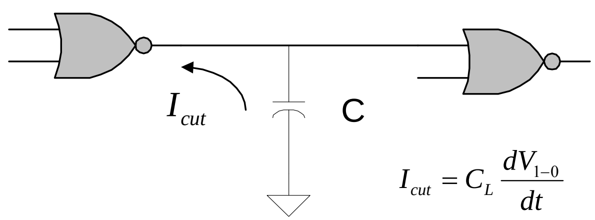
Equivalent Model





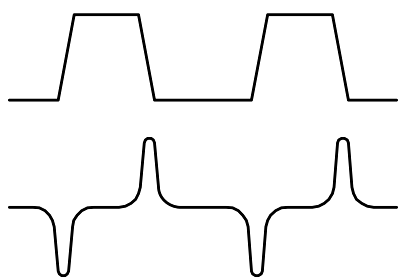
Mechanism of the Power Noise : low-speed view

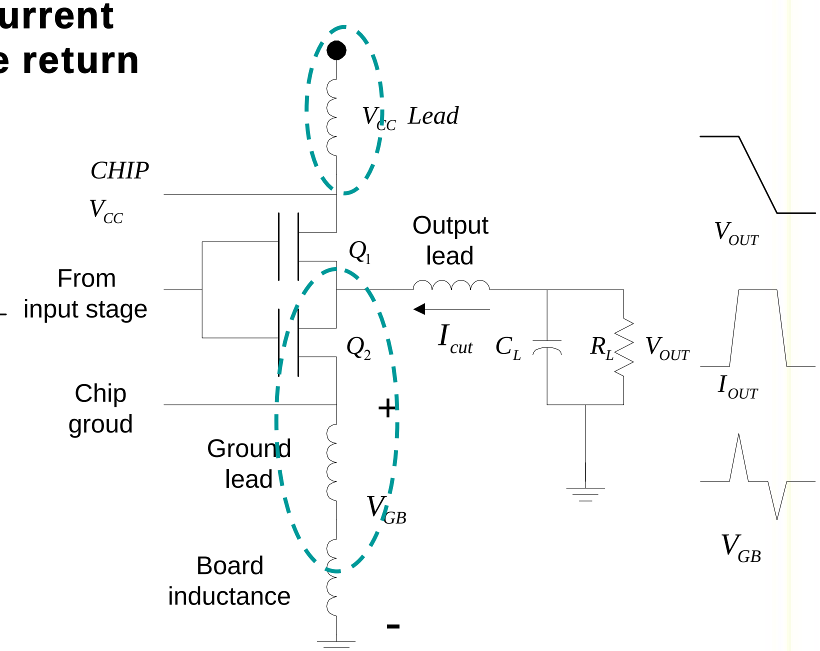
P/G noise arises whenever a changing current flow through the total inductance of the return path



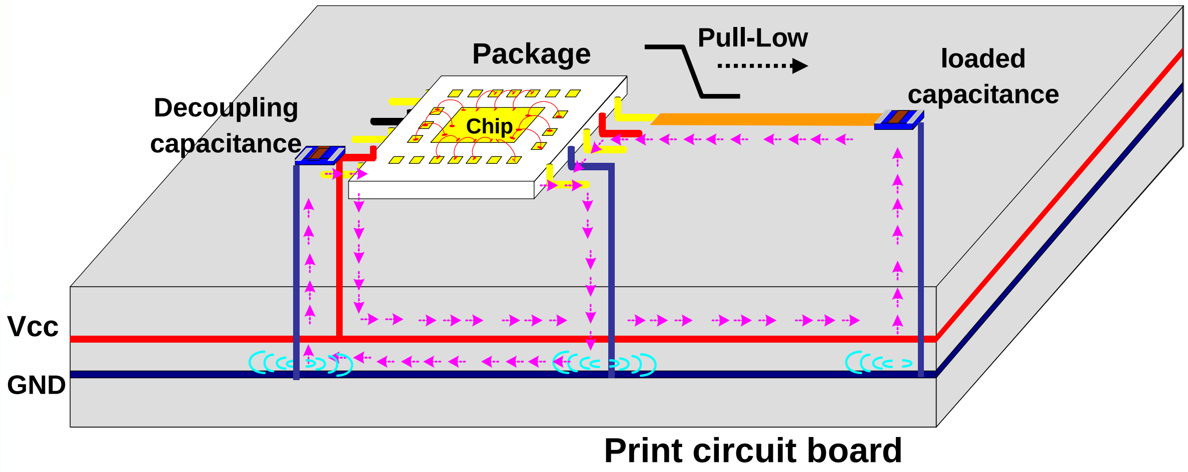
switching voltage

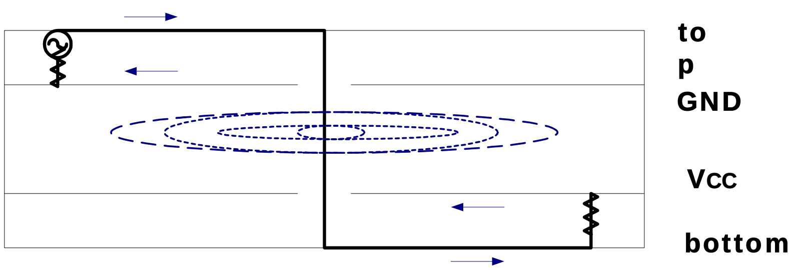
transient current $(\Delta - I \;\; noise)$



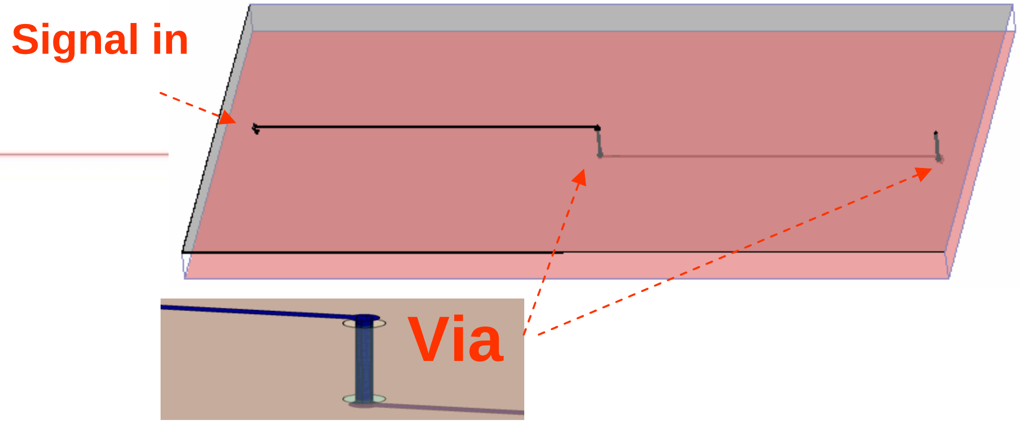


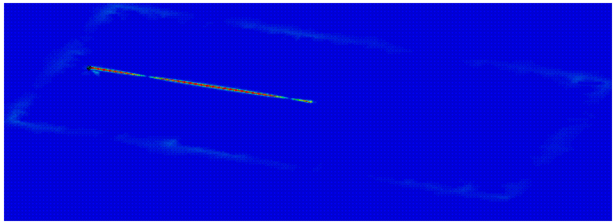
Mechanism of the GBN : high-speed view



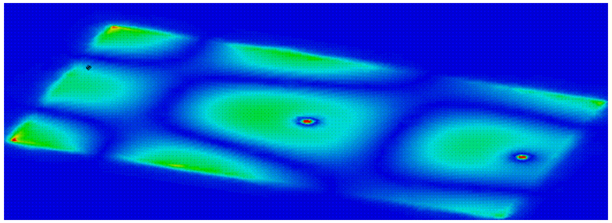


A 4-layer PCB

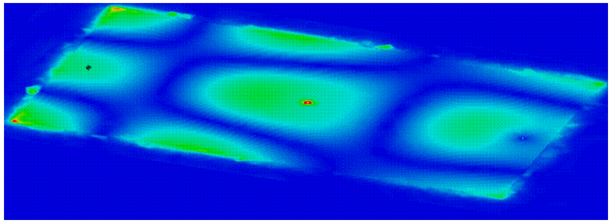




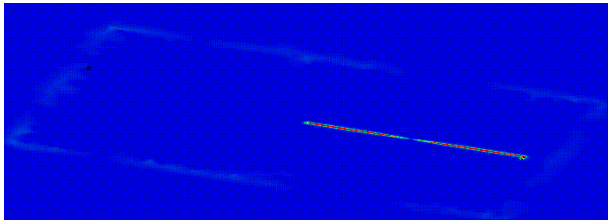
Layer 1



Layer 3

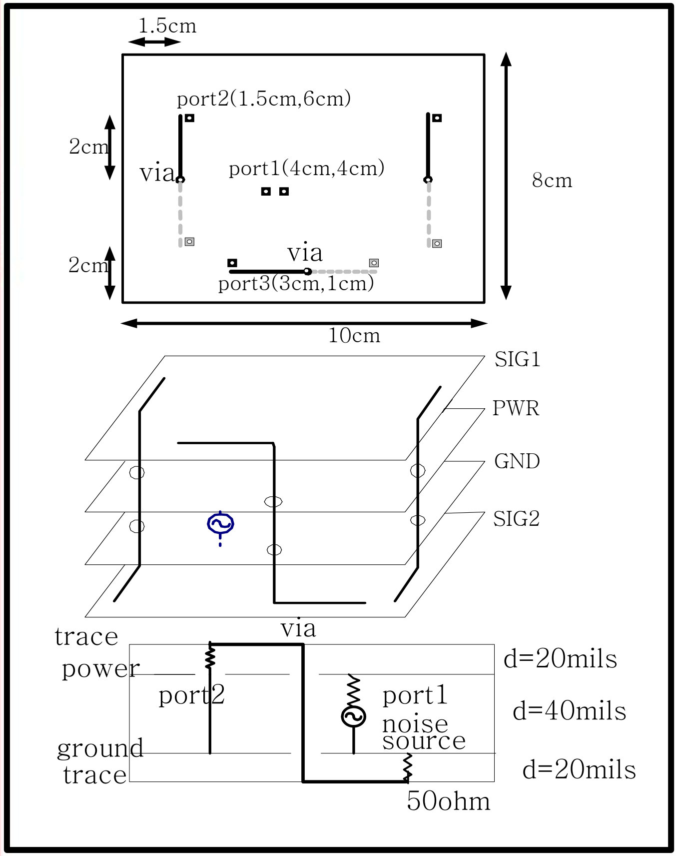


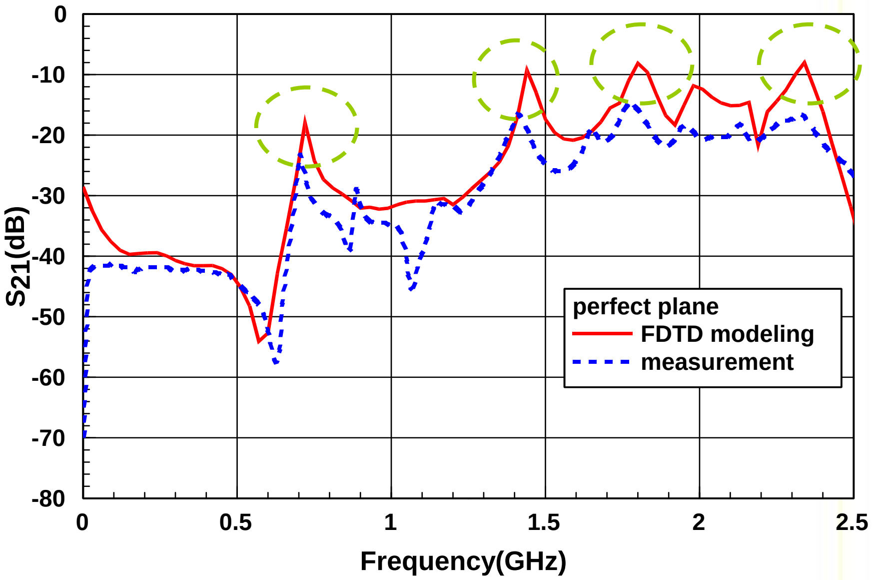
Layer 2



Layer 4

P/GBN Coupling through Via Transition (S_{21})

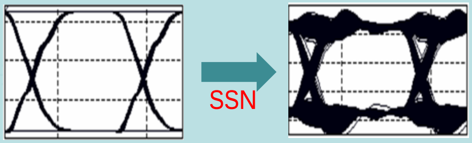




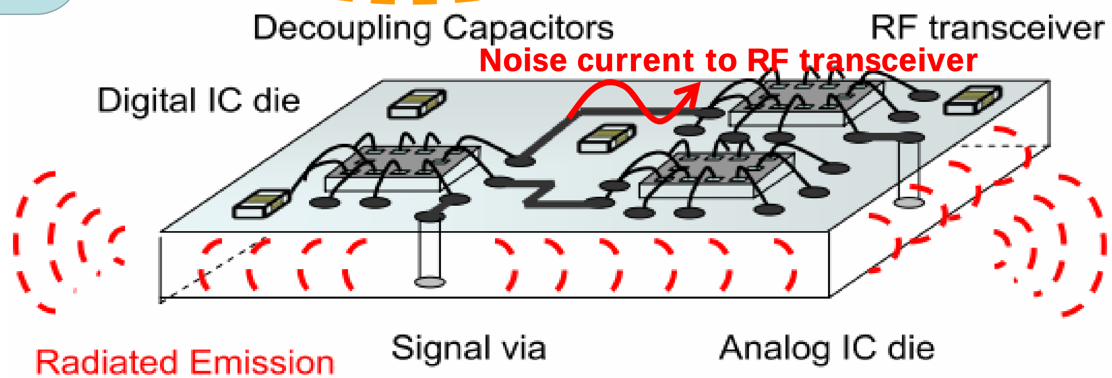
Freq(GHz)	0.72	0.906	1.44	1.706	2.31
mn-mode	1,0	0,1	2,0	2,1	2,2

Issues caused by power noise

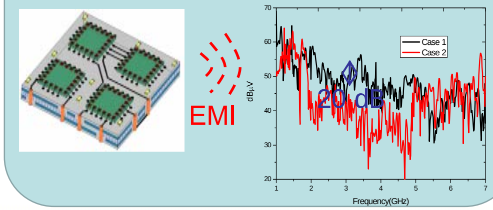
Signal Integrity Issues



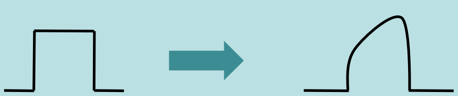
Jitter, Skew
Crosstalk
Eye width/height



EMI Issue



RFI Issues
RF sensitivity



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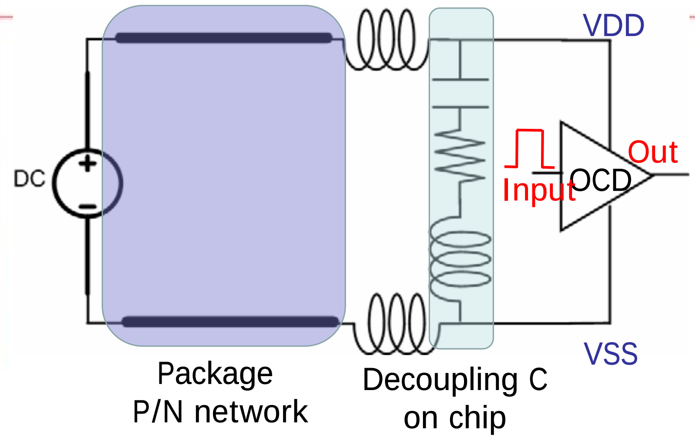
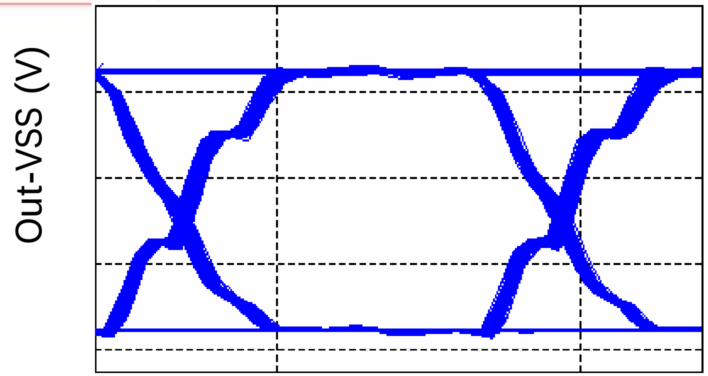
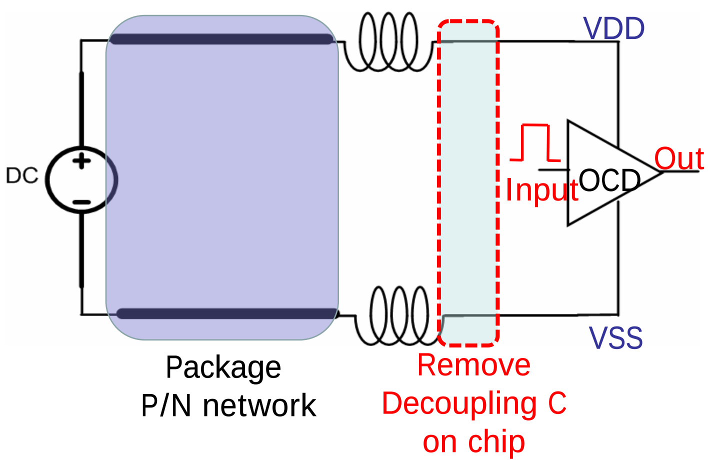
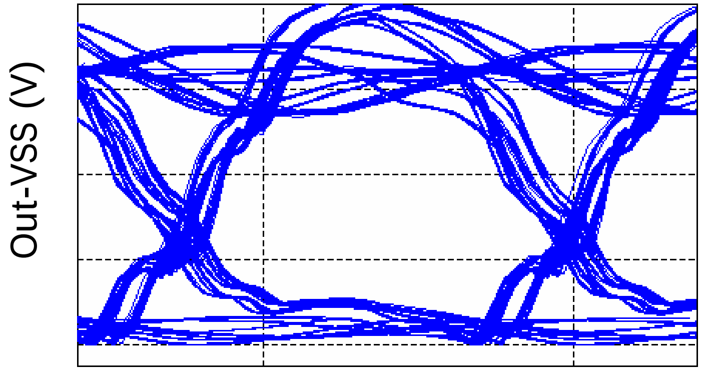
Example of signal integrity issues









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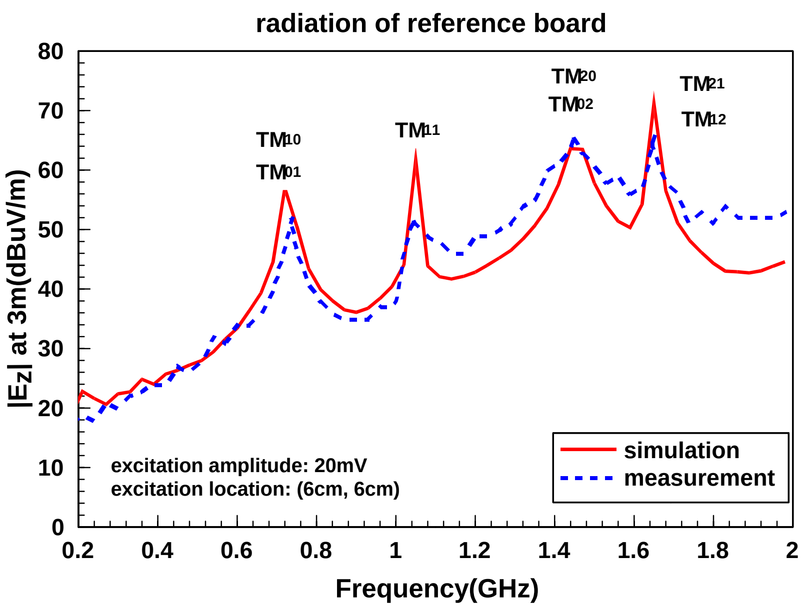
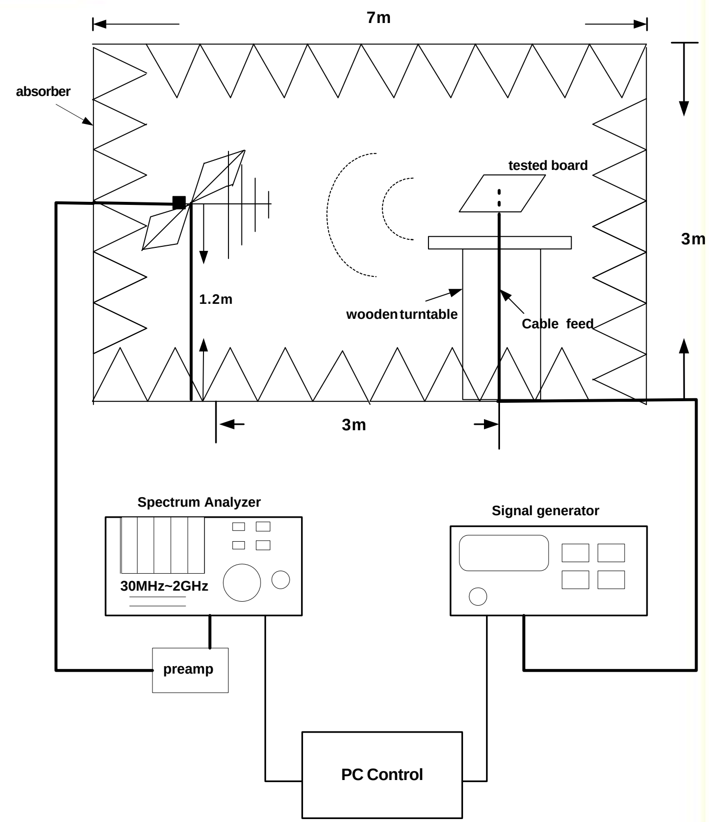
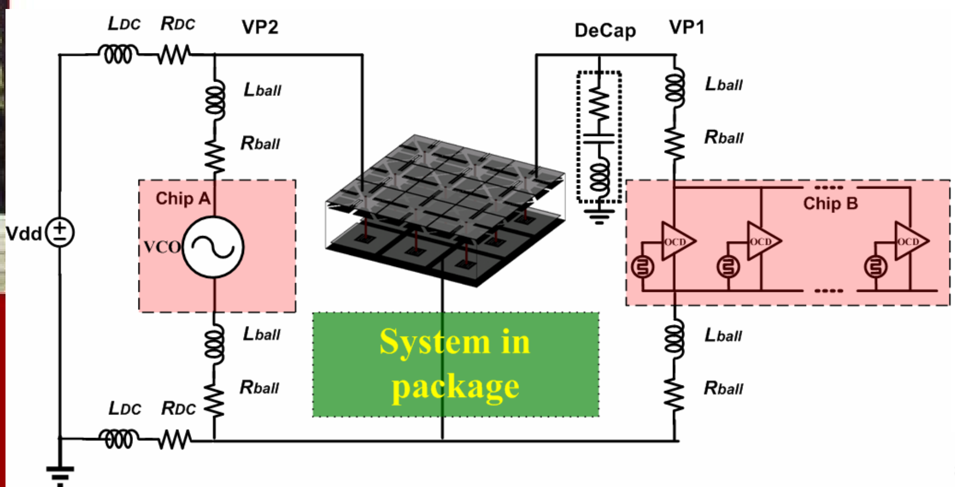
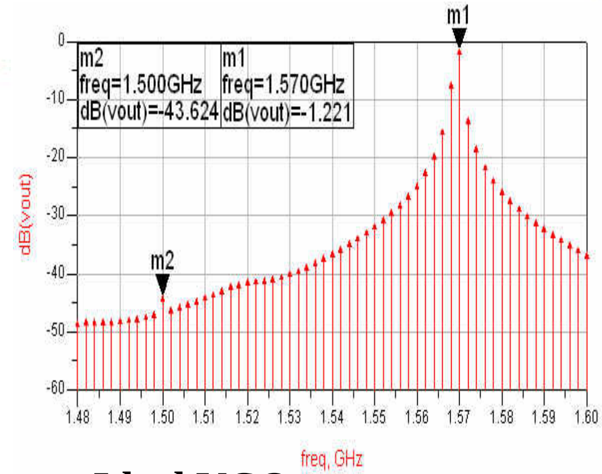
Example of EMI Issues





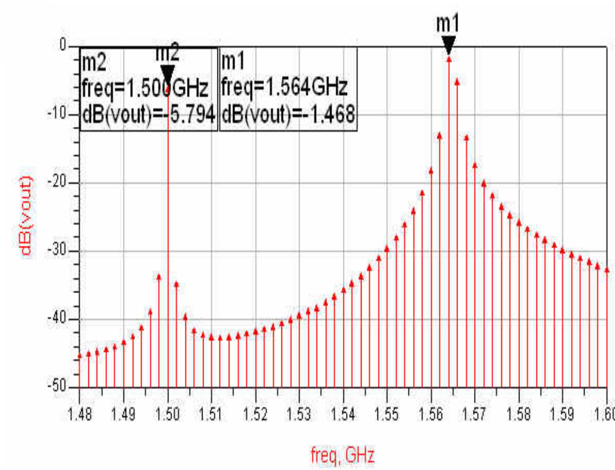
Example of RFI Issues



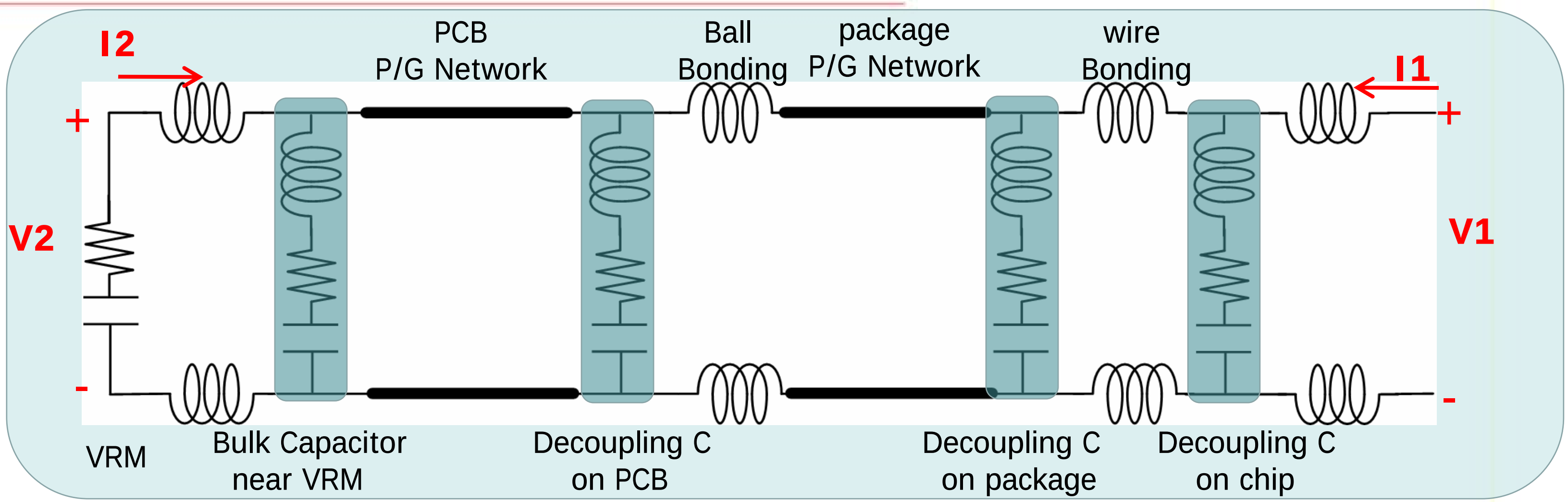


<u>Ideal VCO</u>

<u>VCO's performance is affected by power noise</u>



Quantification of Power Noise: Z parameter



$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} \times \begin{bmatrix} I_1 \\ I_2 \end{bmatrix}$$

$$Z_{11} = \frac{V_1}{I_1} \text{ (Port 2 open)}$$

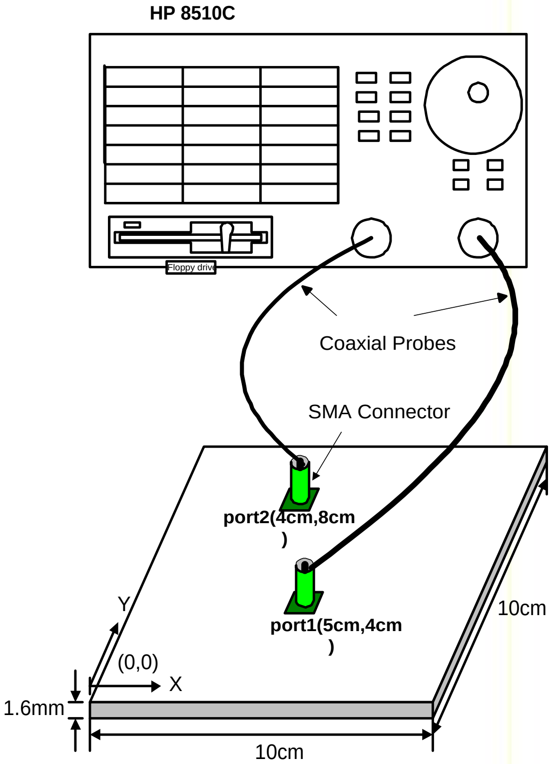
$$Z_{21} = \frac{V_2}{I_1} \text{ (Port 2 open)}$$

PDN Design:

Lower Z_{11} (Target impedance)
Lower Z_{21}

Measurement of PDN Impedance

Z-parameter and S-parameters



Transfer impedance

$$Z_{21} = Z_0 \frac{2S_{21}}{(1-S_{11})(1-S_{22}) - S_{12}S_{21}}$$

Assume

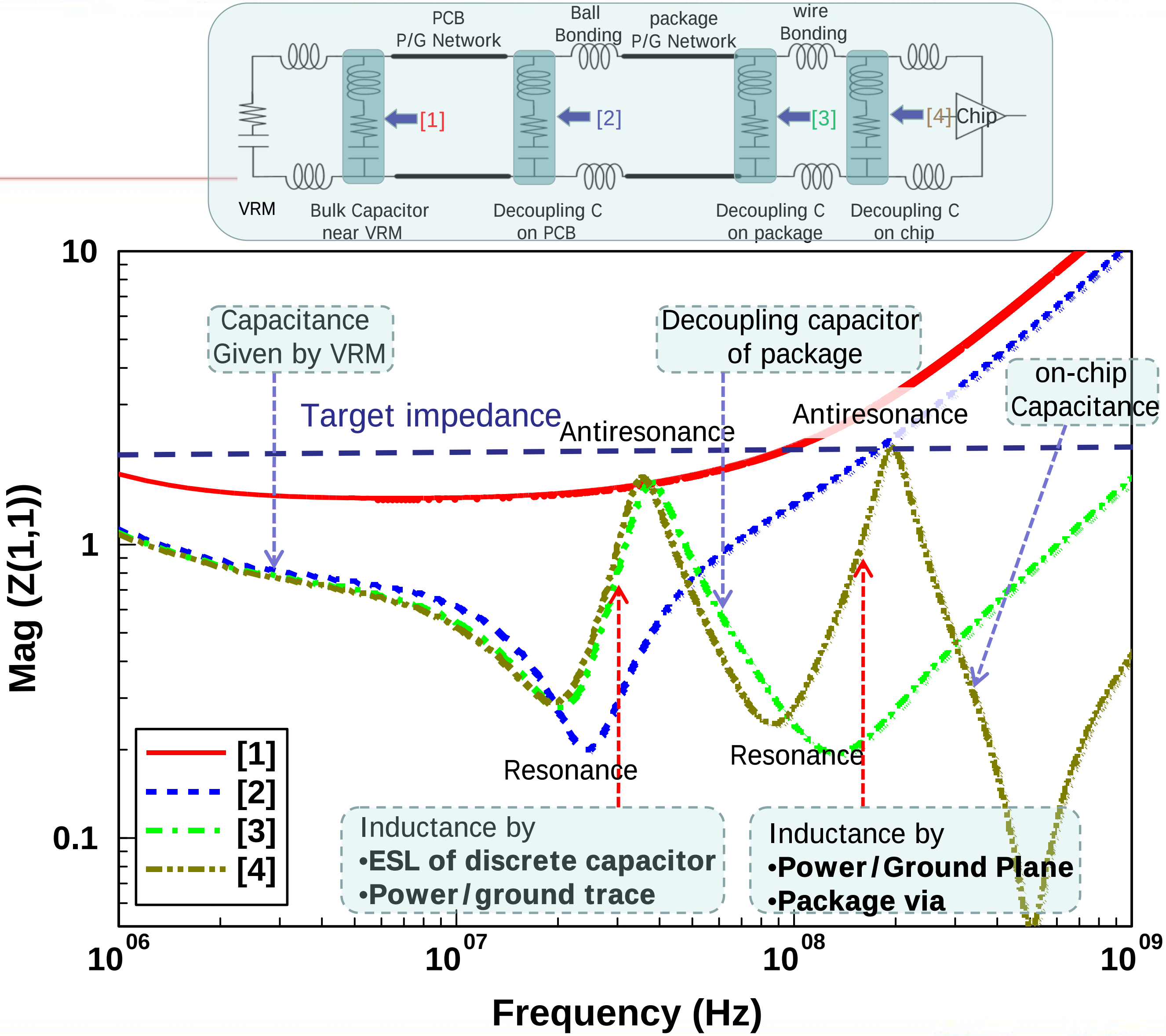
$$S_{11} \approx S_{22} \simeq -1 \quad \text{(Low impedance PDN)}$$

$$S_{12} \cdot S_{21} \simeq 0, Z_0 = 50\Omega$$

$$\Rightarrow \quad Z_{21} \approx 25 \cdot S_{21}$$

Self impedance: (two probes are very close)

$$Z_{11} = \frac{Z_0}{2} \frac{S_{21}}{1-S_{21}} \Rightarrow Z_{11} \approx 25 \cdot S_{21} \quad (\text{assume } S_{21} \ll 1)$$



PCB
P/G Network
Ball
Bonding
package
P/G Network
wire
Bonding
[1]
[2]
[3]
[4]
Chip
VRM
Bulk Capacitor
near VRM
Decoupling C
on PCB
Decoupling C
on package
Decoupling C
on chip
10
1
0.1
Mag (Z(1,1))
Capacitance
Given by VRM
Decoupling capacitor
of package
on-chip
Capacitance
Target impedance
Antiresonance
Antiresonance
Resonance
Resonance
[1]
[2]
[3]
[4]
Inductance by
•ESL of discrete capacitor
•Power/ground trace
Inductance by
•Power/Ground Plane
•Package via
10^06
10^07
10^08
10^09
Frequency (Hz)

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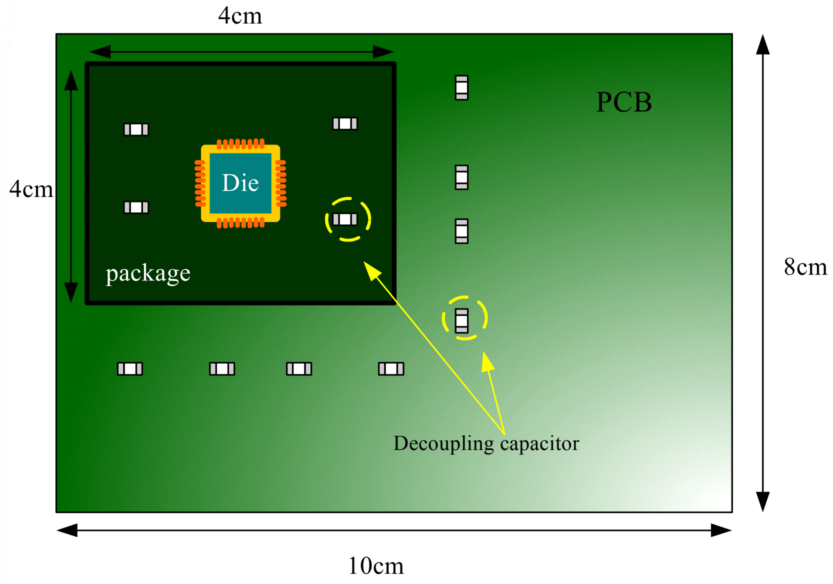
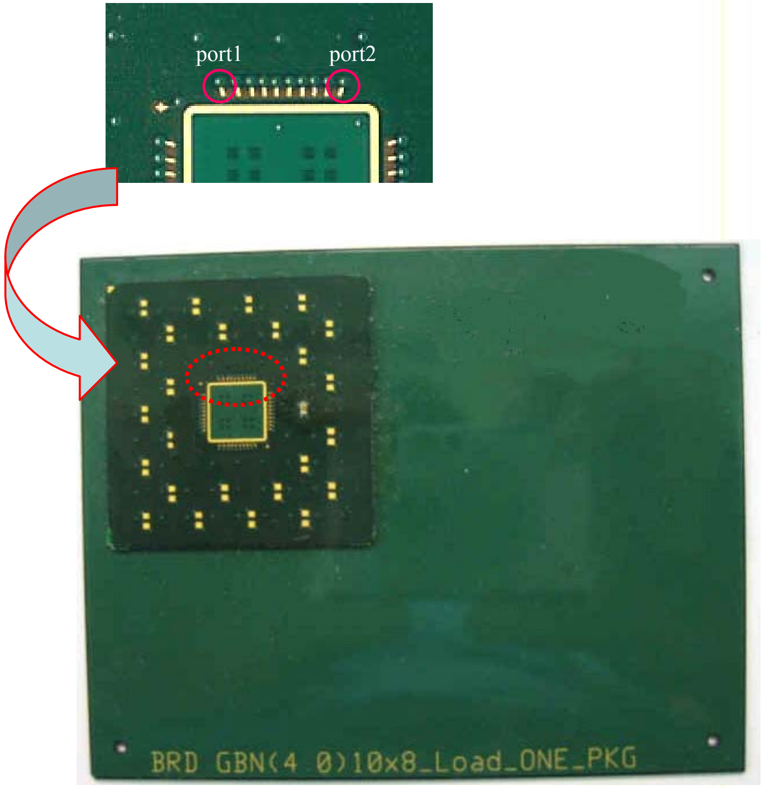
Power/Ground Planes

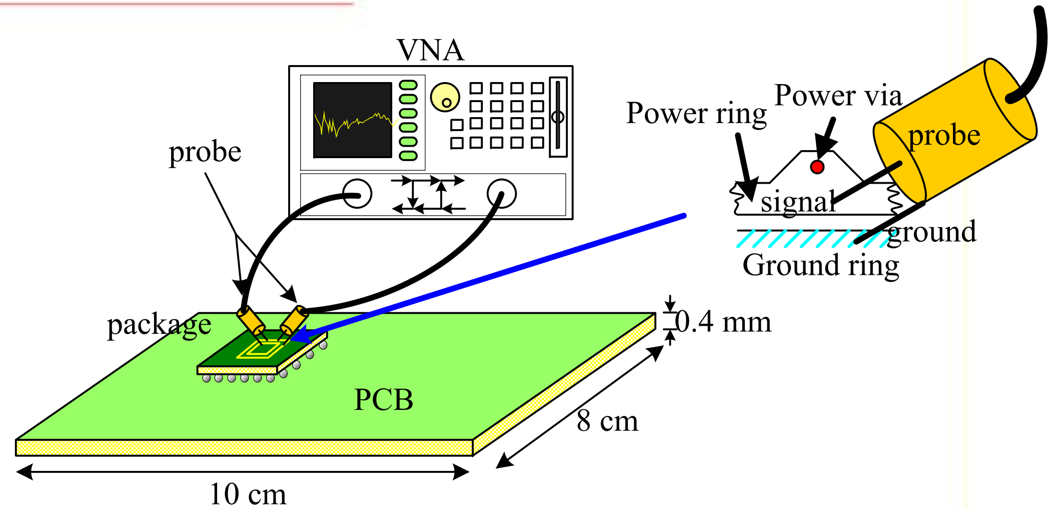
A Test Sample

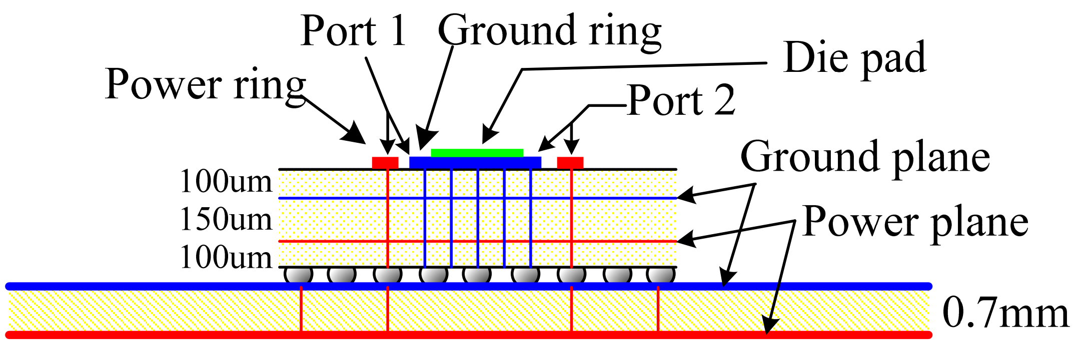




Power/Ground Planes

Measurement setup

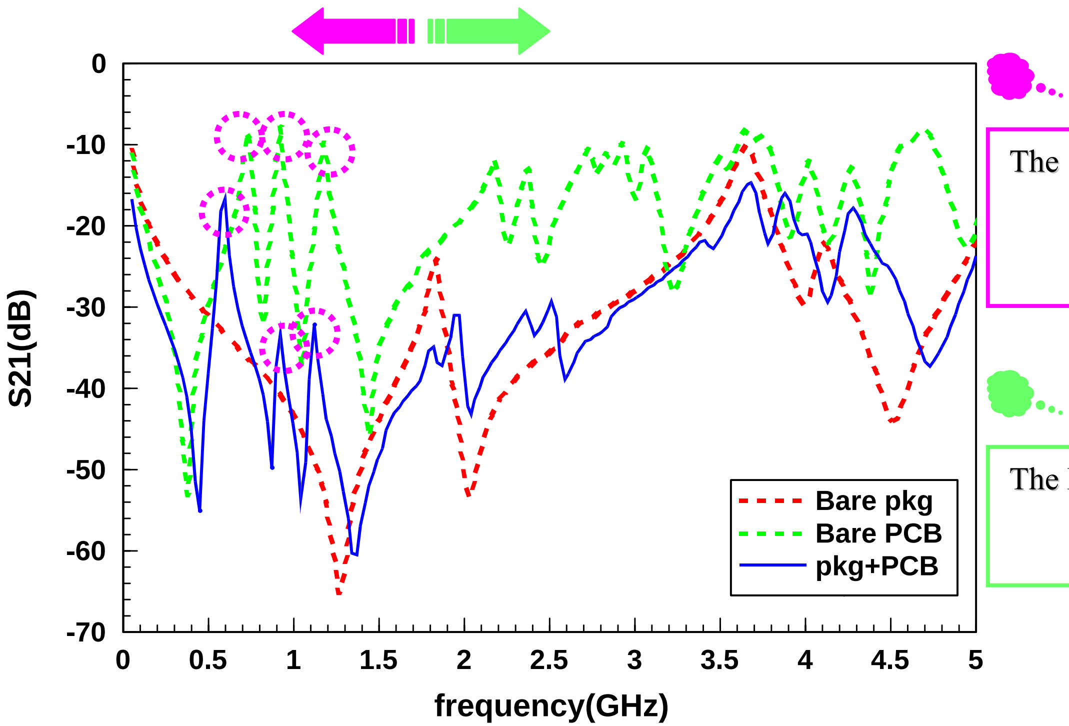




Power/Ground Planes

Coupling between PKG and PCB

Measurement Results



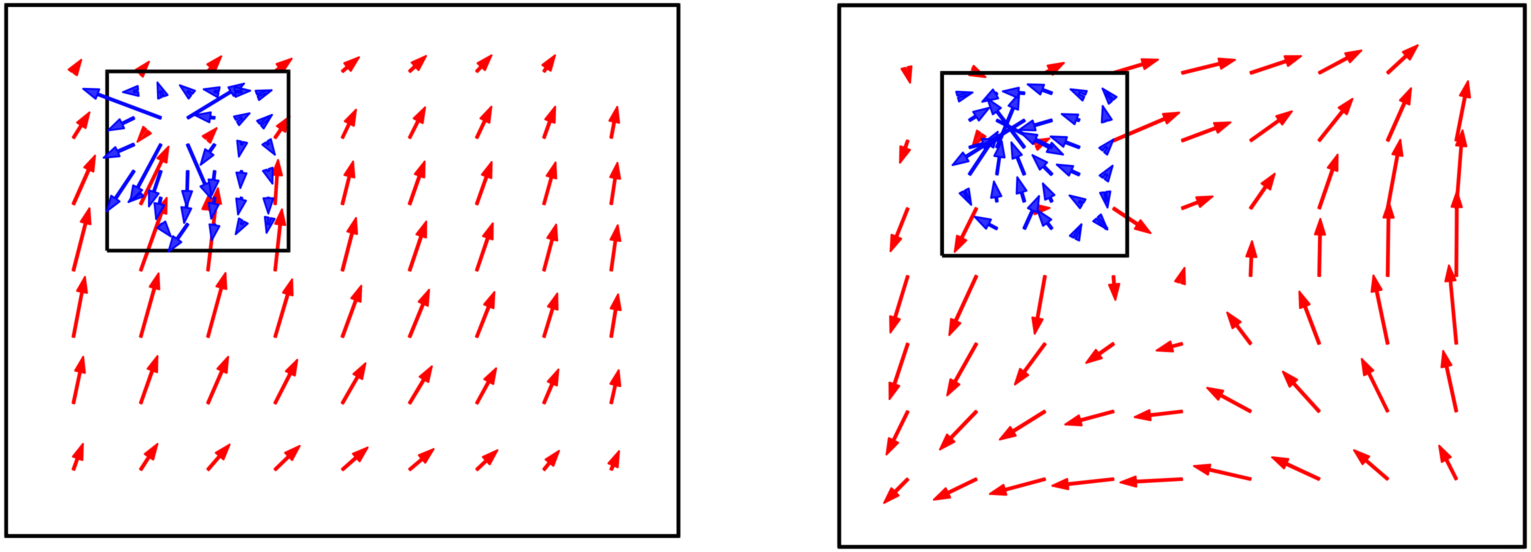
The SSN could be magnified by the interaction of these two cavities and degrades the power integrity of the packaged integrated circuits.

The PDS behavior of combining the package and PCB is similar to that of considering only the package.

Sin-Ting Chen, Ting-Kuang Wang, Chi-Wei Tsai, Sung-Moa Wu, James L. Drewniak, Tzong-Lin Wu, "Modeling Noise Coupling Between Package and PCB Power/Ground Planes with an Efficient 2D-FDTD/Lumped Element Method", IEEE Transaction on Advanced Packaging, Vol. 30, No. 4, pp. 864 – pp. 871, Nov. 2007.

Power/Ground Planes

Cavity resonance



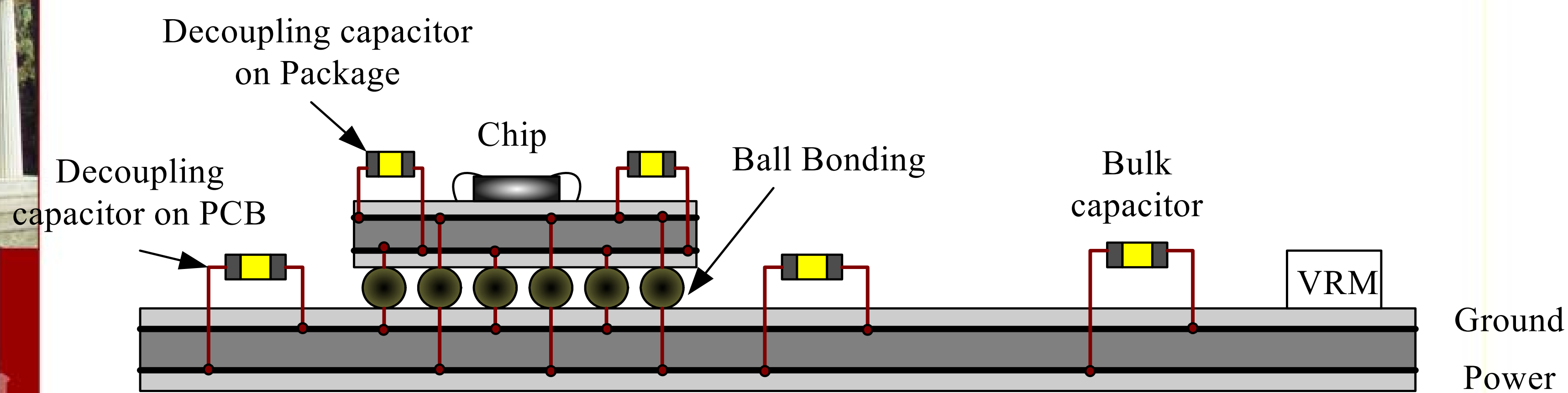
900 MHz

TM_{10}

1.1GHz

TM_{11}

SMT Capacitors

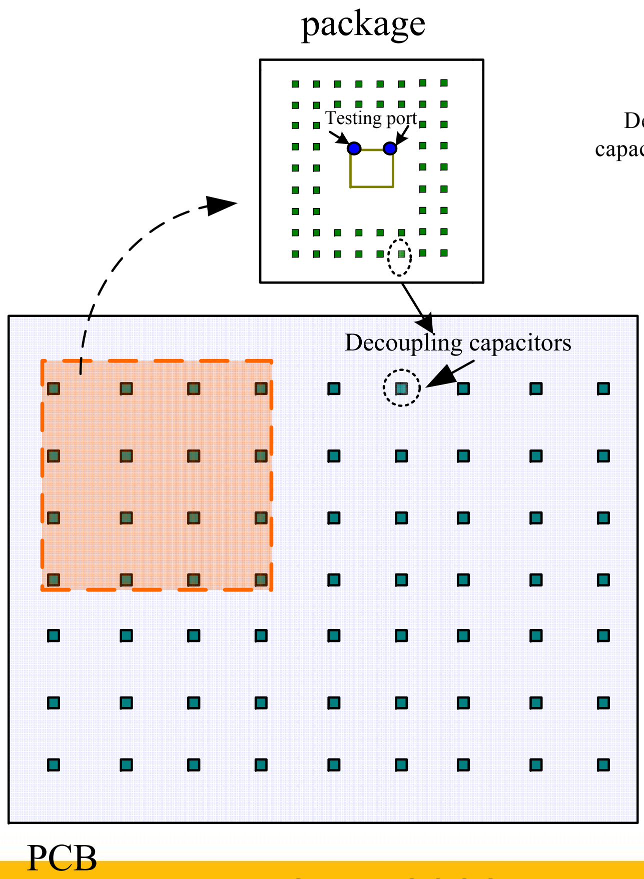


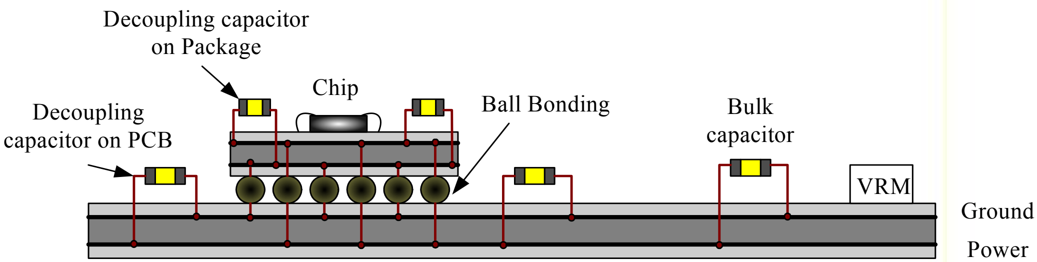
Design Question?

- Locations?
- Numbers?
- Values?

SMT Decoupling Capacitors

Capacitors placed either on Package or PCB

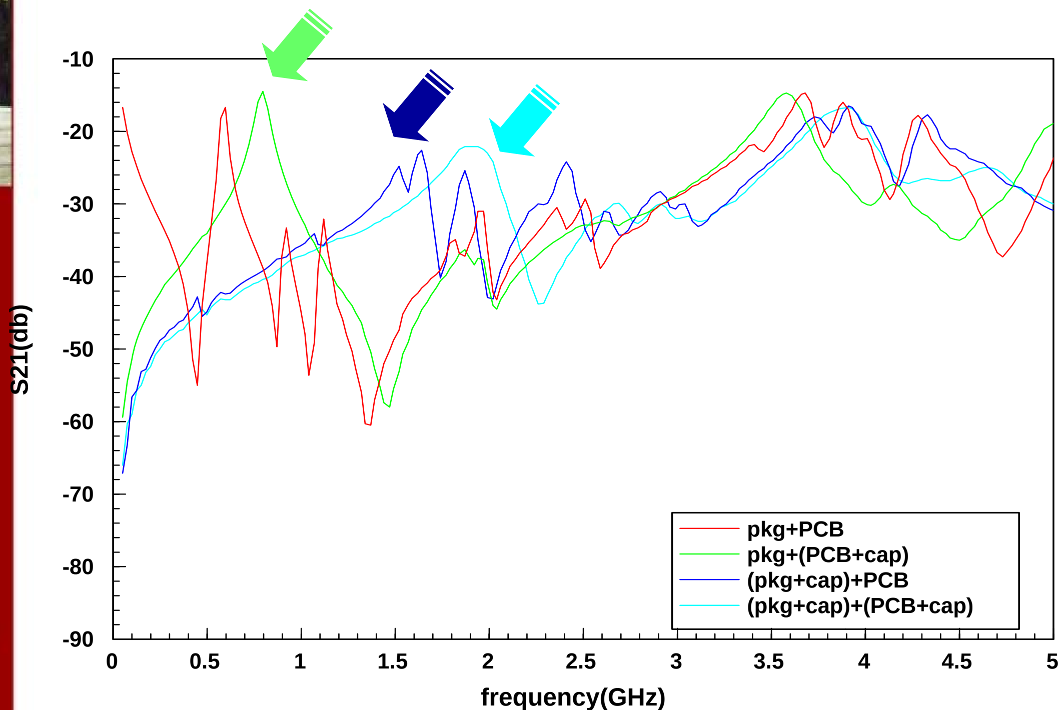




- 52 capacitors on package
- 63 capacitors on PCB
- Capacitance : 100 nF
- ESR : 0.04ohm ESL :0.63nH

SMT Decoupling Capacitors for Suppressing the P/GBN

Capacitors placed either on Package or PCB

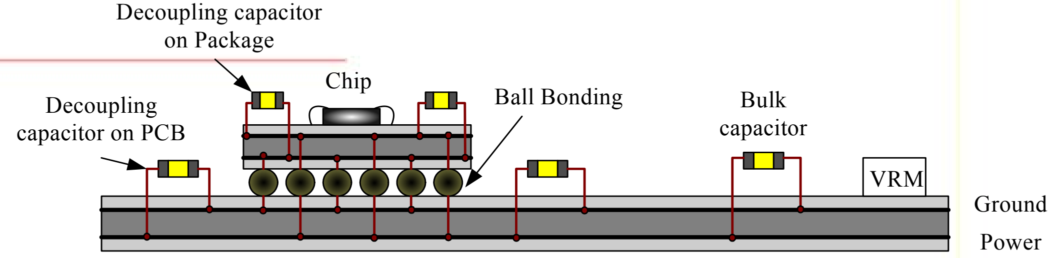


The additional resonance peak worsens the PDN performance.

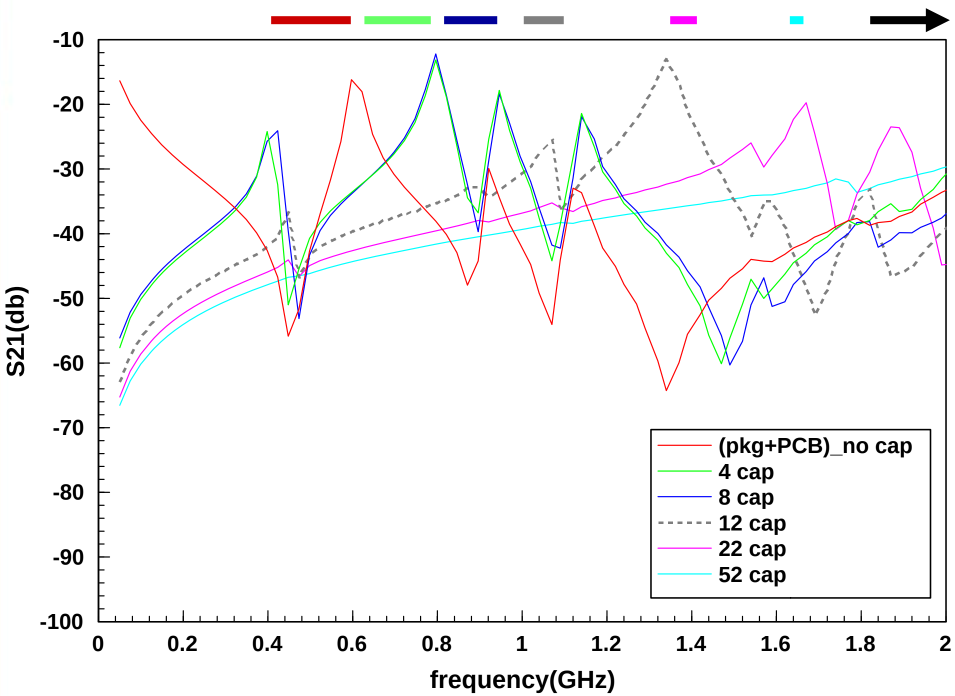
Decoupling capacitors placed on package have better performance.

The behavior of the PDN is similar to that with the caps mounted on the package.

SMT Decoupling Capacitors



Capacitors Number Effect



With increasing the number of decoupling capacitors, the peaks move to higher frequency and their magnitude become smaller.

C:100nF (on Package)

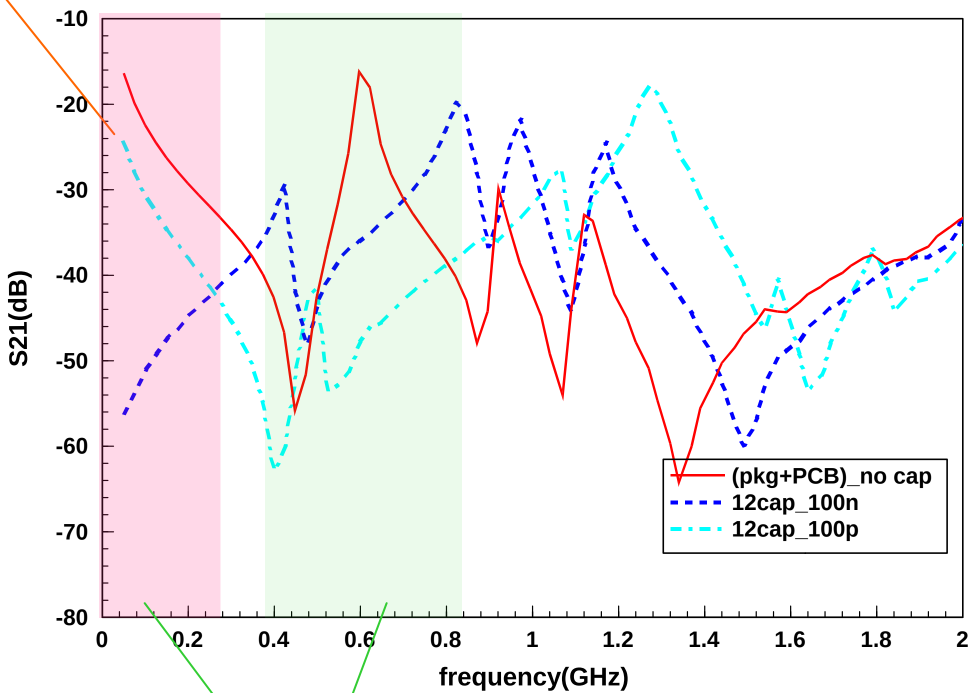
ESR:0.04ohm

ESL:0.63nH

SMT Decoupling Capacitors

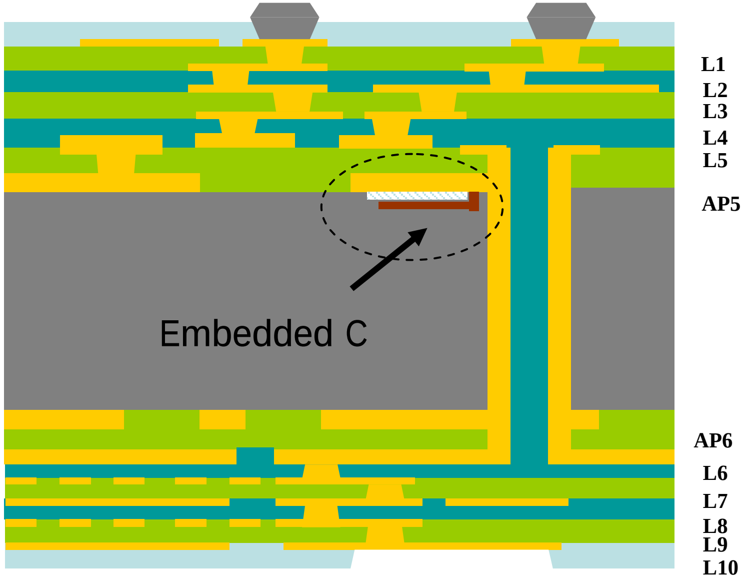
Capacitance value Effect

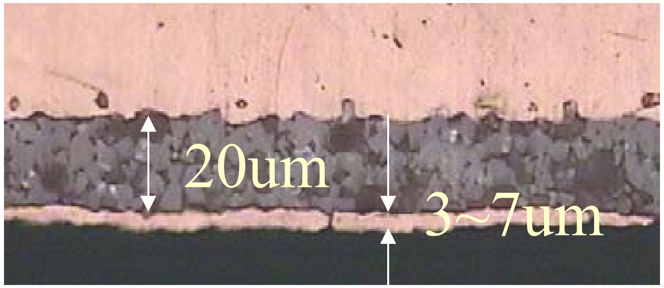
100nF capacitors have better performance to reduce noise at low frequency.



100pF capacitors have better performance at higher frequency. At low frequency, the capacitors can reduce noise about 8 dB.

Embedded Capacitor

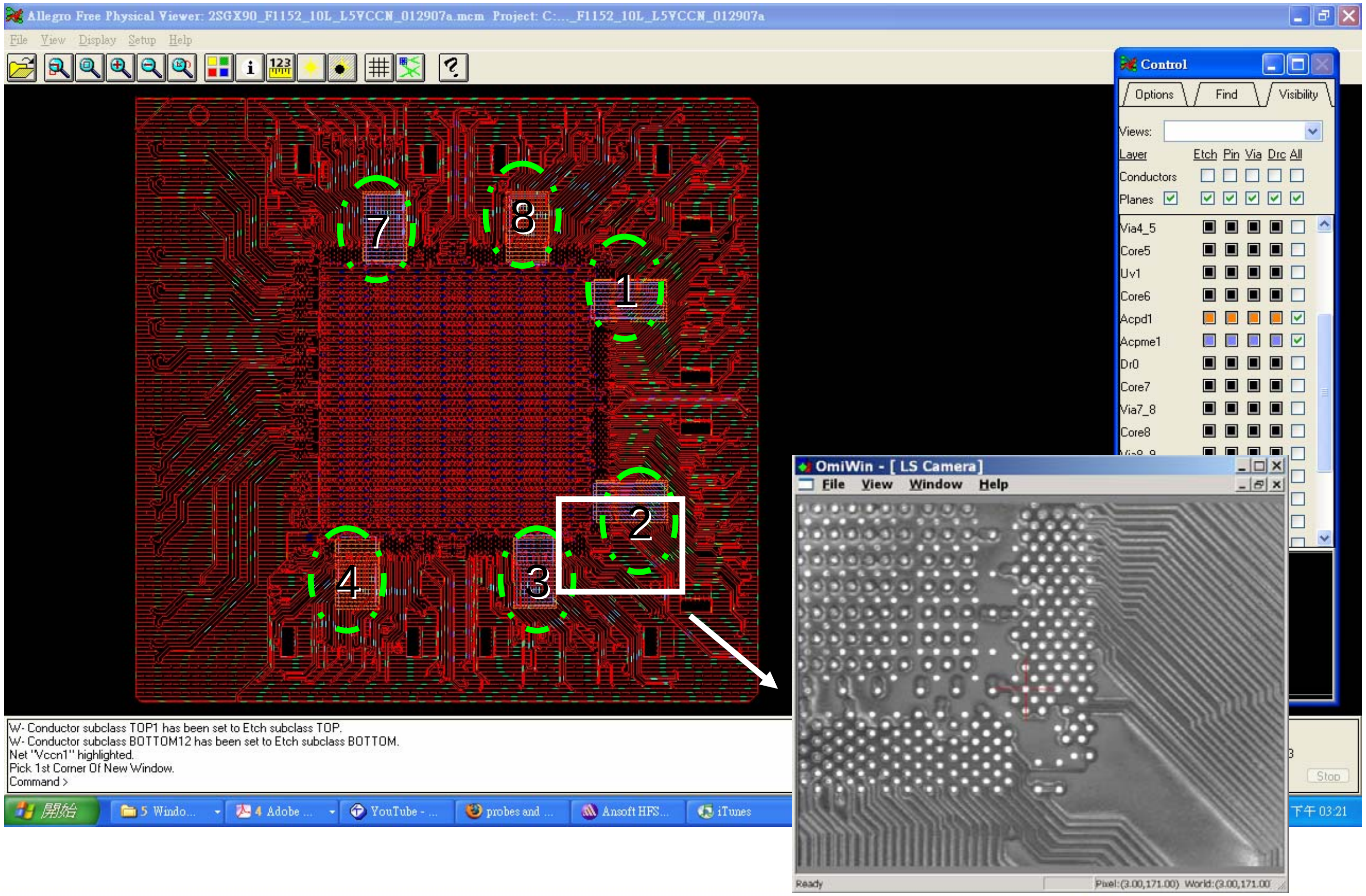




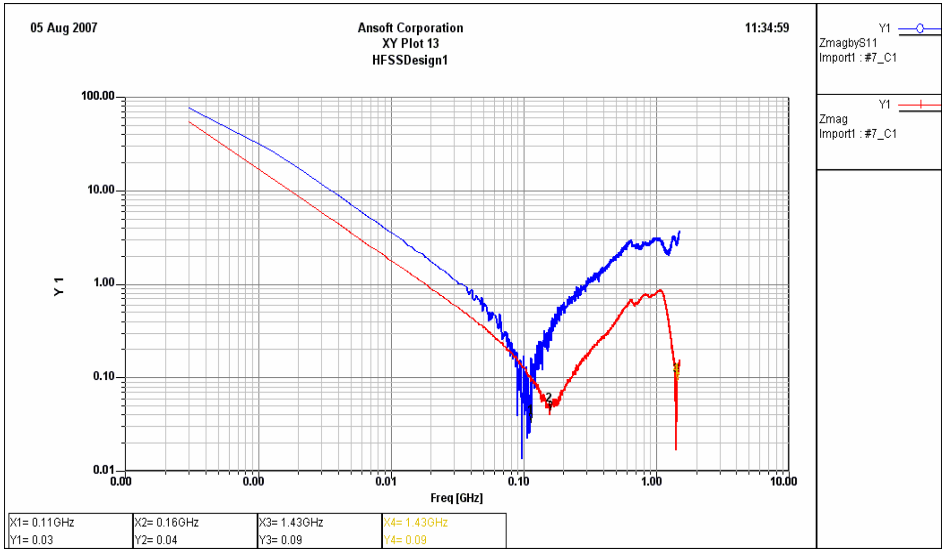
Embedded Capacitor Properties:

Dk (10kHz): 3000
Capacitance Density: 1.0 nF/mm^2
thickness: 20- 30 um
Cu Electrode thickness: 5~7um

Caps location



Impedance measurement



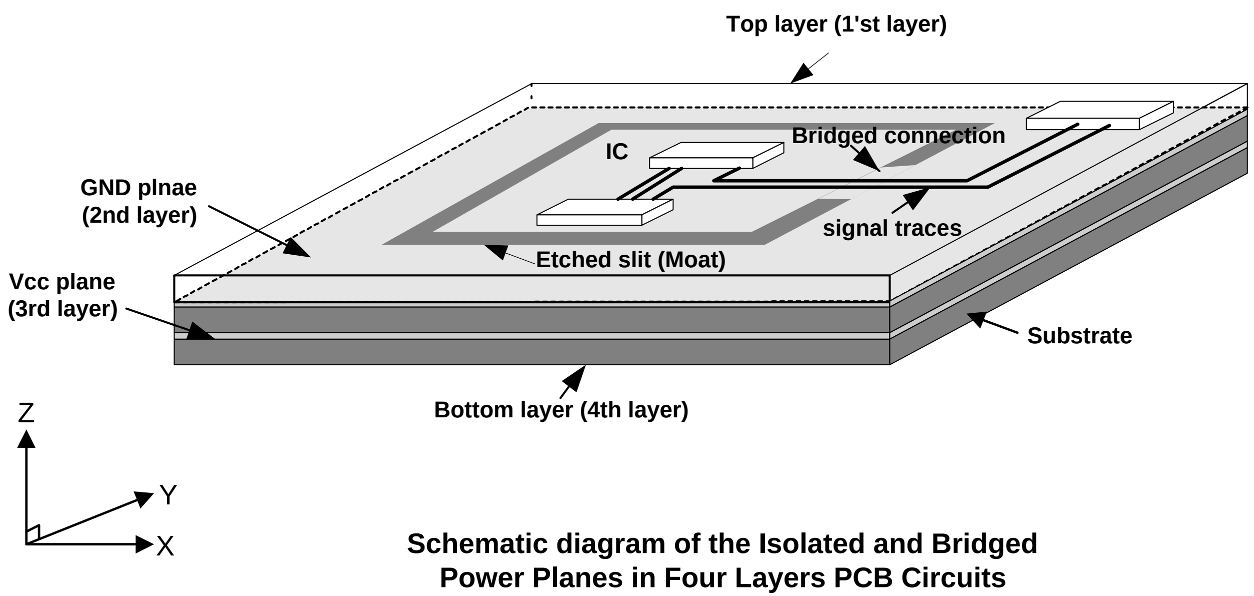
Good capacitor is seen below SRF.

SRF is in the several MHz range
due to large ESL of the connecting vias.

The bandwidth could be enhanced by designing the capacitor closer to the surface of the package.

	Cap (nF)	ESL (pH)	SRF (MHz)
Cap4	8.87	214	115.6

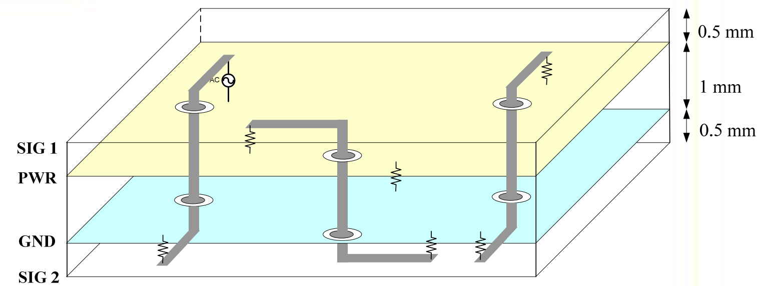
Isolation by etched slot with bridges



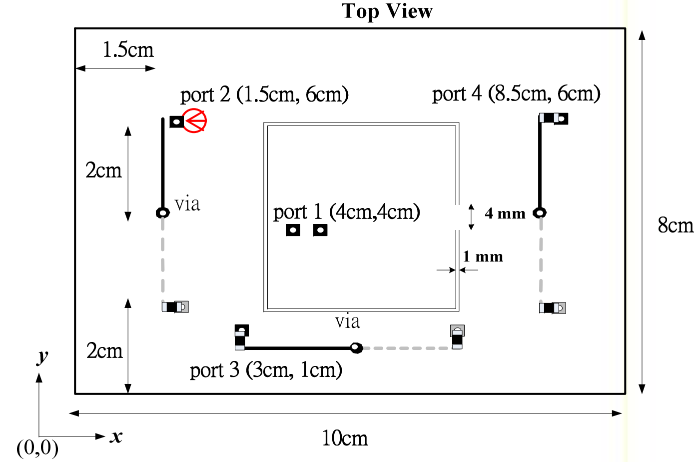
Schematic diagram of the Isolated and Bridged Power Planes in Four Layers PCB Circuits

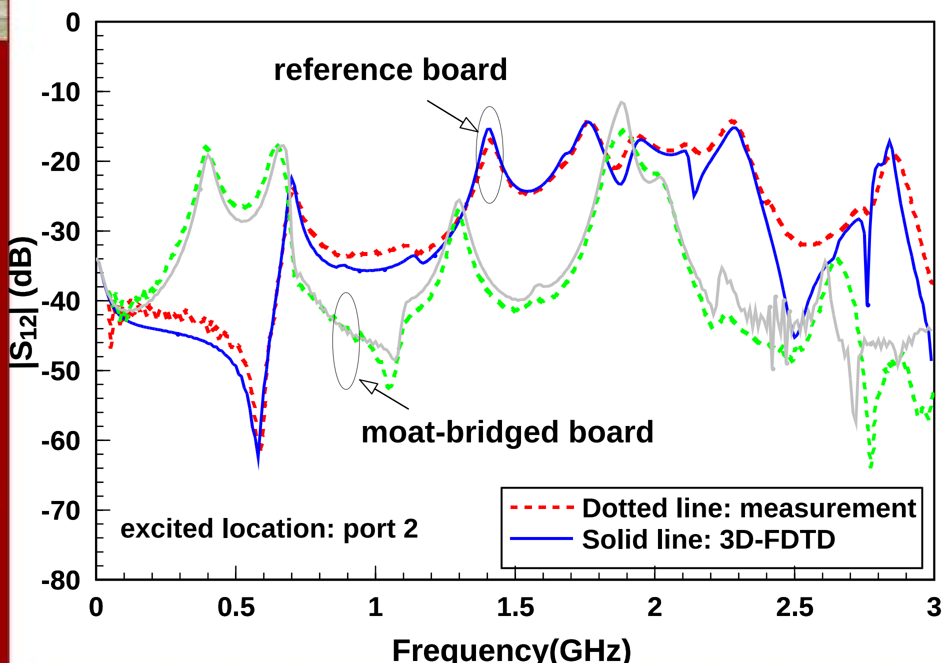
Isolation slots with bridge

3D View



Top View





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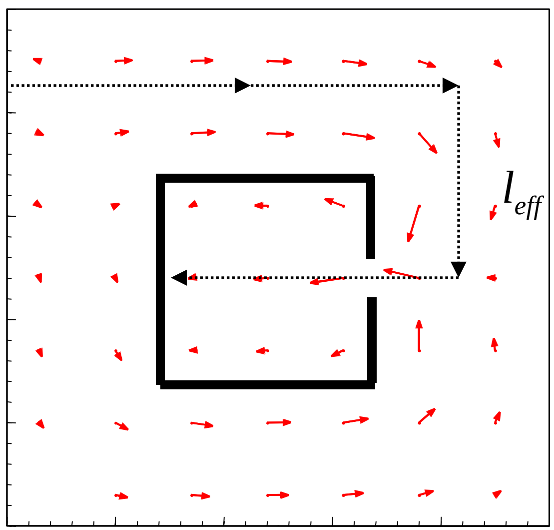
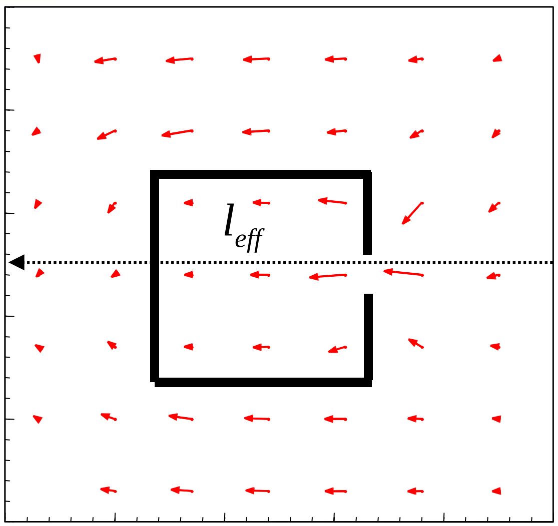
NTU National Taiwan University

Isolation by etched slot with bridge

(P/G Noise of the bridged board)



TM10-like



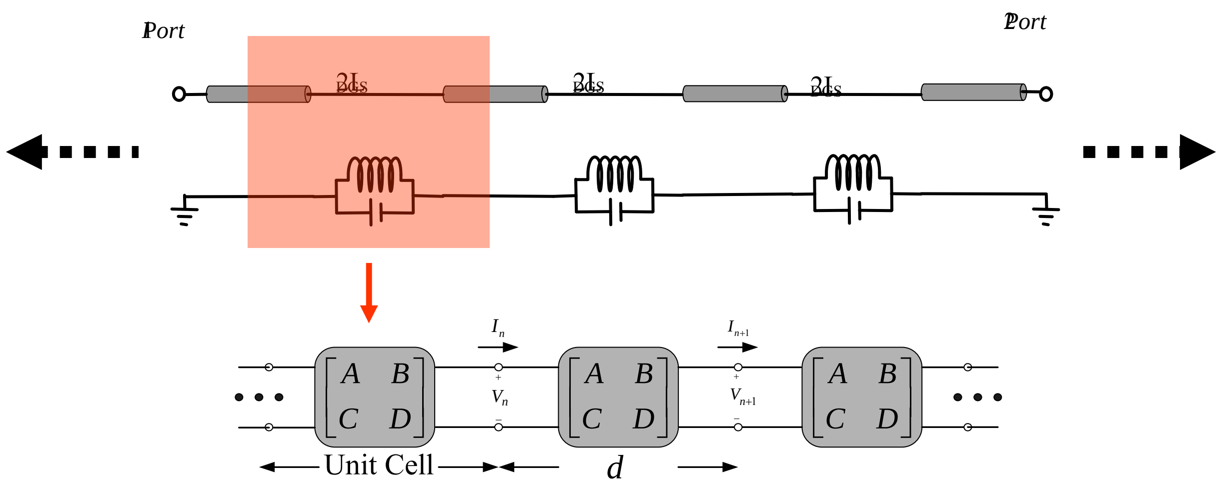
TM10

J. N. Hwang and T. L. Wu,"The Bridging Effect of the Isolation Moat on the EMI Caused by Ground Bounce Noise between Power/Ground planes of PCB,"*2001 IEEE EMC Symposium*, Montreal, Canada, Vol. 1, pp. 471 -474, Aug. 2001.

T. L. Wu, J. N. Huang, C. C. Kuo, Y. H. Lin,"Numerical and Experimental Investigation of Radiation Caused by the Switching Noise on the Partitioned DC Reference Planes of High Speed Digital PCB," *IEEE Transactions on Electromagnetic Compatibility*, Feb. 2004.

Fundamentals for EBG Structure

circuit view

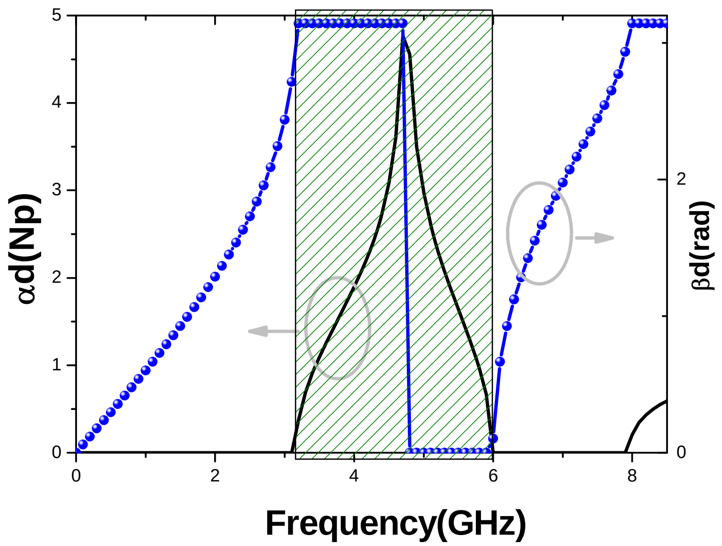


$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{unit\ cell} = \begin{bmatrix} \cos\frac{\theta}{2} & jZ_0 \sin\frac{\theta}{2} \\ jY_0 \sin\frac{\theta}{2} & \cos\frac{\theta}{2} \end{bmatrix} \begin{bmatrix} 1 & jX \\ 0 & 1 \end{bmatrix} \begin{bmatrix} \cos\frac{\theta}{2} & jZ_0 \sin\frac{\theta}{2} \\ jY_0 \sin\frac{\theta}{2} & \cos\frac{\theta}{2} \end{bmatrix}$$

$$= \begin{bmatrix} \cos\theta - \frac{X}{2} Y_0 \sin\theta & jX \cos^2\frac{\theta}{2} \\ \frac{Y_0}{2} \sin\theta (1+j) - jXY_0^2 \sin^2\frac{\theta}{2} & \cos\theta - \frac{X}{2} Y_0 \sin\theta \end{bmatrix}$$

Fundamentals for EBG Structure

circuit view



- **Case 1 : (Pass Band)**

$$\alpha = 0 \ \beta \neq 0, \pi$$

$$\cos \beta d = \cos\theta - \frac{X}{2} Z_0 \sin\theta$$

$$\left| \cos\theta - \frac{X}{2} Z_0 \sin\theta \right| \leq 1$$

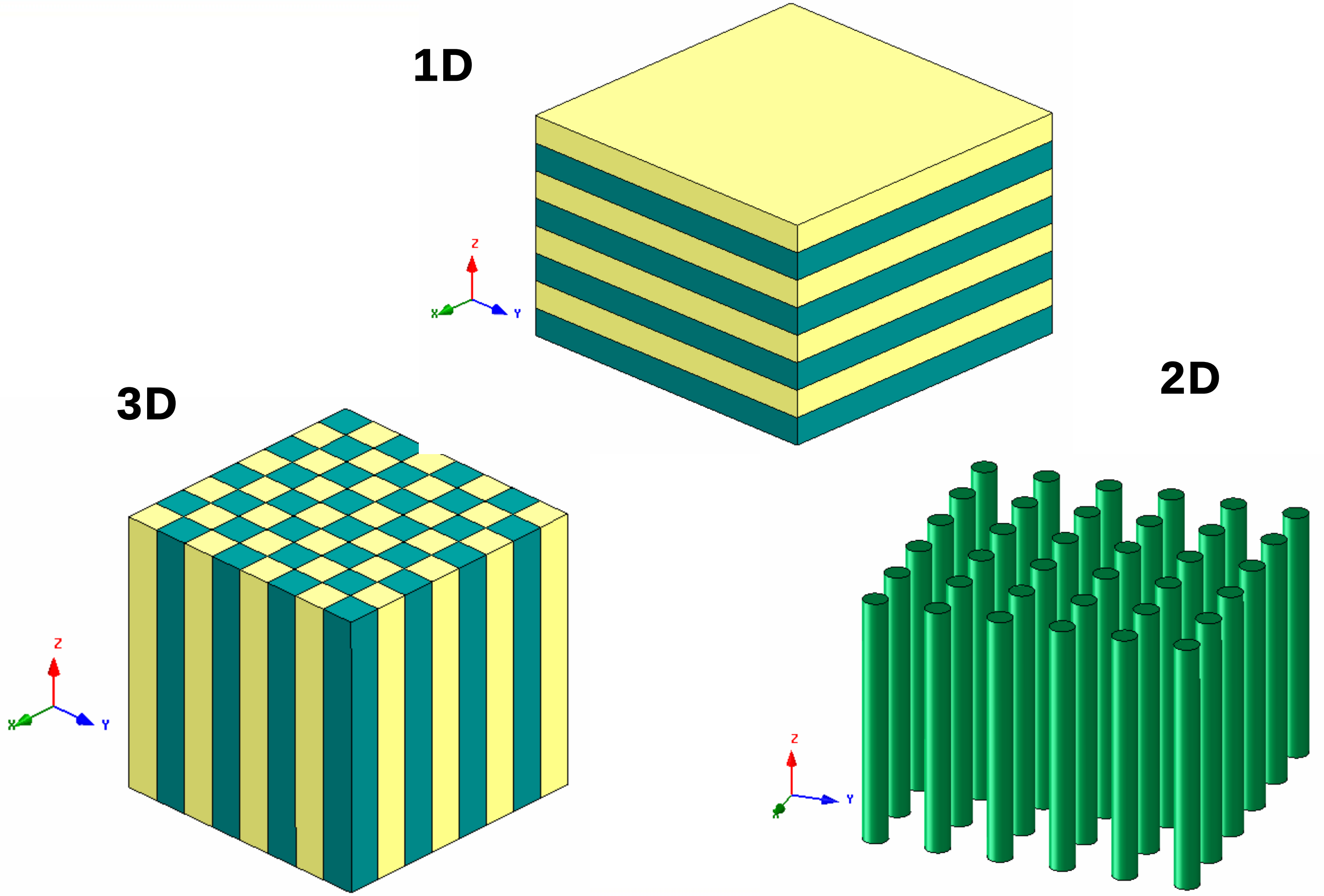
- **Case 2 : (Stop Band)**

$$\alpha \neq 0 \ \beta = 0, \pi$$

$$\cosh \alpha d = \left| \cos\theta - \frac{X}{2} Z_0 \sin\theta \right| \geq 1$$

Fundamentals for EBG/PBG Structure

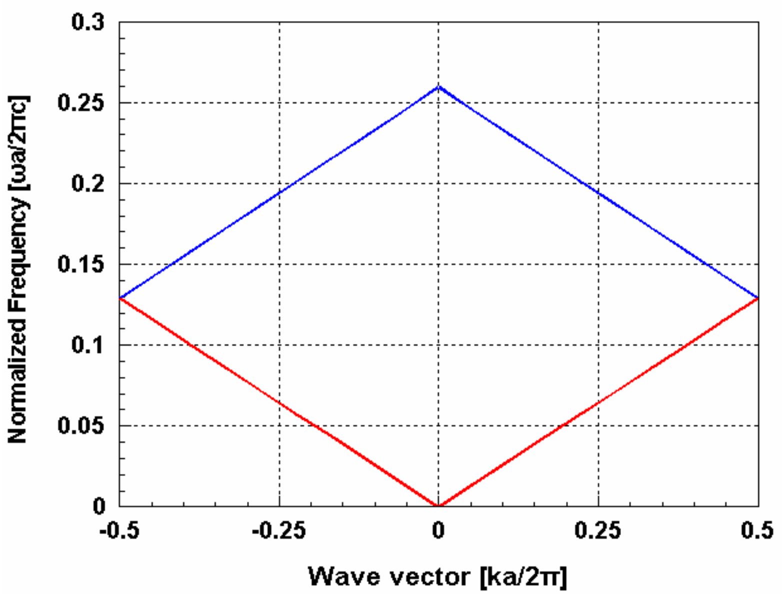
wave view

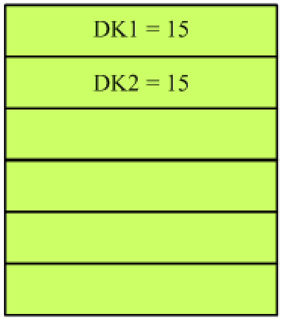


Fundamentals for EBG / PBG Structure

wave view

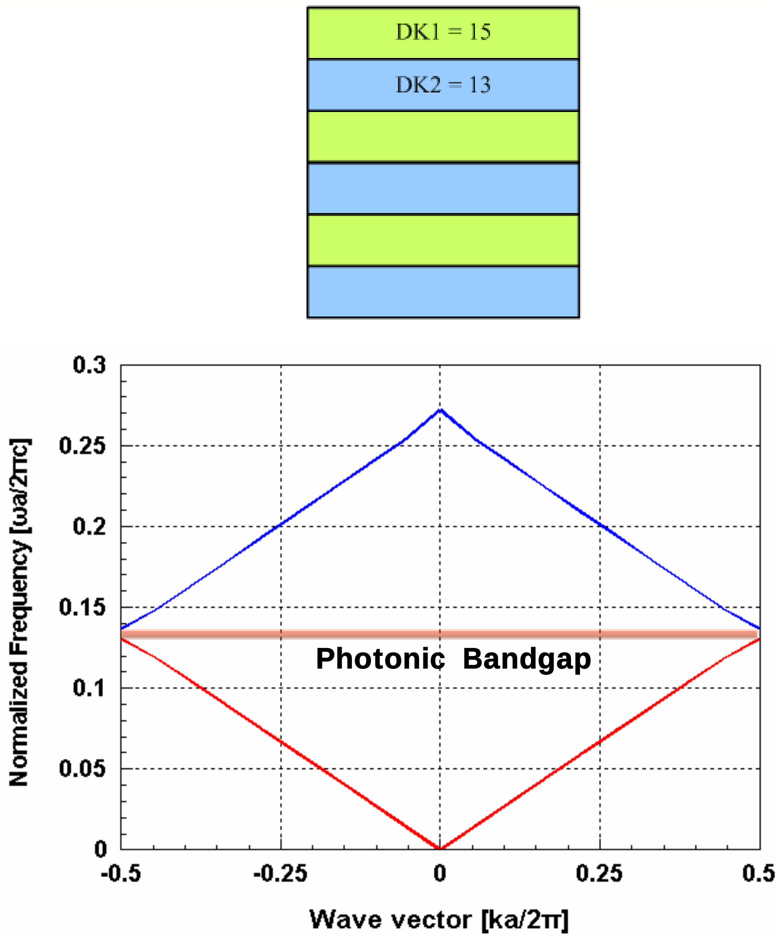
1D example (no DK contrast)

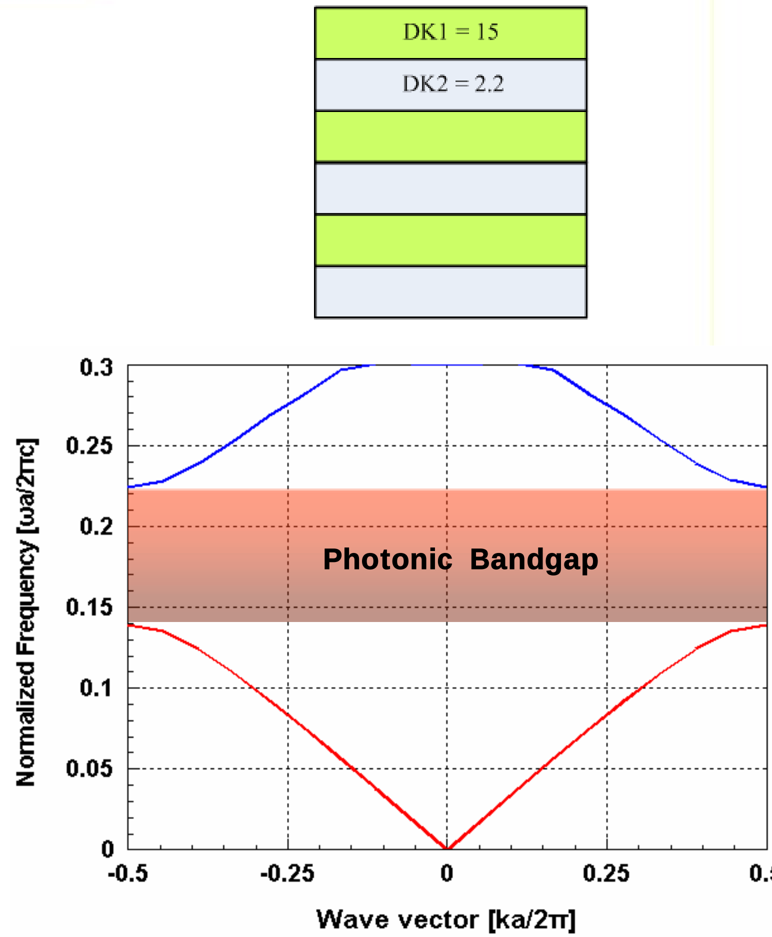




Fundamentals for EBG / PBG Structure

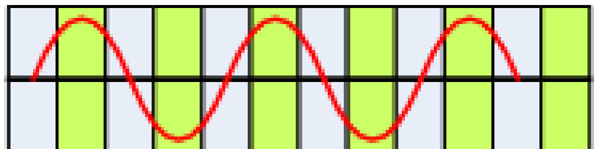
wave view





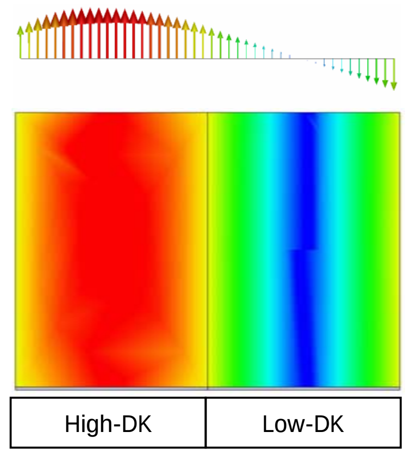
Fundamentals for EBG/PBG Structure

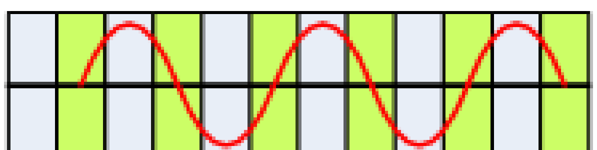
wave view



E-field for mode at top of band I

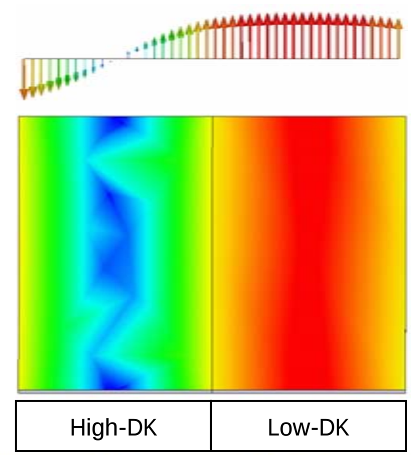
Local power in E-field , top of band I





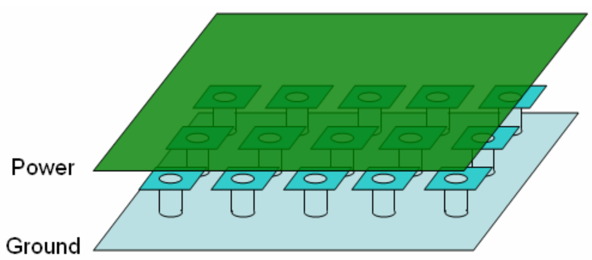
E-field for mode at bottom of band II

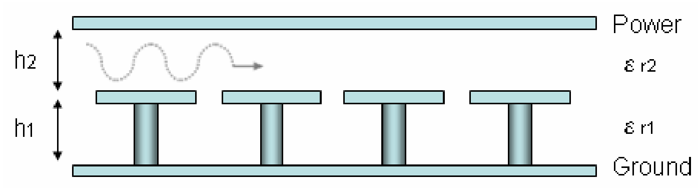
Local power in E-field, bottom of band II

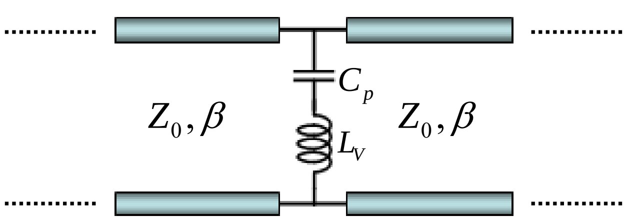


High-impedance Surface (mush-room)

concept







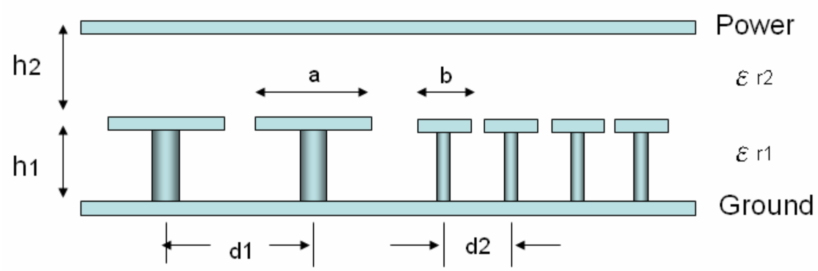
$$f_{start} = \frac{1}{2\pi\sqrt{C_p\left[L_v + \frac{\mu_0 h}{4}\right]}}$$

Shawn D. Rogers, "Electromagnetic-Bandgap Layers for Broad-Band Suppression of TEM Modes in Power Planes", *IEEE Trans. Microwave Theory and Tech.*, Vol.53, No. 8, pp.2495-2505, Aug. 2005

High-impedance Surface (mush-room)

bandwidth enhancement

Cascaded HIS: to improve the bandwidth

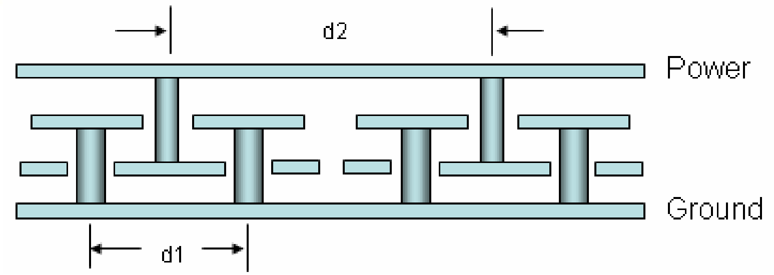


Shahrooz Shahparnia and Omar M. Ramahi, "Electromagnetic Interference (EMI) Reduction From Printed Circuit Boards (PCB) Using Electromagnetic Bandgap Structures", *IEEE Trans. Electromagntic Compatibility*, Vol.46, No.4, Nov. 2004.

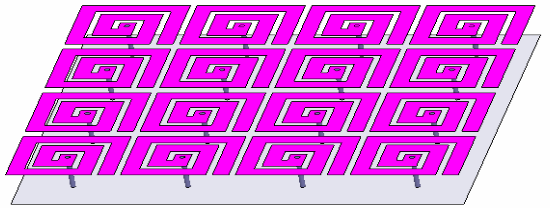
High-impedance Surface (mush-room)

bandwidth enhancement

(c) Double-Stacked HIS



(d) Spiral HIS

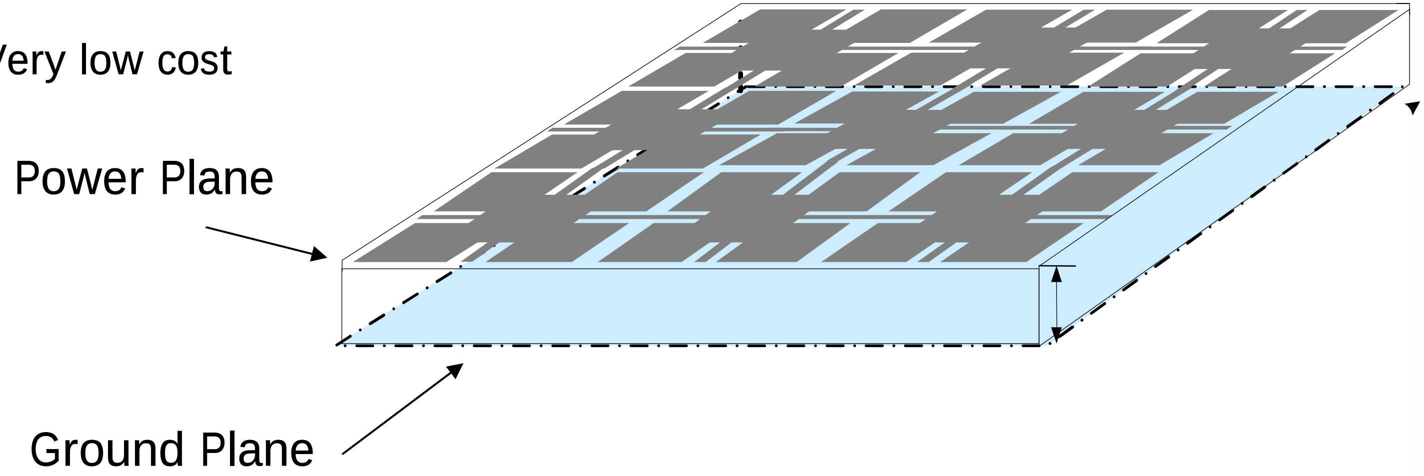


Jongbae Park, Albert Chee W. Lu, Kai M. Chua, Lai L. Wai, Junho Lee, and Joungho Kim, "Double-Stacked EBG Structure for Wideband Suppression of Simultaneous Switching Noise in LTCC-Based SiP Applications", *IEEE Microwave and Wireless Components Letters*, vol. 15, No.8, pp. 505-507, Aug. 2005.

Chien-Lin Wang, Guang-Hwa Shiue, and Ruey-Beei Wu, "EBG-Enhanced Split Power Planes for Wideband Noise Suppression", *Proc. IEEE 14th Topical Meeting Elect. Performance Electron. Package.*, 2005, pp.61-64.

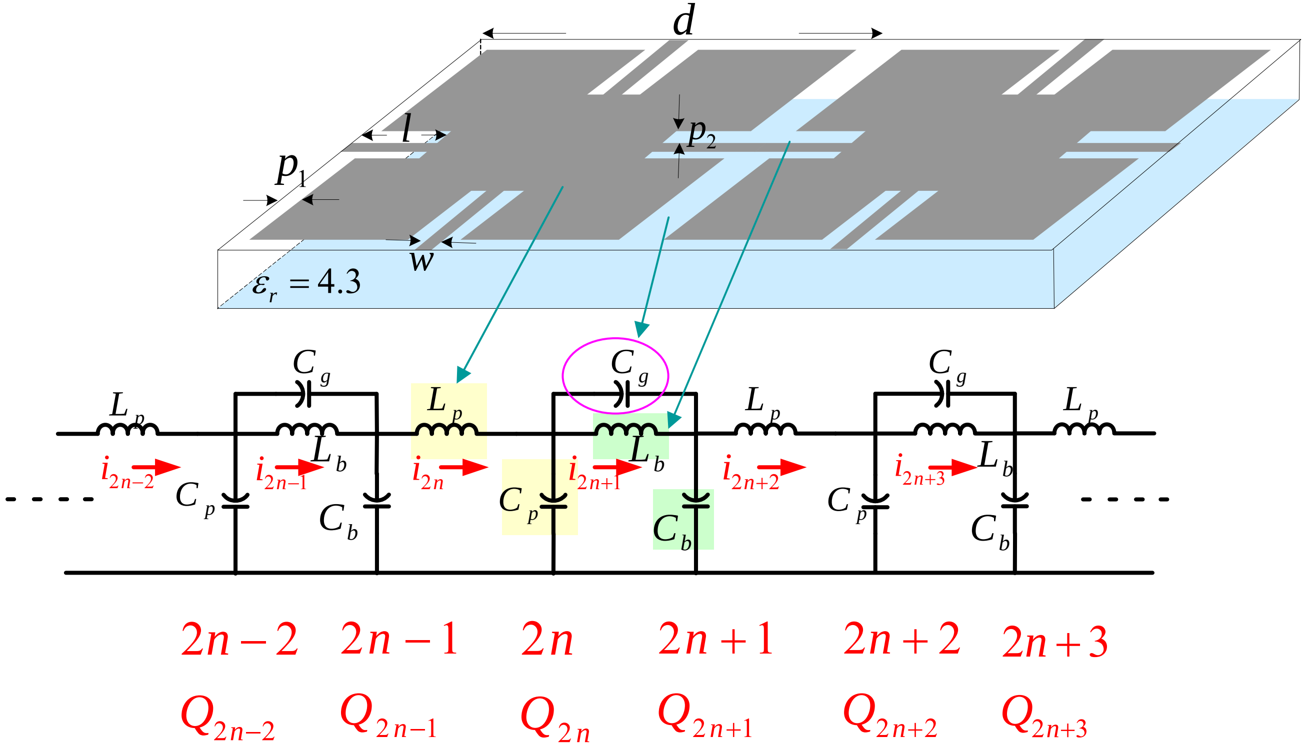
Electromagnetic Bandgap (EBG) Power Planes

- Broadband suppression of the P/GBN
- Low EMI caused by the P/GBN
- Isotropically elimination of the P/GBN
- Very low cost

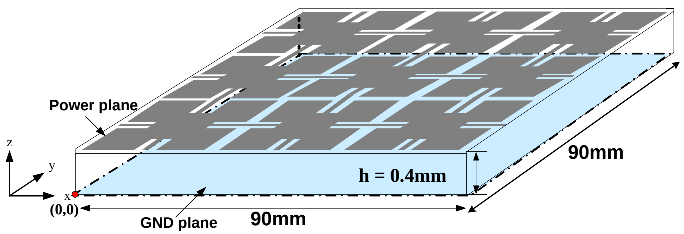


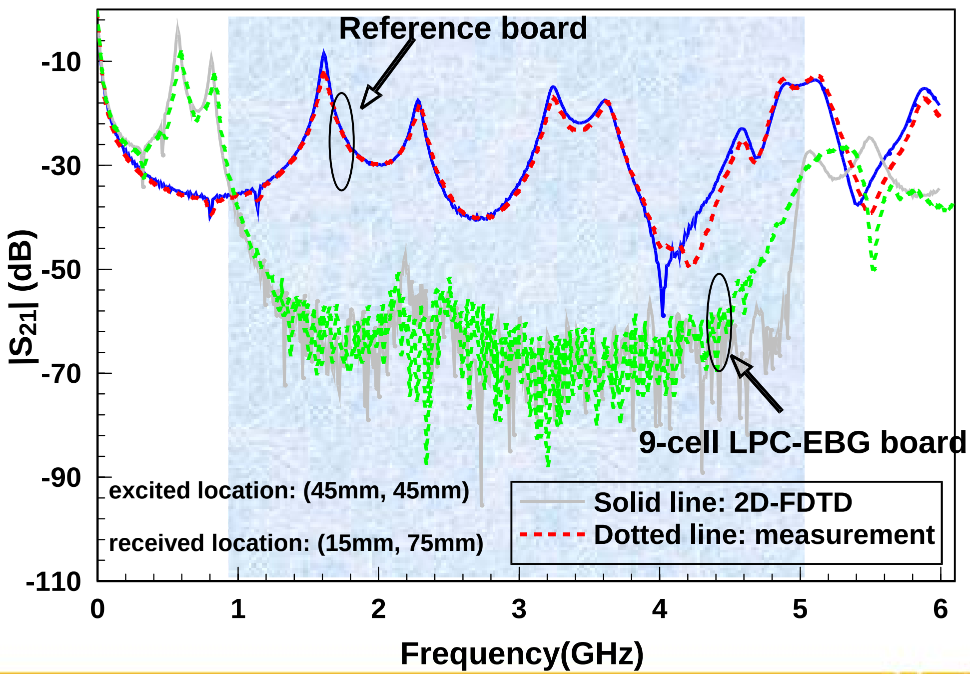
Tzong-Lin Wu, Yen-Hui Lin, and Sin-Ting Chen, "A Novel Power Planes With Low Radiation and Broadband Suppression of Ground Bounce Noise Using Photonic Bandgap Structures," *IEEE Microwave and Wireless Components Letters*, Vol. 14, No. 7, pp. 337-339, Jul. 2004

1D-equivalent circuit model

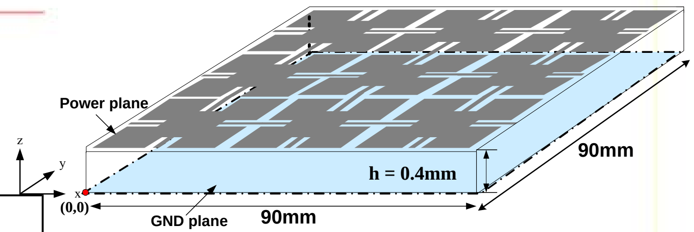


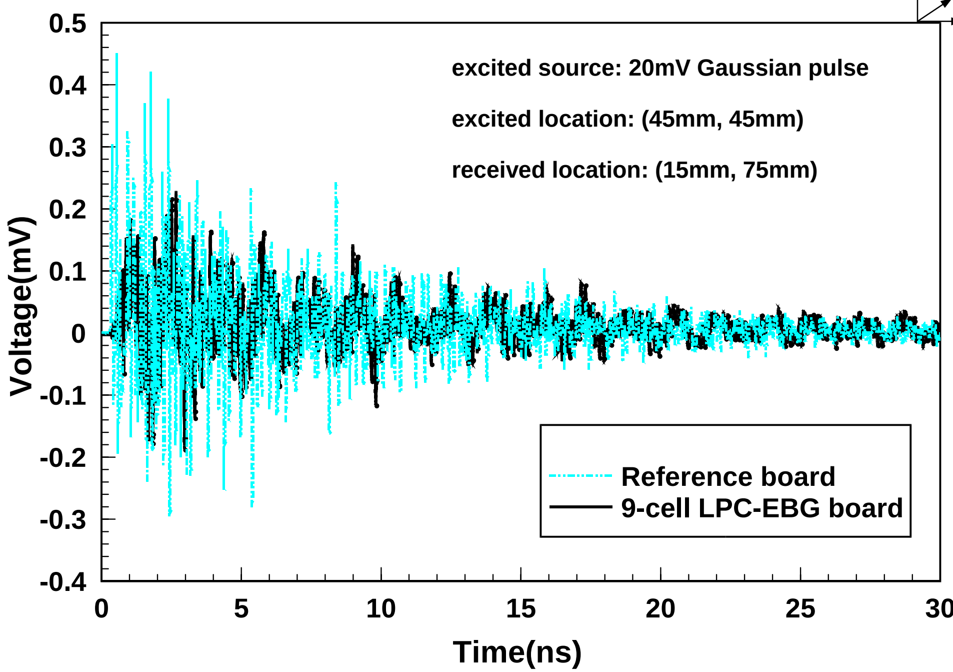
P/GBN suppression— Frequency domain





P/GBN suppression— Time domain (3D-FDTD)





There is over 35% of the GBN suppression rate by LPC-EBG power plane design.

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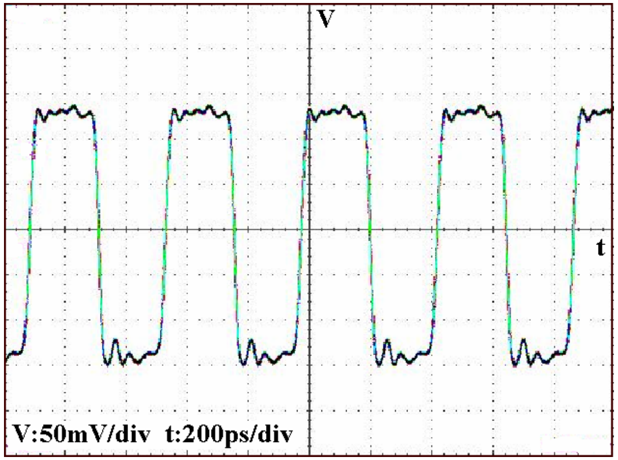
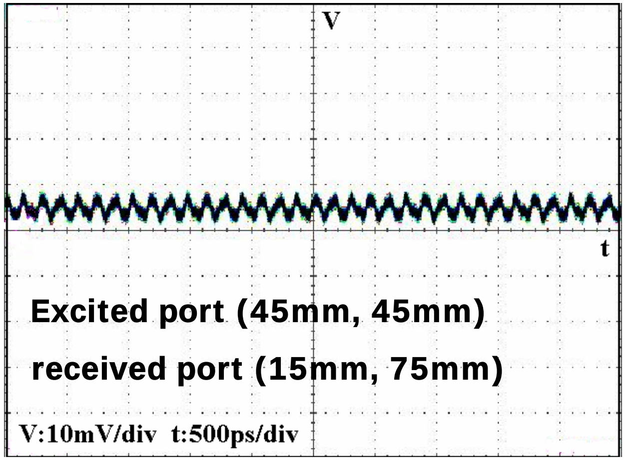
P/GBN suppression — Time domain (measurement)



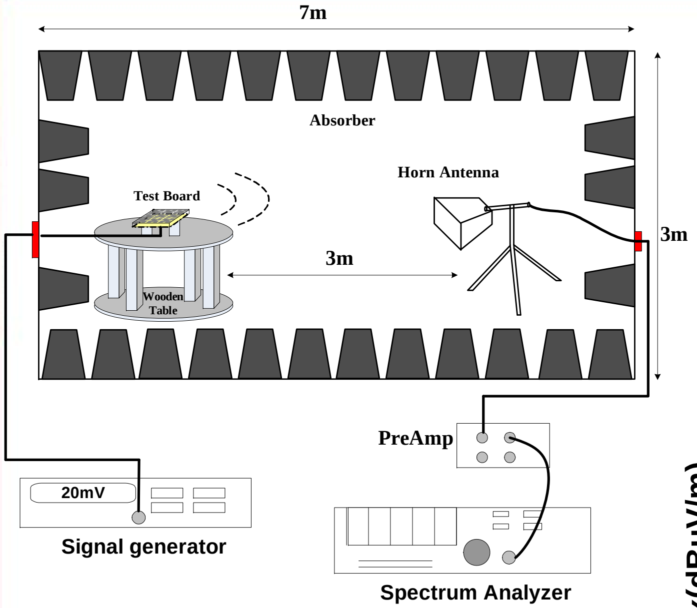
Excitation source(2.25GHz clock with amplitude of ±125mV)

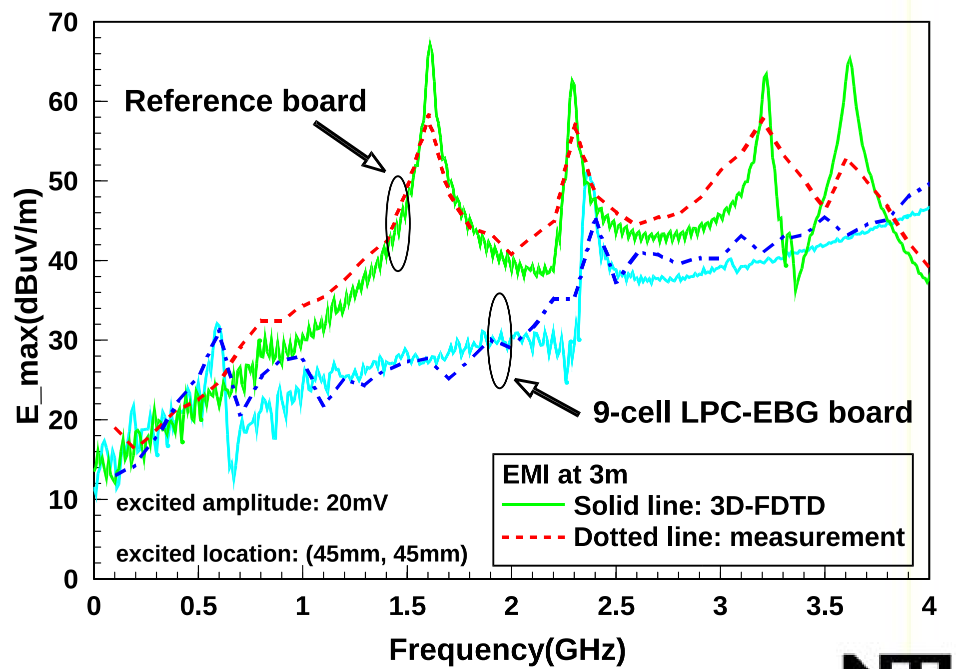


47

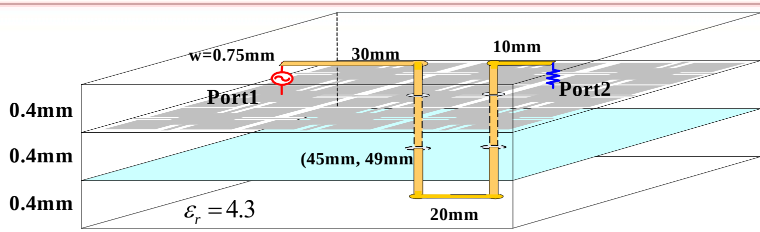
9cell-EBG board (peak to peak 7mV)

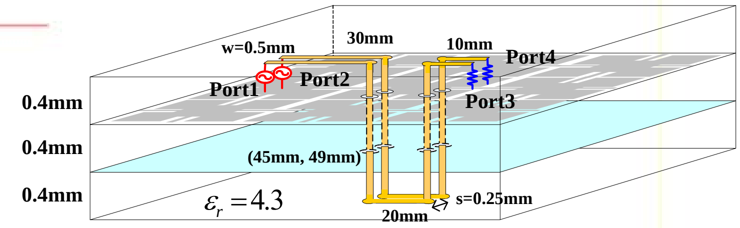
EMI elimination
— LPC-EBG structure

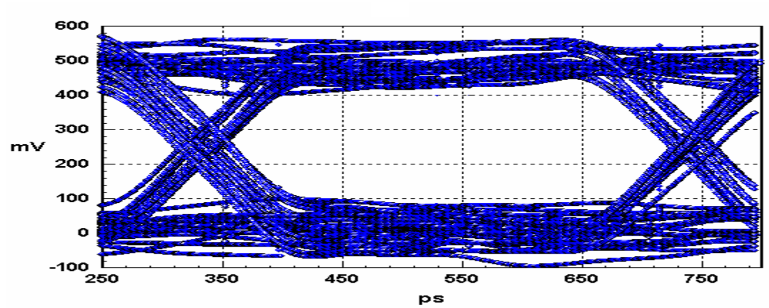


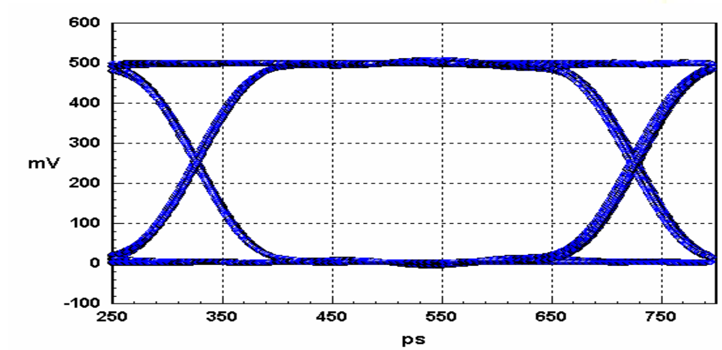


Impact on SI — Traces referring to EBG planes









MEO=363mV MEW=370ps

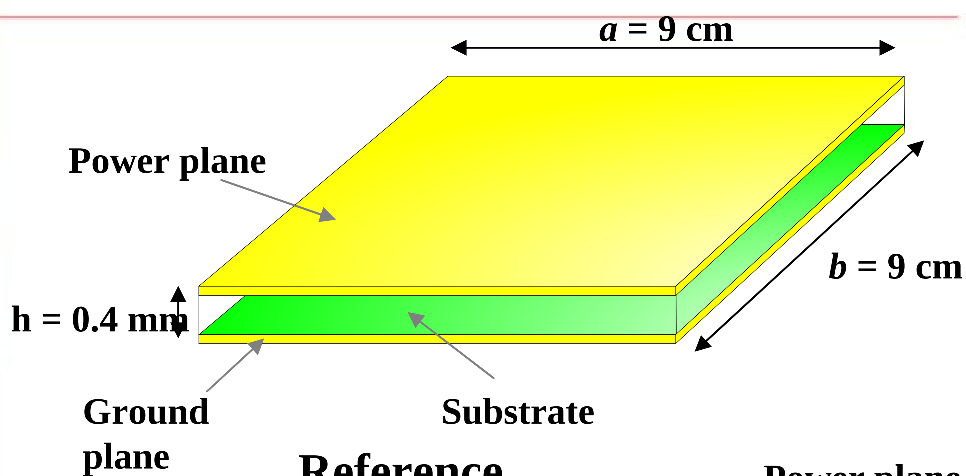
MEO=471mV MEW=389ps

Reference board (with solid power/ground planes)

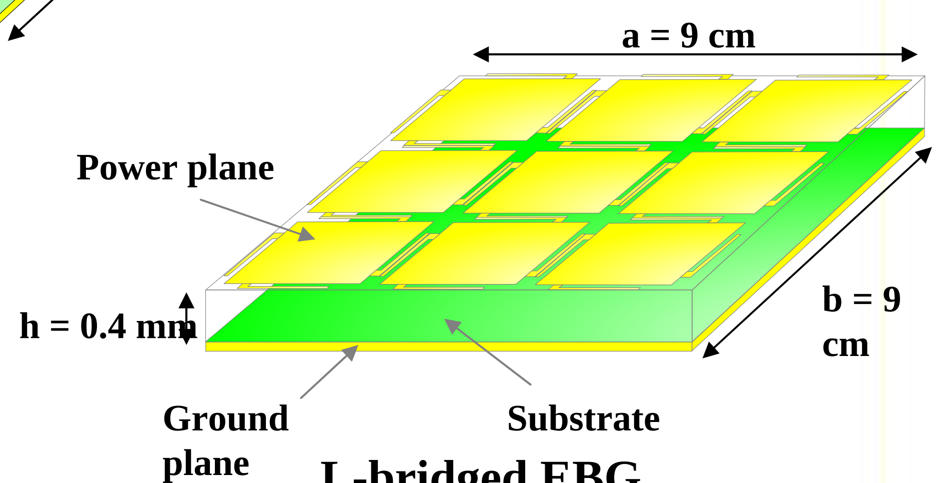
MEO=440mV MEW=388ps

Tzong-Lin Wu, Yen-Hui Lin, Ting-Kuang Wang, Chien-Chung Wang, and Sin-Ting Chen, "Electromagnetic Bandgap Power/Ground Planes for Wideband Suppression of Ground Bounce Noise and Radiated Emission in High-speed Circuits," *IEEE Transactions on Microwave Theory and Techniques*, vol. 53, No. 9, pp. 2935 - 2942, Sept. 2005

L-bridged EBG Power Plane



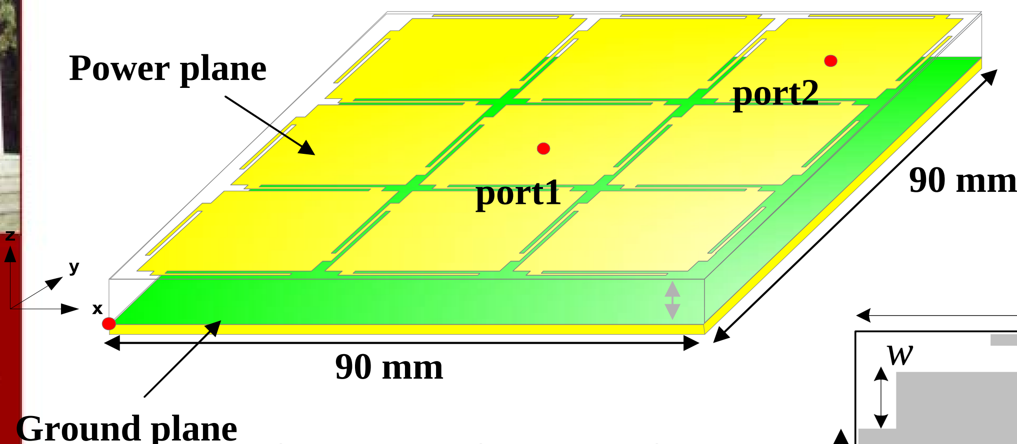
Reference board



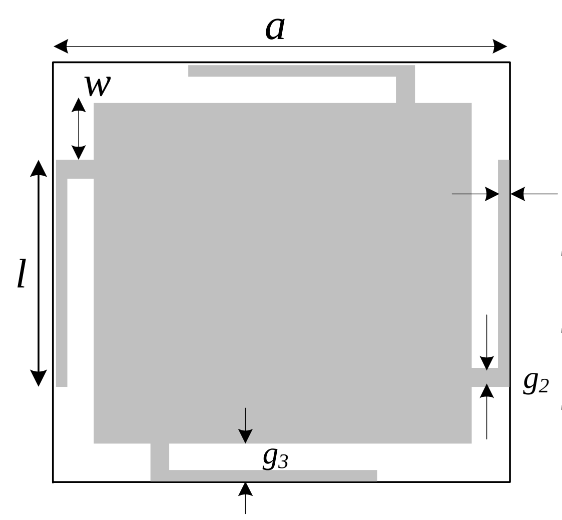
L-bridged EBG board

Tzong Lin Wu, Yen-Hui Lin and Ting-Kuang Wang, "A Novel Power Plane with super-Wideband Elimination of Ground Bounce Noise on High Speed Circuits," *IEEE Microwave and Wireless Components Letters*, Vol. 15, No. 3, pp. 174-176, Mar. 2005

L-bridged EBG geometrical parameters



90mm x 90mm x 0.4mm



$a = 30$ mm

$w = 6.65$ mm

$g_1 = 0.1$ mm

$g_2 = 0.2$ mm

$g_3 = 0.75$ mm

$l = 15.2$ mm

Unit Cell

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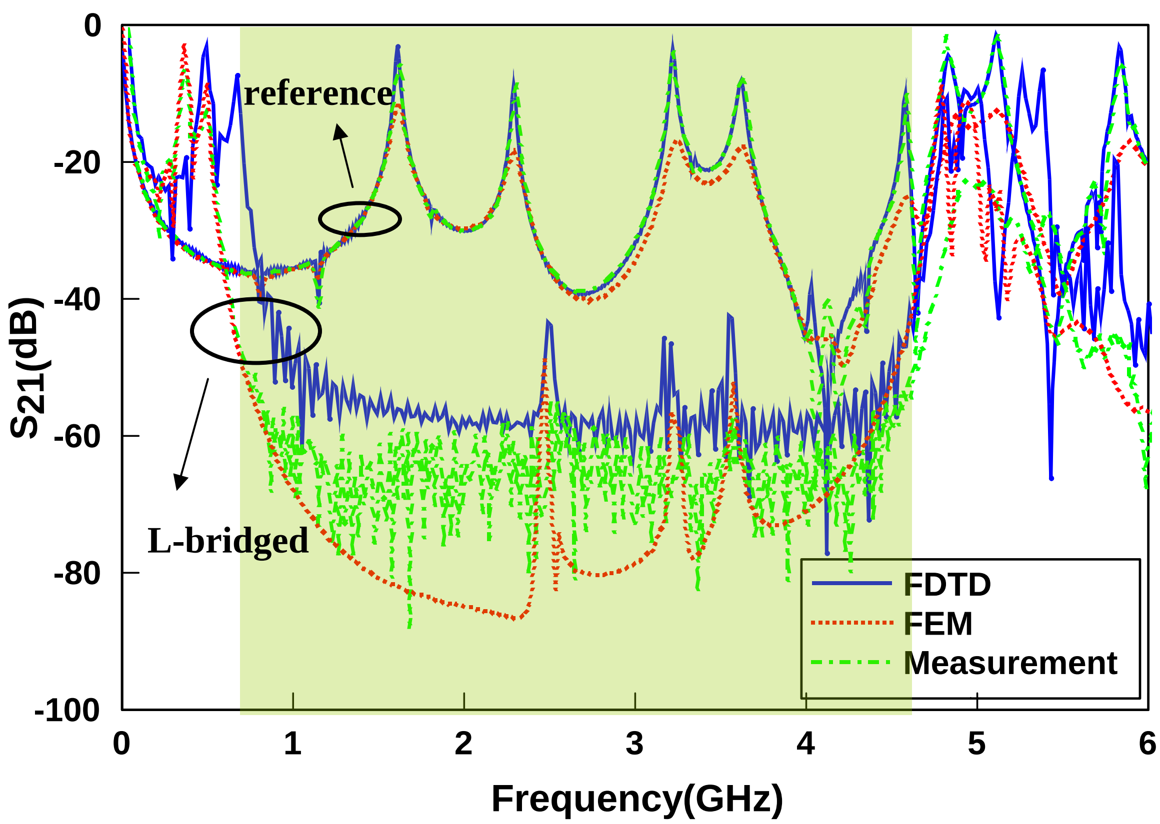
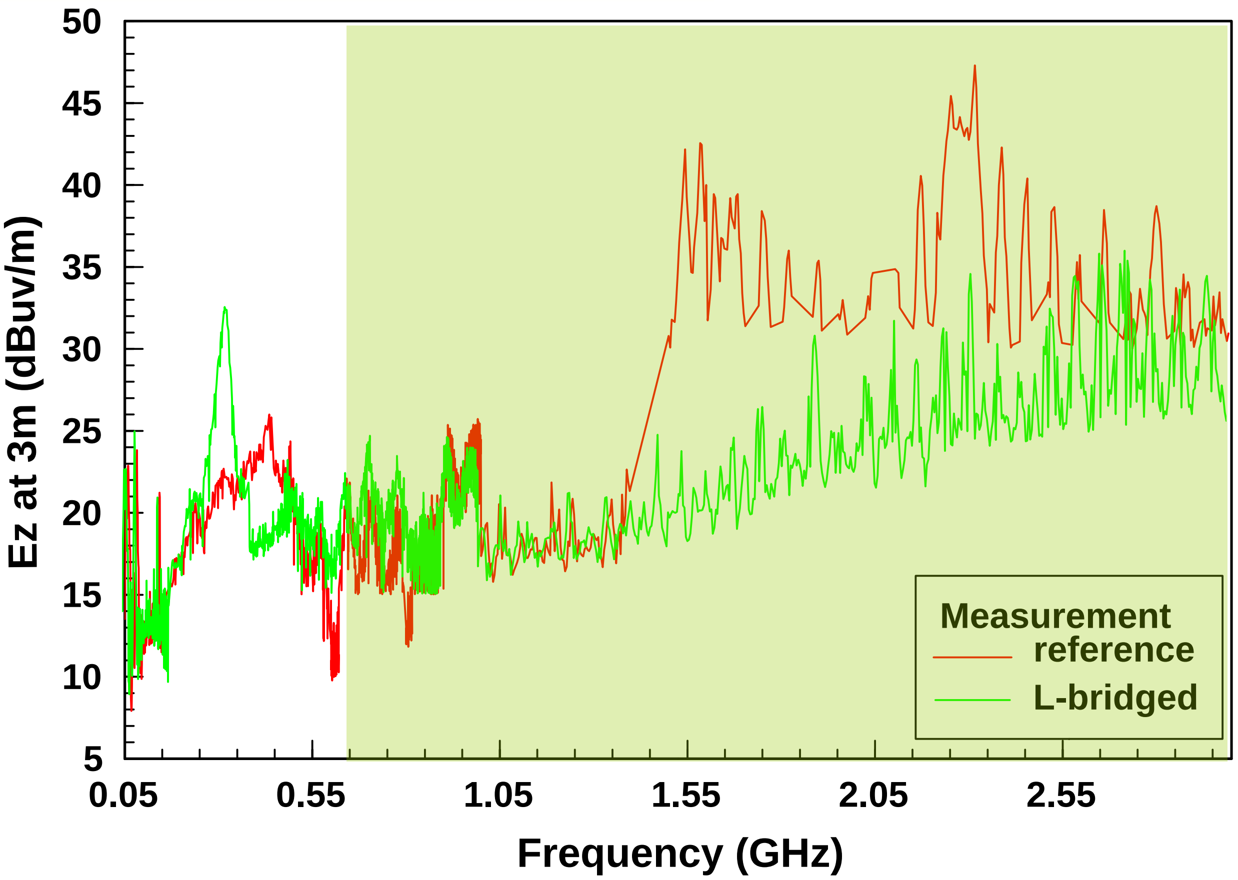
Wideband suppression



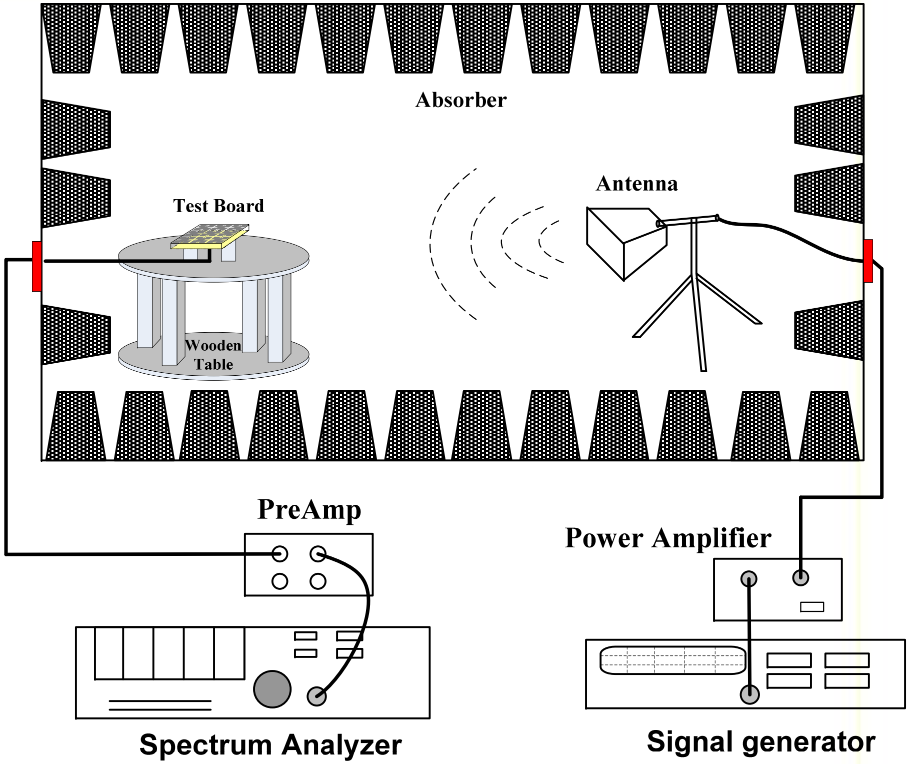
EMI performance



EMS measurement setup

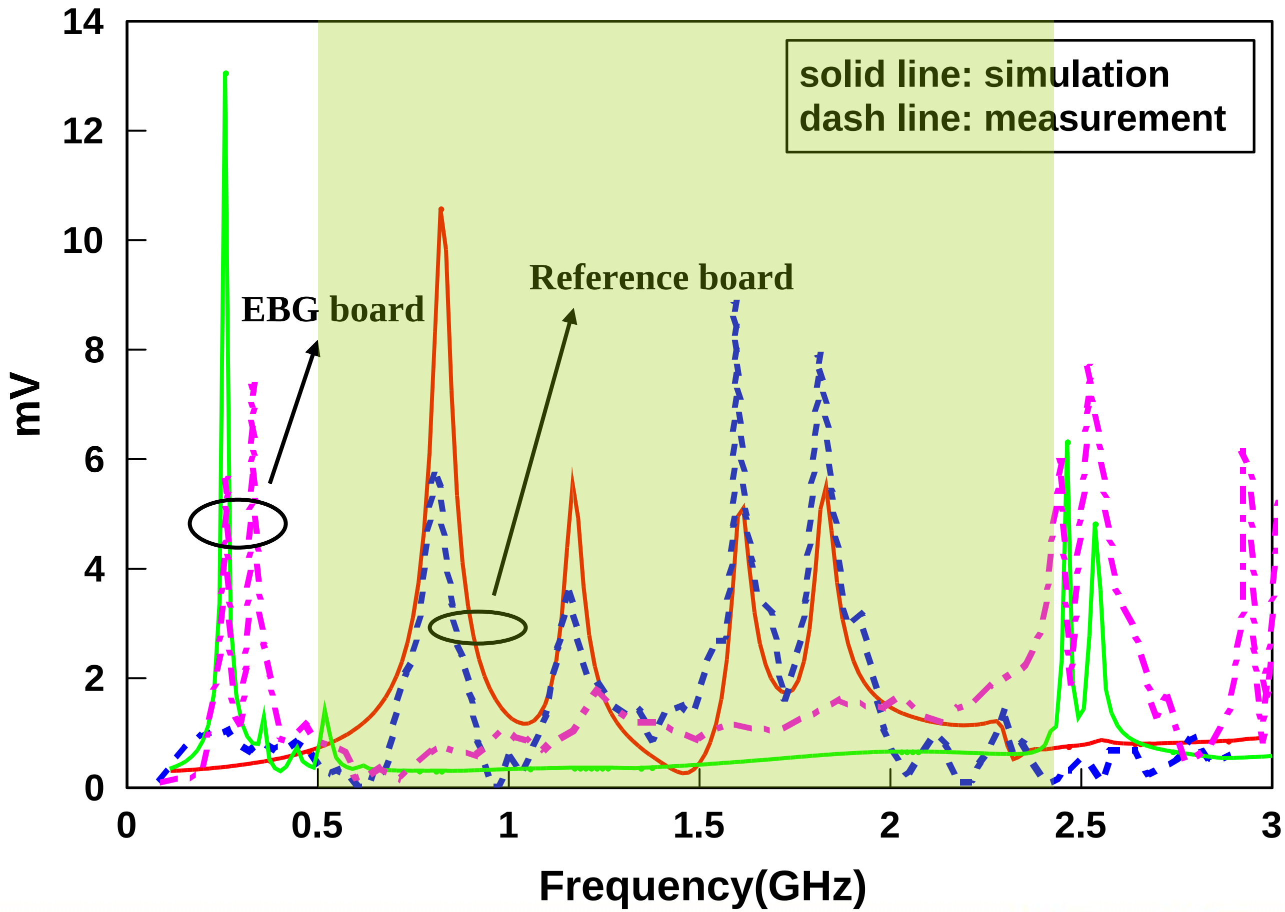
- According to IEC61000-4-3

- Modulation：CW
- Frequency Range：80 MHz ~ 3 GHz
- Dwell time：1 sec
- Frequency step：2%
- Electric field intensity：3 V/m



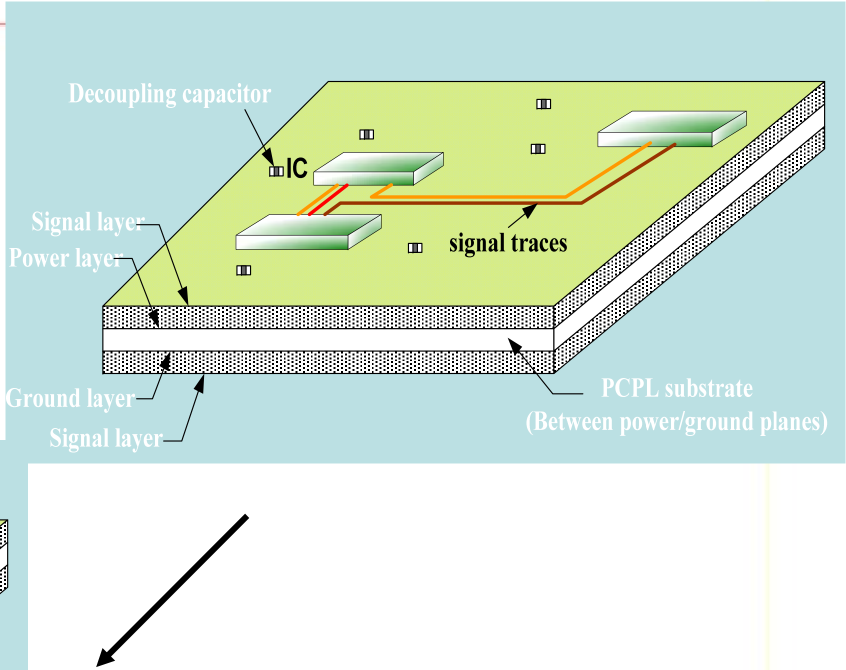
Hung-Chun Kuo Sin-Ting Chen Tzong-Lin Wu , "Improving the Radiated Immunity of the Strip-Lines Using a Novel Hybrid EBG Structure", IEEE 15th Topical Meeting on Electrical Performance of Electronic Packaging **(EPEP)**, Scottsdale, AZ, USA, 2006

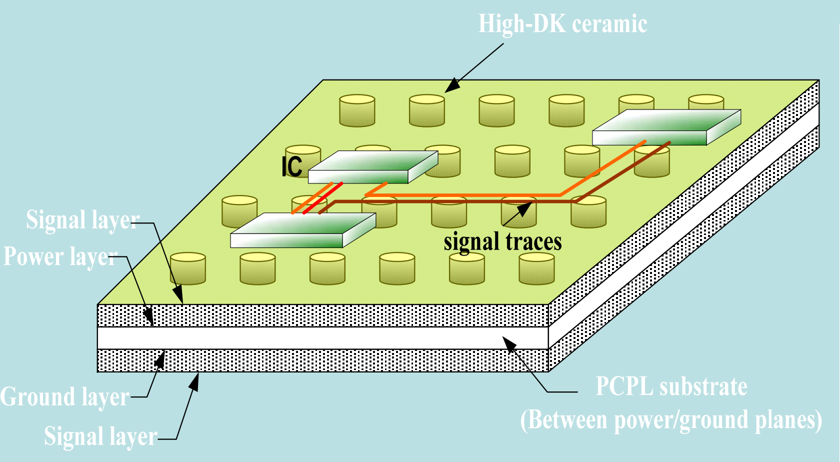
EMS frequency-domain response



Photonic Crystal Power Layer (PCPL)

Multilayer PCB substrate





Tzong-Lin Wu and Sin-Ting Chen, "An Electromagnetic Crystal Power Substrate with Efficient Suppression of Power/Ground Plane Noise on High-speed Circuits," *IEEE Microwave and Wireless Components Letters*, VOL. 16, NO. 7, Page(s):413 - 415, Jun. 2006

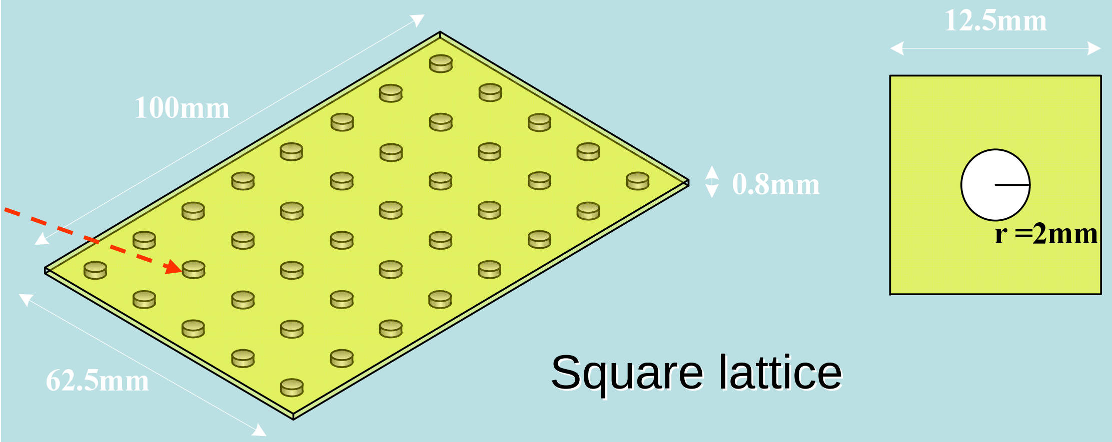
The geometry of the PCPL

High-DK material

High-DK material

ε_r =110

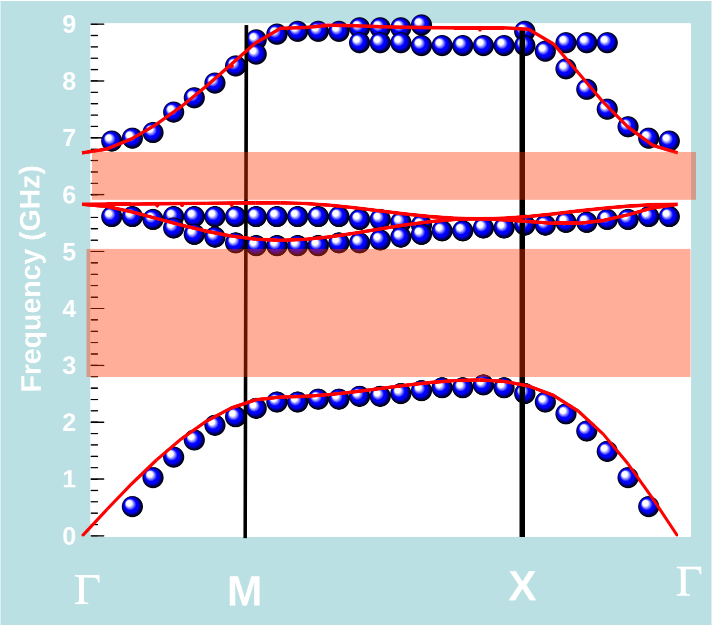
Q=1003 (f = 7GHz)



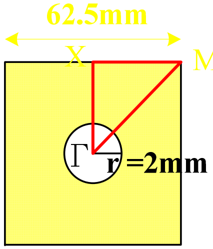
Square lattice

Rogers RT/duroid 5870 (tm)
K=2.33

Dispersion diagram for the PCPL



SL-PCPL



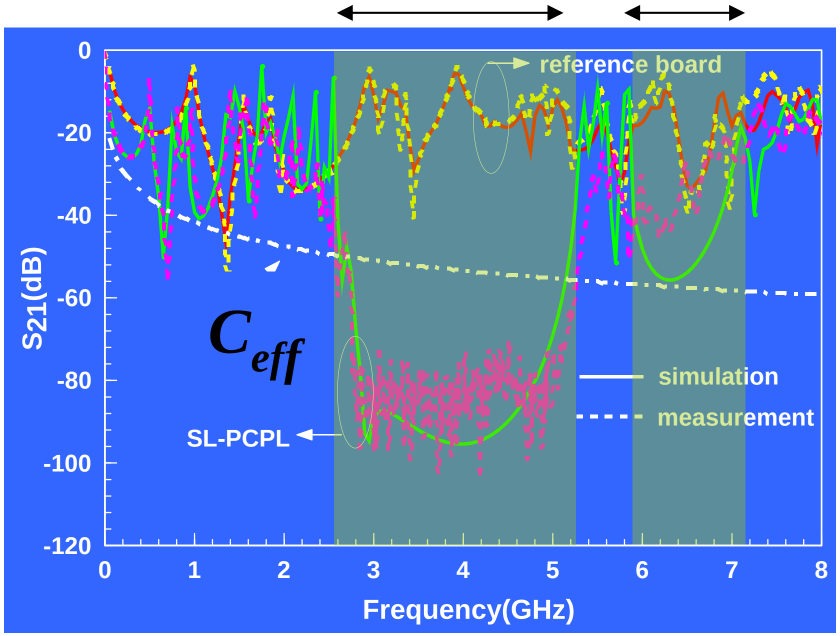
Square lattice

The dots -- FDTD method
The solid lines -- MIT photonic band tool

In this diagram, the bandgap is represented by frequency range in which there is no propagating mode for any propagation vectors.

P/GBN suppression – Frequency domain

Bandgaps



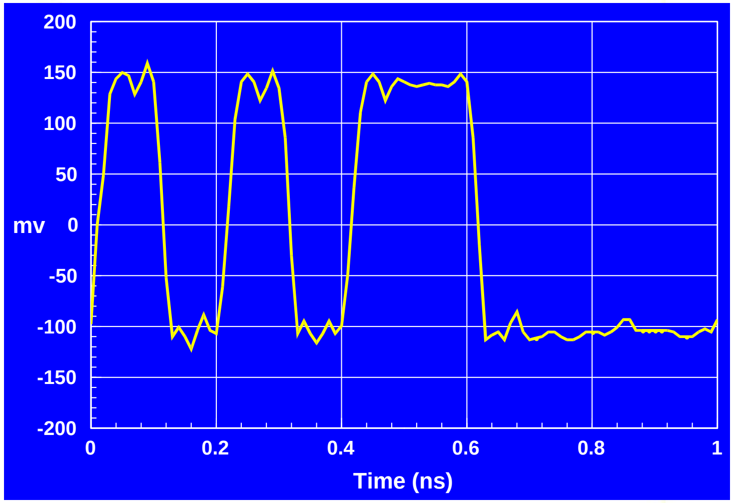
$$\varepsilon_{eff} = A_r \varepsilon_{r1} + (1 - A_r)\varepsilon_{r0}$$

$$\varepsilon_{eff} = 10.348$$

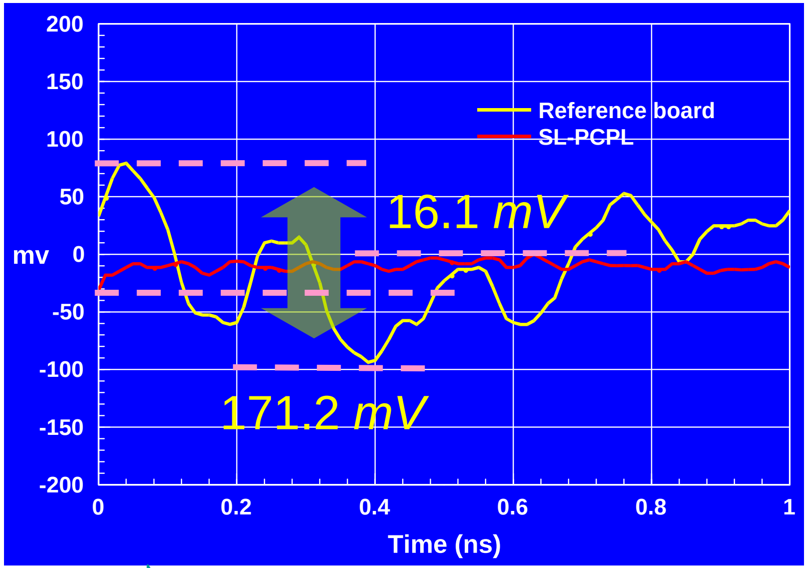
$$C_{eff} = 716\text{pF}$$

P/GBN suppression – Time domain

The waveform of the excitation source
10Gbps and amplitude ±125 *mV*

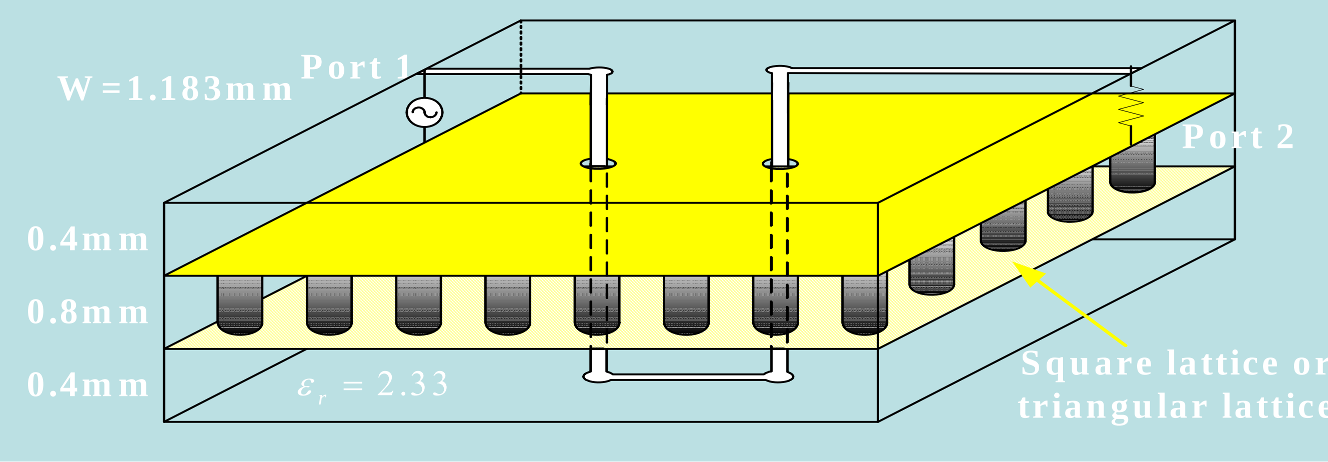


Square lattice



SSN can be reduced about 91%

Signal Integrity Performance



Input signal :

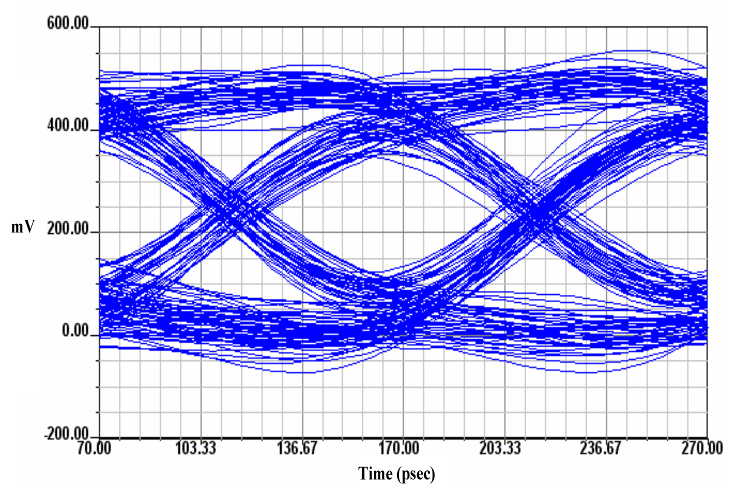
2^9-1 pseudo random bit sequence (PRBS), nonreturn to zero (NRZ), coded at 10GHz.

Bit rate : 10 Gbps

Amplitude : 500 mv

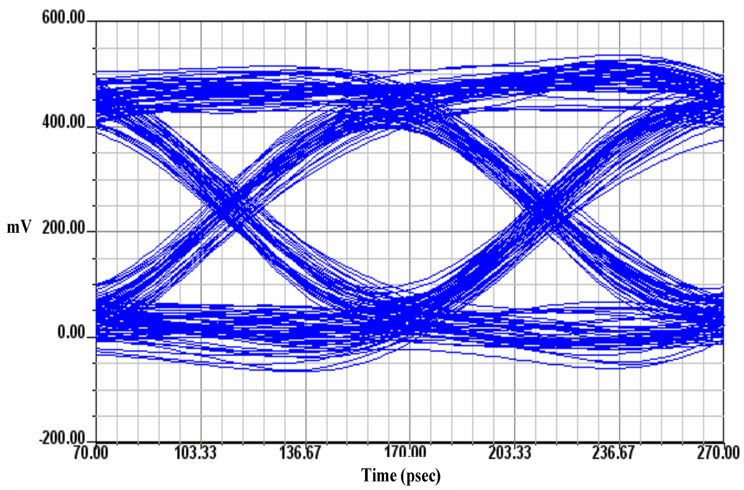
Edge rate : 35 ps

Eye Pattern Simulation (TL-PCPL)



MEO = 245 mV, MEW = 72 ps

Ref brd



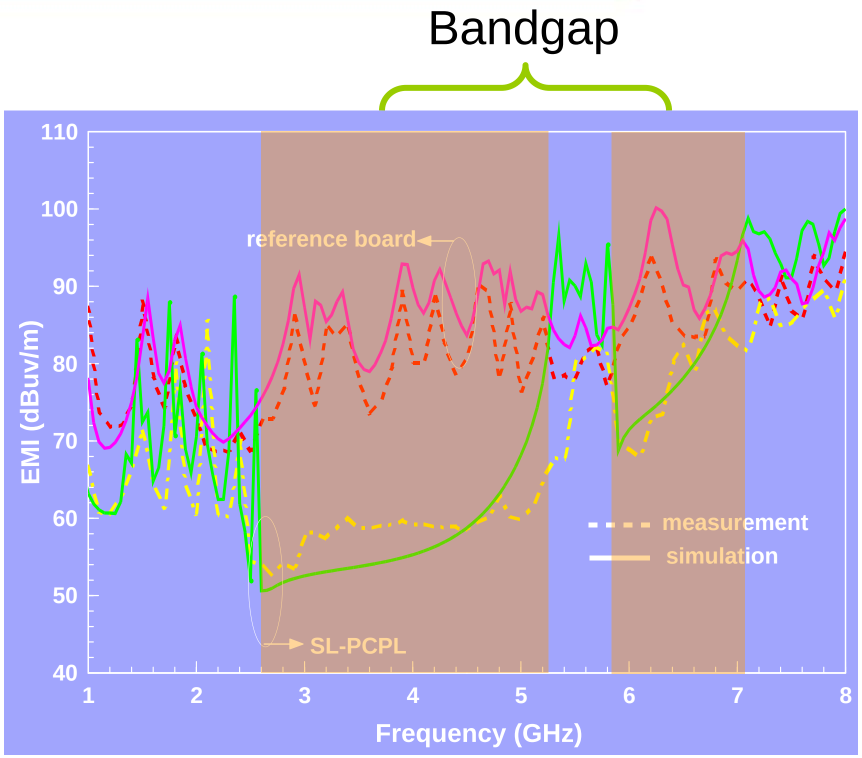
MEO = 292 mV, MEW = 85 ps

PCPL

MEO → Maximum Eye Open

MEW → Maximum Eye Width

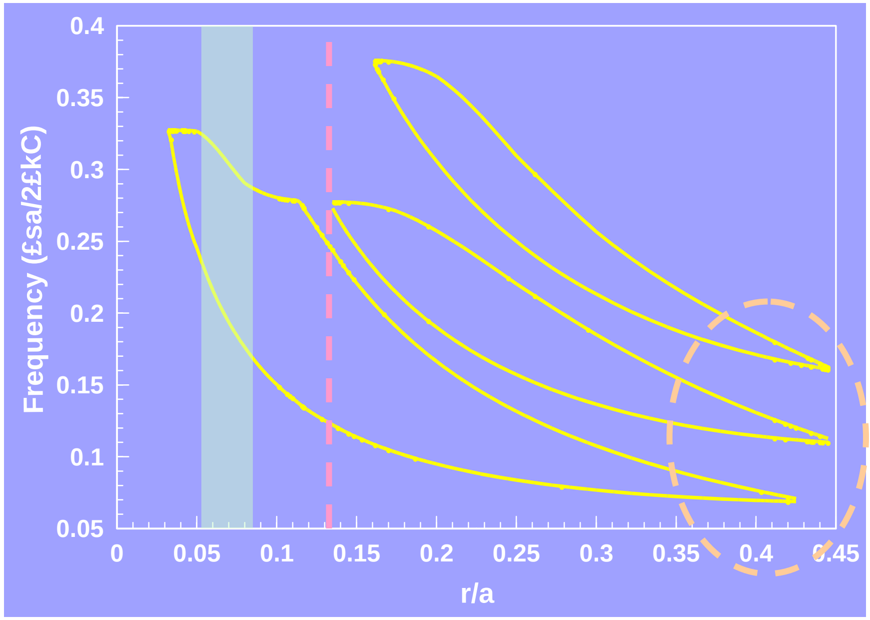
EMI elimination — PCPL structure



At the frequency range of the bandgap, the radiation resulted from the SSN is significantly suppressed with over 30dB reduction.

Gap map for PCPL structure

Area of maximum bandwidth for the first bandgap

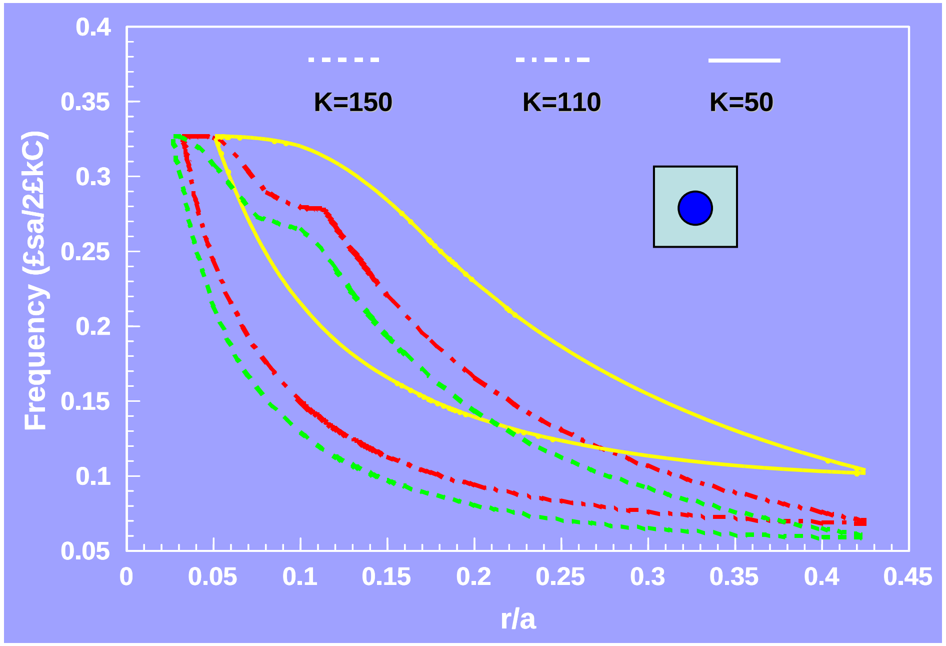


The substrate almost filled with high-DK rods

For the application, we need the broad stopband at low frequency. Therefore, there is design tradeoff between the bandwidth and the center frequency for the PCPL structure.

Tzong-Lin Wu, Sin-Ting Chen, "A photonic crystal power/ground layer for eliminating simultaneously switching noise in high-speed circuit," *IEEE Transactions on Microwave Theory and Techniques*, VOL. 54, NO. 8, pp. 3398 - 3406, Sept. 2006

Gap map of the PCPL structure for different dielectric constant



- The bandgap appears at smaller r/a for larger dielectric constant.
- The center frequency of the band at the same r/a is higher for the smaller dielectric constant.

Conclusion

- P/GBN is one of the key issues for designing high-speed digital circuit with good signal integrity (SI) and EMC performance.

- Several approaches to eliminate the P/GBN on the power delivery systems are investigated by both numerical simulations and experimental measurement.