Innovative PDN Design Guidelines for Practical High Layer-Count PCBs
Session 11 - WA - 1
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Motivation

Multiple power nets, each with its own power plane, and decoupling capacitors.

Power area fills on inner layer of PCB stack up.

Critical decisions about the PDN design:
- Location of capacitors
- Location of power plane in stack up
- Distance of capacitors from the IC
- Location of the return vias and the return planes

How do these choices affect the PDN response?
Outline

• Physics Based Model for Real PCB PDNs

• $L_{EQ}$ and $L_{IC}$ using the Geometry – Model – Response Paradigm

• Case Studies for Design Guidelines

• Trends in $L_{EQ}$ and $L_{IC}$ with Change PCB Stack Up Thickness

• Conclusions
Equivalent Circuit Model for a Single Cavity

\[ L_{ij} = \frac{\mu d}{ab} \sum_{m=0}^{\infty} \sum_{n=0}^{\infty} \frac{e_{m} e_{n}}{k_{mn}} f(x_{i}, y_{i}, x_{j}, y_{j}) \mid_{(m,n) \neq (0,0)} \]

\[ f(x_{i}, y_{i}, x_{j}, y_{j}) = \cos \left( \frac{m\pi x_{i}}{a} \right) \sin c \left( \frac{m\pi y_{i}}{a} \right) \cos \left( \frac{n\pi y_{j}}{a} \right) \sin c \left( \frac{n\pi y_{j}}{a} \right) \]

\[ k_{mn} = \left( \frac{m\pi}{a} \right)^2 + \left( \frac{n\pi}{b} \right)^2 \]

Where,

- \( L_{ij} \): Self or Mutual Inductance between \( i \)th and \( j \)th via
- \( a, b \): Dimension of the plane in \( x, y \) direction,
- \( d \): Thickness of cavity in the \( z \) direction,
- \( m, n \): Mode numbers in \( x \) and \( y \) directions \((x_{i}, y_{i})\): Location of Via \( i \), and
- \( t_{x_{i}}, t_{y_{i}} \): \( x \) and \( y \) dimensions of Via \( i \) (rectangular).

A Real PCB PDN Geometry

The stack up and layout is used to indicate a real production PCB, with and irregular power fill, many power return planes, many decoupling capacitors and power their power and power return vias.
Equivalent Circuit Model for the Real PCB PDN

Model Validation

The model results and measurements are for a real 28 layer production board with 17 IC power vias, 19 decoupling capacitors placed around the IC, 243 return vias in the modeled region, and many return planes.
## Case Study Considerations

<table>
<thead>
<tr>
<th>Cases</th>
<th>Variation 1</th>
<th>Variation 2</th>
<th>Variation 3 …</th>
</tr>
</thead>
<tbody>
<tr>
<td>Capacitor Location</td>
<td><img src="ic1.png" alt="Image" /> 16 Top Capacitors</td>
<td><img src="ic2.png" alt="Image" /> 16 Bottom Capacitors</td>
<td><img src="ic3.png" alt="Image" /> 16 Bottom Capacitors, Under the IC</td>
</tr>
<tr>
<td>Capacitor Distance</td>
<td><img src="dist1.png" alt="Image" /> 300 mils</td>
<td><img src="dist2.png" alt="Image" /> 8.5 mils</td>
<td><img src="dist3.png" alt="Image" /> 4 mils</td>
</tr>
<tr>
<td>Power Plane Location</td>
<td><img src="plane1.png" alt="Image" /> Top Power Layer</td>
<td><img src="plane2.png" alt="Image" /> Middle Power Layer</td>
<td><img src="plane3.png" alt="Image" /> Bottom Power Layer</td>
</tr>
<tr>
<td>Return Via for Capacitor</td>
<td><img src="via1.png" alt="Image" /> 10 mils</td>
<td><img src="via2.png" alt="Image" /> 100 mils</td>
<td><img src="via3.png" alt="Image" /> 300 mils</td>
</tr>
<tr>
<td>Return Planes</td>
<td><img src="planes1.png" alt="Image" /></td>
<td><img src="planes2.png" alt="Image" /></td>
<td><img src="planes3.png" alt="Image" /></td>
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</tbody>
</table>

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## Stack Up and Layout of the Reference Geometry

- **44 Layer**:
  - GND, PWR_TOP
  - GND, GND, GND, GND, GND, GND
  - GND, PWR_MID1,2
  - GND, GND, GND, GND, GND
  - GND, GND, GND, GND, GND
  - GND, GND, GND, GND, GND
  - GND, GND, GND, GND, GND
  - GND, GND, GND, GND, GND
  - GND, GND, GND, GND, GND
  - GND, GND, GND, GND, GND

- **Possible Power Net Locations**:
  - ~300 mils
  - 12" mils

- **Reference Net**:
  - Signal Layer

- **IC region**
  - 12"

- **100 mils**
### Case 1 and Case 2 - Capacitor and Power Layer Location: Geometry

<table>
<thead>
<tr>
<th>Power plane at top</th>
<th>Power plane at mid</th>
<th>Power plane at bottom</th>
</tr>
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<tbody>
<tr>
<td>Top decaps only</td>
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</tr>
<tr>
<td>IC 16 Decaps</td>
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</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bottom decaps only</td>
<td>Bottom decaps only</td>
<td>Bottom decaps only</td>
</tr>
<tr>
<td>IC 16 Decaps</td>
<td>IC 16 Decaps</td>
<td>IC 16 Decaps</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Under the IC</td>
<td>Under the IC</td>
<td>Under the IC</td>
</tr>
<tr>
<td>IC 16 Decaps</td>
<td>IC 16 Decaps</td>
<td>IC 16 Decaps</td>
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<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Away from the IC</td>
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<td>Away from the IC</td>
</tr>
<tr>
<td>IC 16 Decaps</td>
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- **Power Net under test**
- **Reference Net**
- **Floating Net**
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<td><img src="image1" alt="Diagram" /></td>
<td><img src="image2" alt="Diagram" /></td>
<td><img src="image3" alt="Diagram" /></td>
</tr>
<tr>
<td><strong>Bottom decaps only</strong></td>
<td><img src="image4" alt="Diagram" /></td>
<td><img src="image5" alt="Diagram" /></td>
<td><img src="image6" alt="Diagram" /></td>
</tr>
<tr>
<td><strong>Under the IC</strong></td>
<td><img src="image7" alt="Diagram" /></td>
<td><img src="image8" alt="Diagram" /></td>
<td><img src="image9" alt="Diagram" /></td>
</tr>
<tr>
<td><strong>Away from the IC</strong></td>
<td><img src="image10" alt="Diagram" /></td>
<td><img src="image11" alt="Diagram" /></td>
<td><img src="image12" alt="Diagram" /></td>
</tr>
</tbody>
</table>

- **Power Net under test**: Orange
- **Reference Net**: Green
- **Floating Net**: Blue
Case 1 and Case 2 - Capacitor and Power Layer Location: Geometry

<table>
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</table>

Legend:
- Orange: Power Net under test
- Green: Reference Net
- Blue: Floating Net
The capacitors should be placed as close as possible to the power layer. If available, the placement of capacitors under the IC is best, except when the board is thick and power layer is near the top of PCB.
Case 1 - Capacitor Location: Response

The capacitors should be placed as close as possible to the power layer. If available, the placement of capacitors under the IC is best, except when the board is thick and power layer is near the top of PCB.

Case 2 - Power Layer Location: Response

The power layer should be placed as close as possible to the IC.
Case 2 - Power Layer Location: Response

The power layer should be placed as close as possible to the IC.

**Case 3 - Distance of Capacitor from IC: Geometry**

<table>
<thead>
<tr>
<th>X (mils)</th>
<th>Capacitor Distance</th>
</tr>
</thead>
<tbody>
<tr>
<td>300</td>
<td>16 Capacitor Ring</td>
</tr>
<tr>
<td>500</td>
<td>16 Capacitor Ring</td>
</tr>
<tr>
<td>1000</td>
<td>16 Capacitor Ring</td>
</tr>
<tr>
<td>4000</td>
<td>16 Capacitor Ring</td>
</tr>
</tbody>
</table>
Case 3 - Distance of Capacitor from IC: Response

Case 4 - Distance of Return Via from Capacitor: Geometry

<table>
<thead>
<tr>
<th>X (mils)</th>
<th>PWR vias</th>
<th>GND vias</th>
</tr>
</thead>
<tbody>
<tr>
<td>50</td>
<td></td>
<td></td>
</tr>
<tr>
<td>100</td>
<td></td>
<td></td>
</tr>
<tr>
<td>300</td>
<td></td>
<td></td>
</tr>
<tr>
<td>300 – Use IC GND via</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Case 4 - Distance of Return Via from Capacitor: Response

A return via should be placed as close as possible to each capacitor.

Case 5 - Distance of Reference Plane from Power Plane: Geometry

Intermediate GND planes removed

Intermediate GND planes removed

Intermediate GND planes removed

Intermediate GND planes removed
Case 5 - Distance of Reference Plane from Power Plane: Response

The closest ground plane from the power plane is most important. Other ground planes in the stack up will not affect the $L_{EQ}$ or $L_{IC}$ significantly. A return layer should be placed as close as possible to the power layer.

Trends for $L_{EQ}$ and $L_{IC}$

Indicative trends for $L_{EQ}$ and $L_{IC}$ are found for the different variations in geometry.

Possible Power Net Locations

Reference Net

Signal Layer

Variation 1

Variation 2

Variation 3
\[ L_{EQ} vs h_1 \] for Different Capacitor Locations

- **Top Caps only**
- **Bottom Caps only**
- **Bottom Caps only, Under the IC**

\[ Z_{11} = \omega L_{EQ} \]

\[ |Z_{11}| - Middle PWR \]

\[ |Z_{11}| - Top Cap \]

\[ |Z_{11}| - Bottom Cap-Away \]

\[ |Z_{11}| - Bottom Cap- Under the IC \]

\[ L_{IC} vs Distance Between IC and Power Plane \]

\[ |Z_{11}| - Top Cap \]

\[ |Z_{11}| - Power plane at Top \]

\[ |Z_{11}| - Power plane Middle \]

\[ |Z_{11}| - Power plane Bottom \]
$L_{EQ}$ vs $h_1$ for Different Capacitor Distances from IC

$|Z_{11}| = \omega L_{EQ}$

$|Z_{11}|$ - Effect of Cap Distance from IC Via Field

$L_{EQ}$ vs $h_1$ for Different Capacitor Return Via Spacing

$|Z_{11}| = \omega L_{EQ}$

$X$ (mils)
- 50
- 100
- 300 - Use IC GND via

$|Z_{11}|$ - Capacitor Return Via Spacing
Conclusions

• The case study demonstrates an innovative principle behind the guidelines, to lower the input impedance of PDN by lowering the $L_{EQ}$ and $L_{IC}$.

• The guidelines show a process to minimize the $L_{IC}$ and $L_{EQ}$ during the layout phase. $L_{IC}$ being the lowest value that $L_{EQ}$ can achieve, it $L_{IC}$ should be minimized at first.
  – The power plane should be placed closest to IC to achieve lowest $L_{IC}$ and capacitors should be placed closest to the power planes, for a low $L_{EQ}$.
  – A return plane should be placed as close as possible to the power plane in the PCB stack up, to lower the inductance contribution form the planes to the $L_{EQ}$.
  – A return via should be placed as close as possible to every capacitor power via.
  – The capacitors should be placed around the IC as close as possible to it, when the distance between the capacitor and power planes is small. In thick boards with thin power cavities, the distance of capacitors from the IC will not significantly affect the results.

• Trends provide an intuition for comparative rate of increase in the $L_{IC}$ and $L_{EQ}$ values for different layout geometry aspects. This helps to make tradeoffs when layout is for multiple power nets sharing limited resources.

Thank You
References

Physics – Mid PWR Layer – Top Cap vs Cap sharing IC vias

Reference Plane Distance – Current Path for All Reference Planes Present
Reference Plane Distance – Current Path for No Close Reference Planes