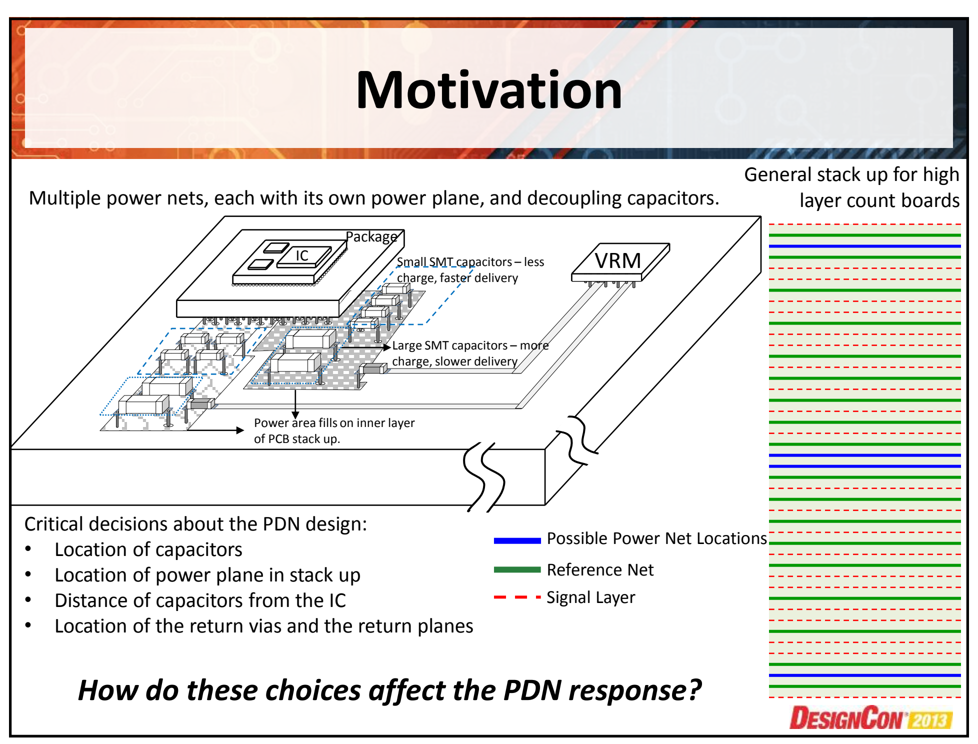
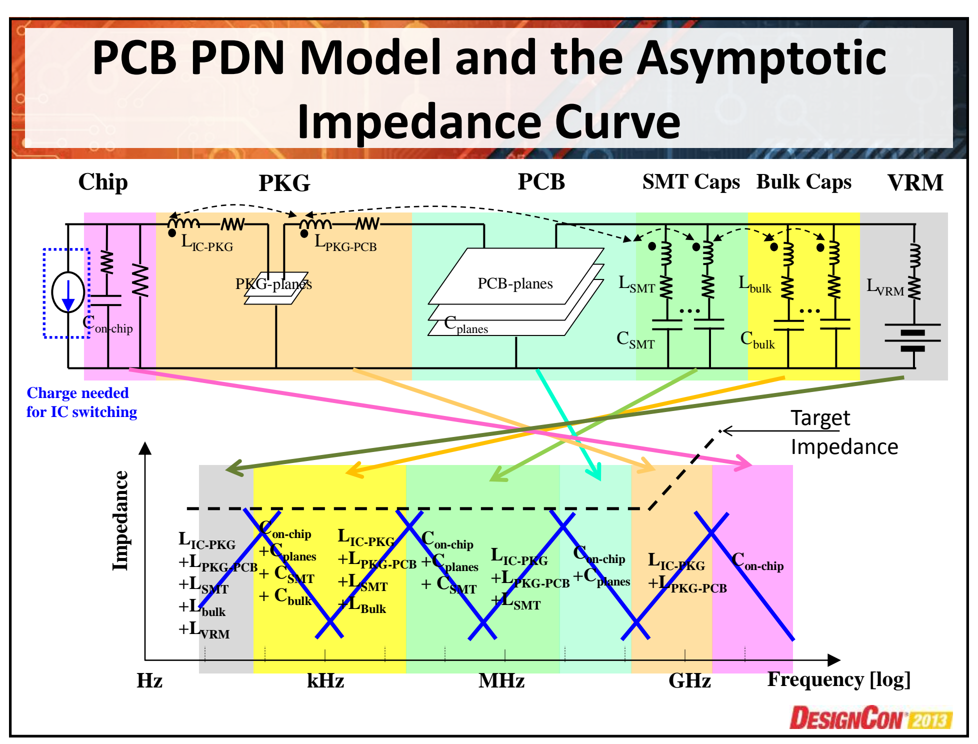
DesignCon® 2013
JANUARY 28-31, 2013
SANTA CLARA CONVENTION CENTER
Innovative PDN Design Guidelines for Practical High Layer-Count PCBs
Session 11 - WA - 1
Ketan Shringarpure, Siming Pan, Jingook Kim, Brice Achkir, Bruce Archambeault, Jun Fan and James Drewniak
EMC
cisco
IBM
UNIST
UBM Tech

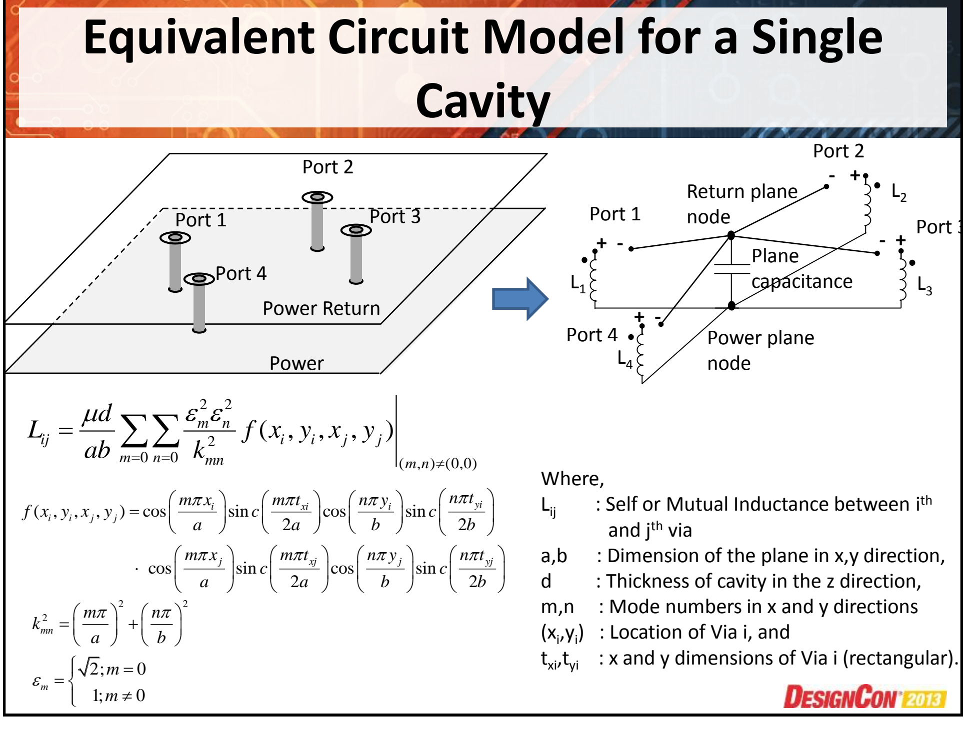

Motivation
Multiple power nets, each with its own power plane, and decoupling capacitors.
General stack up for high layer count boards
Package
IC
Small SMT capacitors – less charge, faster delivery
VRM
Large SMT capacitors – more charge, slower delivery
Power area fills on inner layer of PCB stack up.
Critical decisions about the PDN design:
• Location of capacitors
• Location of power plane in stack up
• Distance of capacitors from the IC
• Location of the return vias and the return planes
Possible Power Net Locations
Reference Net
Signal Layer
How do these choices affect the PDN response?
DesignCon 2013

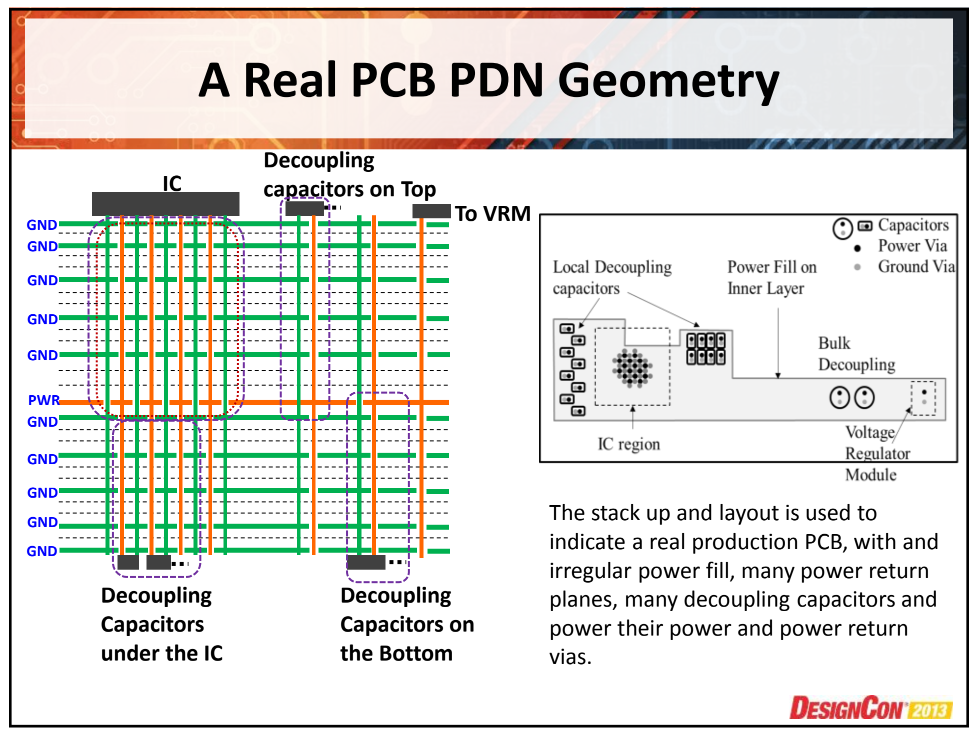
Outline

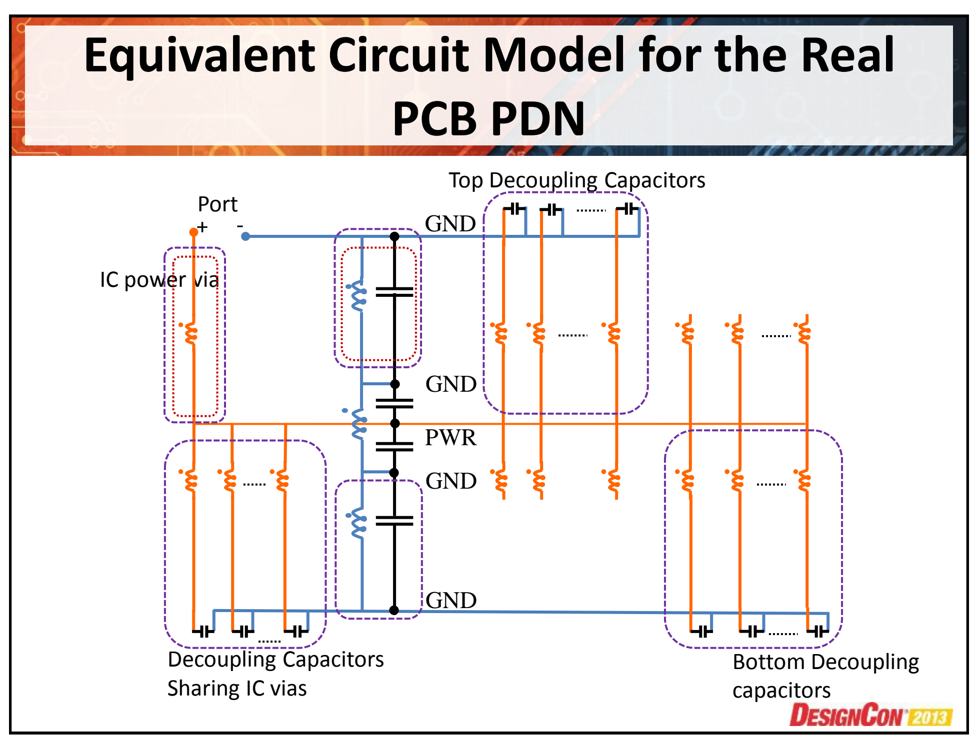
- Physics Based Model for Real PCB PDNs
- L_{EQ} and L_{IC} using the Geometry – Model – Response Paradigm
- Case Studies for Design Guidelines
- Trends in L_{EQ} and L_{IC} with Change PCB Stack Up Thickness
- Conclusions

DESIGNCON 2013

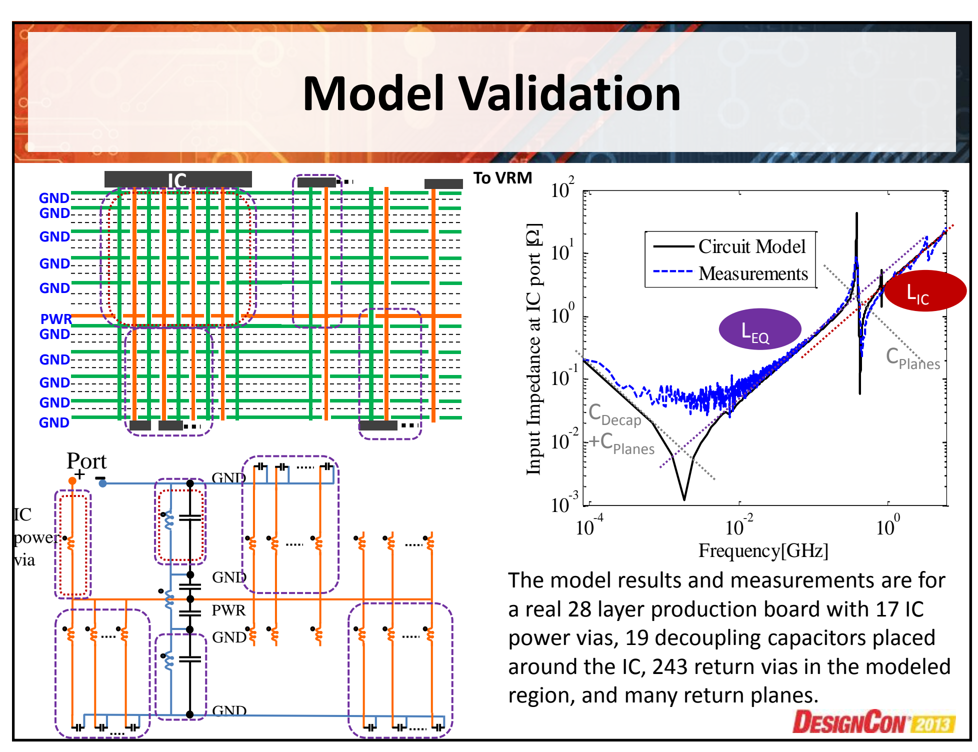



Equivalent Circuit Model for a Single Cavity
Port 2
Port 1
Port 3
Port 4
Power Return
Power
Return plane node
Plane capacitance
Power plane node
L_1
L_2
L_3
L_4
$$L_{ij} = \frac{\mu d}{ab}\sum_{m=0}\sum_{n=0}\frac{\varepsilon_m^2\varepsilon_n^2}{k_{mn}^2} f(x_i, y_i, x_j, y_j)\Big|_{(m,n)\neq(0,0)}$$
$$f(x_i, y_i, x_j, y_j) = \cos\left(\frac{m\pi x_i}{a}\right)\operatorname{sinc}\left(\frac{m\pi t_{xi}}{2a}\right)\cos\left(\frac{n\pi y_i}{b}\right)\operatorname{sinc}\left(\frac{n\pi t_{yi}}{2b}\right) \cdot \cos\left(\frac{m\pi x_j}{a}\right)\operatorname{sinc}\left(\frac{m\pi t_{xj}}{2a}\right)\cos\left(\frac{n\pi y_j}{b}\right)\operatorname{sinc}\left(\frac{n\pi t_{yj}}{2b}\right)$$
$$k_{mn}^2 = \left(\frac{m\pi}{a}\right)^2 + \left(\frac{n\pi}{b}\right)^2$$
$$\varepsilon_m = \begin{cases}\sqrt{2}; m=0 \\ 1; m\neq 0\end{cases}$$
Where,
L_{ij} : Self or Mutual Inductance between i^{th} and j^{th} via
a,b : Dimension of the plane in x,y direction,
d : Thickness of cavity in the z direction,
m,n : Mode numbers in x and y directions
(x_i,y_i) : Location of Via i, and
t_{xi},t_{yi} : x and y dimensions of Via i (rectangular).
DesignCon 2013

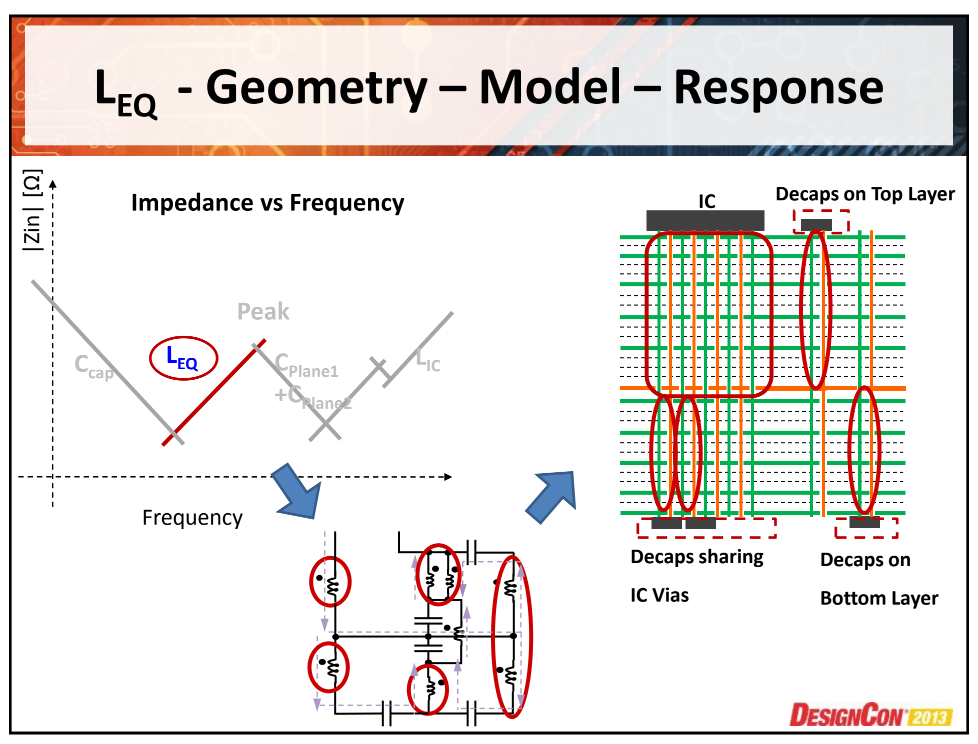

A Real PCB PDN Geometry
IC
Decoupling capacitors on Top
To VRM
GND
PWR
Decoupling Capacitors under the IC
Decoupling Capacitors on the Bottom
Capacitors
Power Via
Ground Via
Local Decoupling capacitors
Power Fill on Inner Layer
Bulk Decoupling
IC region
Voltage Regulator Module
The stack up and layout is used to indicate a real production PCB, with and irregular power fill, many power return planes, many decoupling capacitors and power their power and power return vias.
DesignCon 2013



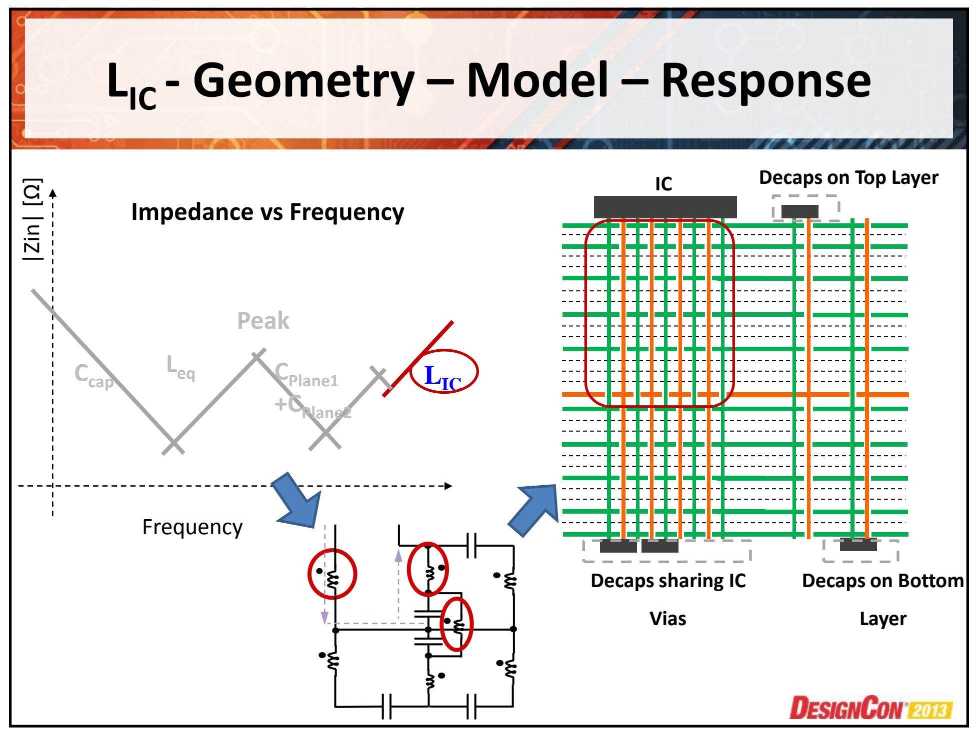
Equivalent Circuit Model for the Real PCB PDN
Top Decoupling Capacitors
Port
IC power via
GND
GND
PWR
GND
GND
Decoupling Capacitors Sharing IC vias
Bottom Decoupling capacitors
DesignCon 2013



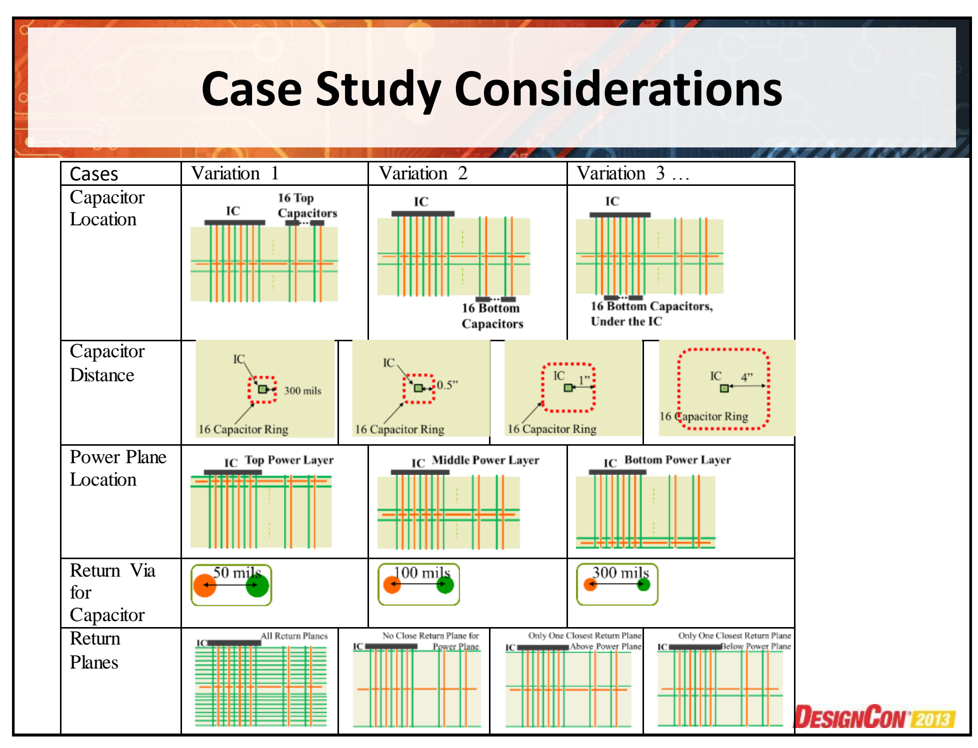
Model Validation
IC
To VRM
GND
PWR
Port
IC power via
Circuit Model
Measurements
Input Impedance at IC port [Ω]
Frequency[GHz]
The model results and measurements are for a real 28 layer production board with 17 IC power vias, 19 decoupling capacitors placed around the IC, 243 return vias in the modeled region, and many return planes.
DesignCon 2013

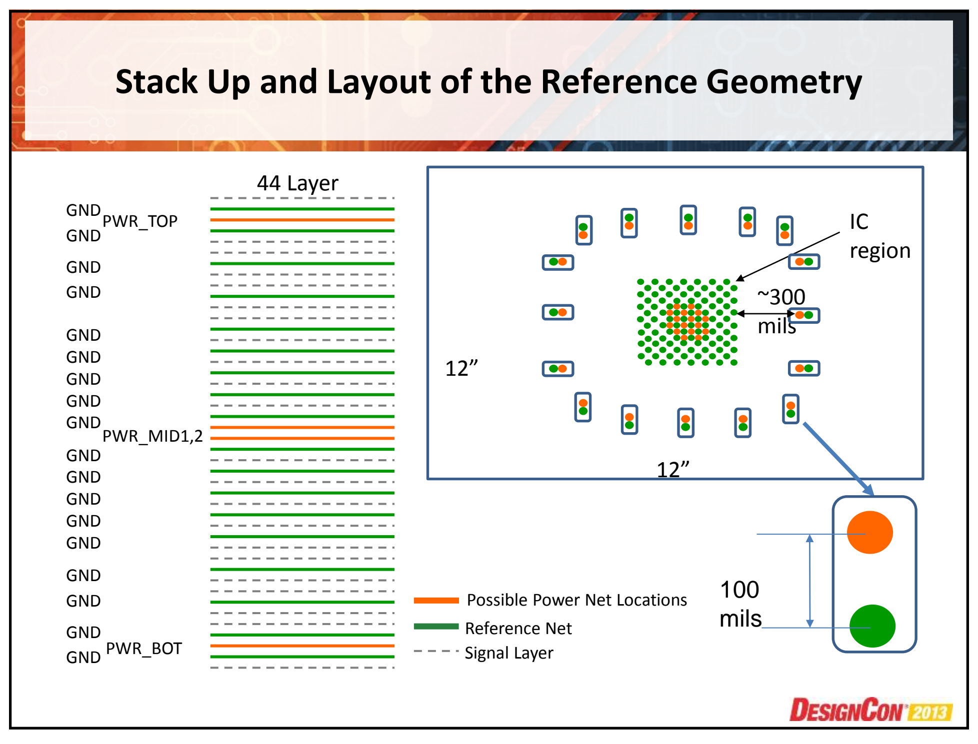


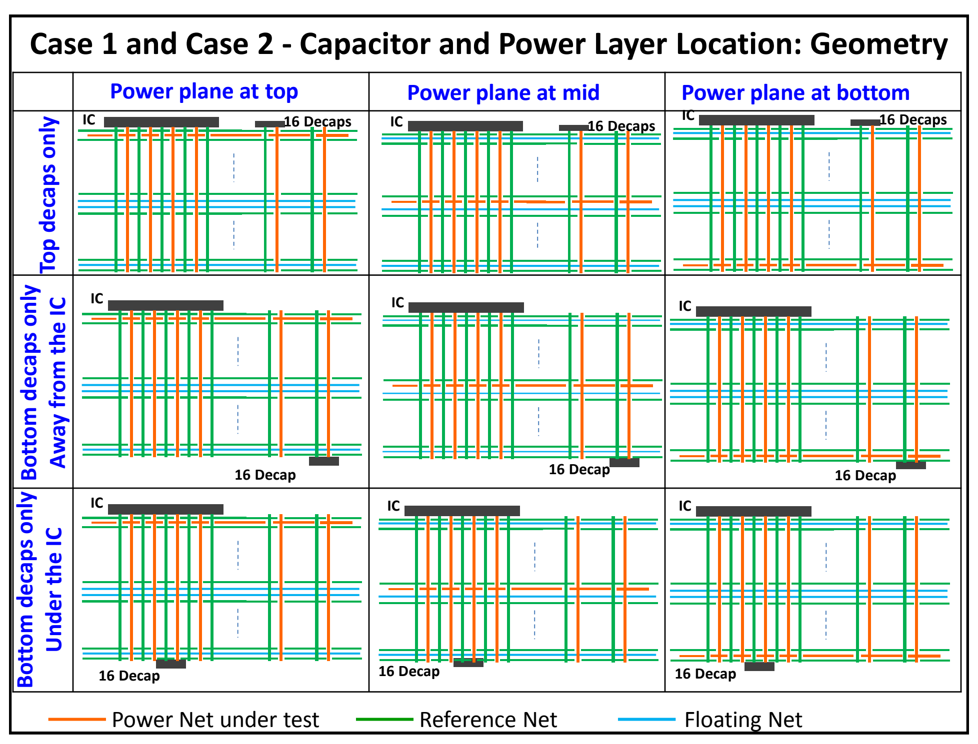
L_{EQ} - Geometry – Model – Response
Impedance vs Frequency
|Zin| [Ω]
Peak
Ccap
LEQ
CPlane1
+CPlane2
LIC
Frequency
IC
Decaps on Top Layer
Decaps sharing
IC Vias
Decaps on
Bottom Layer
DesignCon 2013

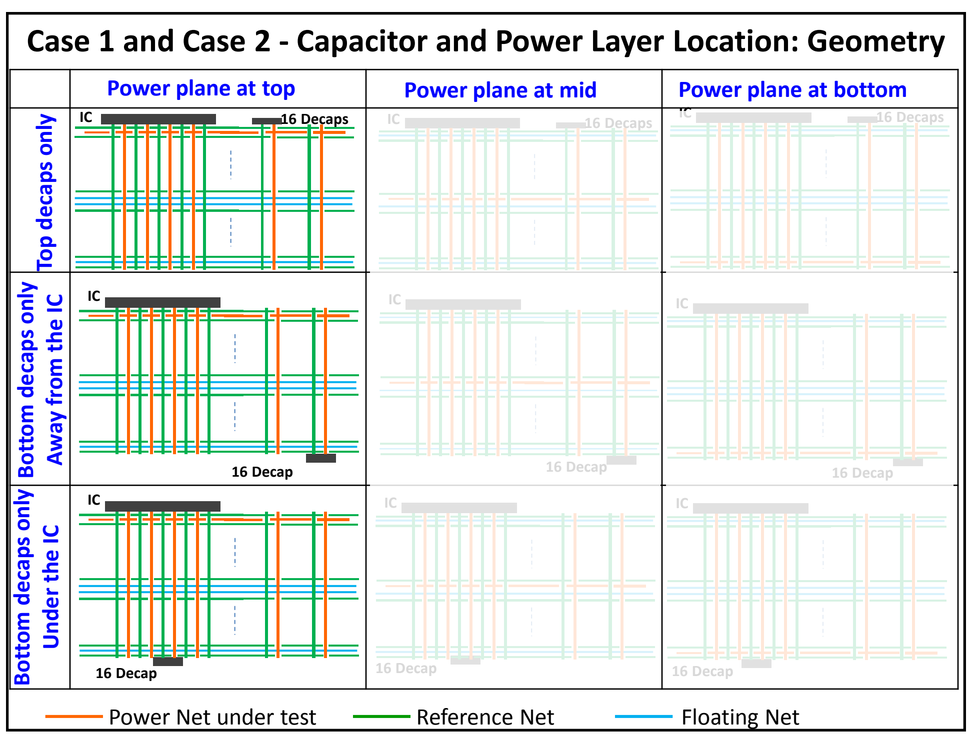


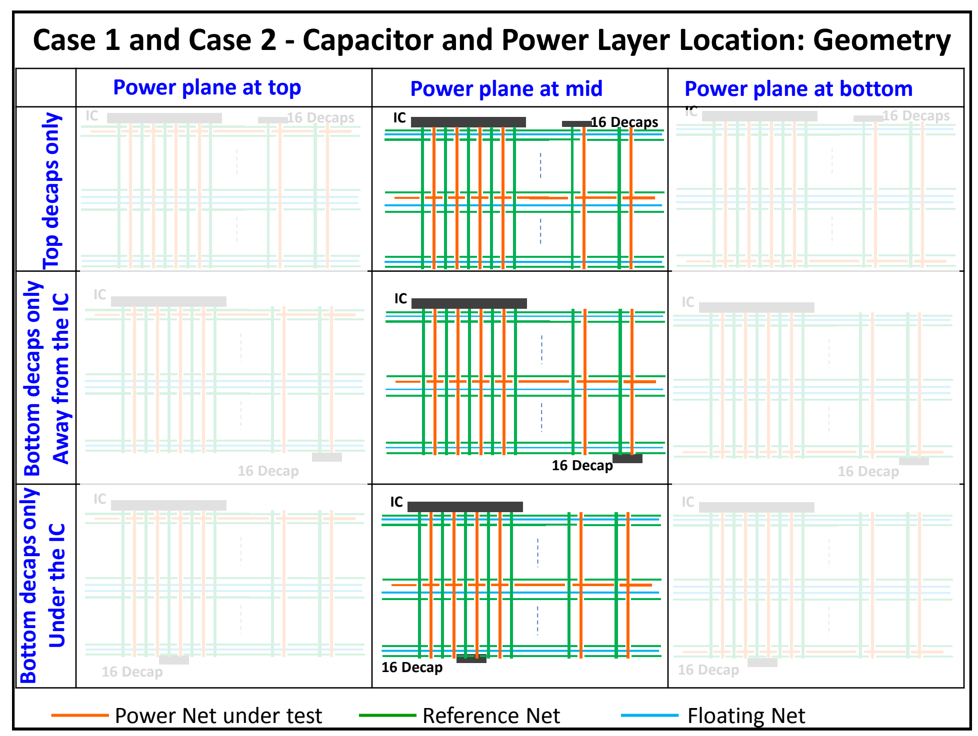
L_{IC} - Geometry – Model – Response
Impedance vs Frequency
|Zin| [Ω]
Peak
Ccap
Leq
CPlane1
+CPlane2
LIC
Frequency
IC
Decaps on Top Layer
Decaps sharing IC
Vias
Decaps on Bottom
Layer
DesignCon 2013


Case Study Considerations
Cases
Variation 1
Variation 2
Variation 3 …
Capacitor Location
IC
16 Top Capacitors
16 Bottom Capacitors
16 Bottom Capacitors, Under the IC
Capacitor Distance
300 mils
0.5"
1"
4"
16 Capacitor Ring
Power Plane Location
Top Power Layer
Middle Power Layer
Bottom Power Layer
Return Via for Capacitor
50 mils
100 mils
300 mils
Return Planes
All Return Planes
No Close Return Plane for Power Plane
Only One Closest Return Plane Above Power Plane
Only One Closest Return Plane Below Power Plane
DesignCon 2013

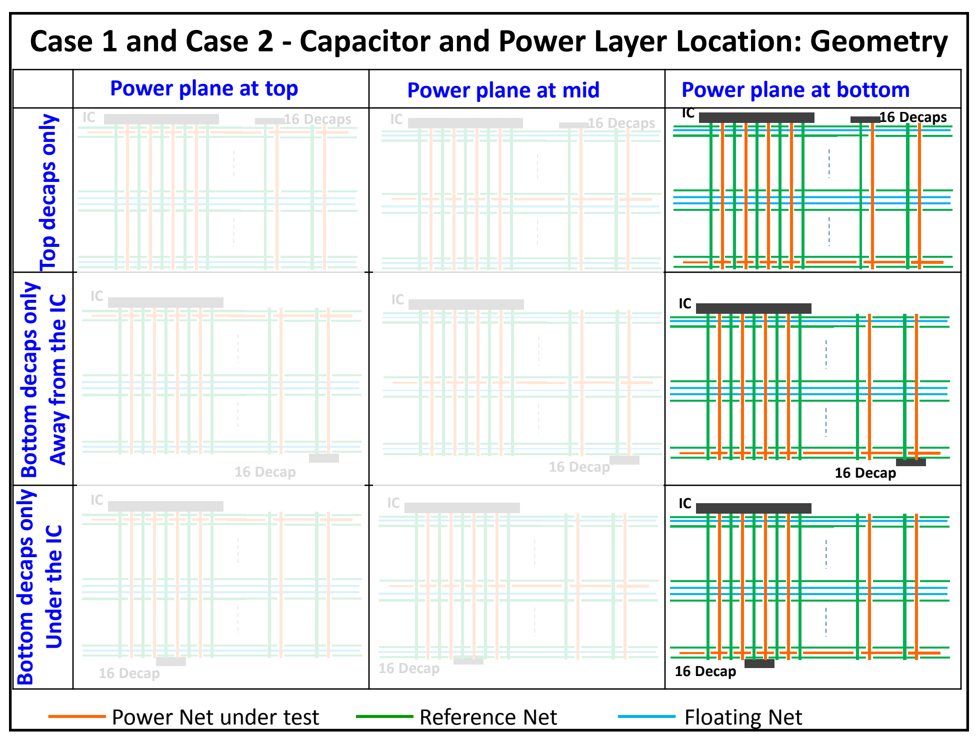

Stack Up and Layout of the Reference Geometry
44 Layer
GND
PWR_TOP
PWR_MID1,2
PWR_BOT
IC region
~300 mils
12"
12"
100 mils
Possible Power Net Locations
Reference Net
Signal Layer
DesignCon 2013


Case 1 and Case 2 - Capacitor and Power Layer Location: Geometry
Power plane at top
Power plane at mid
Power plane at bottom
Top decaps only
Bottom decaps only Away from the IC
Bottom decaps only Under the IC
IC
16 Decaps
16 Decap
Power Net under test
Reference Net
Floating Net

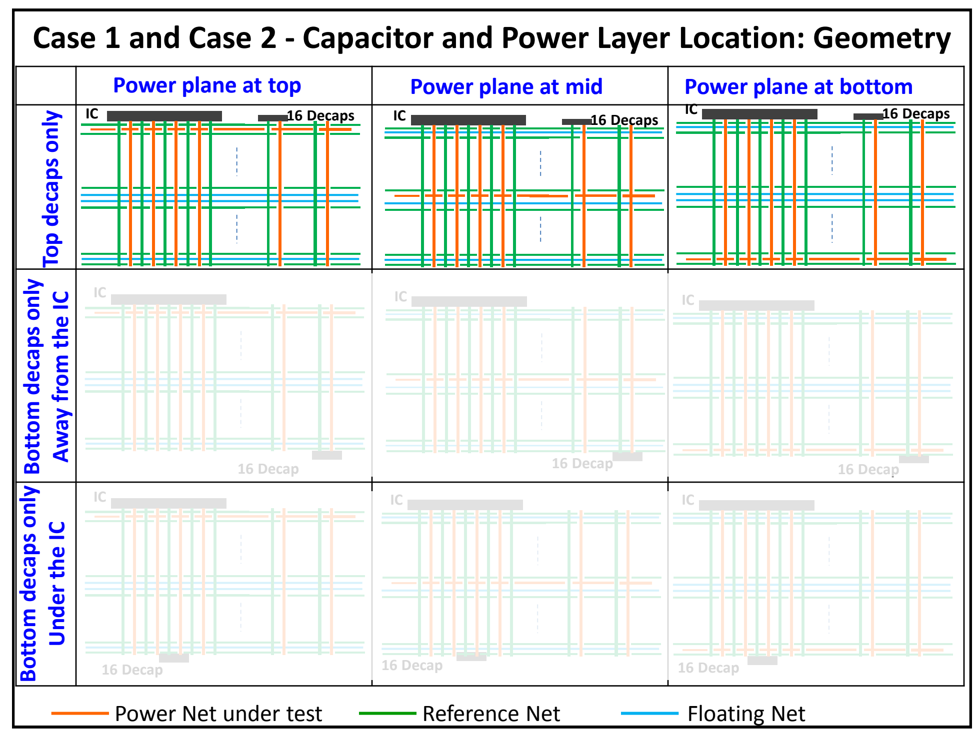

Case 1 and Case 2 - Capacitor and Power Layer Location: Geometry
Power plane at top
Power plane at mid
Power plane at bottom
Top decaps only
Bottom decaps only Away from the IC
Bottom decaps only Under the IC
IC
16 Decaps
16 Decap
Power Net under test
Reference Net
Floating Net



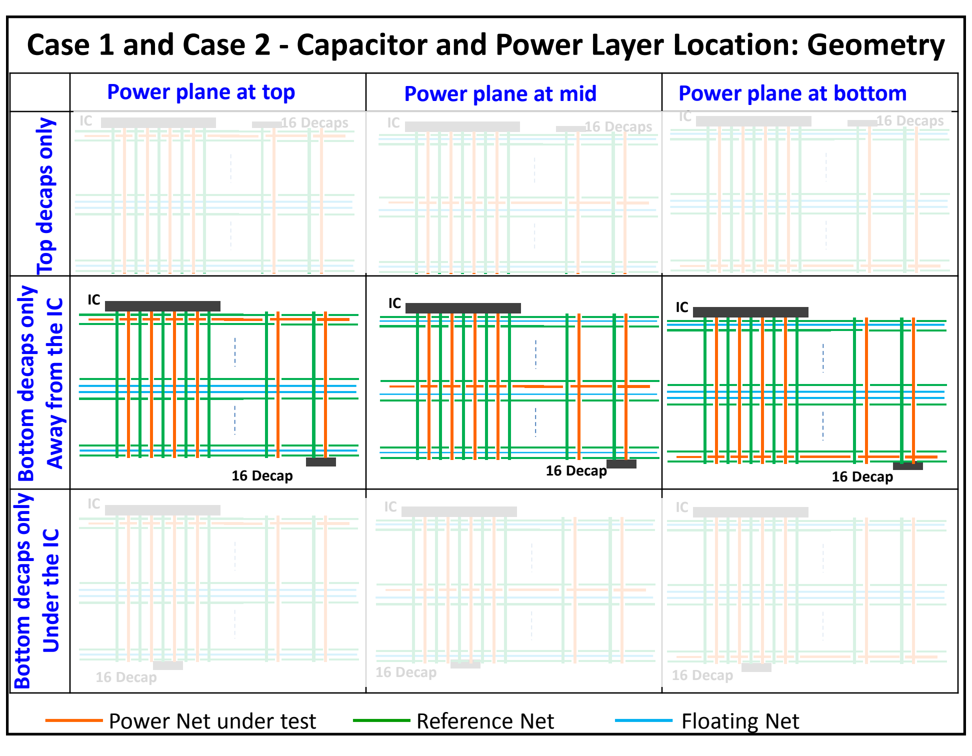
Case 1 and Case 2 - Capacitor and Power Layer Location: Geometry
Power plane at top
Power plane at mid
Power plane at bottom
Top decaps only
Bottom decaps only Away from the IC
Bottom decaps only Under the IC
IC
16 Decaps
16 Decap
Power Net under test
Reference Net
Floating Net



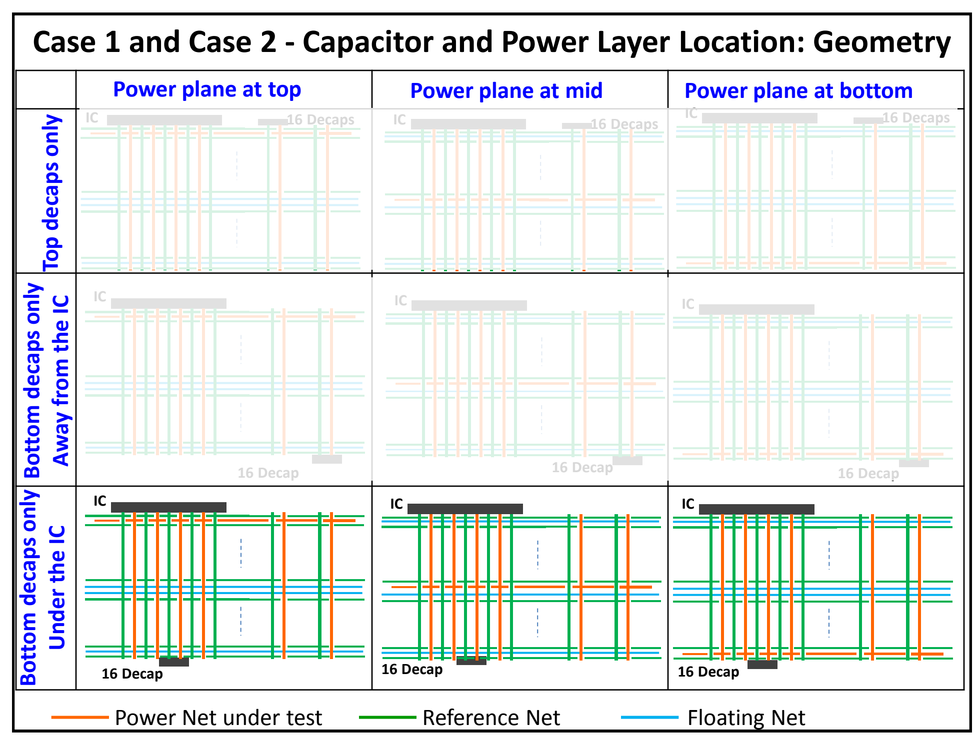
Case 1 and Case 2 - Capacitor and Power Layer Location: Geometry
Power plane at top
Power plane at mid
Power plane at bottom
Top decaps only
Bottom decaps only Away from the IC
Bottom decaps only Under the IC
IC
16 Decaps
16 Decap
Power Net under test
Reference Net
Floating Net

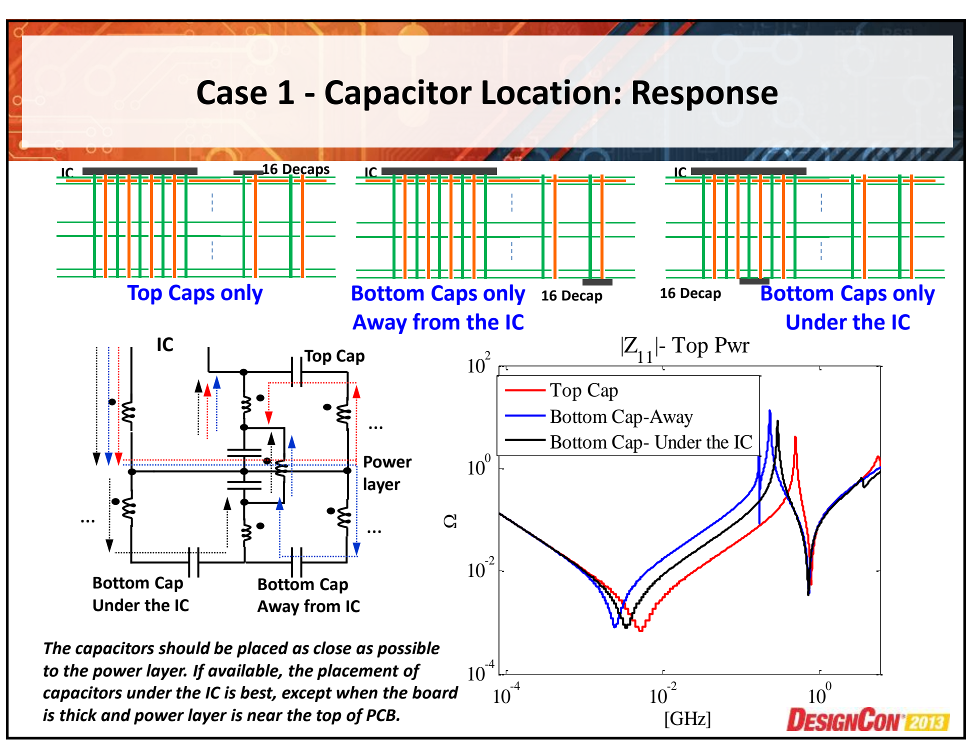


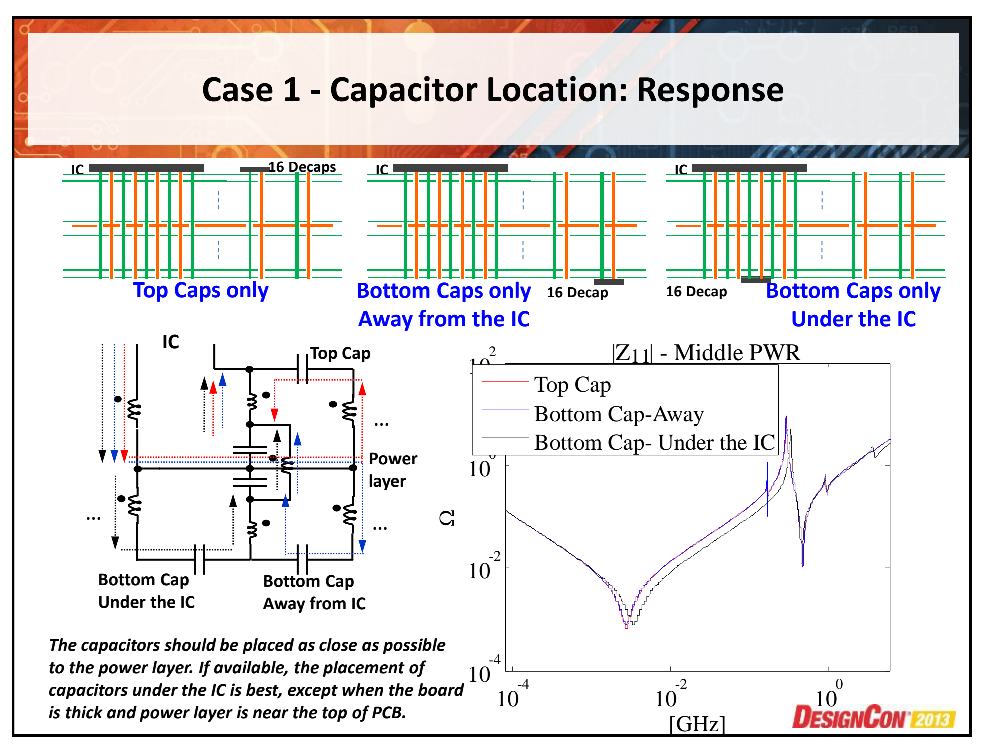
Case 1 and Case 2 - Capacitor and Power Layer Location: Geometry
Power plane at top
Power plane at mid
Power plane at bottom
Top decaps only
Bottom decaps only Away from the IC
Bottom decaps only Under the IC
IC
16 Decaps
16 Decap
Power Net under test
Reference Net
Floating Net

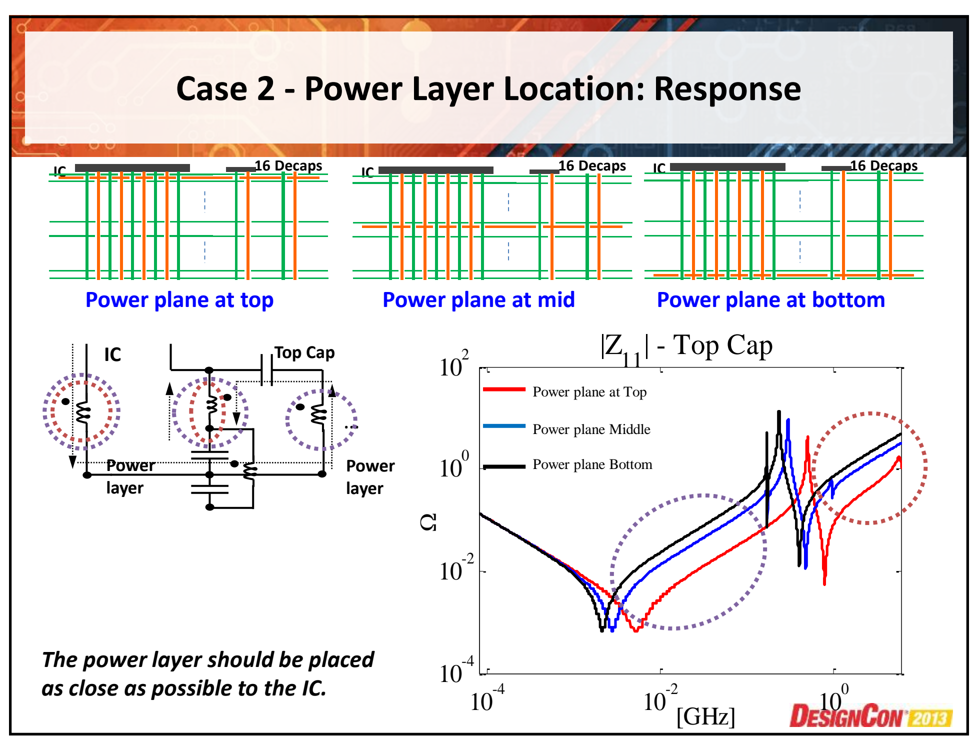


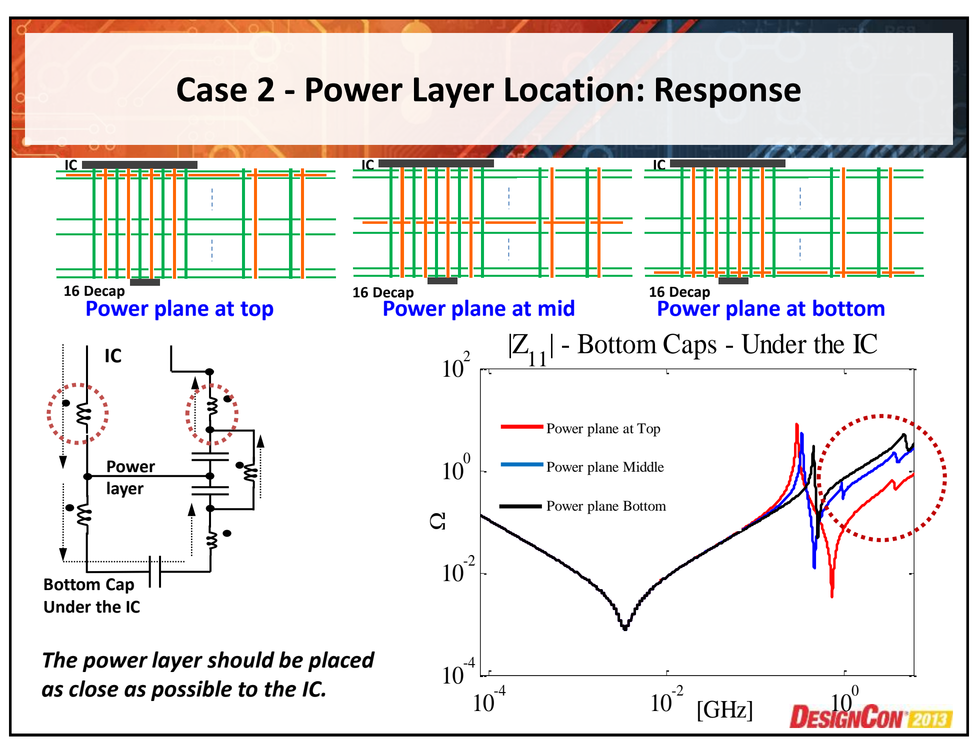
Case 1 and Case 2 - Capacitor and Power Layer Location: Geometry
Power plane at top
Power plane at mid
Power plane at bottom
Top decaps only
Bottom decaps only Away from the IC
Bottom decaps only Under the IC
IC
16 Decaps
16 Decap
Power Net under test
Reference Net
Floating Net


Case 1 and Case 2 - Capacitor and Power Layer Location: Geometry
Power plane at top
Power plane at mid
Power plane at bottom
Top decaps only
Bottom decaps only
Away from the IC
Bottom decaps only
Under the IC
IC
16 Decaps
16 Decap
Power Net under test
Reference Net
Floating Net

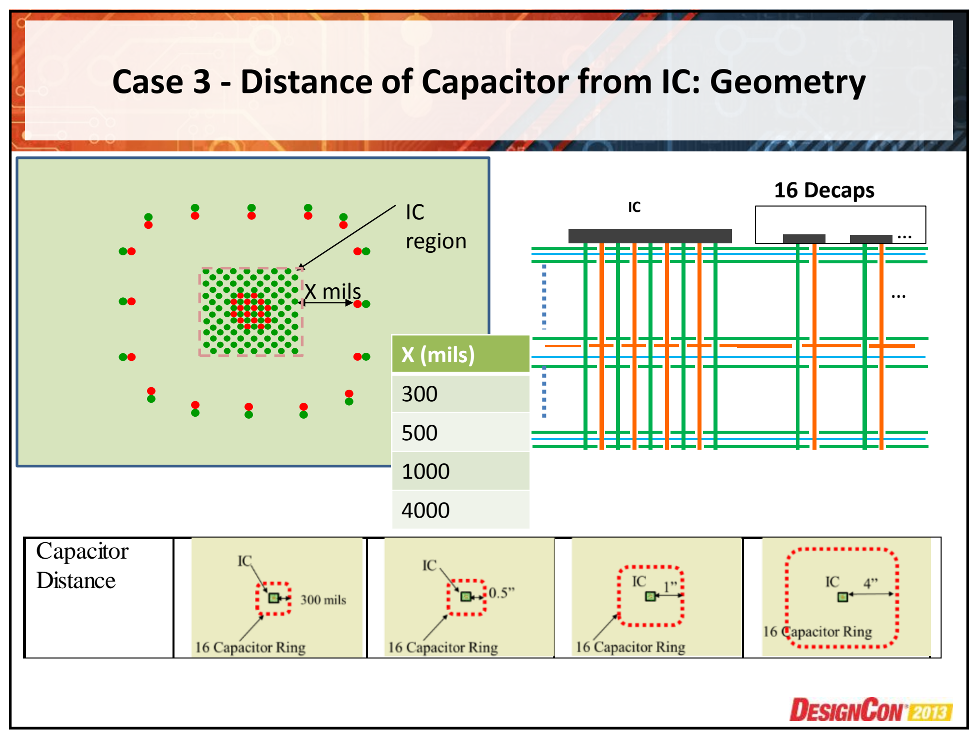

Case 1 - Capacitor Location: Response
IC
16 Decaps
16 Decap
Top Caps only
Bottom Caps only
Away from the IC
Bottom Caps only
Under the IC
Top Cap
Power
layer
Bottom Cap
Under the IC
Bottom Cap
Away from IC
|Z11|- Top Pwr
Top Cap
Bottom Cap-Away
Bottom Cap- Under the IC
Ω
[GHz]
The capacitors should be placed as close as possible to the power layer. If available, the placement of capacitors under the IC is best, except when the board is thick and power layer is near the top of PCB.
DesignCon 2013


Case 1 - Capacitor Location: Response
IC
16 Decaps
Top Caps only
Bottom Caps only
Away from the IC
16 Decap
Bottom Caps only
Under the IC
Top Cap
Power
layer
Bottom Cap
Under the IC
Bottom Cap
Away from IC
|Z11| - Middle PWR
Top Cap
Bottom Cap-Away
Bottom Cap- Under the IC
Ω
[GHz]
The capacitors should be placed as close as possible to the power layer. If available, the placement of capacitors under the IC is best, except when the board is thick and power layer is near the top of PCB.
DesignCon 2013

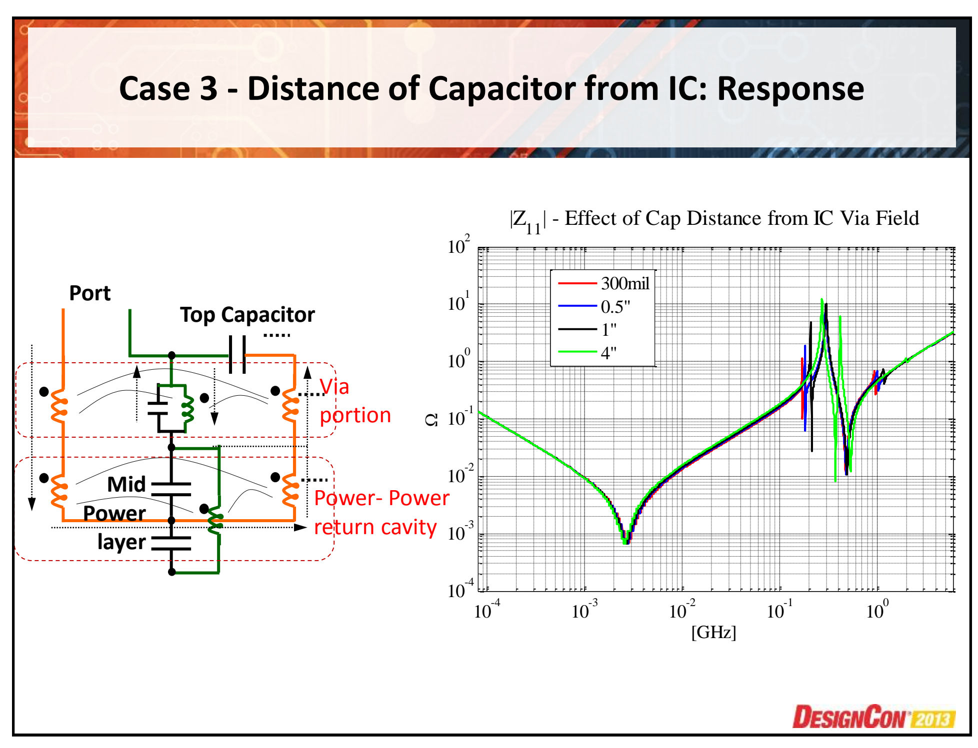

Case 2 - Power Layer Location: Response
IC
16 Decaps
Power plane at top
Power plane at mid
Power plane at bottom
Top Cap
Power
layer
|Z11| - Top Cap
Power plane at Top
Power plane Middle
Power plane Bottom
Ω
[GHz]
The power layer should be placed as close as possible to the IC.
DesignCon 2013



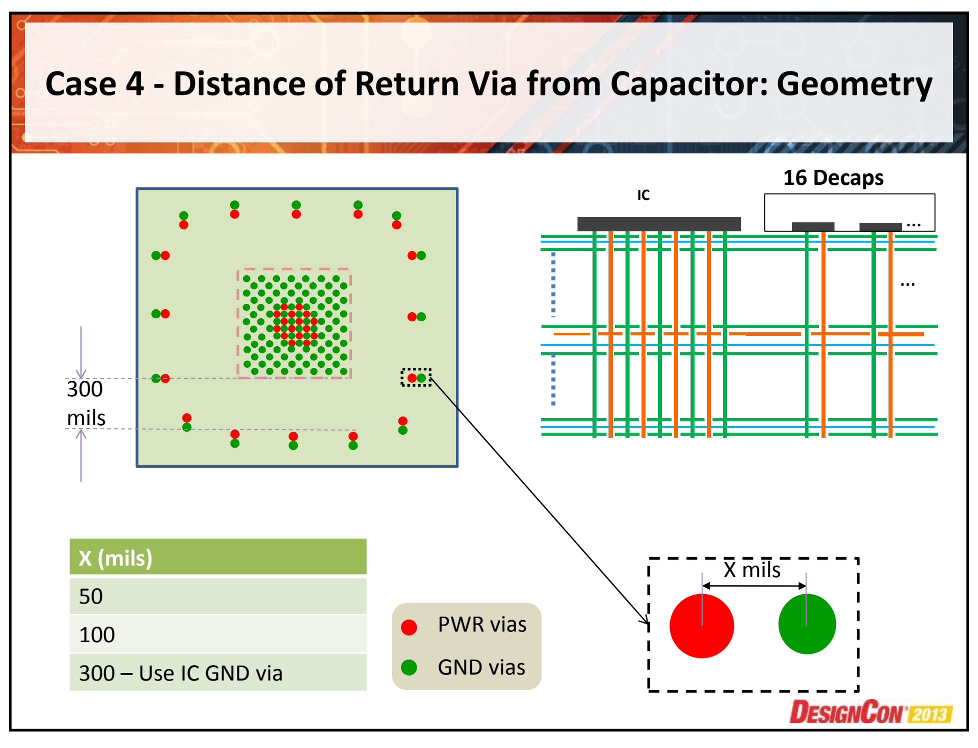
Case 2 - Power Layer Location: Response
IC
16 Decap
Power plane at top
Power plane at mid
Power plane at bottom
IC
Power layer
Bottom Cap Under the IC
The power layer should be placed as close as possible to the IC.
|Z11| - Bottom Caps - Under the IC
Power plane at Top
Power plane Middle
Power plane Bottom
Ω
[GHz]
DesignCon 2013



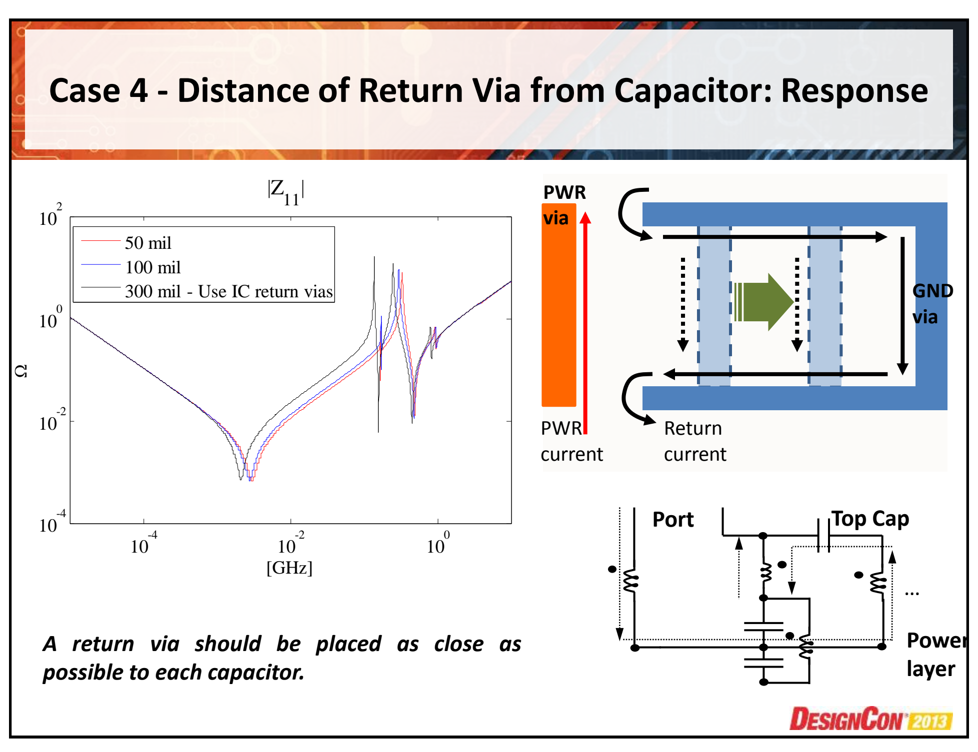
Case 3 - Distance of Capacitor from IC: Geometry
IC region
X mils
X (mils)
300
500
1000
4000
16 Decaps
IC
Capacitor Distance
IC
300 mils
0.5"
1"
4"
16 Capacitor Ring
DesignCon 2013

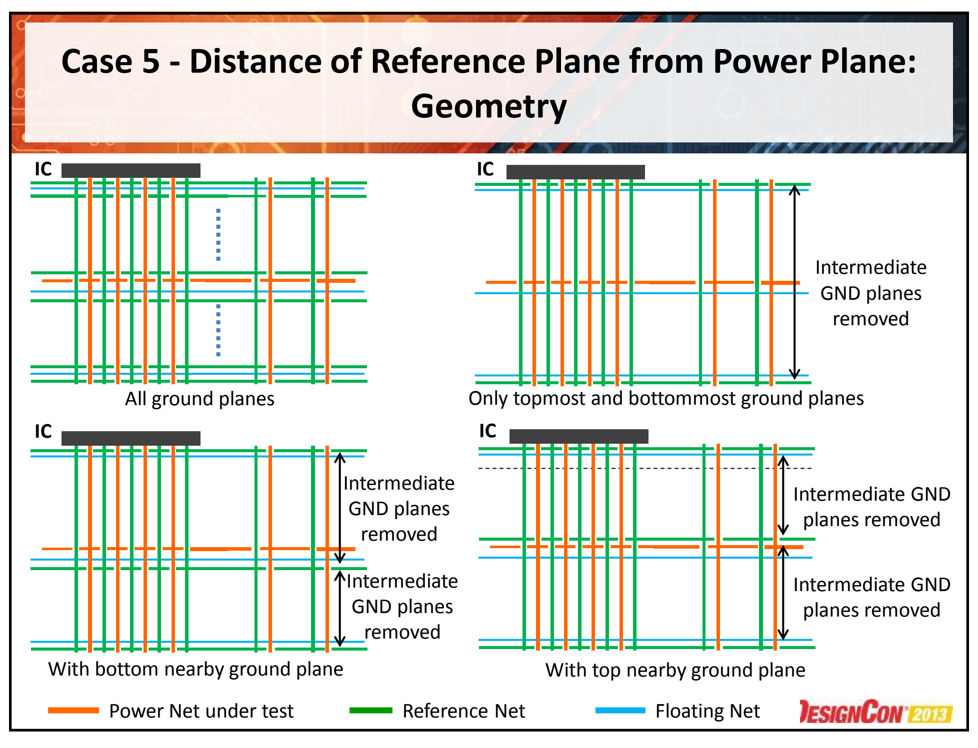


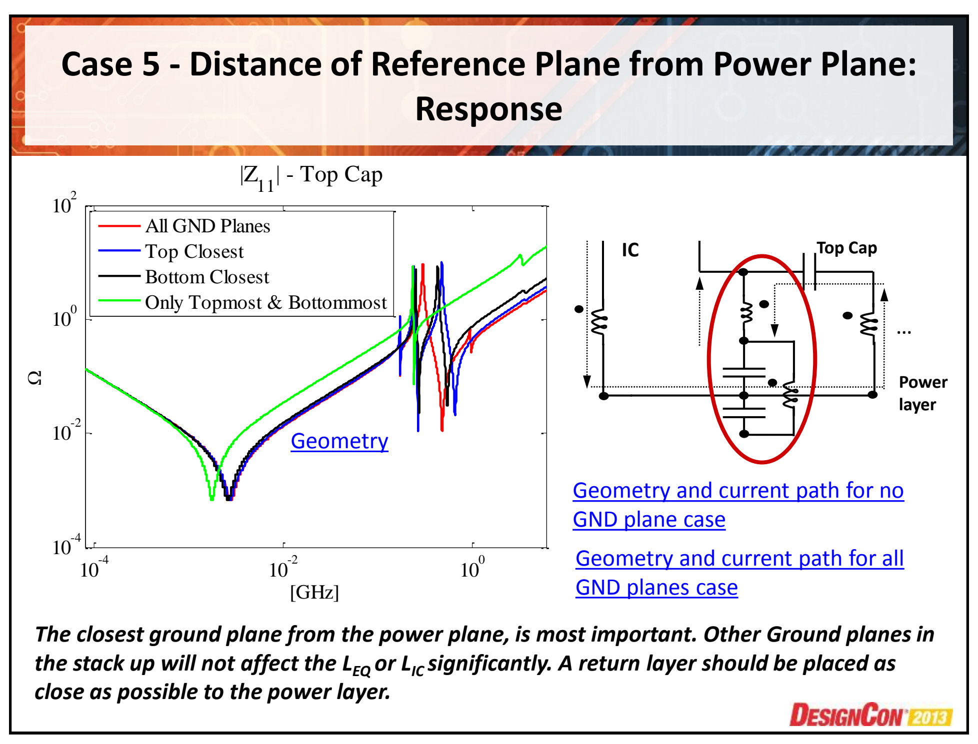
Case 3 - Distance of Capacitor from IC: Response
Port
Top Capacitor
Via portion
Mid Power layer
Power- Power return cavity
|Z11| - Effect of Cap Distance from IC Via Field
300mil
0.5"
1"
4"
Ω
[GHz]
DesignCon 2013



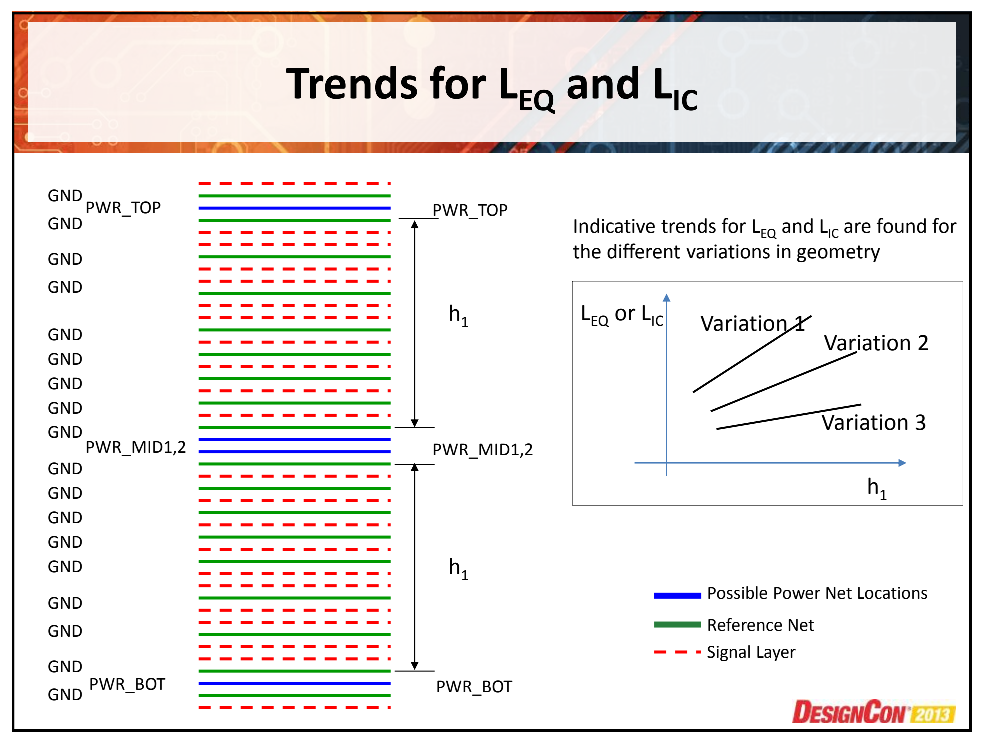
Case 4 - Distance of Return Via from Capacitor: Geometry
300 mils
IC
16 Decaps
X (mils)
50
100
300 – Use IC GND via
PWR vias
GND vias
X mils
DesignCon 2013


Case 4 - Distance of Return Via from Capacitor: Response
|Z11|
50 mil
100 mil
300 mil - Use IC return vias
Ω
[GHz]
PWR via
GND via
PWR current
Return current
Port
Top Cap
Power layer
A return via should be placed as close as possible to each capacitor.
DesignCon 2013

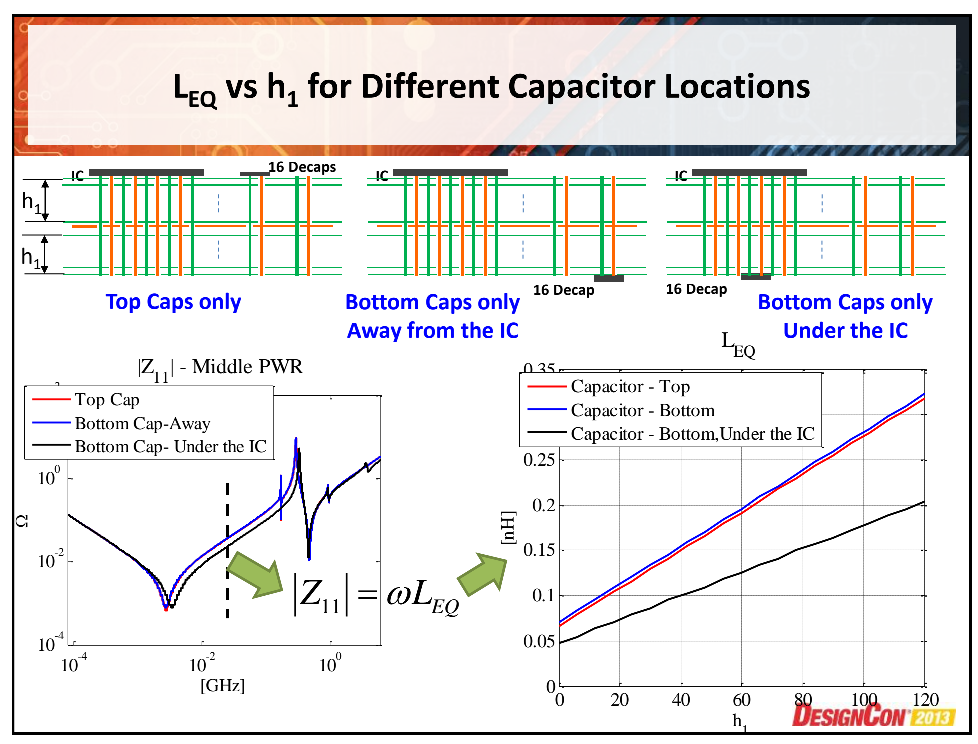

Case 5 - Distance of Reference Plane from Power Plane: Geometry
IC
All ground planes
Only topmost and bottommost ground planes
Intermediate GND planes removed
With bottom nearby ground plane
With top nearby ground plane
Intermediate GND planes removed
Power Net under test
Reference Net
Floating Net
DesignCon 2013

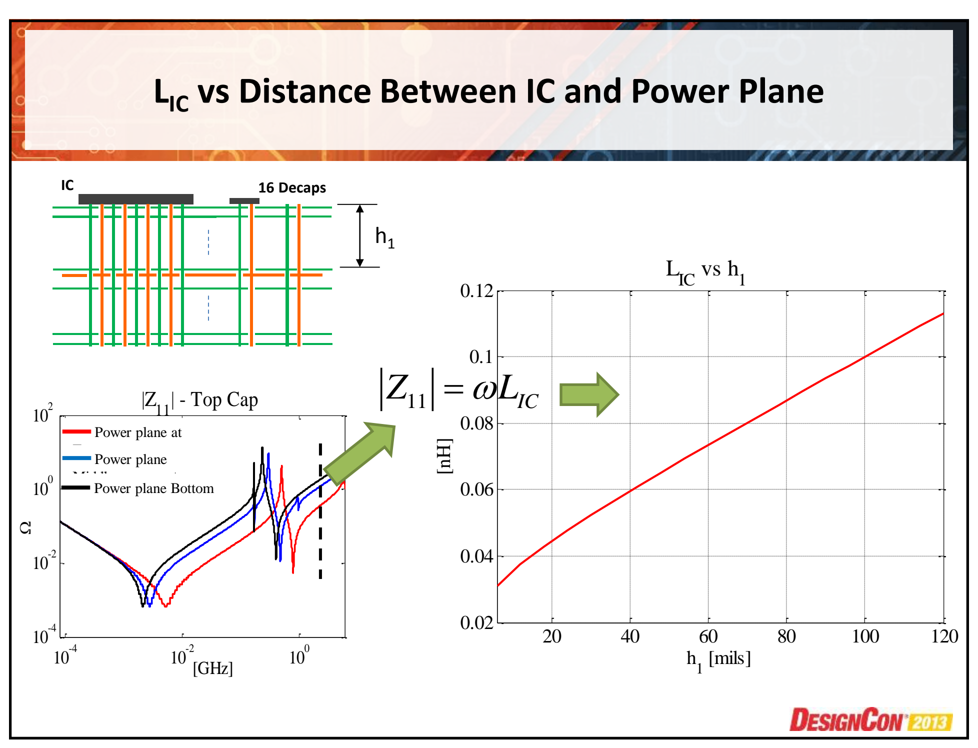


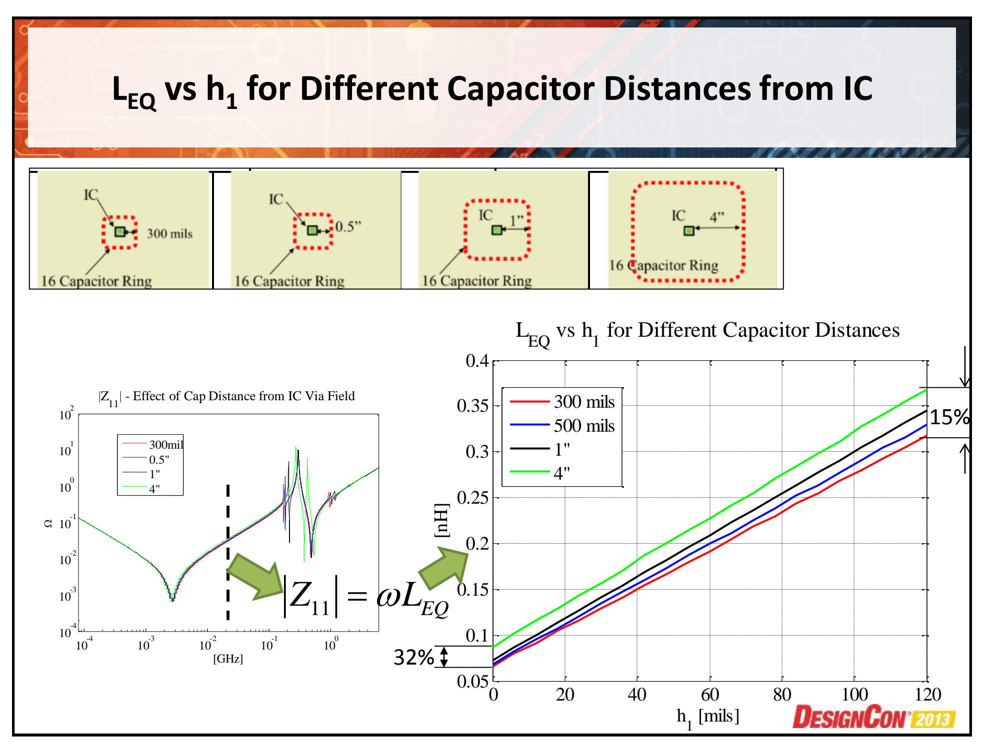
Case 5 - Distance of Reference Plane from Power Plane: Response
|Z11| - Top Cap
All GND Planes
Top Closest
Bottom Closest
Only Topmost & Bottommost
Geometry
[GHz]
Ω
IC
Top Cap
Power layer
Geometry and current path for no GND plane case
Geometry and current path for all GND planes case
The closest ground plane from the power plane, is most important. Other Ground planes in the stack up will not affect the L_EQ or L_IC significantly. A return layer should be placed as close as possible to the power layer.
DesignCon 2013



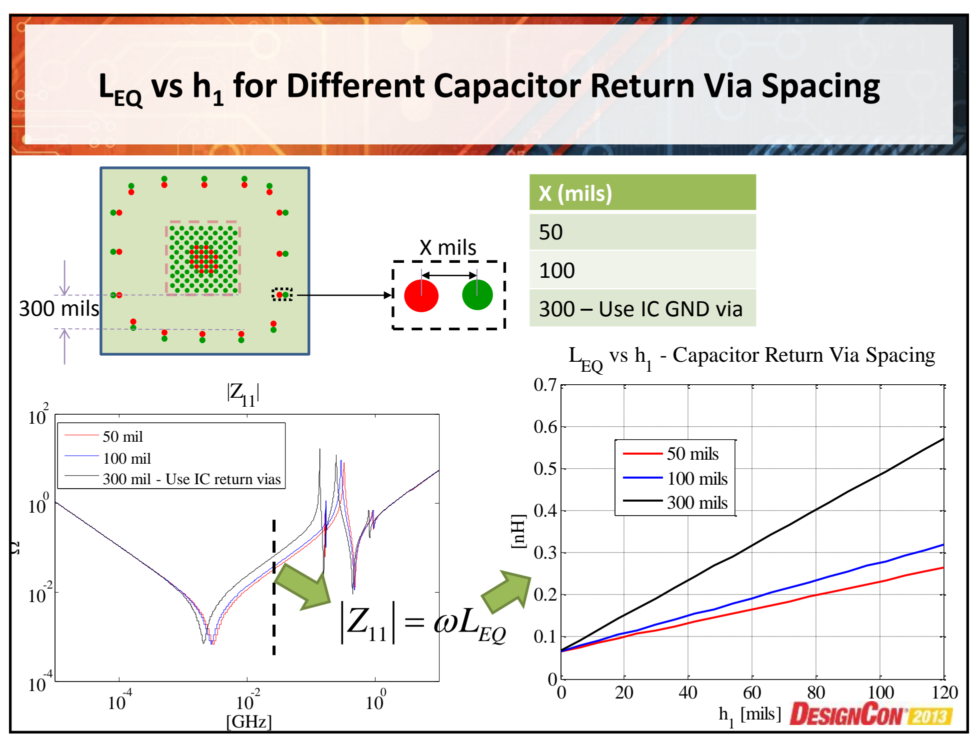
Trends for L_EQ and L_IC
GND
PWR_TOP
PWR_MID1,2
PWR_BOT
h1
Indicative trends for L_EQ and L_IC are found for the different variations in geometry
L_EQ or L_IC
Variation 1
Variation 2
Variation 3
Possible Power Net Locations
Reference Net
Signal Layer
DesignCon 2013


L_{EQ} vs h_1 for Different Capacitor Locations
IC
16 Decaps
h_1
h_1
Top Caps only
IC
16 Decap
Bottom Caps only
Away from the IC
IC
16 Decap
Bottom Caps only
Under the IC
$|Z_{11}|$ - Middle PWR
Top Cap
Bottom Cap-Away
Bottom Cap- Under the IC
Ω
[GHz]
$|Z_{11}| = \omega L_{EQ}$
L_{EQ}
Capacitor - Top
Capacitor - Bottom
Capacitor - Bottom,Under the IC
[nH]
h_1
DesignCon 2013


L_{IC} vs Distance Between IC and Power Plane
IC
16 Decaps
h_1
$|Z_{11}|$ - Top Cap
Power plane at
Power plane
Power plane Bottom
Ω
[GHz]
$|Z_{11}| = \omega L_{IC}$
L_{IC} vs h_1
[nH]
h_1 [mils]
DesignCon 2013



L_{EQ} vs h_1 for Different Capacitor Distances from IC
IC
300 mils
16 Capacitor Ring
IC
0.5”
16 Capacitor Ring
IC
1”
16 Capacitor Ring
IC
4”
16 Capacitor Ring
|Z11| - Effect of Cap Distance from IC Via Field
300mil
0.5"
1"
4"
[GHz]
$|Z_{11}| = \omega L_{EQ}$
L_{EQ} vs h_1 for Different Capacitor Distances
300 mils
500 mils
1"
4"
[nH]
15%
32%
h_1 [mils]
DesignCon 2013



L_{EQ} vs h_1 for Different Capacitor Return Via Spacing
300 mils
X mils
X (mils)
50
100
300 – Use IC GND via
|Z11|
50 mil
100 mil
300 mil - Use IC return vias
[GHz]
$|Z_{11}| = \omega L_{EQ}$
L_{EQ} vs h_1 - Capacitor Return Via Spacing
50 mils
100 mils
300 mils
[nH]
h_1 [mils]
DesignCon 2013

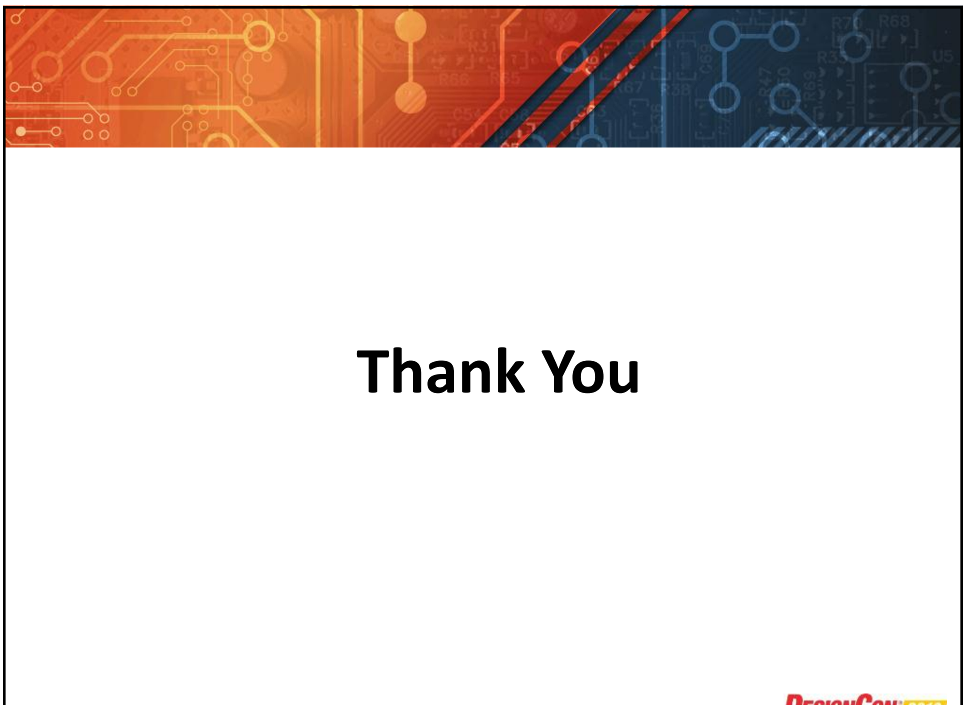
Conclusions

- The case study demonstrates an innovative principle behind the guidelines, to lower the input impedance of PDN by lowering the L_{EQ} and L_{IC}.

- The guidelines show a process to minimize the L_{IC} and L_{EQ} during the layout phase. L_{IC} being the lowest value that L_{EQ} can achieve, it L_{IC} should be minimized at first.
  - The power plane should be placed closest to IC to achieve lowest L_{IC} and capacitors should be placed closest to the power planes, for a low L_{EQ}.
  - A return plane should be placed as close as possible to the power plane in the PCB stack up, to lower the inductance contribution form the planes to the L_{EQ}.
  - A return via should be placed as close as possible to every capacitor power via.
  - The capacitors should be placed around the IC as close as possible to it, when the distance between the capacitor and power planes is small. In thick boards with thin power cavities, the distance of capacitors from the IC will not significantly affect the results.

- Trends provide an intuition for comparative rate of increase in the L_{IC} and L_{EQ} values for different layout geometry aspects. This helps to make tradeoffs when layout is for multiple power nets sharing limited resources.

DesignCon 2013



References

[1] "International Technology Roadmap on Semiconductors," ed. www.itrs.net.

[2] M. Swaminathan, J. Kim, I. Novak, and J. P. Libous, "Power distribution networks for system-on-package: status and challenges," *Advanced Packaging, IEEE Transactions on,* vol. 27, pp. 286-300, 2004.

[3] J. Park, J. Lee, H. Kim, and J. Kim, "Prediction and verification of power/ground plane edge radiation excited by through-hole signal via based on balanced TLM and via coupling model," in *Electrical Performance of Electronic Packaging, 2003*, 2003, pp. 181-184.

[4] L. D. Smith, R. E. Anderson, D. W. Forehand, T. J. Pelc, and T. Roy, "Power distribution system design methodology and capacitor selection for modern CMOS technology," *Advanced Packaging, IEEE Transactions on,* vol. 22, pp. 284-291, 1999.

[5] Jingook Kim; Songping Wu; Hanfeng Wang; Takita, Y.; Takeuchi, H.; Araki, K.; Gang Feng; Jun Fan; , "Improved target impedance and IC transient current measurement for power distribution network design," *Electromagnetic Compatibility (EMC), 2010 IEEE International Symposium on* , vol., no., pp.445-450, 25-30 July 2010.

[6] Y. Lo, D. Solomon, and W. Richards, "Theory and experiment on microstrip antennas," *Antennas and Propagation, IEEE Transactions on,* vol. 27, pp. 137-145, 1979.

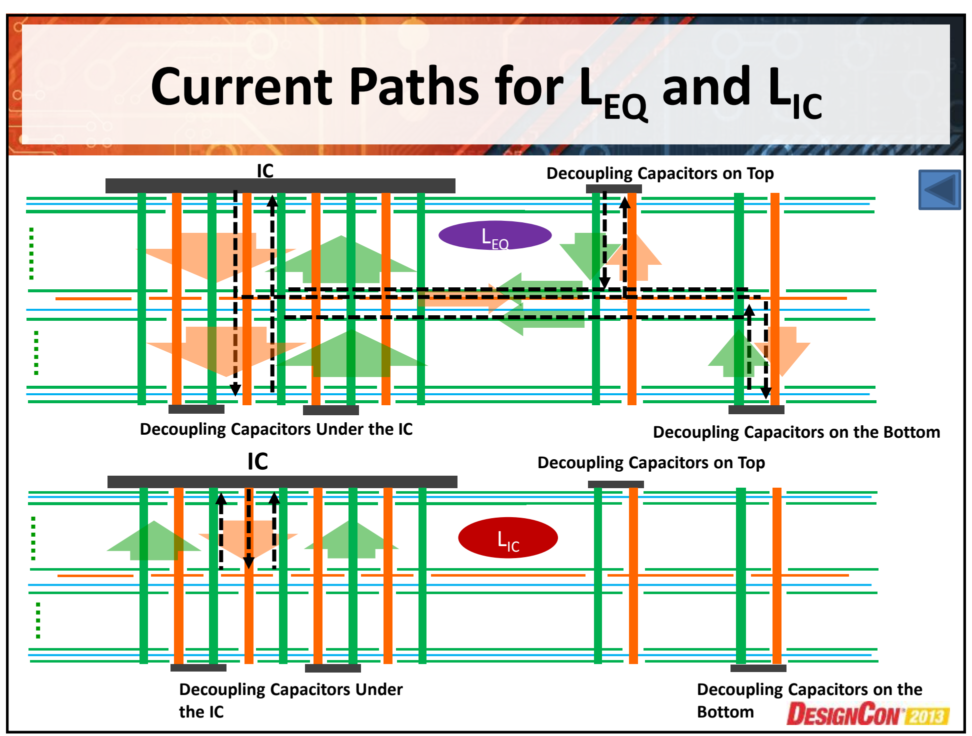
[7] J. Kim, K. Shringarpure, J. Fan, J. Kim, and J. L. Drewniak, "Equivalent Circuit Model for Power Bus Design in Multi-Layer PCBs With Via Arrays," *Microwave and Wireless Components Letters, IEEE,* vol. 21, pp. 62-64, 2011.

[8] K. Shringarpure, S. Pan, J. Kim, B. Achkir, B. Archambeault, J. Fan, J. Drewniak, "Lumped Circuit Modeling and Analysis of the Power Distribution Network in a Production Level Multi-layered Printed Circuit Board", *[To Be Published]*.

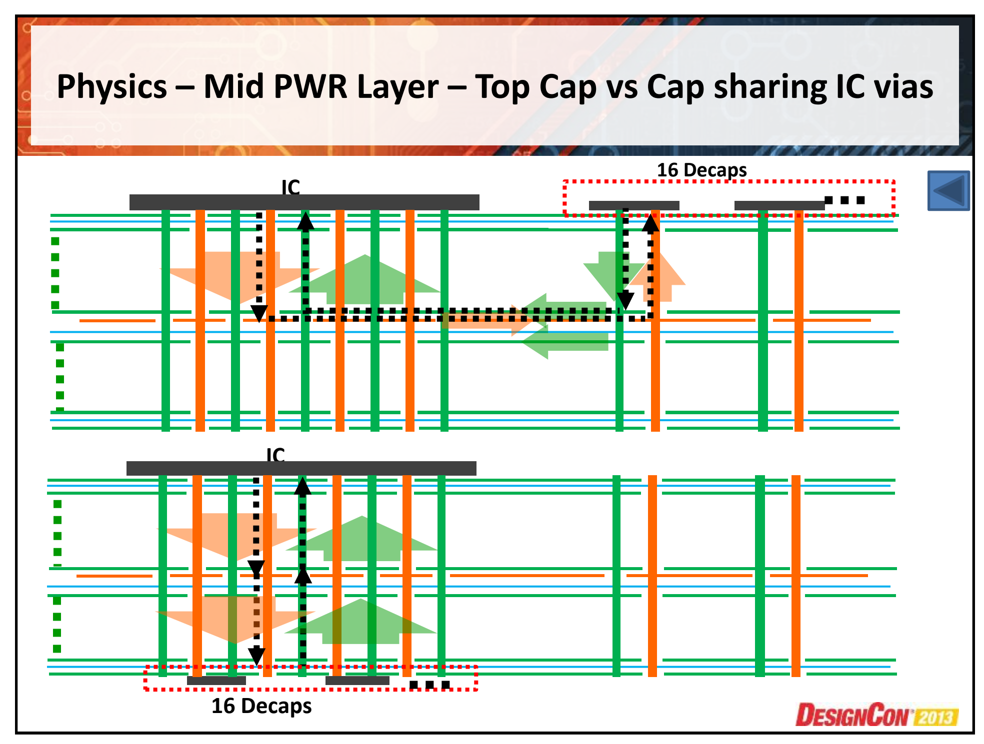
[9] Archambeault, B.; Jingook Kim; Connor, S.; Jun Fan; , "Optimizing decoupling capacitor placement to reduce effective inductance," *Electromagnetic Compatibility (EMC), 2011 IEEE International Symposium on* , vol., no., pp.179-183, 14-19 Aug. 2011

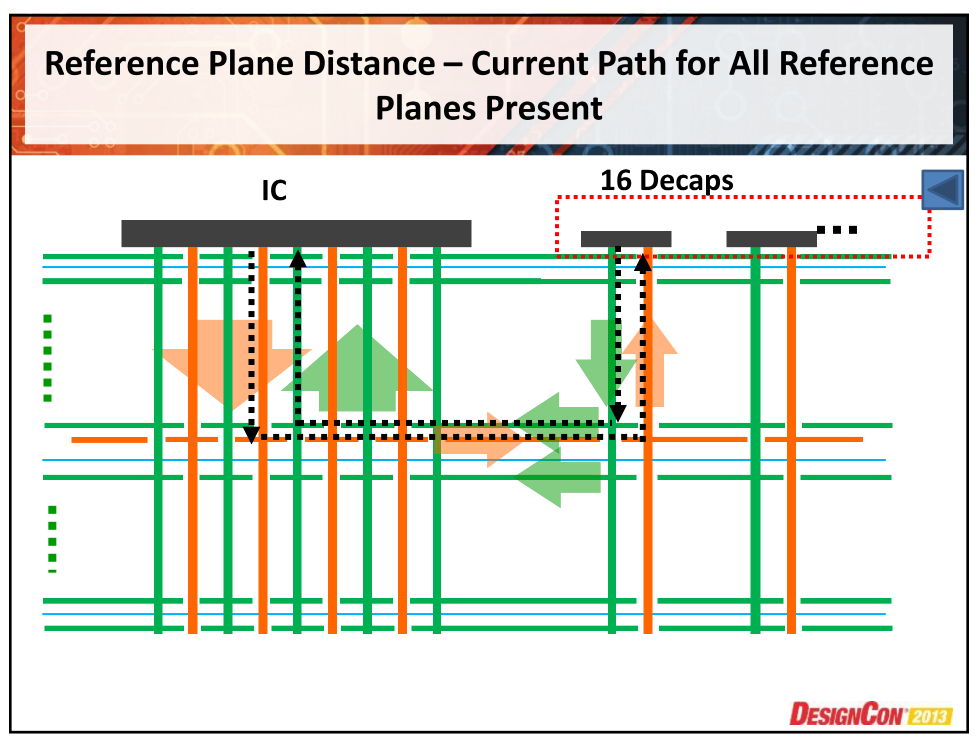
DesignCon 2013

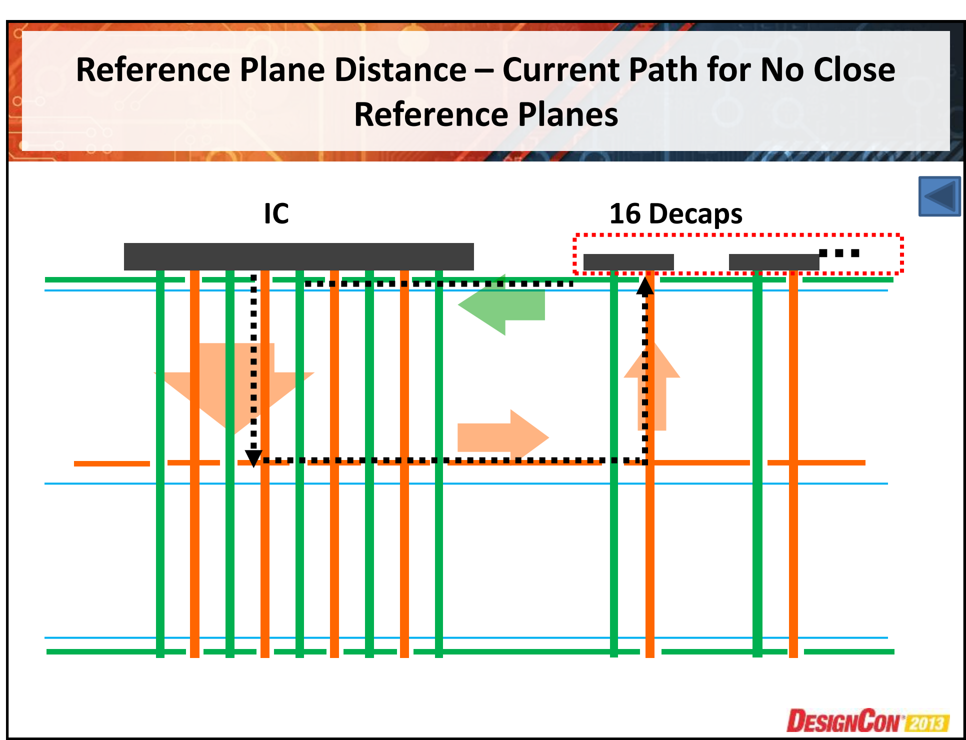
Current Paths for L_{EQ} and L_{IC}



DesignCon 2013


Physics – Mid PWR Layer – Top Cap vs Cap sharing IC vias
IC
16 Decaps
IC
16 Decaps
DesignCon 2013


Reference Plane Distance – Current Path for All Reference Planes Present
IC
16 Decaps
DesignCon 2013


Reference Plane Distance – Current Path for No Close Reference Planes
IC
16 Decaps
DesignCon 2013