A Method of extracting on-chip Decoupling Cap through Board Level

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Introduction

The frequency response of the individual components and their parasitic between those components dictate the ability of system to respond to the current demand from IC. The simplified PDN schematic, shown in Fig.1, includes source, bypass capacitors, PCB P/G plane, PKG P/G plane and the on-chip decoupling capacitor. While analyzing the system power integrity (PI), it's used to extract the P/G plane models of PCB and PKG by commercial electric-magnet (EM) field Solvers, Sigrity/PowerSI is adopted in this paper, which used the physical design databases of the PKG and PCB, and the extracted models are proven accurate from many benchmarks and correlations. However, for the on-chip decoupling capacitor, it's a challenging to derive the detail information from IC vendors since those on-chip information are the commercial secrets. In this section, a methodology is proposed to extract the on-chip decoupling capacitance through some skills of testing and 3D EM modeling.

Introduction of on-chip decoupling capacitor

On-chip power distribution systems for high-performance sub-micron complement metal oxide semiconductor (CMOS) process must provide a local and lower impedance path over a wide frequency range to suppress the internal P/G noise. On-chip decoupling capacitance acts such a local charge component, which effectively lowers the power distribution impedance at high frequencies. Hence the high-frequency switching noise bypasses directly from the low impedance path in the power distribution system, and the supply switching noise is therefore reduced. The on-chip decoupling capacitor includes both intrinsic decoupling capacitors and add-on decoupling capacitors. The intrinsic decoupling capacitors include the junctions of N-Well/P-Well and the devices physical layout which are not sufficient for acceptable noise suppression in high-performance design, therefore some add-on decoupling capacitors are needed to strengthen the capability of noise suppression. In the most of sub-micron IC designs, the add-on decoupling capacitors are often in the form of thin/thick-oxide MOSFET structure which exist the high capacitance per-unit-area and is occupied less area.

Extracting and Modeling Approach

A PCB Test Fixture (C_TFix) is designed for the purpose of extracting the on-chip decoupling capacitance. Fig.3. shows the photograph of the test fixture, the BGA type package and SMA connectors are included in the C_TFix. The size of C_TFix needs as small as possible to minimum the intrinsic capacitance between the planes of C_TFix to benefit model extraction of the on-chip decoupling capacitance. A size of 28mm*35mm is designed and the capacitance of the stacked P/G plane is about 12.8pF extracted by EM solver. A correlation between EM simulation and measurement are done before model extraction, shown in Fig.2, and the results are acceptable for this experiment..

In the proposed methodology, we applied the VNA to measure the s-parameter of whole PDN system, including PCB, PKG and on-chip decoupling capacitor. Since the MOSFET type decoupling capacitor (M-DCap) is a voltage-dependent device, the s-parameter must vary while applying the various voltage biases. The M-DCap has two steady-sate region of

capacitance, one is the inversion mode and the other is accumulation mode. While M-DCap turning on (Applied bias > Threshold voltage), it works on the inversion mode and induce the lower capacitance. Oppositely, if the M-DCap turning off (Applied bias < Threshold voltage), it works on the accumulation mode and operates in the higher capacitance region. Normally, since the anode (Gate) of M-DCap is applied to power supply voltage and the cathode (Silicon Bulk), applied to the ground, the capacitance is always on the accumulation mode with the higher capacitance.

Fig.4 shows the Z-parameter with various applied voltage bias, it's obviously that the impedance varies with the applied voltage, consequently, it proves that the characteristic of on-chip M-DCap is accessed while external bias applying to the C_TFix by means of SMA connectors. While extracting the capacitance value from the image part of Z parameter at low frequency, e.g. setting to 50 MHz, which neglects the inductance effects of BGA wirebond, the C-V curve of whole power delivery network could be derived. After de-embeding the capacitance on C-TFix/BGA, the on-chip decoupling capacitance could be obtained. Fig.5 shows the C-V curves with and without C_TFix / BGA.

For the purpose of co-simulation with other models (IBIS Model, PKG and PCB models), an bias dependent physical model of M-DCap needs to be developed. A tanh(x) based formula and fitting parameters with Hspice format was applied to model the kind of C-V curve which is as the following expression:

$$C_g = (C_{\min} + (dC_{\max} \cdot (1 + V_{leak} \cdot V(n1, n2))) \cdot (1.0 + \tanh((V(n1, n2) - dV_{bias}) / V_{slew})))$$

Fig.5 shows the modeling result of M-DCap based on the prediction of above formula with five fitting parameters, *Cmin*, *Cmax*, *Vleak*, *Vbias* and *Vslew*. Tuning those parameters could obtain the desired modeling results of M-DCap. Consequently, the tanh(x) based formula is suitable for the model of MOSFET type on-chip decoupling capacitor which exist the characteristics of voltage dependent capacitance.

Conclusions

A method of extracting on-chip decoupling capacitance will benefit the SI/PI engineers to complete the models in PDN and this will enhance the accurate prediction of power integrity analysis. A methodology is proposed to extract and model the on-chip decoupling capacitance through the system board level, and good results were demonstrated.

References

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[2] John Kane "Optimizing Power Delivery Performance through Chip-Package-Board Co-design" User Conference 2007, Taiwan

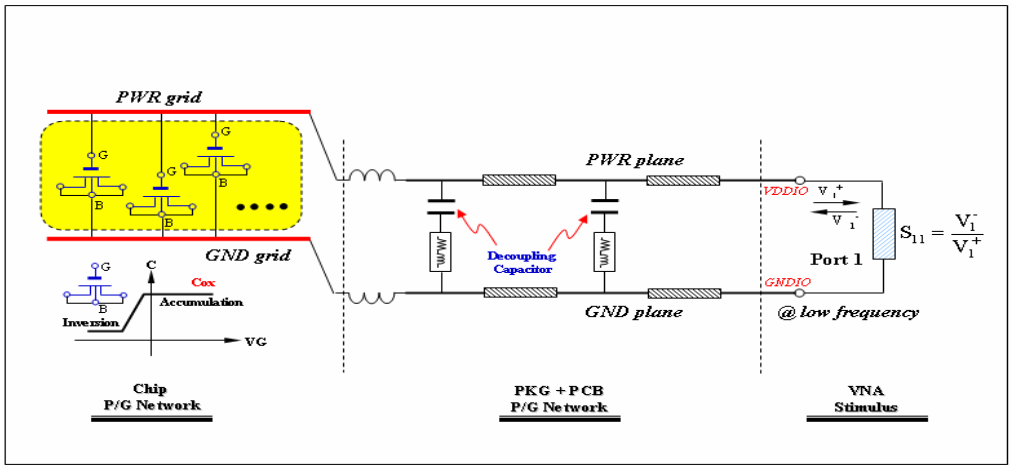

Fig.1. Schematic of on chip decoupling capacitor

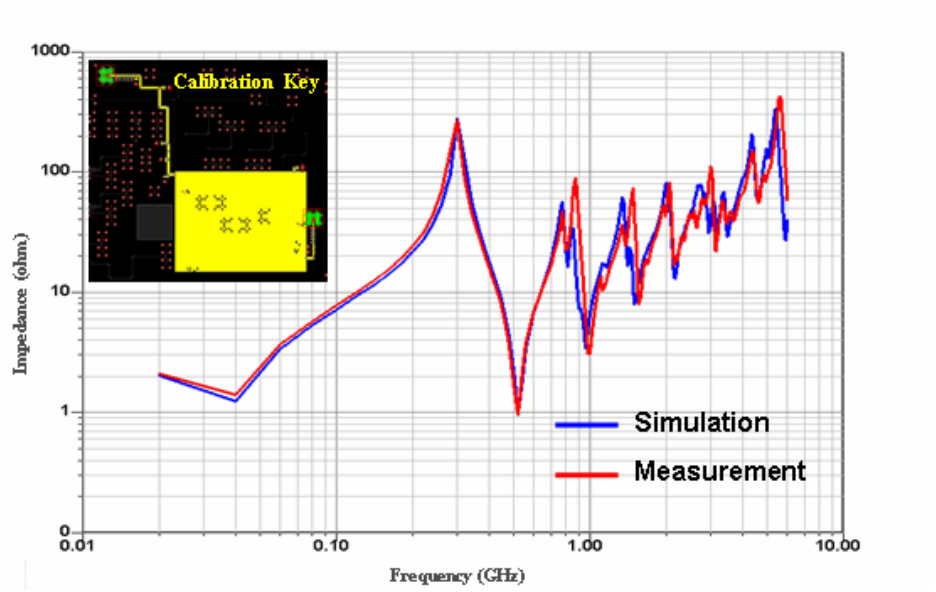

Fig.2. Calibration results of 3D EM tool and measurement data

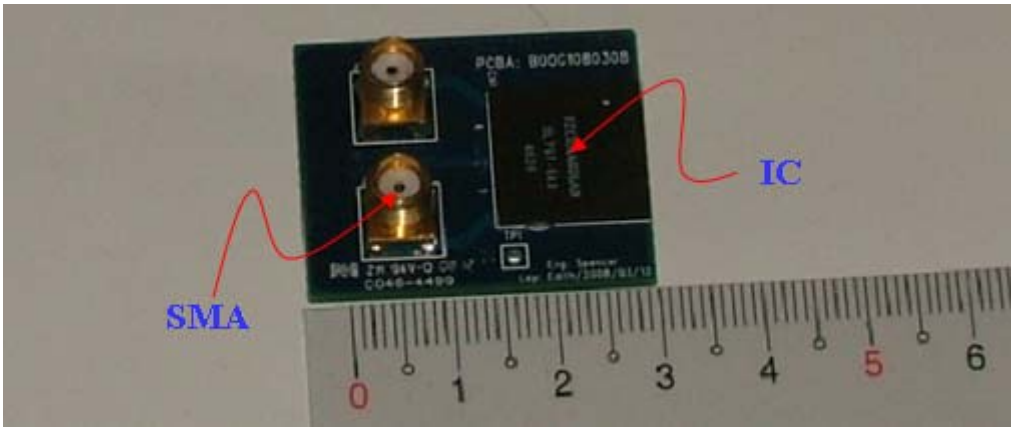

Fig.3. Photograph of C_TFix

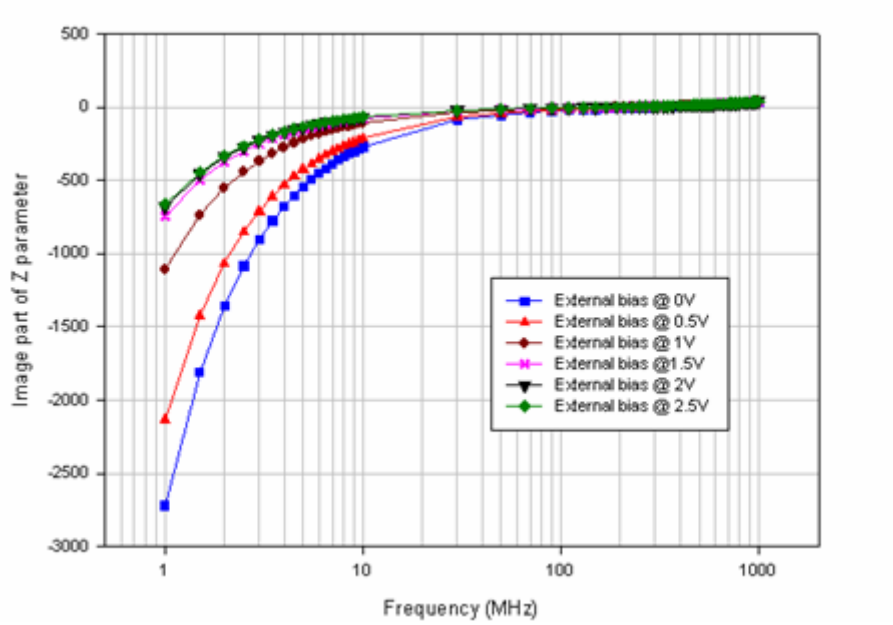

Fig.4. Z impedance with various applied bias

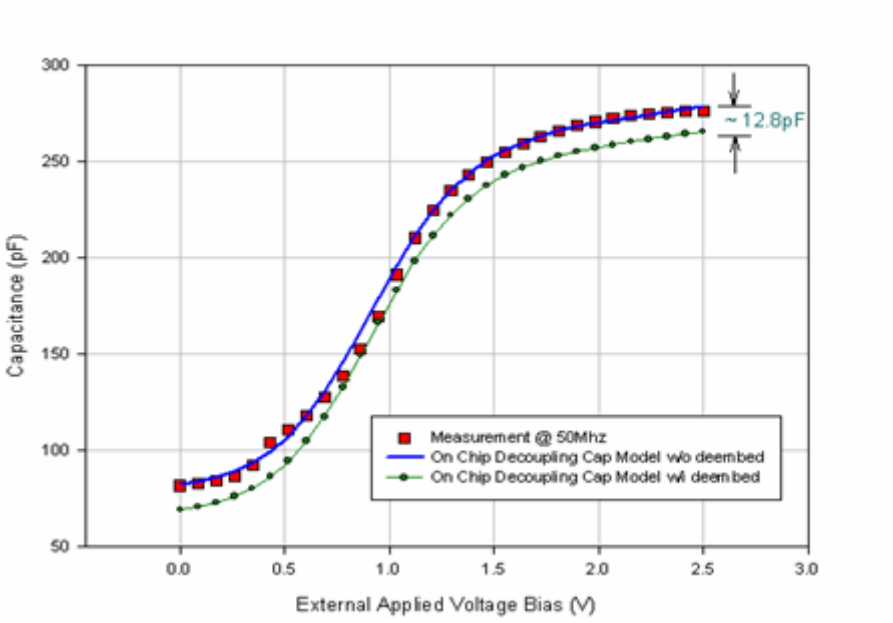

Fig.5. Characteristic and modeling of on chip capacitance