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Experimental Optimization of Decoupling Capacitors in FPGA Designs by On-Die Measurement of Power Distribution Impedance Frequency Profile

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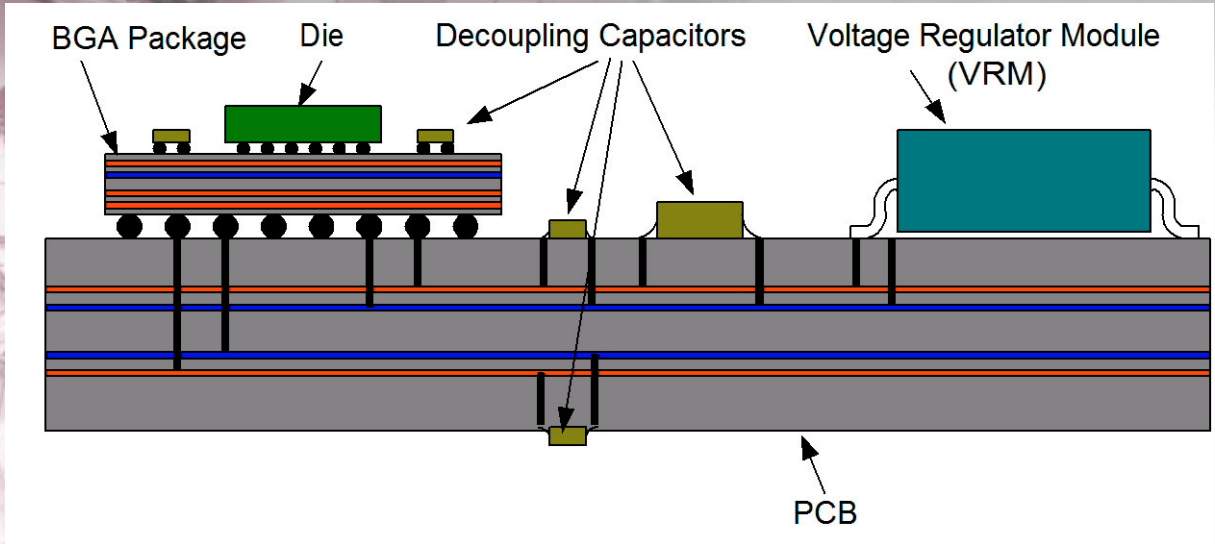
Outline

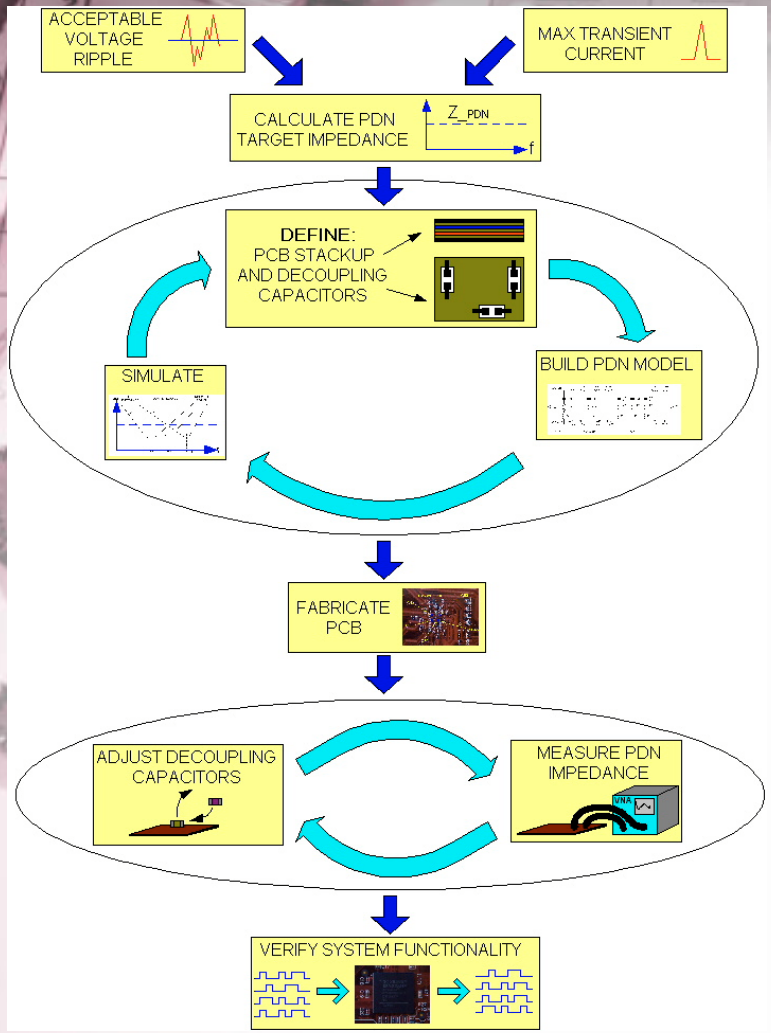
- Overview of PDN Design and Optimization
- Typical PDN Design Methodology
- Differences Between PDN Impedance On-Die and On-PCB
- Proposed PDN Design Methodology
- FPGA Configuration for On-Die PDN Impedance Measurement
- Case Study Implemented in a Spartan 3A FPGA
- Conclusions

Overview of PDN Design and Optimization



- Define power and ground planes in PCB stackup
- Assign physical location of decoupling capacitors on the PCB
- Determine values and types of decoupling capacitors
- Design mounting layout structures for decoupling capacitors

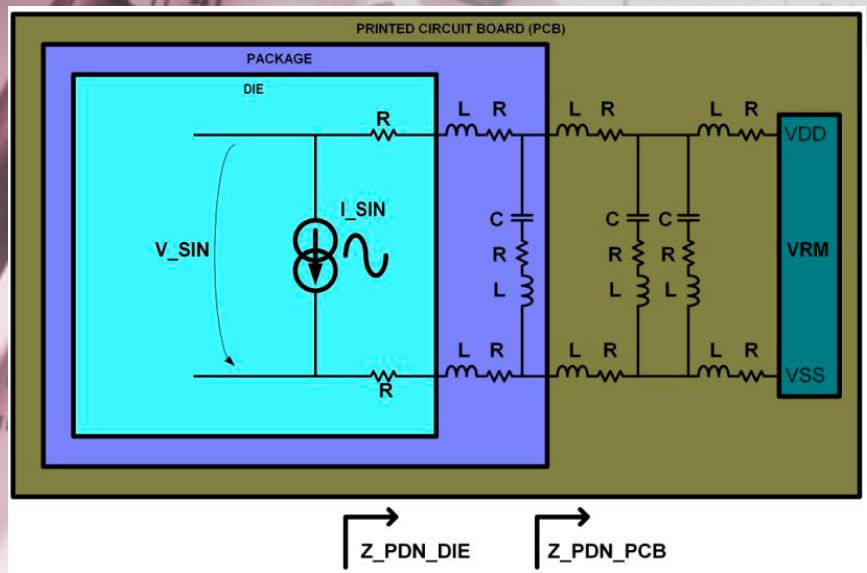
Typical PDN Design Methodology

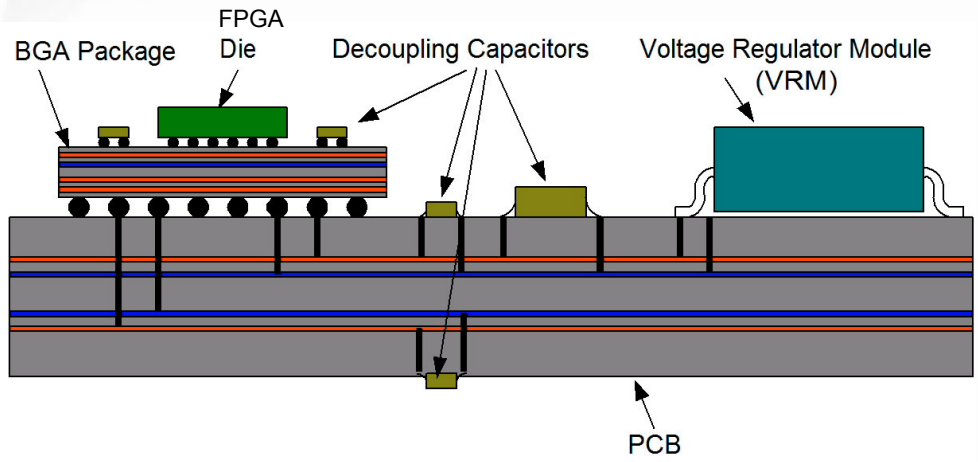


- Iterative process may consume significant schedule time
- Modeling and simulation tools increase cost

- Expensive measurement instruments (VNA …)
- No visibility of PDN impedance seen by on-die circuits

Differences Between PDN Impedance On-Die and On-PCB

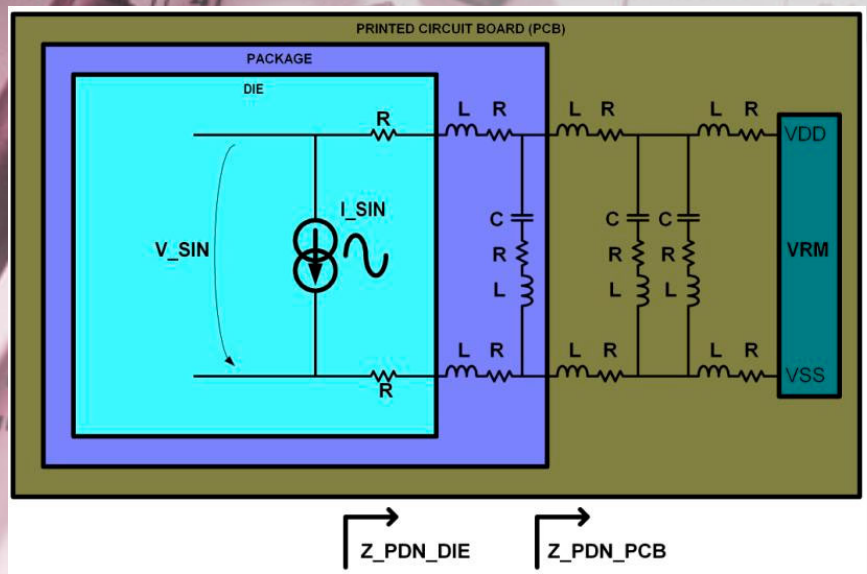


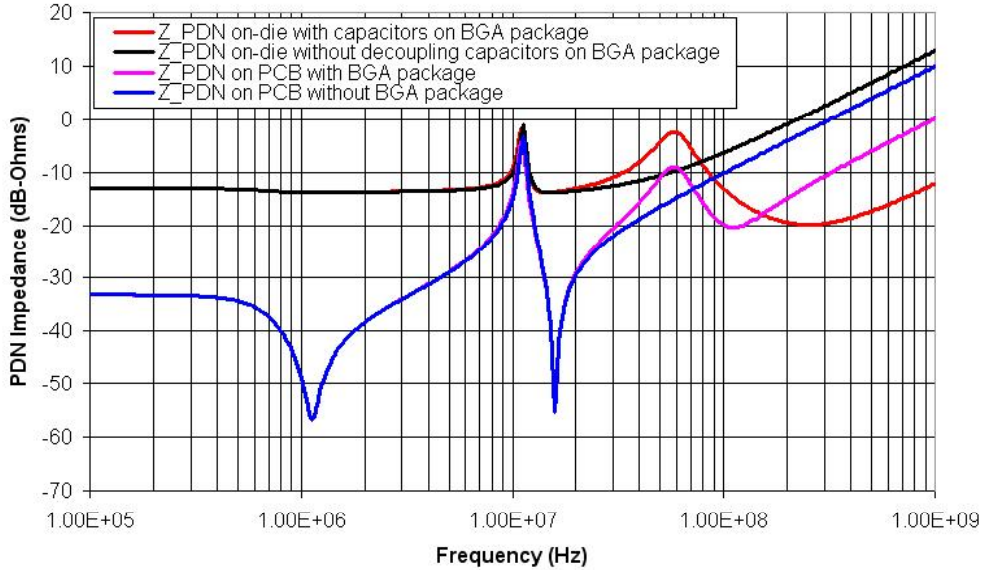


As seen by on-PCB measurements (example VNA one-port or two-port)

As seen by the FPGA on-die circuits - which generate transient currents and are affected by supply noise

Differences Between PDN Impedance On-Die and On-PCB





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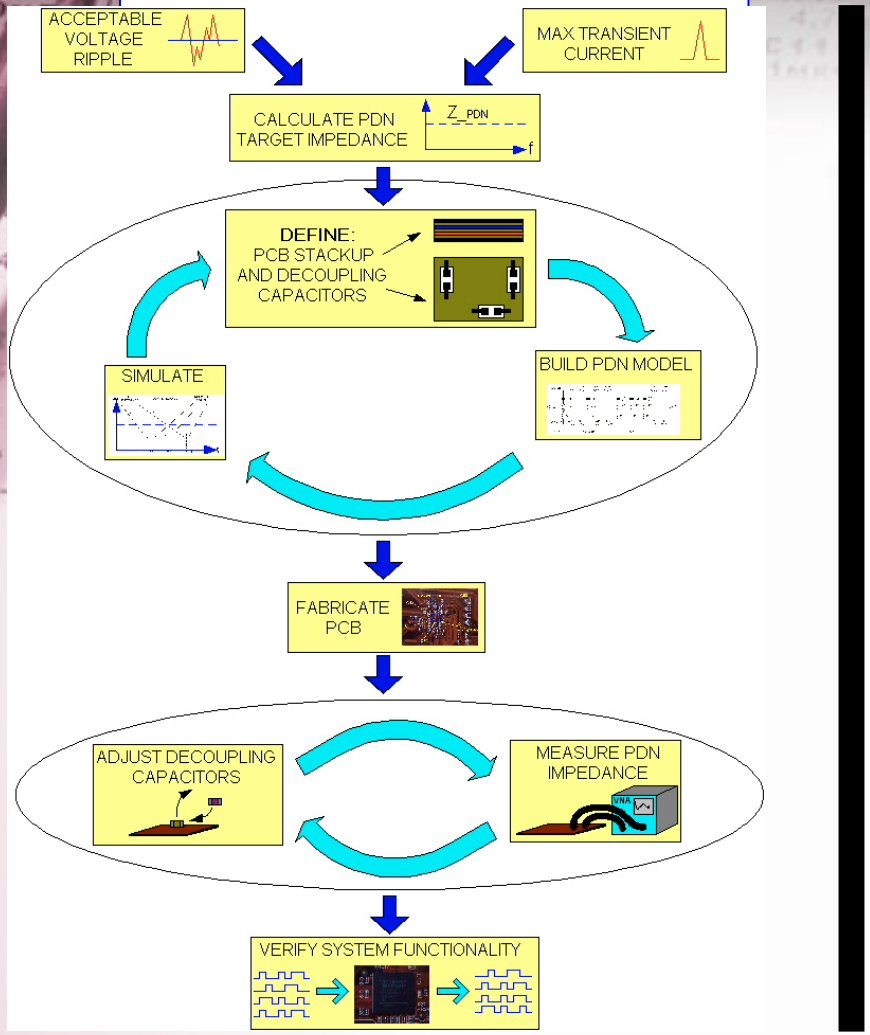
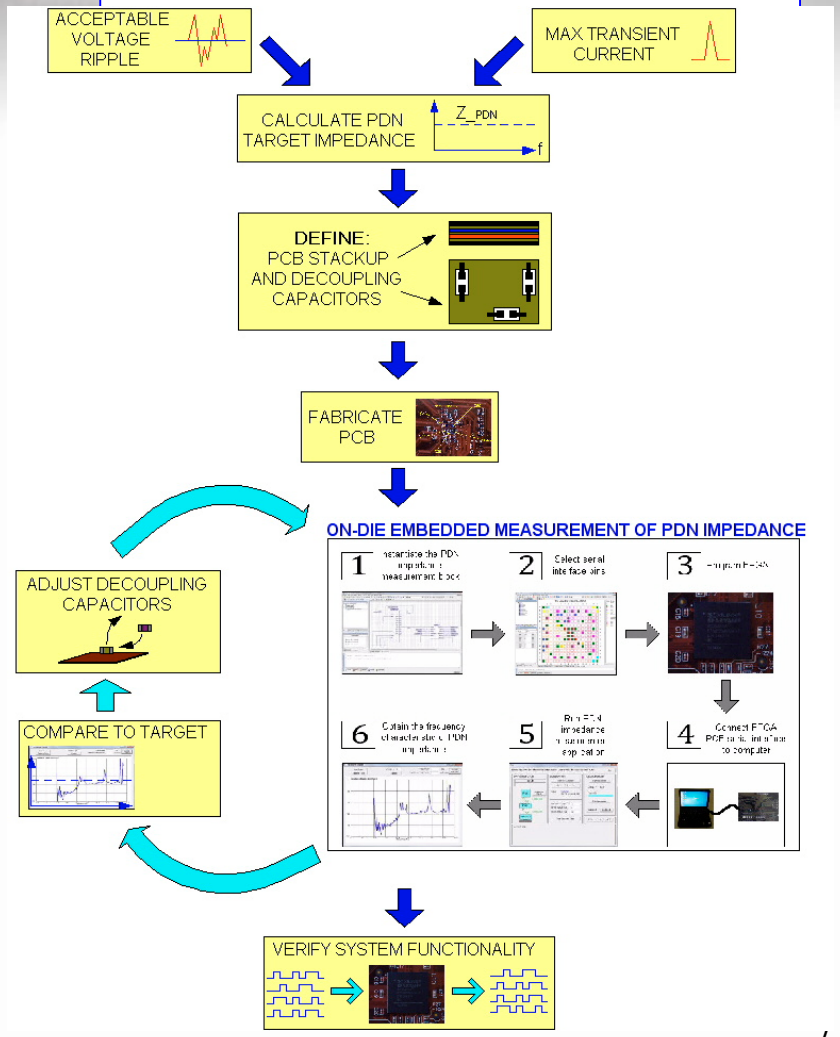
Proposed PDN Design Methodology

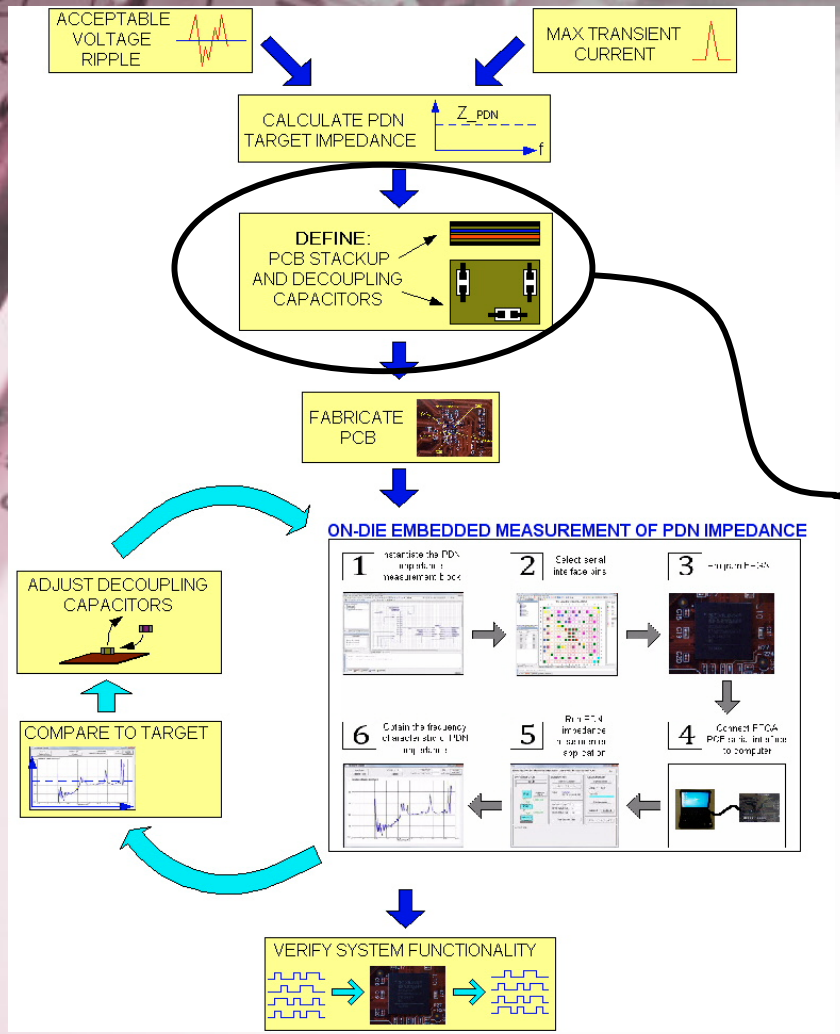
Typical Methodology



Proposed Methodology



Proposed PDN Design Methodology



PCB Stackup:

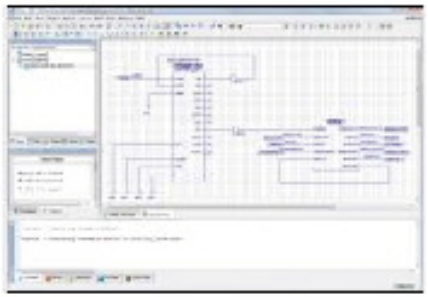
- Reduce spacing between power/ground planes

PCB Layout:

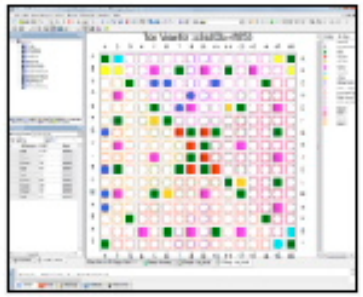
- Place “open” capacitor pads as many as could be fit
- Use multiple pad sizes
- Place pads close to FPGA as floorplan allows
- Larger pads for electrolytic or tantalum may be further apart

On-Die PDN Impedance Measurement

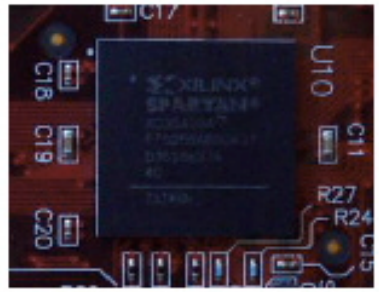
1 Instantiate the PDN impedance measurement block



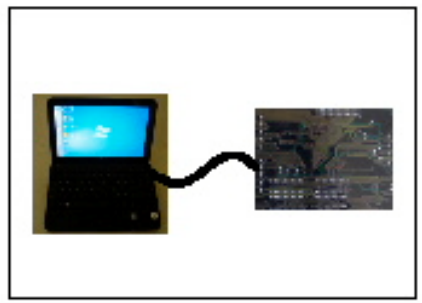
2 Select serial interface pins



3 Program FPGA

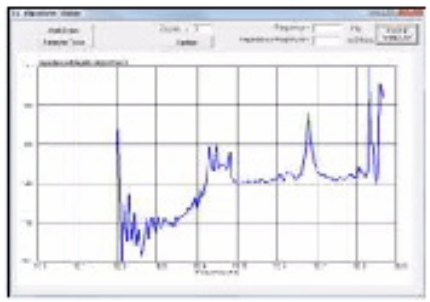


4 Connect FPGA PCB serial interface to computer

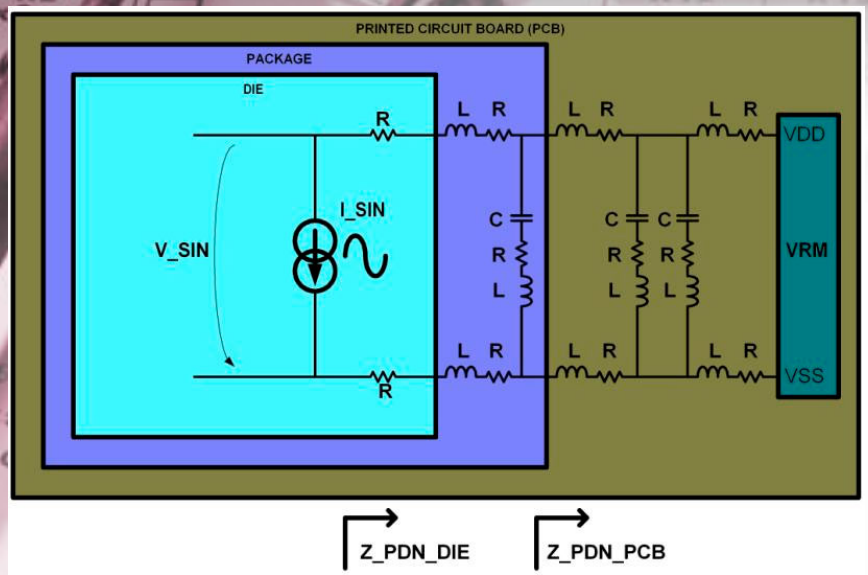


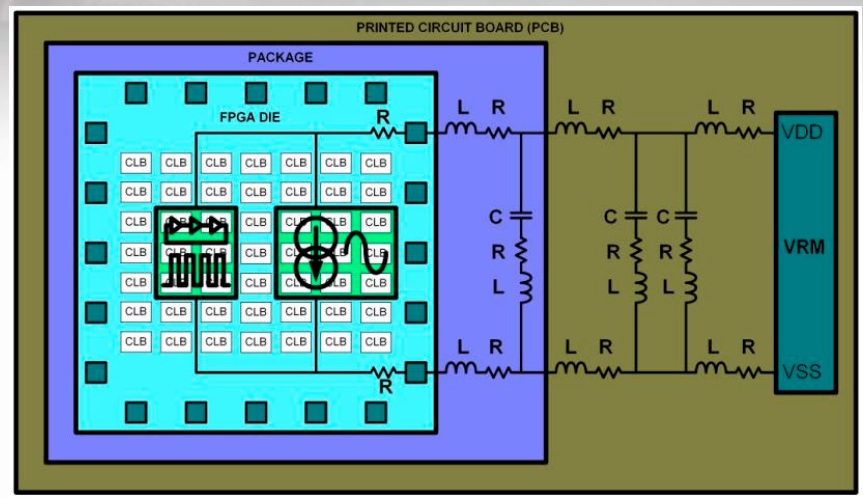
5 Run PDN impedance measurement application

6 Obtain the frequency characteristic of PDN impedance



AC Steady-State Analysis Implemented in FPGAs

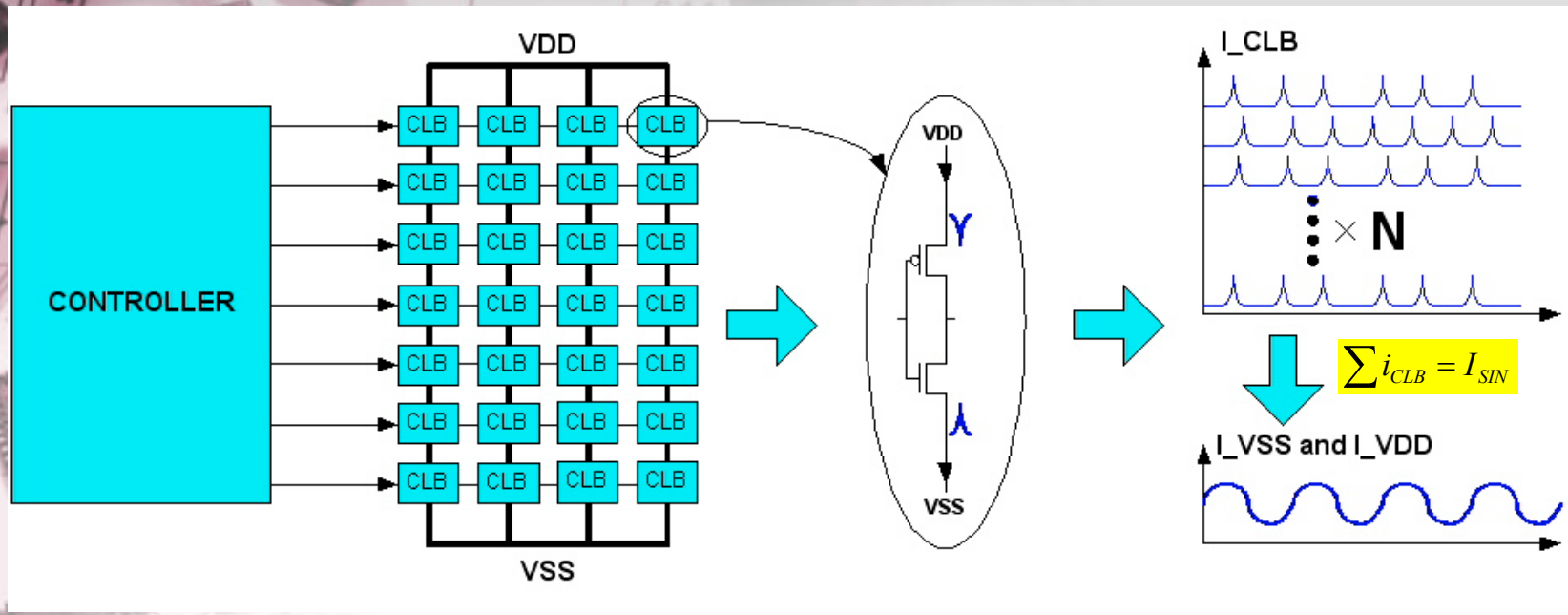




- A group of FPGA configurable logic blocks is configured to function as a sinusoidal current source
- Another group of FPGA configurable logic blocks is configured to form a ring oscillator

(patent pending technology)

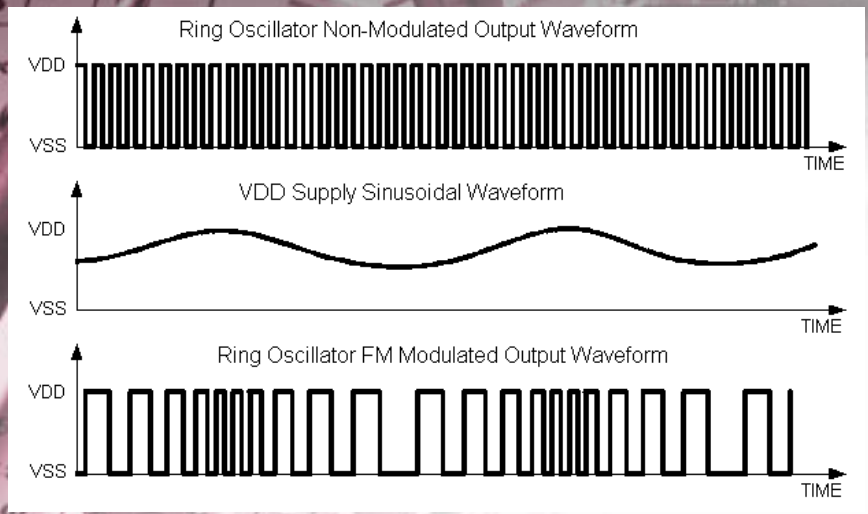
Sinusoidal Current Source Implemented with FPGA Logic Blocks

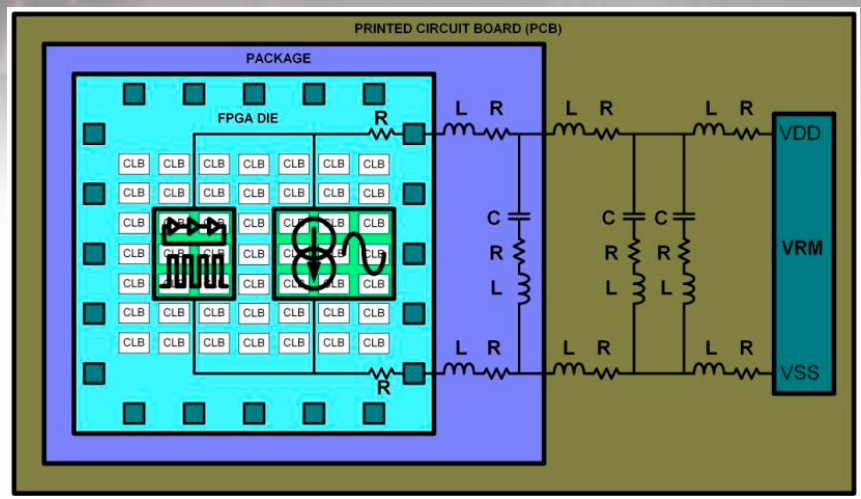


The sinusoidal current is obtained by summing the dynamic load charging and discharging currents of multiple CMOS gates, built as part of CLB blocks

(patent pending technology)

AC Steady-State Analysis Implemented in FPGAs



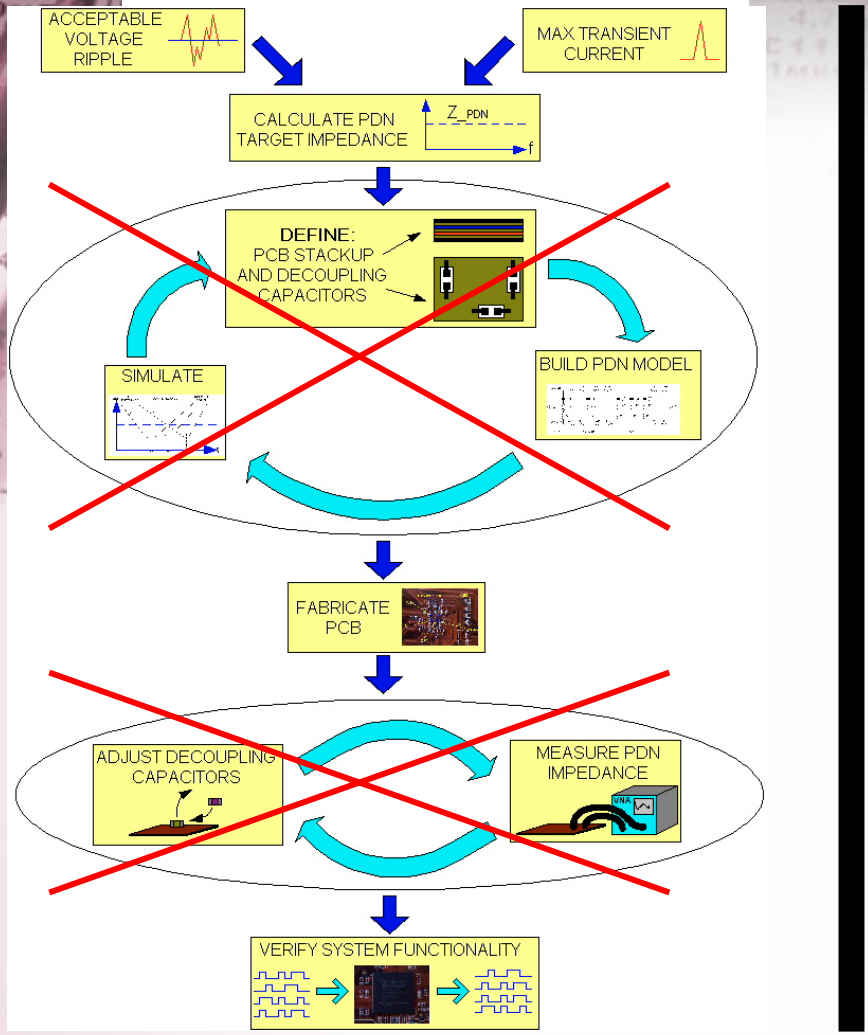


- The sinusoidal current flows through the power distribution network and generates sinusoidal variation of the on-die power supply voltage
- The sinusoidal variation of the voltage supply modulates the frequency of the ring oscillator
- A counter circuit measures the frequency of the ring oscillator
- PDN impedance is calculated from the average frequency deviation

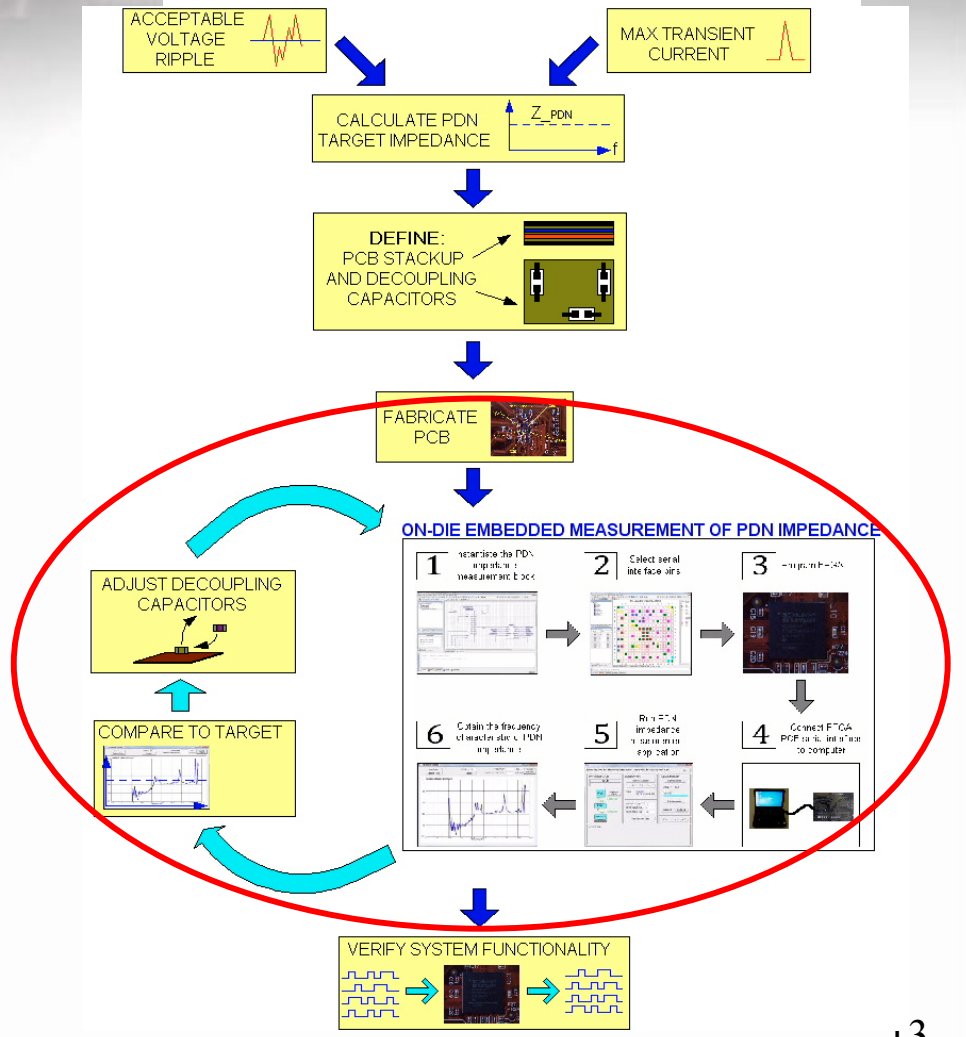
(patent pending technology)

Proposed PDN Design Methodology

Typical Methodology



Proposed Methodology

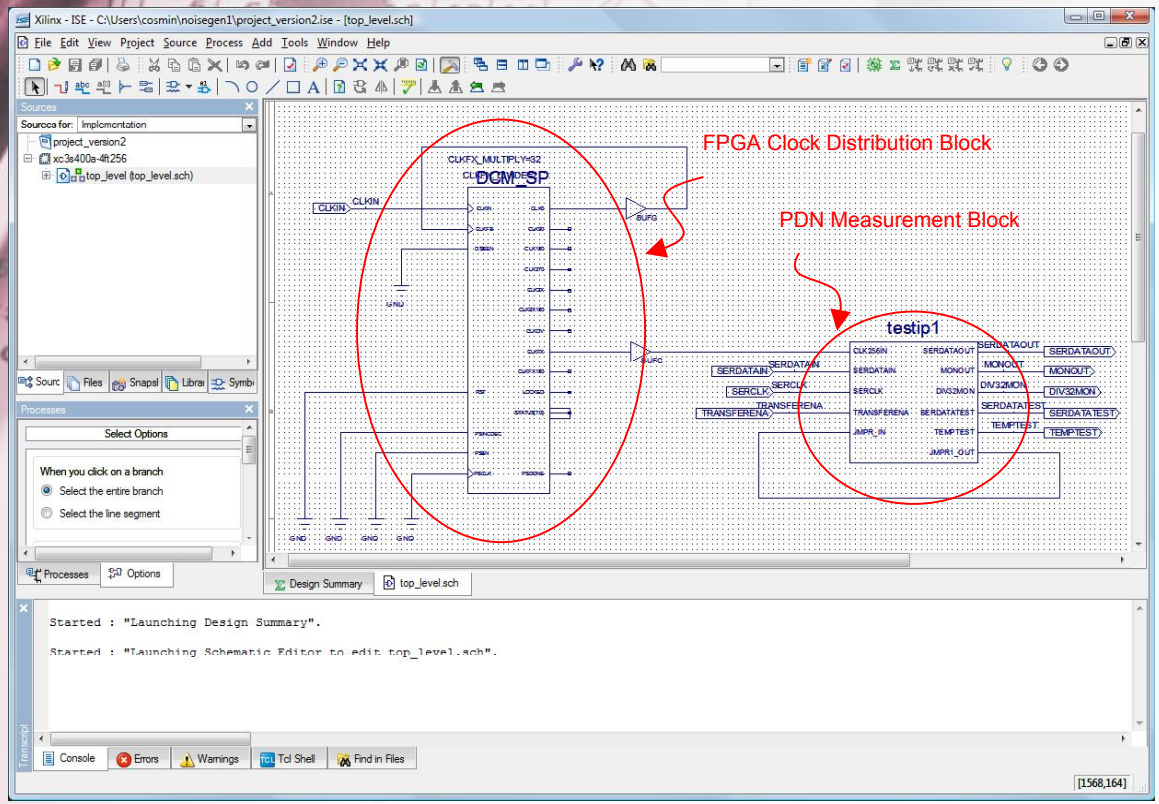


Case Study

- The proposed PDN impedance measurement technique implemented in a Spartan 3A FPGA on a test board
- PDN impedance frequency profile measured at frequencies up to 500MHz
- Decoupling capacitors chosen by experimental optimization
- Additional design tradeoffs studied through this technique
- FPGA clock frequency chosen based on on-die PDN impedance profile

Case Study

Implementation of PDN Measurement Method



The PDN measurement block needs a clock signal, which is provided by the FPGA clock distribution

The PDN measurement block uses a serial interface connected to FPGA I/O blocks

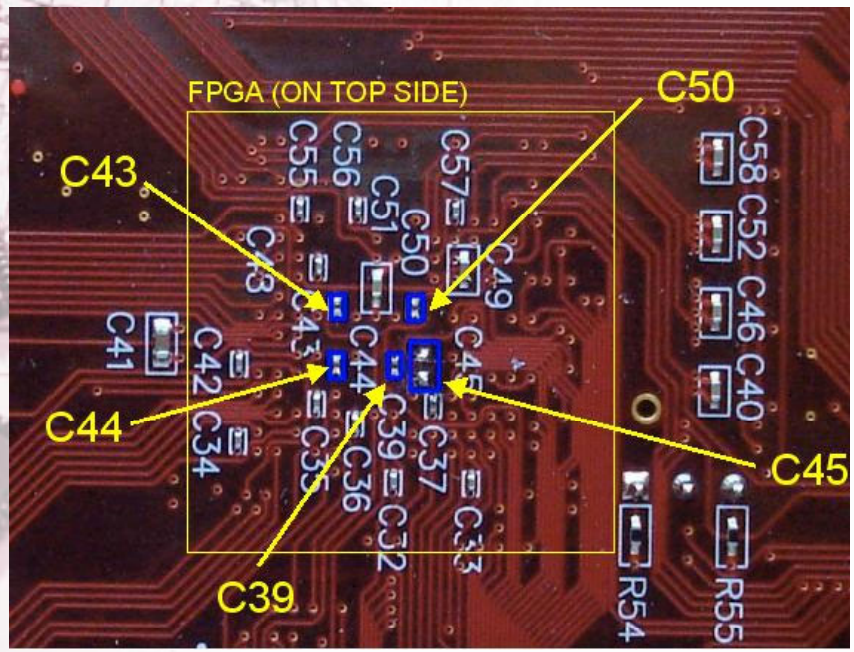
Case Study

Device Utilization Summary in a Spartan 3A FPGA

Device Utilization Summary			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Flip Flops	209	7,168	2%
Number of 4 input LUTs	725	7,168	10%
Logic Distribution			
Number of occupied Slices	582	3,584	16%
Number of Slices containing only related logic	582	582	100%
Number of Slices containing unrelated logic	0	582	0%
Total Number of 4 input LUTs	740	7,168	10%
Number used as logic	725		
Number used as a route-thru	15		
Number of bonded IOBs	9	195	4%
Number of BUFGMUXs	6	24	25%
Number of DCMs	2	4	50%
Number of RPM macros	3		

Case Study

Experimental Optimization of Decoupling Capacitors

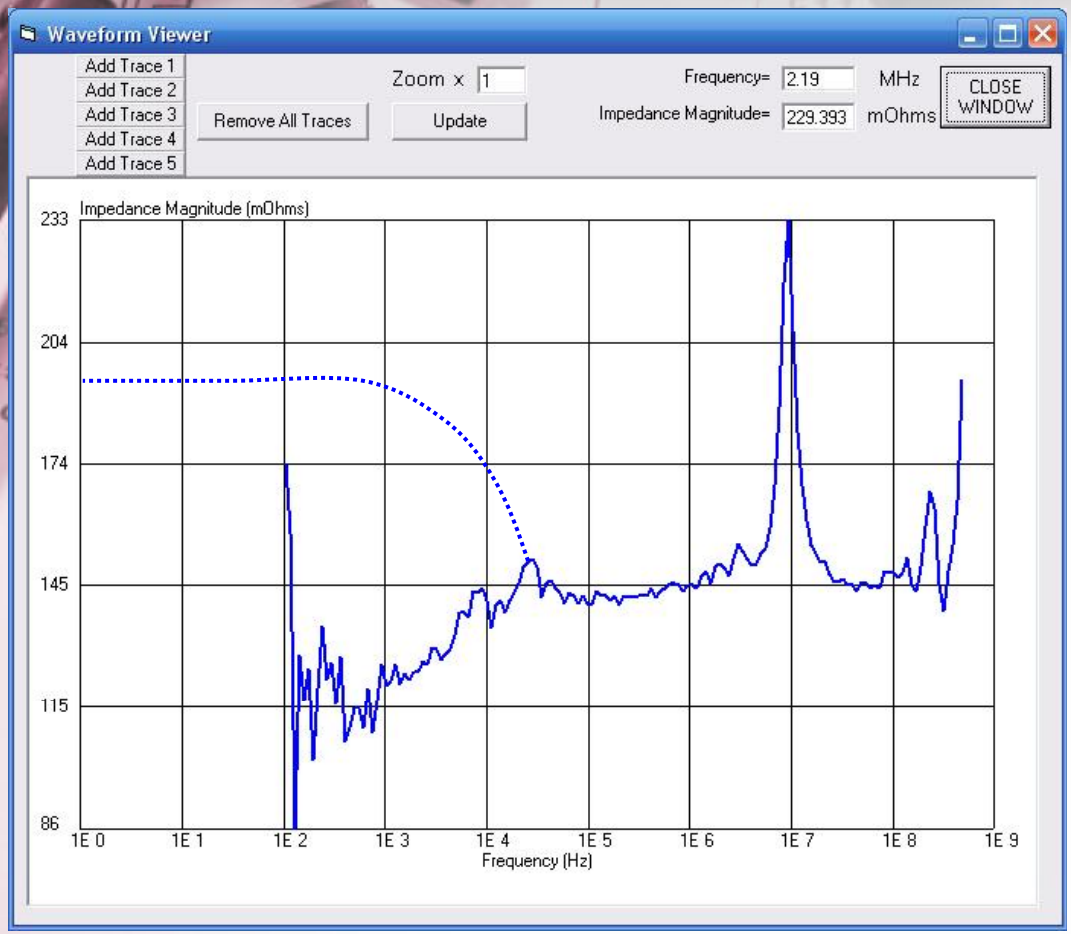


Start with “open pads” or “best guess” values for decoupling capacitors:

C39, C43, C44, C45, C50

Case Study

Measured on-die PDN impedance frequency profile



Measurement up to 500MHz

Not accurate below 20kHz

Accuracy can be extended below 20kHz with the expense of increased measurement time

Case Study

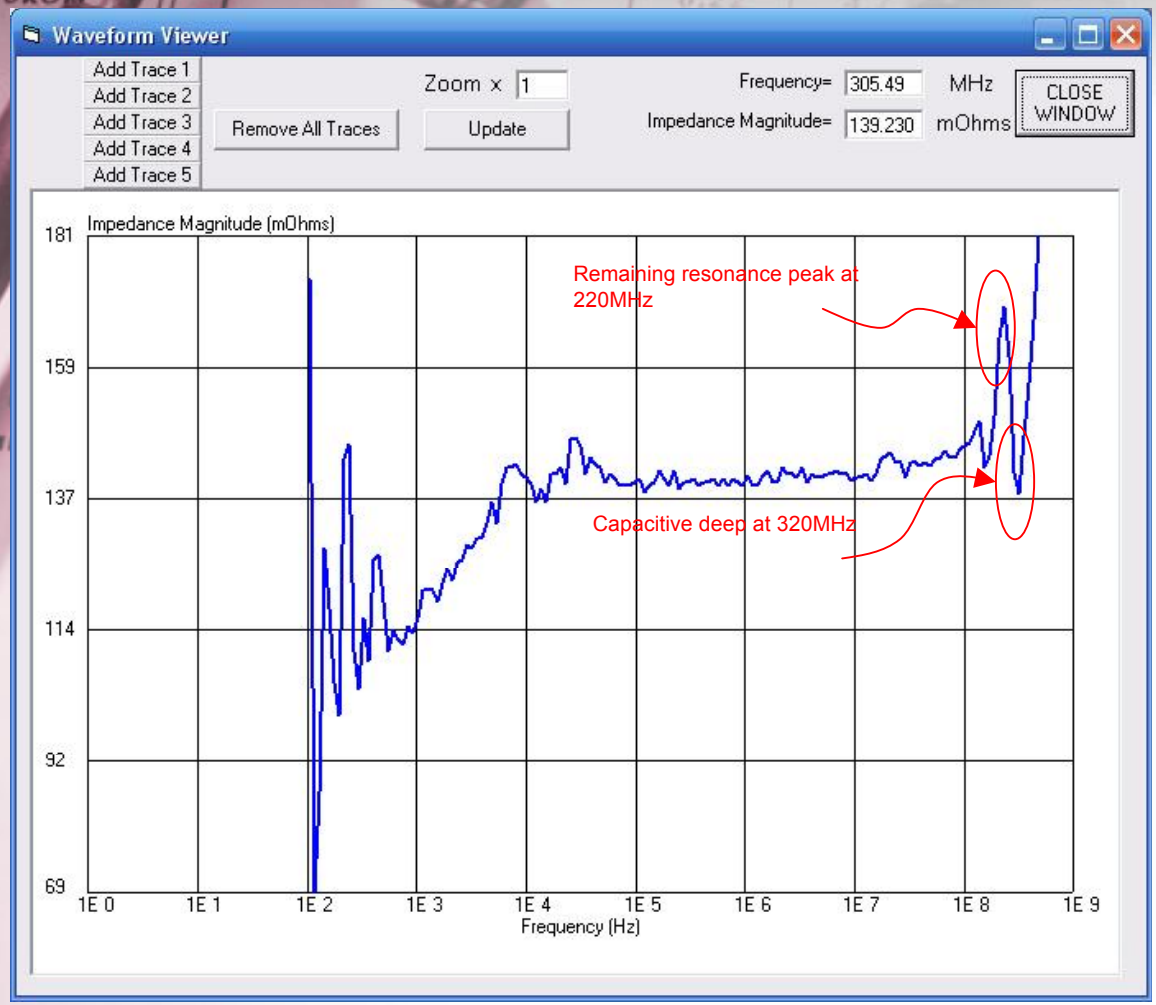
Experimental Optimization of C45

Starts with 1nF and gradually increases up to 220nF

Values larger than 220nF do not further reduce the impedance

Case Study

Package and Die Contribution



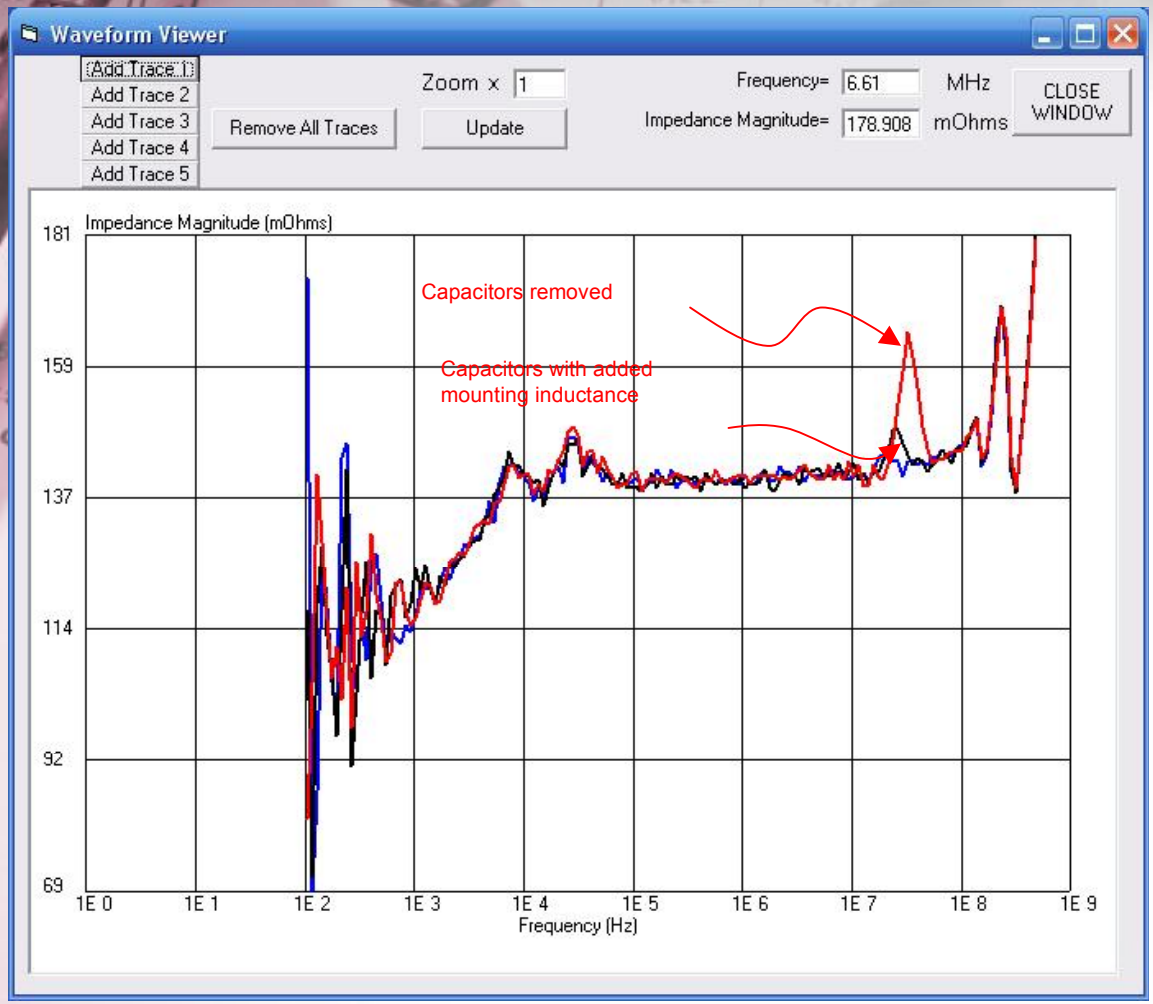
After optimization a resonant peak at 220MHz still remains

This resonant peak is caused by inductance and decoupling capacitors in the package

The intended FPGA clock frequency of 200MHz is changed to 320MHz where the PDN impedance has a minimum

Case Study

Example of Further PDN Optimization Study



Feasibility study of moving C39, C43, C44, C50 outside the FPGA region and using full vias instead of blind vias

Additional inductance added by lifting capacitors and adding wire jumpers

Test Case Summary

This test case has evaluated how the proposed FPGA on-die PDN impedance measurement technique can help with:

- Selection of decoupling capacitors' values and types
- Trade-off between placement of decoupling capacitors and PCB manufacturing cost reduction (blind vias versus full vias)
- Identifying that the intended FPGA core clock frequency of 200MHz was too close to a PDN resonance peak at 220MHz
- Locating a minimum PDN impedance at 320MHz where the FPGA clock has been set to operate

Some of these PDN improvements have not been possible with only on-board PDN impedance measurements since the significant contributors were the interconnects and decoupling capacitors on the FPGA package and die

Conclusions

- Low cost alternative to existing PDN design methods
- Uses only logic blocks commonly available in any FPGA
- Can be implemented in any existing FPGA without the need of built-in dedicated measurement circuits
- Eliminates expensive test bench instruments and simulation software tools
- A case study has exemplified experimental optimization of decoupling capacitors and has studied various PDN design tradeoffs