Experimental Optimization of Decoupling Capacitors in FPGA Designs by On-Die Measurement of Power Distribution Impedance Frequency Profile

Cosmin Iorga
NoiseCoupling.com

cosmin.iorga@noisecoupling.com (805) 231-9786
Outline

Overview of PDN Design and Optimization

Typical PDN Design Methodology

Differences Between PDN Impedance On-Die and On-PCB

Proposed PDN Design Methodology

FPGA Configuration for On-Die PDN Impedance Measurement

Case Study Implemented in a Spartan 3A FPGA

Conclusions
Overview of PDN Design and Optimization

- Define power and ground planes in PCB stackup
- Assign physical location of decoupling capacitors on the PCB
- Determine values and types of decoupling capacitors
- Design mounting layout structures for decoupling capacitors
Typical PDN Design Methodology

- Iterative process may consume significant schedule time
- Modeling and simulation tools increase cost
- Expensive measurement instruments (VNA …)
- No visibility of PDN impedance seen by on-die circuits
Differences Between PDN Impedance On-Die and On-PCB

As seen by on-PCB measurements (example VNA one-port or two-port)

As seen by the FPGA on-die circuits - which generate transient currents and are affected by supply noise
Differences Between PDN Impedance On-Die and On-PCB

As seen by on-PCB measurements (example VNA one-port or two-port)

As seen by the FPGA on-die circuits - which generate transient currents and are affected by supply noise
Proposed PDN Design Methodology

**Typical Methodology**

1. Acceptable Voltage Ripple
2. Calculate PDN Target Impedance
3. Define: PCB Stackup and Decoupling Capacitors
4. Simulate
5. Build PDN Model
6. Fabricate PCB
7. Adjust Decoupling Capacitors
8. Measure PDN Impedance
9. Compare to Target
10. Verify System Functionality

**Proposed Methodology**

1. Acceptable Voltage Ripple
2. Calculate PDN Target Impedance
3. Define: PCB Stackup and Decoupling Capacitors
4. Fabricate PCB
5. On-Die Embedded Measurement of PDN Impedance
6. Adjust Decoupling Capacitors
7. Compare to Target
8. Verify System Functionality
Proposed PDN Design Methodology

PCB Stackup:
- Reduce spacing between power/ground planes

PCB Layout:
- Place “open” capacitor pads as many as could be fit
- Use multiple pad sizes
- Place pads close to FPGA as floorplan allows
- Larger pads for electrolytic or tantalum may be further apart
On-Die PDN Impedance Measurement

1. Instantiate the PDN impedance measurement block
2. Select serial interface pins
3. Program FPGA
4. Connect FPGA PCB serial interface to computer
5. Run PDN impedance measurement application
6. Obtain the frequency characteristic of PDN impedance
AC Steady-State Analysis Implemented in FPGAs

- A group of FPGA configurable logic blocks is configured to function as a sinusoidal current source.
- Another group of FPGA configurable logic blocks is configured to form a ring oscillator.
  (patent pending technology)
Sinusoidal Current Source Implemented with FPGA Logic Blocks

The sinusoidal current is obtained by summing the dynamic load charging and discharging currents of multiple CMOS gates, built as part of CLB blocks

(patent pending technology)
AC Steady-State Analysis Implemented in FPGAs

- The sinusoidal current flows through the power distribution network and generates sinusoidal variation of the on-die power supply voltage.
- The sinusoidal variation of the voltage supply modulates the frequency of the ring oscillator.
- A counter circuit measures the frequency of the ring oscillator.
- PDN impedance is calculated from the average frequency deviation.

(patent pending technology)
Proposed PDN Design Methodology

Typical Methodology

1. Acceptable Voltage Ripple
2. Max Transient Current
3. Calculate PDN Target Impedance
4. Define: PCB Stackup and Decoupling Capacitors
5. Simulate
6. Build PDN Model
7. Fabricate PCB
8. Adjust Decoupling Capacitors
9. Measure PDN Impedance
10. Verify System Functionality

Proposed Methodology

1. Acceptable Voltage Ripple
2. Max Transient Current
3. Calculate PDN Target Impedance
4. Define: PCB Stackup and Decoupling Capacitors
5. Fabricate PCB
6. On-Die Embedded Measurement of PDN Impedance
7. Adjust Decoupling Capacitors
8. Compare to Target
9. Verify System Functionality
10. Confirm PDN Impedance

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Case Study

- The proposed PDN impedance measurement technique implemented in a Spartan 3A FPGA on a test board
- PDN impedance frequency profile measured at frequencies up to 500MHz
- Decoupling capacitors chosen by experimental optimization
- Additional design tradeoffs studied through this technique
- FPGA clock frequency chosen based on on-die PDN impedance profile
Case Study

Implementation of PDN Measurement Method

The PDN measurement block needs a clock signal, which is provided by the FPGA clock distribution.

The PDN measurement block uses a serial interface connected to FPGA I/O blocks.
## Case Study

### Device Utilization Summary in a Spartan 3A FPGA

<table>
<thead>
<tr>
<th>Logic Utilization</th>
<th>Used</th>
<th>Available</th>
<th>Utilization</th>
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</thead>
<tbody>
<tr>
<td>Number of Slice Flip Flops</td>
<td>209</td>
<td>7,168</td>
<td>2%</td>
</tr>
<tr>
<td>Number of 4 input LUTs</td>
<td>725</td>
<td>7,168</td>
<td>10%</td>
</tr>
<tr>
<td><strong>Logic Distribution</strong></td>
<td></td>
<td></td>
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<tr>
<td>Number of occupied Slices</td>
<td>582</td>
<td>3,584</td>
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<tr>
<td>Number of Slices containing only related logic</td>
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<td>582</td>
<td>100%</td>
</tr>
<tr>
<td>Number of Slices containing unrelated logic</td>
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<td>0%</td>
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<tr>
<td><strong>Total Number of 4 input LUTs</strong></td>
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<td>7,168</td>
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</tr>
<tr>
<td>Number used as logic</td>
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<tr>
<td>Number used as a route-thru</td>
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<td>Number of bonded I/Os</td>
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<tr>
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<td>50%</td>
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<tr>
<td>Number of RPM macros</td>
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<td></td>
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</tbody>
</table>
Case Study

Experimental Optimization of Decoupling Capacitors

Start with “open pads” or “best guess” values for decoupling capacitors:

C39, C43, C44, C45, C50
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Measured on-die PDN impedance frequency profile

- Measurement up to 500MHz
- Not accurate below 20kHz
- Accuracy can be extended below 20kHz with the expense of increased measurement time
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Experimental Optimization of C45

Starts with 1nF and gradually increases up to 220nF

Values larger than 220nF do not further reduce the impedance
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Package and Die Contribution

After optimization a resonant peak at 220MHz still remains

This resonant peak is caused by inductance and decoupling capacitors in the package

The intended FPGA clock frequency of 200MHz is changed to 320MHz where the PDN impedance has a minimum
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Example of Further PDN Optimization Study

Feasibility study of moving C39, C43, C44, C50 outside the FPGA region and using full vias instead of blind vias

Additional inductance added by lifting capacitors and adding wire jumpers
Test Case Summary

This test case has evaluated how the proposed FPGA on-die PDN impedance measurement technique can help with:

- Selection of decoupling capacitors’ values and types
- Trade-off between placement of decoupling capacitors and PCB manufacturing cost reduction (blind vias versus full vias)
- Identifying that the intended FPGA core clock frequency of 200MHz was too close to a PDN resonance peak at 220MHz
- Locating a minimum PDN impedance at 320MHz where the FPGA clock has been set to operate

Some of these PDN improvements have not been possible with only on-board PDN impedance measurements since the significant contributors were the interconnects and decoupling capacitors on the FPGA package and die
Conclusions

- Low cost alternative to existing PDN design methods
- Uses only logic blocks commonly available in any FPGA
- Can be implemented in any existing FPGA without the need of built-in dedicated measurement circuits
- Eliminates expensive test bench instruments and simulation software tools
- A case study has exemplified experimental optimization of decoupling capacitors and has studied various PDN design tradeoffs