

# Comparative Electromigration Performance of Pb Free Flip Chip Joints with Varying Board Surface Condition

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## Abstract

For the past several years, the semiconductor industry has been responding to the RoHS directive to eliminate certain hazardous substances from electronic components. One of the areas where work is still ongoing to comply is in the area of flip chip interconnects. Currently, leaded flip chip interconnects are allowed under an exemption in the RoHS directive due to a perceived lack of a technically viable solution. Recently, a number of Pb-Free flip chip interconnects have been introduced to the industry and have been in high volume production for a few years.

Electromigration is an area which has received quite a bit of attention over the years. There is a large body of data in the area of High-Pb and Sn/Pb eutectic flip chip interconnect systems, but there is still a relatively small database with regard to Pb-Free flip chip interconnects. This paper addresses relative electromigration performance on different base surface finishes of organic laminates, which is one of the key aspects where additional knowledge is needed to understand the proper implementation direction for Pb-Free flip chip interconnects.

The impact of ENIG, ENEPIG, and bare Cu on Sn/Ag bump electromigration including FA results is presented.

## I. Introduction

Electromigration (EM) is a diffusion controlled process that results in a mass transport of metal atoms in the presence of a current. In the past four decades, extensive efforts have been made on understanding the electromigration in aluminum and copper lines in integrated circuits so as to better control it [1, 2]. However, the continuing drive to improve device performance has been accompanied by an increased packing density of I/O, coupled with a reduction in the pitch and size of flip-chip solder interconnections. This phenomenon has emerged as a critical concern for the electromigration reliability of solder bumps carrying an increasing current density with shrinking dimensions.

Literature indicates guidelines of ~200mA per bump, with a current density of  $1 \times 10^4 \text{A/cm}^2$  based on UBM area [3, 4]. The current density, which results in EM of solder joints, is about two orders of magnitude smaller than those in Al or Cu interconnects. The main reason for the lower threshold current density is due to the low melting point and high atomic diffusivity of solder alloys [4]. This poses a physical limit to the continual shrinkage of flip-chip arrays and requires solutions to circumvent the reliability issue at hand.

Although research on Al(Cu) interconnect electromigration has developed acceleration tests and models that predict long term reliability of the phenomena [5], extension of these models and accelerated tests to solder bumps is challenging due to the differences between these two materials [2-4]. One of the most significant distinctions is that solder EM is complicated by the unique Al/Cu line to bump geometry. Due to the irregular geometry, current distribution is non-uniform. Where the current enters the corner of the bump, high current density is experienced due to current crowding effect. The local temperature in this region is extremely high due to the joule heating. The other main difference is that in solder bumps, the complex interaction of under bump metallization (UBM), the binary/ternary solder alloys, the substrate finish, trace routings and other factors will affect EM life. The EM of chip interconnects on the other hand, are much simpler and straight forward with less material interactions.

Despite the contrast between line interconnect and solder bump EM, Brandeburg and Yeh [6] studied the electromigration of eutectic solder joints and concluded that the life time of the joint adheres to Black's equation [7], which is widely used as a model to estimate the life time of chip-level interconnects. While it is unlikely that Black's equation can be applied without modification to solder bumps, further work will be needed to propose a more comprehensive model [8, 9]. Black's equation is given by:

$$\text{MTTF} = \text{A} \cdot \text{J}^{-n} \cdot \exp(\text{Ea}/kT)$$

where MTTF is the median time to failure, A is the constant to be determined experimentally, J is the current density and n is the current density associated exponent, Ea is the activation energy, k is the Boltzmann constant and T is the temperature of the joint. The two main stress drivers for electromigration are constant current and temperature and usually a matrix of experiments is setup to determine n and Ea. These two Black's equation model parameters are necessary in order to be able to project the life time of the device from accelerated test conditions to use/field conditions.

While there are many studies on the solder EM reliability and its associated failure mechanisms, there are relatively fewer works which actually determine the n and Ea values of the solder bump interconnections [10-14]. For high lead solder (95Pb-5Sn), the parameters of the model were found to be  $\text{Ea} = 0.8\text{eV}$  and  $n = 1.8$  [15]. The n value is reasonable compared in light of the  $n = 2$  as proposed by Black for the

current density constant for aluminum lines [7]. However, other researchers found for high Pb and Eutectic Sn/Pb, Ea values of 0.91eV and 0.86eV respectively [12]. Due to the experimental time constraint, n values were assumed to be 1-2. Plotted graphs in their works [12, 13, 16] showed the relative trend among high Pb, eutectic Sn/Pb and Pb-free solders. High Pb solders had the longest EM life followed by Pb-free solders (i.e. 97Sn-3Ag) while eutectic Sn/Pb bumps had the worst performance with the shortest MTTF.

For Pb-free solders such as the popular eutectic Sn/Ag, the n and Ea values are uncertain. Min et al [13] estimated the n to vary between 1-2 and Ea to be from 0.68-1.07eV. On the contrary, Lee et al [11] found that for Sn-3.5Ag solder bumps, the Ea =1.63eV and n = 4.6. The values obtained are quite high and according to them, is due to the presence of severe joule heating. Ebersberger et al [10] attributes the variation in n values to the fact that the current density exponent is not a constant and asserts the value of n is dependent upon the failure criterion chosen.

To alleviate the effects of current crowding, joule heating and eventual electromigration induced crack propagation, copper pillar bumps have been proposed as an alternative technology [17]. In addition, the thick copper column may also serve to prevent rapid UBM consumption/dissolution [18, 19]. The structure also allows fine pitch and high density I/Os devices to be fabricated but the effect on the thermomechanical reliability especially on fragile copper low-k silicon chips has still not been sufficiently investigated. Nonetheless, published data shows two magnitudes of improvements in electromigration MTTF using copper pillars, which make it a promising candidate for future interconnections [20].

Another issue to address is that changes in substrate surface finish [21, 22] or under bump metallization [14] often account for differing EM behaviors, even when the solder bumps are of the same composition. In [21], two substrate surface finishes, Au/Ni and organic solder preservative (OSP), with eutectic Sn/Pb solder bumps were compared. It was observed that OSP finish had the effect of extending the MTTF of the solder bump by six times. In addition, Lu and co-workers [22] compared the EM performance for Sn/Ag and Sn/Cu solders with different surface finishes (using copper wire test structure) and found that Cu finish laminates with Sn/Ag had the longest EM life. Furthermore, the Ni based UBM is found to have a better EM performance as compared to Cu based UBM [14, 22].

Review of literature shows that Amkor solder EM reliability is advancing in the right direction with offerings of Ni-based UBM and Sn/Ag solder bumps. This work extends the research of relative comparisons based on the wire test structure [22] to solder bump chain test vehicles in order to study the effects that varying surface treatments have on EM performance as well as to obtain the MTTF, n and Ea values so that projection to field use conditions could be made.

## II. Test Vehicle Description

As stated earlier, the purpose of this evaluation is to investigate the impact that varying board surface treatments have on electromigration. In order to give a consistent

comparison, a single test vehicle was chosen to evaluate while varying only the surface treatment of the laminate substrate. The test vehicle is a silicon test chip design incorporating EM test structures. The die is in a 42.5mm package with a build up substrate. Details of the test vehicle are in Table 1.

One of the areas of extensive study with regard to electromigration is the phenomenon of current crowding. When studying the electromigration effects of a particular alloy system, it is desirable to design the test structure so that the effects of current crowding are minimized so that these current crowding effects don't introduce error in the analysis. In this test vehicle, the primary path of study is with electrons flowing from the silicon die through the bump to the substrate. In order to minimize the effect of current crowding, the electrons that are feeding the bump on stress are fed from multiple bumps. In this way, the current is supplied by multiple paths minimizing the effects of current crowding. Figure 1 shows a cross sectional view of how the bump on stress is fed from the adjacent bumps. Figure 2 is a top down view showing how the bump on stress is fed from multiple sides thereby minimizing current crowding effects.

Feature Description	Designed Dimension
UBM Stack	Sputtered Ti/Cu Plated Ni
UBM Diameter	90 μm
Bump Alloy	Sn2.3%Ag
Substrate Pad Size (SRO)	85 μm
Substrate Finish	Cu + SOP
	ENIG + SOP
	NiPdAu (ENEPIG) + SOP
SOP Alloy	SAC305

Table 1. EM Test Vehicle Attributes

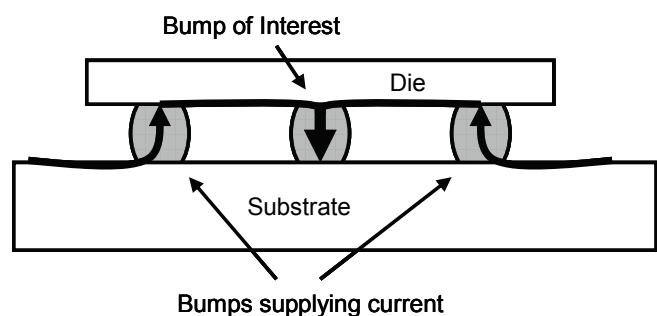


Figure 1. Cross Section Schematic of EM Structure

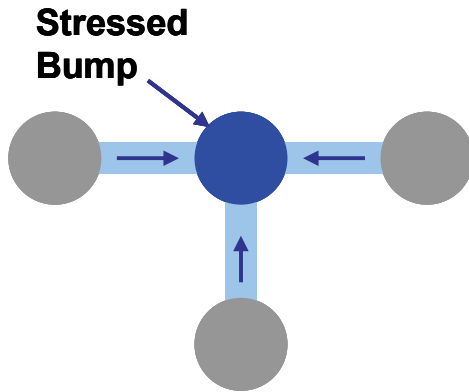


Figure 2. Top View of EM Structure

### III. Experiment Plan

The objective of this experiment is to compare the electromigration performance of Amkor's Sn/Ag Pb-Free bumps on varying laminate substrate surfaces. The overall experiment plan is to collect EM failure data at various temperatures and current levels for each laminate surface treatment. Table 2 describes the basic experimental matrix.

Lot	Substrate Finish	Oven Temperature (°C)	Bump Temperature (°C)	Current (mA)
Lot A	Cu + SOP	126	135	500
				700
		141	150	500
				700
Lot B	ENIG + SOP	126	135	500
				700
		141	150	500
				700
Lot C	NiPdAu + SOP	126	135	500
				700
		141	150	500
				700

Table 2. Electromigration Stress Matrix

The test vehicle has temperature sensors on the die just under the bump being stressed. In this way, during the initial characterization of the test chamber, the temperature sensors can be calibrated, and used to calculate the joule heating of the test structure. Although joule heating varies from part-to-part and condition-to-condition, an average of 9°C temperature increase was observed. The oven temperature setting was then chosen knowing the joule heating so that the desired final bump temperature was achieved.

The damage to the bump caused by the electromigration phenomenon causes voiding in the solder joint which effectively reduces the cross sectional area of the bump. This reduction in cross sectional area increases the density of current flowing through the bump. The electrical resistance of the bump also increases with the effective decrease in current carrying area. These two effects increase the effective temperature of the bump through increased joule heating, and also increase the rate at which the EM damage occurs as the

current density increases. Since the rate of damage accelerates during the course of the test, it is important to make a good judgment as to when the part has failed. If parts are pulled too soon due to strict criteria, it is difficult to derive meaningful data and understanding from the results. Conversely, if the chosen failure criteria allow the parts to be stressed too long, the bump can become too damaged. As the damage increases, the joule heating can easily reach a point where the solder melts. If the solder melts, there is very little, if any, knowledge that can be ascertained regarding the electromigration mechanism at work. There is also some debate regarding the best definition of failure criteria. Some choose a percent change in resistance to identify the extent of damage that could reasonably yield the most knowledge and understanding of the system under stress. In this evaluation, the authors chose an absolute change of 10mΩ as the failure criteria. The choice to use an absolute resistance change rather than a percent change was due to the fact that the resistance of the bump was very small in comparison to the overall resistance of the test circuit. Since the resistance of the bump itself is generally on the order of a few milliohms, the criteria of 10mΩ absolute change accounts for a high percentage change in resistance for the bump, and also allows for some resistance increase of the overall test circuit as it is also under some level of stressing.

The experiment was performed using a two-oven Qualitau MIRA (modular integrated reliability analyzer) EM tester. The voltmeters and ovens were calibrated to ensure the accuracy of the readings. Two oven temperatures and two stress currents were used for each of the lots A-C with different surface finishes. The EM tester was set to take four point Kelvin measurements at logarithmic intervals of 100 per decade. While the ovens ramp up to the stress temperatures, the calibration of temperature coefficient of resistance (TCR) was performed on the test vehicles at four different temperatures before the actual stress temperature was achieved. The joule heating effect for each device under test (DUT) can be determined by the EM modules and software of the equipment. The tester was also modified to include a National Instruments data acquisition system to separately and independently perform the TCR measurements also by a four point resistance measurement. This was done by using the temperature sensors beneath the solder bumps to more accurately determine the joule heating experienced by the solder bumps so that temperature corrections could be made.

### IV. Results and Analysis

As was expected, there was a difference seen in the electromigration performance of the Sn/Ag joint depending on the substrate surface treatment condition. Table 3 shows a summary of results where it can be seen that the parts using the ENIG and ENEPIG had a significantly lower life than the parts using just the base copper surface with OSP which is presumably burned off during the chip joining process, and is not present in the system during the EM stressing.

The data for each surface treatment is plotted in Figures 3-5. There are a number of areas where there is considerable scatter among the data. In the case of base copper surface (Figure 3), there is considerable scatter as well as early

Leg	Description	UBM Diameter (μm)	Temperature (K) (Oven + Joule Heating)	Current (A)	# Failed / # Tested	Lognormal Parameters		t50 (hrs)
						Mean Life	Sigma	
1A	Cu	90	408	0.500	6 / 7	9.40	2.11	12,035
2A	Cu	90		0.700	7 / 7	6.01	0.52	408
3A	Cu	90	423	0.500	5 / 5	8.45	1.20	4,662
4A	Cu	90		0.700	8 / 8	5.26	0.68	192
1B	ENIG	90	408	0.500	5 / 5	6.60	1.06	736
2B	ENIG	90		0.700	5 / 5	5.12	0.77	168
3B	ENIG	90	423	0.500	8 / 8	5.79	1.30	327
4B	ENIG	90		0.700	6 / 6	4.95	0.97	142
1C	ENEPIG	90	408	0.500	6 / 6	6.51	1.19	671
2C	ENEPIG	90		0.700	7 / 7	5.68	0.98	292
3C	ENEPIG	90	423	0.500	5 / 6	5.46	1.03	235
4C	ENEPIG	90		0.700	8 / 8	4.62	0.98	101

Table 3. Sn/Ag Electromigration Test Results Summary

failures in the most benign condition of 0.5A at 135°C. Due to this, the data for this leg of the experiment seems to be suspect. In the leg using an ENIG finish on the copper base, there is some scatter on the 0.5A conditions at both the 135°C and 150°C temperatures. The scatter for these two conditions with a standard deviation ( $\sigma$ ) of 1.06 and 1.30 respectively are still considerably lower than the scatter of the base copper sample stressed under 0.5A at 135°C where the  $\sigma$  is 2.11. The legs using parts with an ENEPIG finish had more consistent scatter among the different conditions with  $\sigma$  ranging from 0.98 and 1.19. It should also be noted that there was a consistently higher  $\sigma$  on the legs where the parts were stressed at 0.5A compared to those legs stressed at 0.7A.

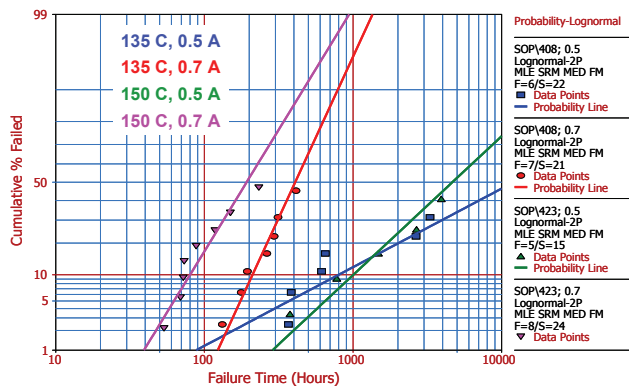


Figure 3. Electromigration Test on Sn/Ag Bump for Cu Finish with SAC305 SOP

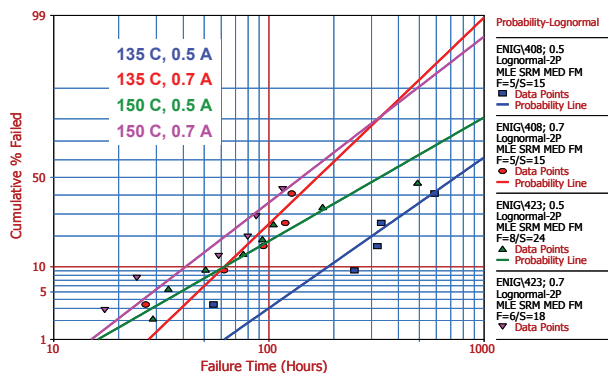


Figure 4. Electromigration Test on Sn/Ag Bump for ENIG Finish with SAC305 SOP

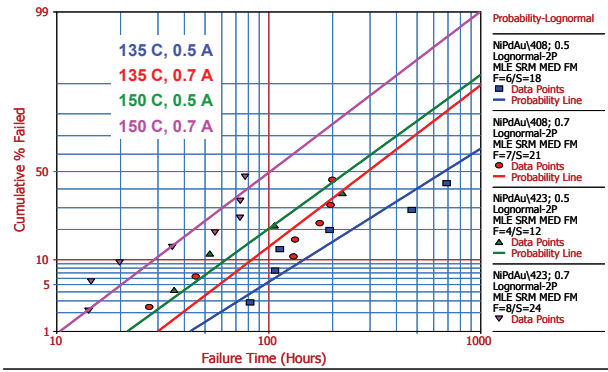


Figure 5. Electromigration Test on Sn/Ag Bump for ENEPIG Finish with SAC305 SOP

Figures 6-9 show the relative performance between the surface conditions at each stress condition. Note that the current densities listed are based on UBM area. In all conditions tested, the base copper parts clearly showed better performance compared to their ENIG and ENEPIG counterparts. The data indicates that the relative performance between base copper and the other surface conditions changes considerably as the current density changes. This would indicate that the acceleration factor due to current is much higher for the base copper case compared to the other surface conditions. This is also reflected in the calculated parameters for Black's Equation shown in Figure 10.

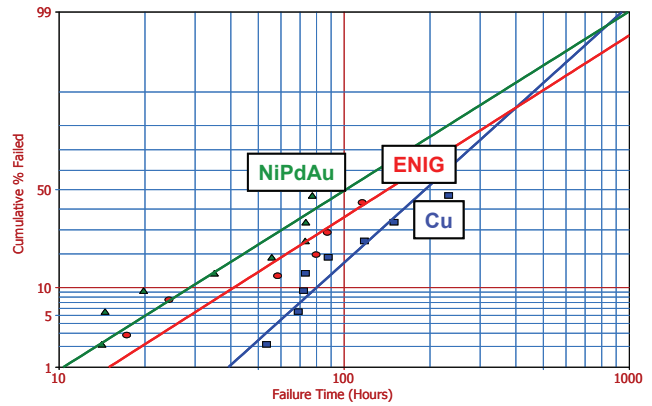


Figure 6. Relative Electromigration Performance - 150°C & 11,000A/cm<sup>2</sup>

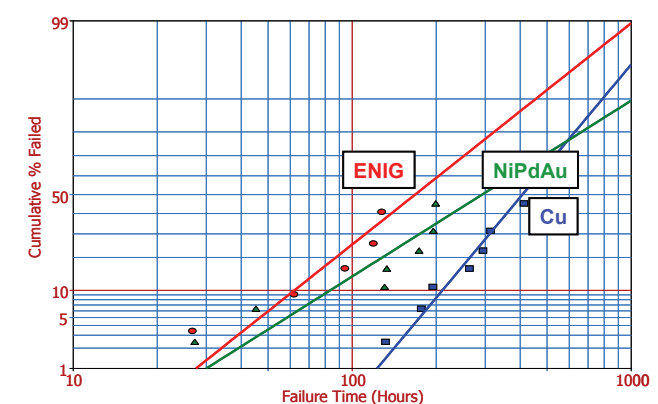


Figure 7. Relative Electromigration Performance - 135°C & 11,000A/cm<sup>2</sup>

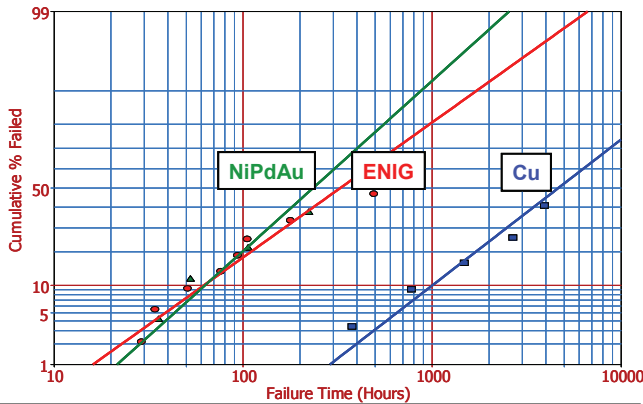


Figure 8. Relative Electromigration Performance - 150°C & 7,860A/cm<sup>2</sup>

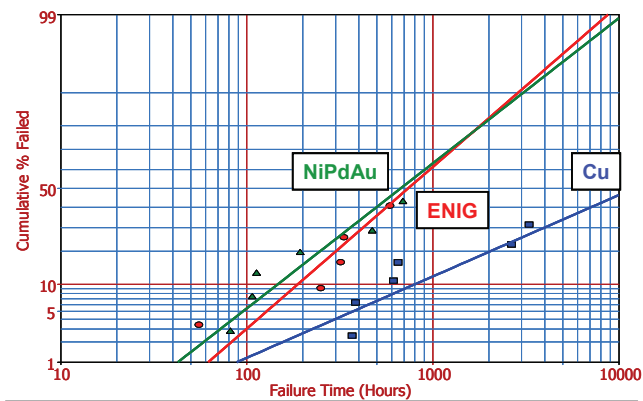


Figure 9. Relative Electromigration Performance - 135°C & 7,860A/cm<sup>2</sup>

The relative performance between ENIG and ENEPIG is much less clear. In three out of the four stress conditions, the ENIG showed better performance than ENEPIG, but the relative performance increase only ranged in a 1.1X to 1.4X longer life. In the stress condition with the lower temperature of 135°C and higher current density of 11,000A/cm<sup>2</sup>, the trend is reversed with ENEPIG showing better performance with an expected life of 1.7X better than ENIG.

Figure 10 shows the calculated parameters for Black's Equation based on this data. The Activation Energy component (Ea) is considerably lower than the expected value of 0.9~1.0 for the ENIG parts. When reviewing the data again in Figure 7, the scatter on the lower current conditions were a bit high with  $\sigma$  values in excess of 1.0, but this level of scatter is certainly not significantly higher than the other legs. At the lower current condition, there seems to be a reasonable difference in performance between the high and low temperatures, however, at the higher current condition, there is very little difference in predicted life between the two temperature conditions. This can be seen graphically in Figure 7, and can also be seen on Table 3 where the predicted t50 life for the 0.7A ENIG leg at 150°C is 142 hours, and the predicted t50 life for the corresponding 135°C leg only increases by 18% to 168 hours. This relatively small increase in expected life between 135°C and 150°C drives the low Ea number calculated.

$$\text{Black's Equation: } MTF = AJ^{-n} \exp\left(\frac{E_a}{KT}\right) \quad *J \text{ in Amps}$$

	ENIG	Cu	NiPdAu
Ea	0.49	0.84	1.04
n	3.44	9.77	2.49

Figure 10. Black's Equation Parameters

Figure 10 also shows a wide range in calculated acceleration due to current (n). In this data, the calculated n value is higher than typically expected, with the n value for the base copper parts being extremely high with a value approaching ten. With the many years of study on the Sn/Pb alloy system, it is generally accepted that this current acceleration factor should be in the range of about 1.0 to 2.0. As Sn/Ag and Sn/Ag/Cu systems are being studied, it is generally believed that this acceleration factor, n, should roughly fall in the same range. This investigation along with some other papers published in the past few years would seem to indicate that the acceleration factor for current in this system is fundamentally different, and higher, than that of the Sn/Pb system.

## V. Failure Analysis and Discussion

In addition to getting the failure rates and calculating acceleration factors, it is always an integral goal of any EM study to try to better understand the mechanisms at work in this fascinating phenomenon. The following figures are intended to give the reader some practical understanding of the damage that is caused as the solder joint is subjected to the high current and temperature conditions. As can be seen in Figures 11-14, which correspond to the ENIG and ENEPIG surface finishes, there is essentially no intermetallic remaining at the UBM interface, and there is a thick intermetallic layer building up at the interface with the substrate. In contrast, as can be seen in Figures 15 and 16, there is still evidence of some nickel intermetallic at the UBM interface, and there is a

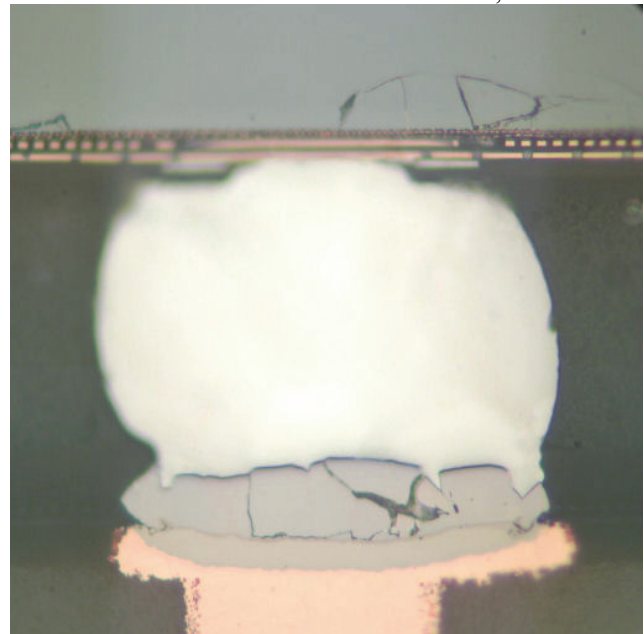
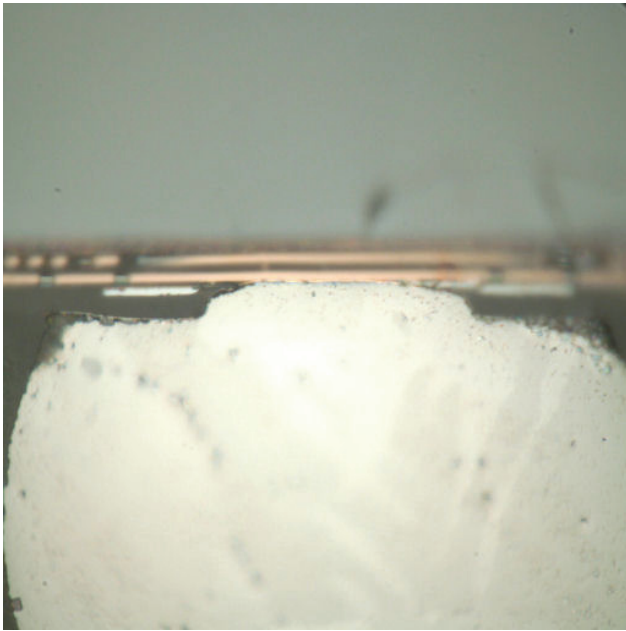
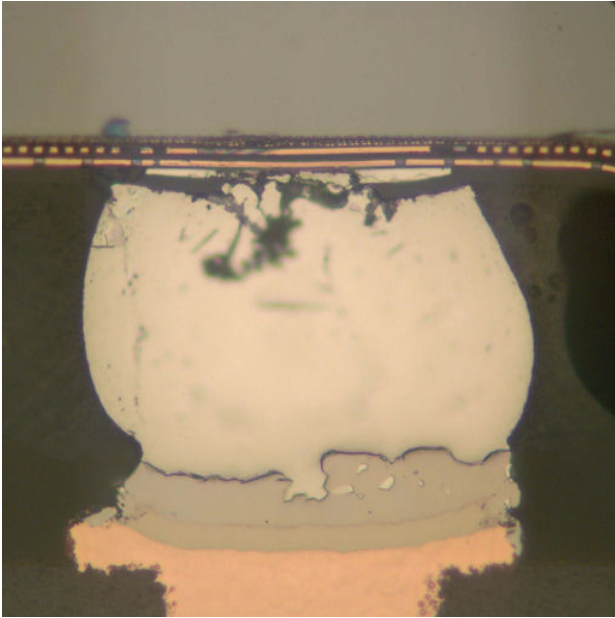


Figure 11. ENIG Sample Cross Section - 257 hrs (150°C, 0.7A)



**Figure 12. ENIG Sample UBM Closeup – 257 hrs (150°C, 0.7A)**

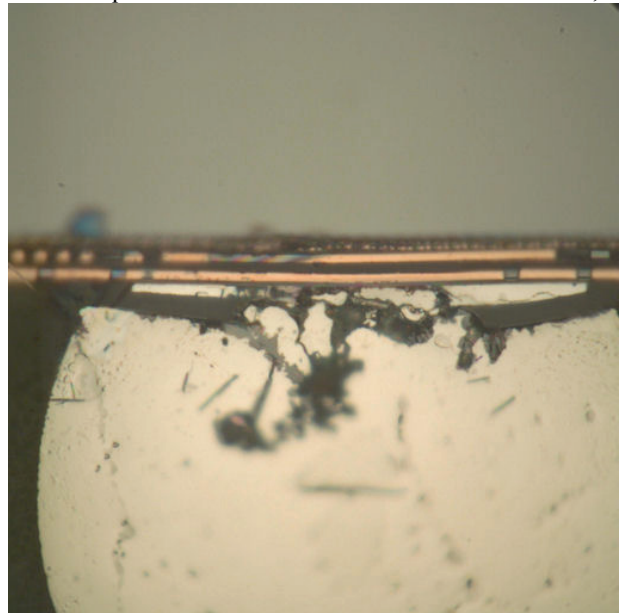


**Figure 13. ENEPIG Sample Cross Section – 61 hrs (150°C, 0.7A)**

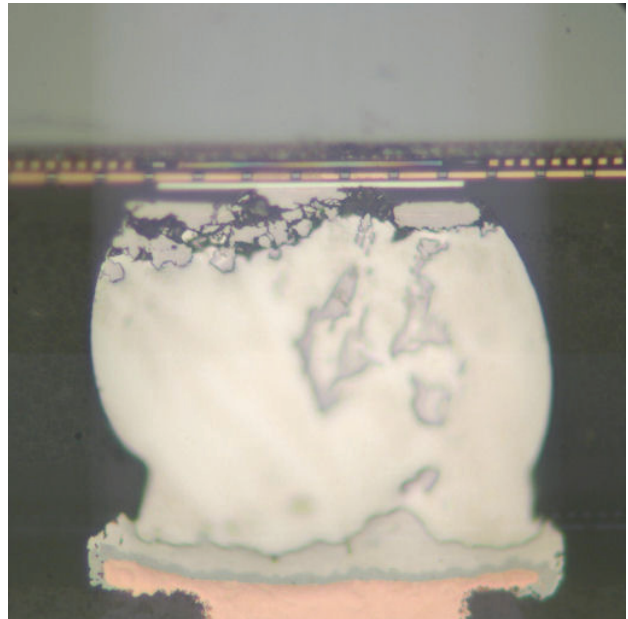
much thinner layer of intermetallic at the interface with the substrate. The failure mode in the ENIG and ENEPIG samples is consistent with the Mode 3 failures identified by Lu, et al [22] produced by the [001] Sn grain orientation aligning with the current direction. Electron Backscatter Detection (EBSD) has verified that the [001] grain orientation was prevalent in these samples after stressing. The effect of grain orientation effects, in which the [001] orientation can result in very fast diffusion rates, can have an impact on the calculated activation energies.

There are a number of aspects to this experiment that do not strictly follow previously published data. Certainly, the level of scatter in the data as shown in the various graphs (Figures 6-9) indicate that there may be some factor introducing error into the results. Although not covered in

detail in this Failure Analysis section, it was determined that some of the failures in this experiment were actually due to a deterioration of the test board being used, and not caused by electromigration at the bump being tested. Unfortunately, there were not enough resources available to do complete FA on all failures in order to determine exactly which ones were failing due to the test board issue, and which ones were truly failing due to EM damage. Since the same test board construction was used on all legs, the authors believe that this error is distributed evenly among all legs. The authors further believe that since the error is distributed evenly, that, from a relative standpoint, the data is valid. However, since there is known error in the data, which the scatter in the data would also indicate, the absolute t50 life expectations, and the Black's Equation acceleration factors include the error, and



**Figure 14. ENEPIG Sample UBM Closeup – 61 hrs (150°C, 0.7A)**



**Figure 15. Copper Sample Cross Section – 933 hrs (150°C, 0.7A)**

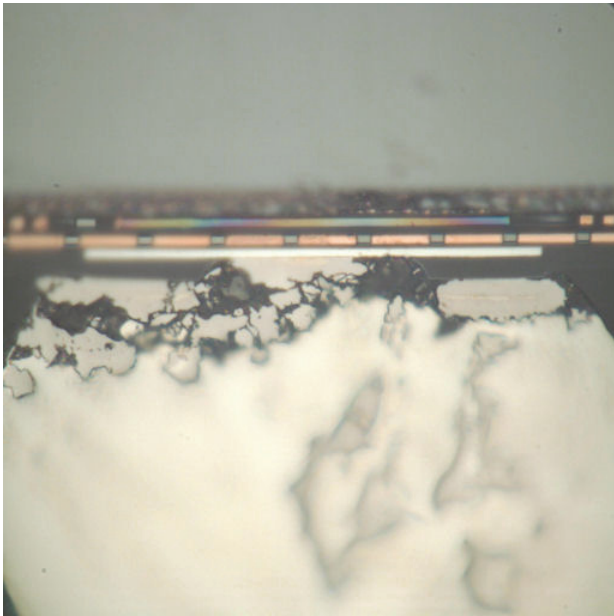


Figure 16. Copper Sample UBM Closeup – 933 hrs (150°C, 0.7A)

therefore, should not be used to compare this data set to other data on Sn/Ag/Cu electromigration. This error may explain the low activation energy ( $E_a$ ) seen on the ENIG parts, and the extremely high current acceleration factor ( $n$ ) seen on the base copper parts.

## VI. Conclusions

There are two basic conclusions or observations that the authors believe that this data support. First, the Sn/Ag/Cu solder joint system has the best electromigration resistance when it is used with a base copper substrate compared to substrates using either an ENIG or an ENEPIG surface finish. There seems to be a consistent phenomenon taking place where the presence of a Ni barrier layer on the substrate causes a faster depletion of UBM intermetallics, and a corresponding accumulation of intermetallics at the substrate interface. This leads to the earlier failure of the parts using the ENIG or ENEPIG surface finishes.

The second conclusion is more of an observation supported by this data in combination with other published data in the past couple of years. It is that there is growing evidence that the assumption that the Sn/Ag/Cu alloy system should have a current acceleration of roughly the same as the Sn/Pb system is not supported. In this experiment, as in a number of previous EM investigations on the Sn/Ag/Cu system, the calculated current acceleration factor ( $n$ ) was found to be higher than the value of 2.0 which has been generally regarded as the practical upper limit for this parameter. In previous investigations, it has been theorized that some error in calculating the joule heating is the cause for this anomaly. Certainly, the change in joule heating which occurs as the bump under test deteriorates is of concern, but the growing number of experiments showing higher  $n$  values for the Sn/Ag/Cu system, give more and more evidence that this cannot simply be waived off as inherent experimental error. It may be indicating that the current acceleration factor for the Sn/Ag/Cu system is fundamentally different than the

Sn/Pb system, or at least complicated by the Sn grain orientation effects and current crowding effects in the test structures. As the body of data on Sn/Ag/Cu grows, it will become apparent if this observation is accurate or not.

## Acknowledgments

The authors would like to acknowledge and thank the manufacturing team in Amkor's P3 factory who built the samples used in this experiment, especially Jose Cabauatan. In addition, the authors would like to thank the FA team at IBM, especially Jim Rosa, Frank Dicesare, and Chuck Goldsmith who provided excellent cross sections and other failure analysis which is invaluable in understanding the mechanisms at work.

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*Note: As related to semiconductor products and materials, the term "lead free" does not mean that a product contains no lead. Rather, the term means that each homogeneous material of a product will likely have a maximum concentration value of 0.1% of lead by weight. The term "lead reduced" indicates that each homogeneous material of a product will likely have a maximum concentration value of 0.1% lead by weight, except those homogeneous materials where a RoHS Direction exemption may apply, such as an alloy containing >85% Pb, or a flip chip solder joint.*

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