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IBIS AMI Modeling of Retimer and Performance Analysis of Retimer based Active Serial Links

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UBM Tech

Overview

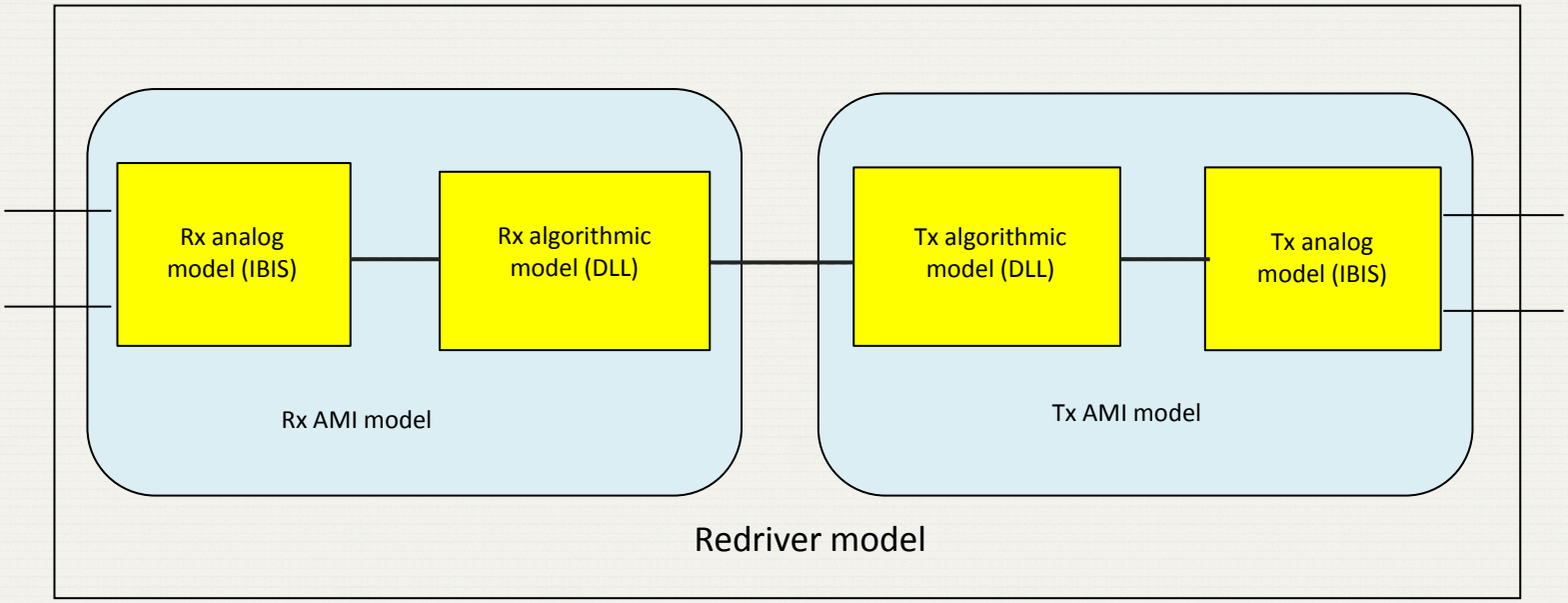
- Retimer implementation and simulation flows based on IBIS-AMI Standard 5.2
- General Retimer topology
- Jitter transfer analysis by using Retimer AMI model
- Full link analysis by using IBIS-AMI models

Background

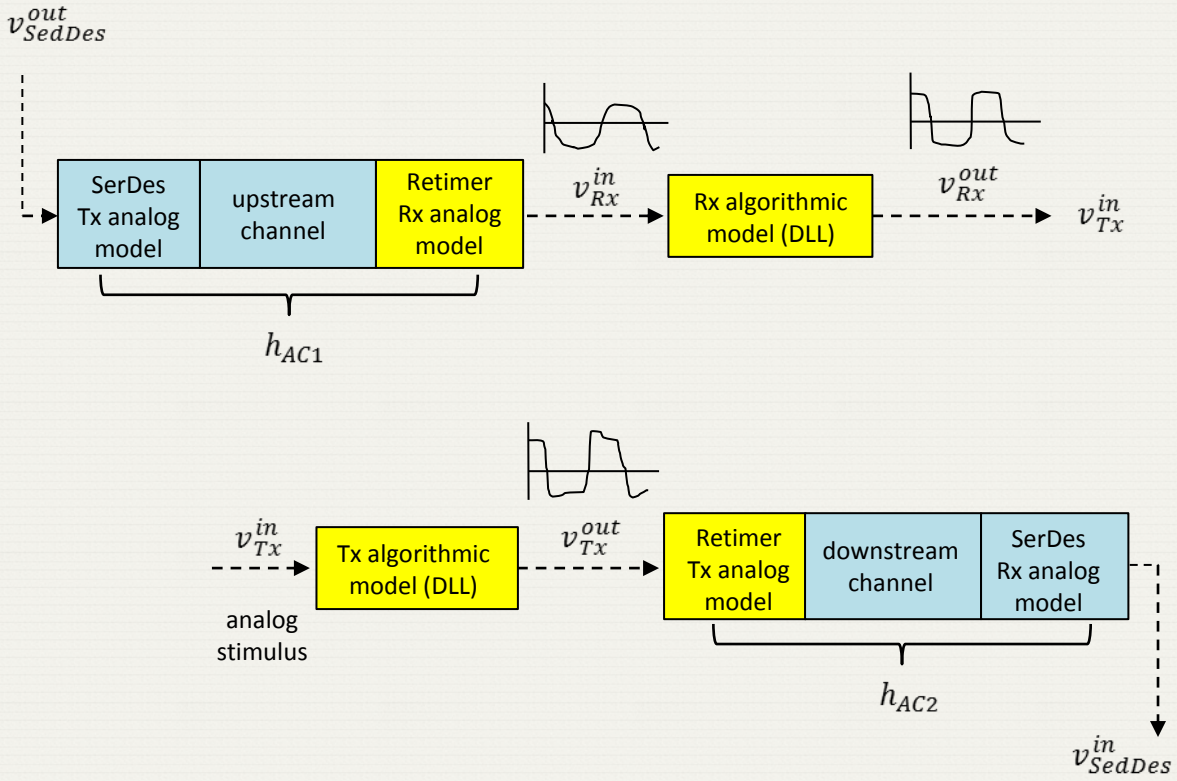
- Repeaters, including redrivers and retimers, are increasingly applied in high-speed interconnects to compensate loss
- Redriver restores the signal with equalization and pre-emphasis
- Retimer employs clock-data-recovery (CDR) to sample the equalized signal and recover the digital signal
- Retimer can track and filter jitters in the incoming signal and fully compensate the upstream channel loss

Existing Redriver AMI Modeling Methodology

- Redriver is modeled by two back-to-back Rx and Tx IBIS-AMI models

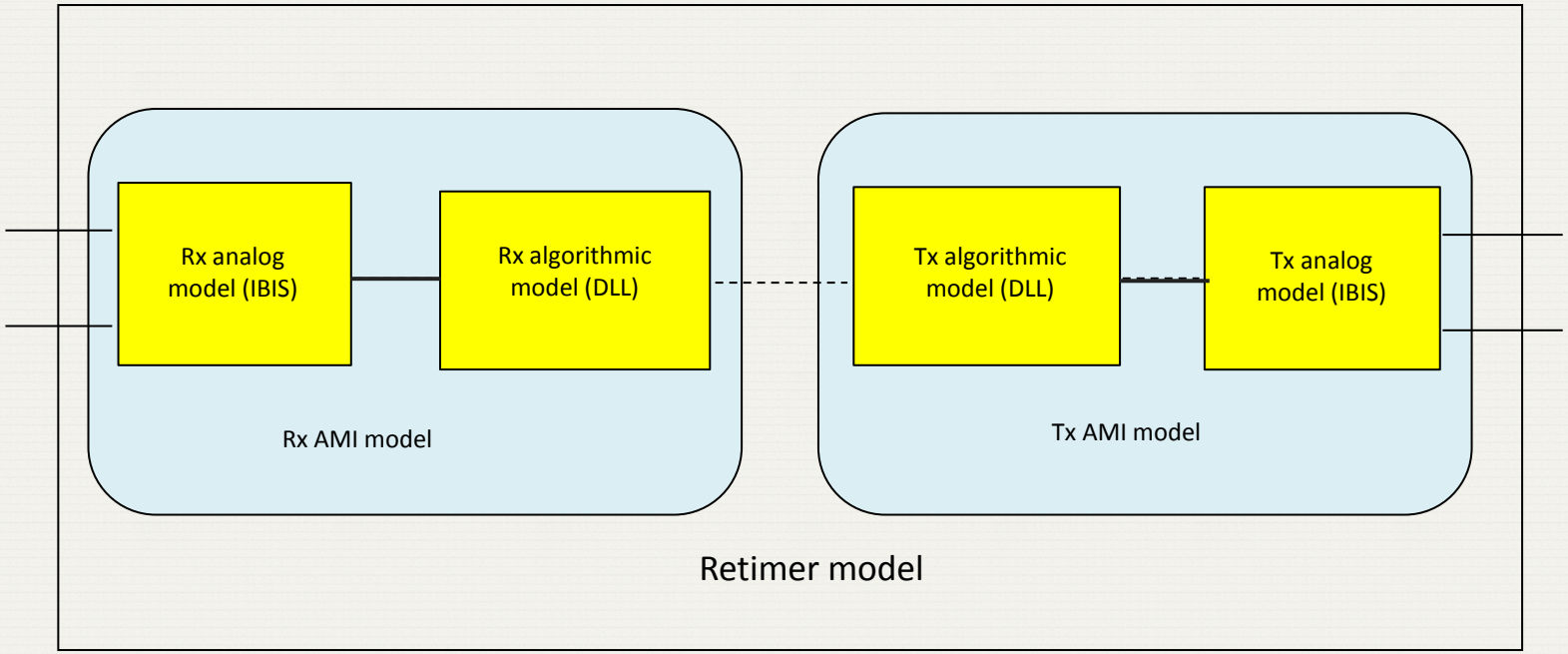


Existing IBIS-AMI Redriver Simulation Flow



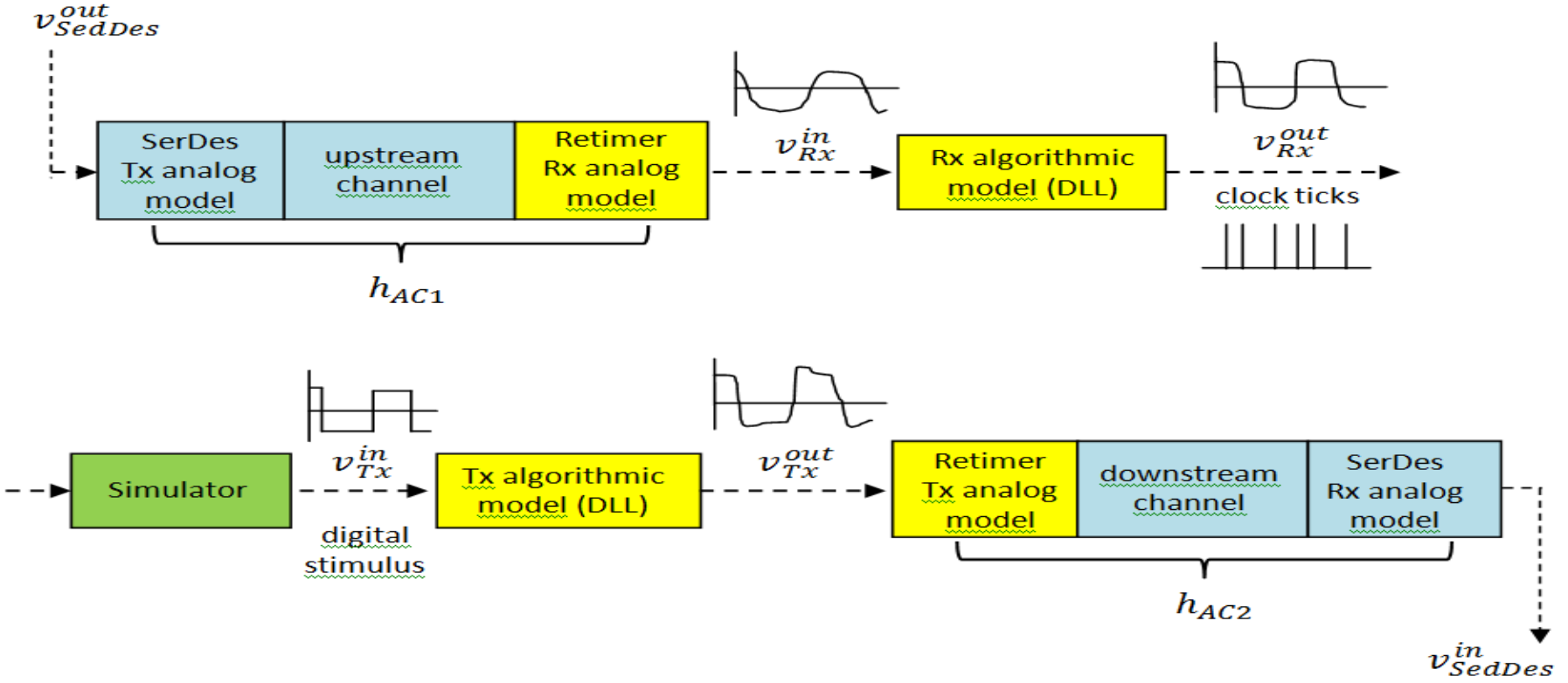
- Redriver Tx is continuously driven by redriver Rx's analog output signal
- Inefficient to model recovered clocks and digital signal in retimer

IBIS-AMI Retimer Model Methodology



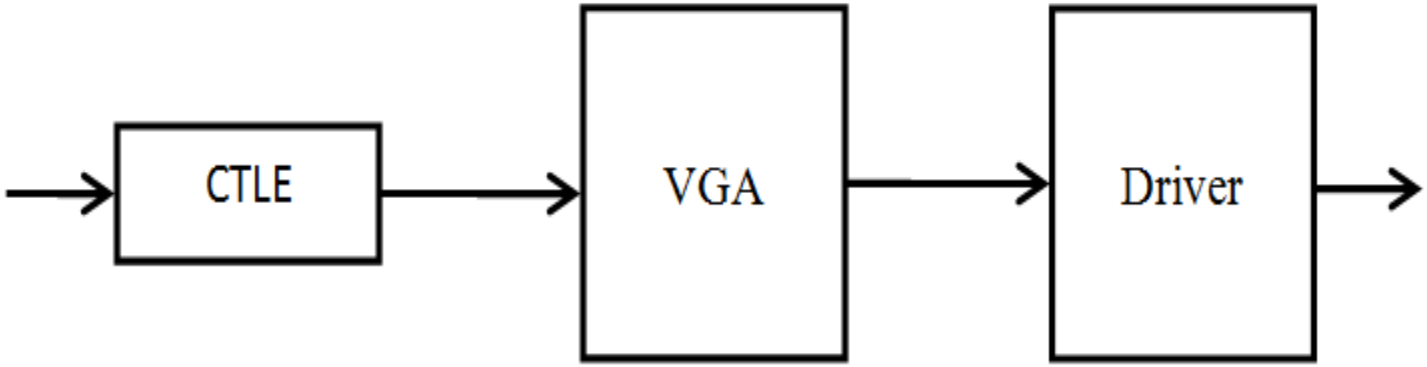
Retimer Rx model must implement AMI_GetWave function, and the function must return clock times.

IBIS-AMI Retimer Simulation Flow

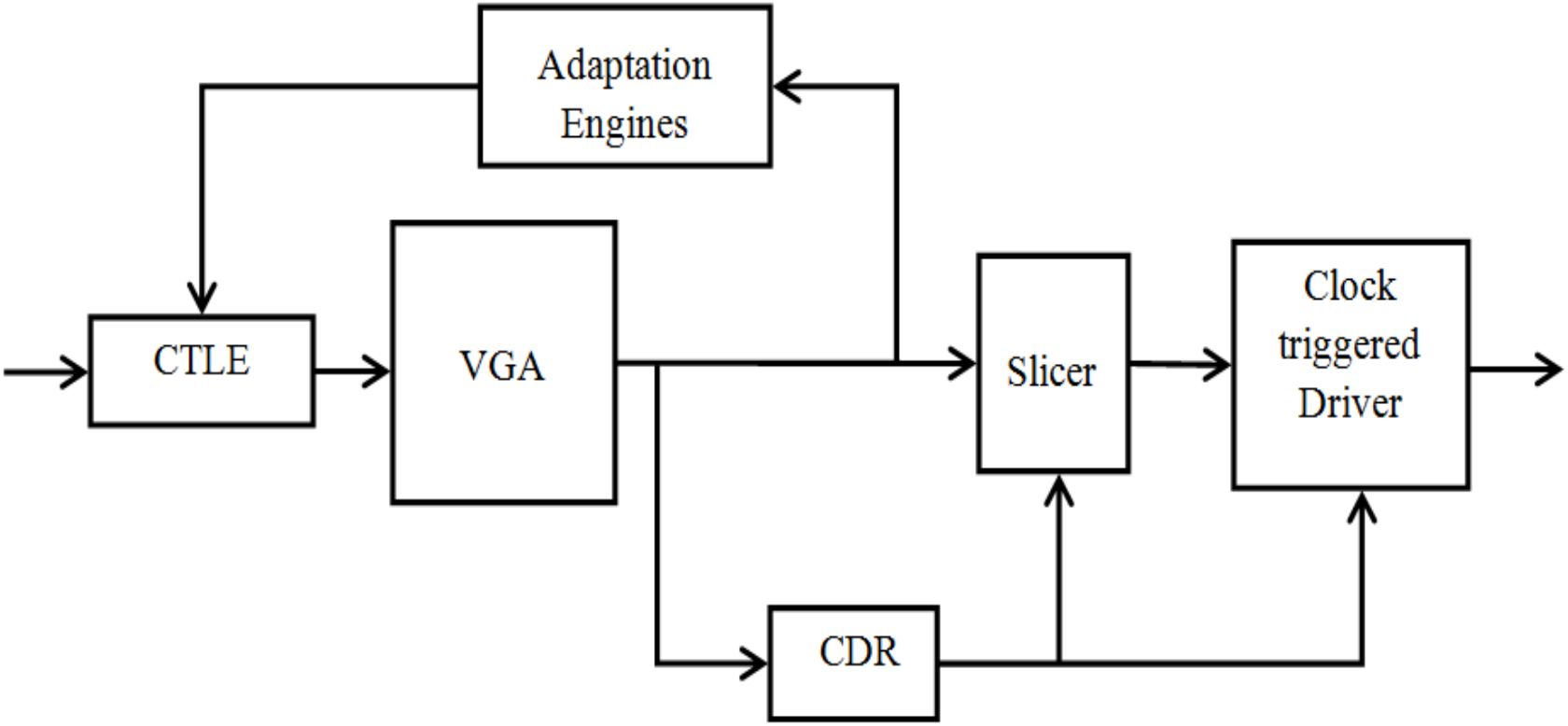


Simulator samples retimer Rx Getwave's output signal at 0.5UI after each clock time returned by Rx, generates the digital stimulus that drives retimer Tx

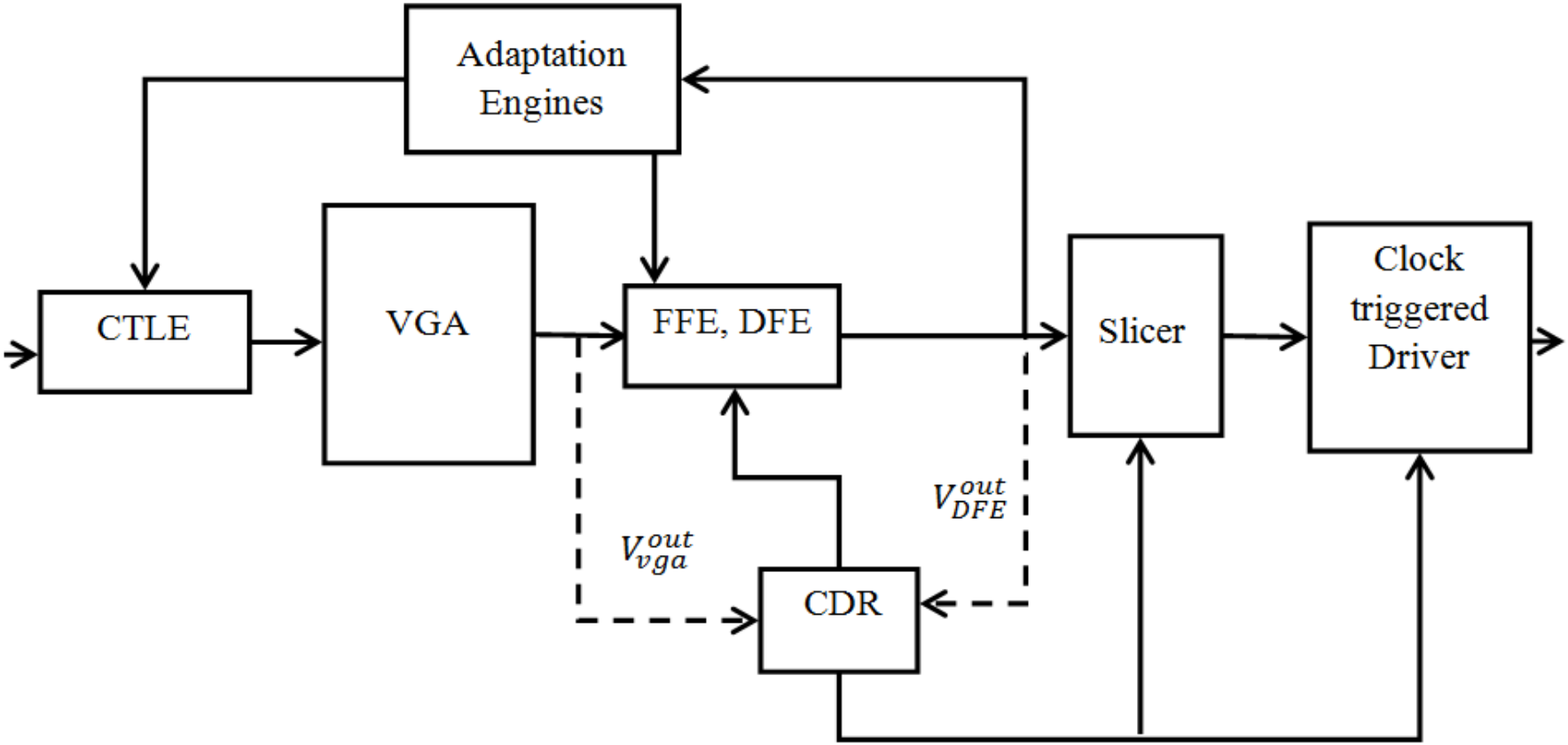
General Redriver Topology



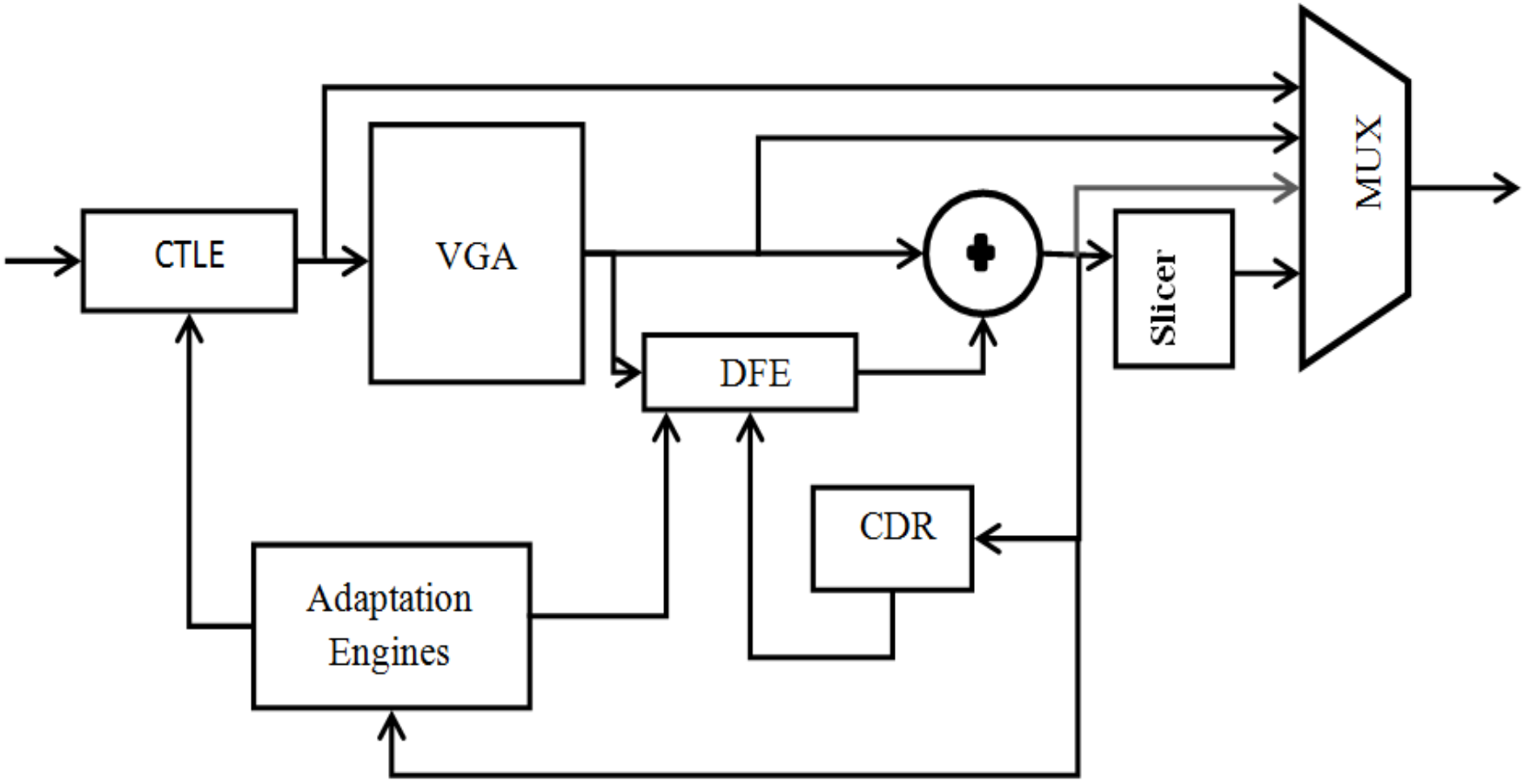
General Retimer Topology



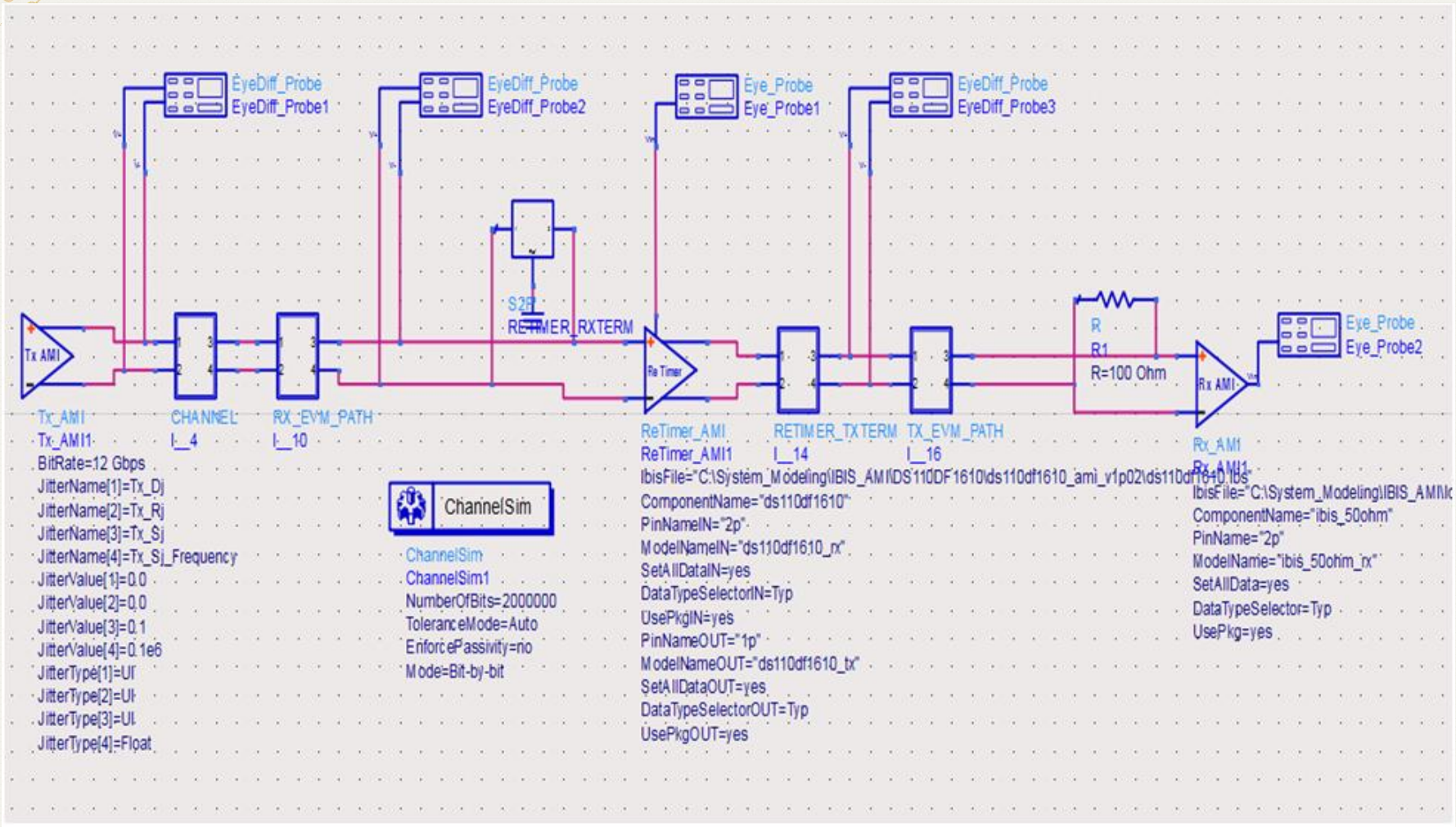
General Retimer Topology (cont'd)



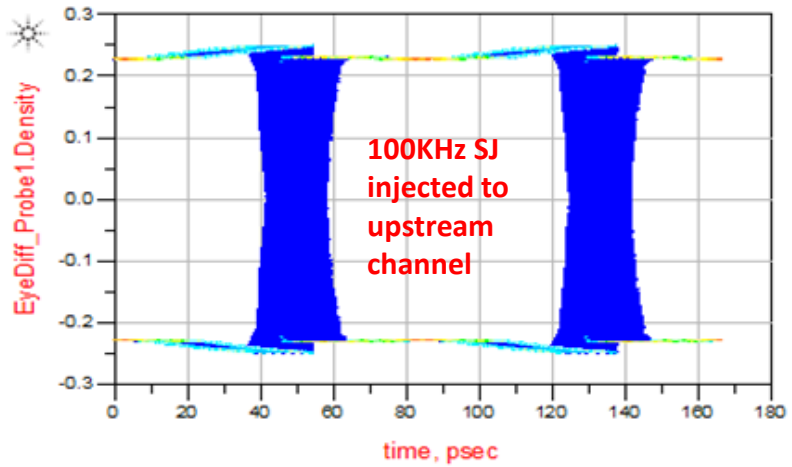
A Retimer-RX AMI model with DFT

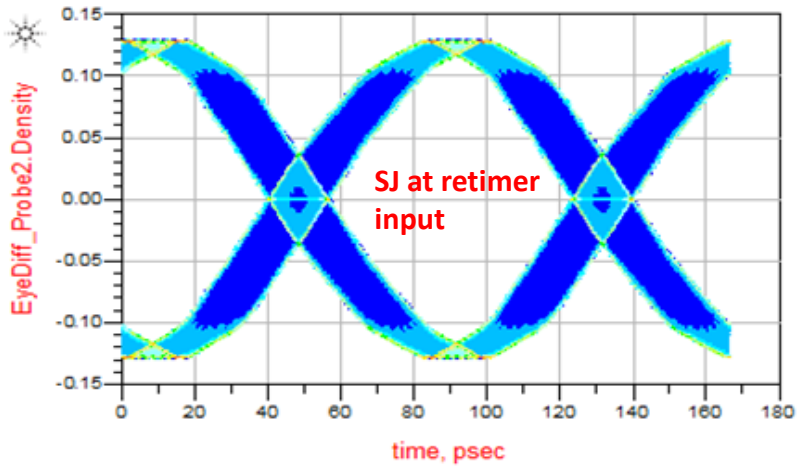


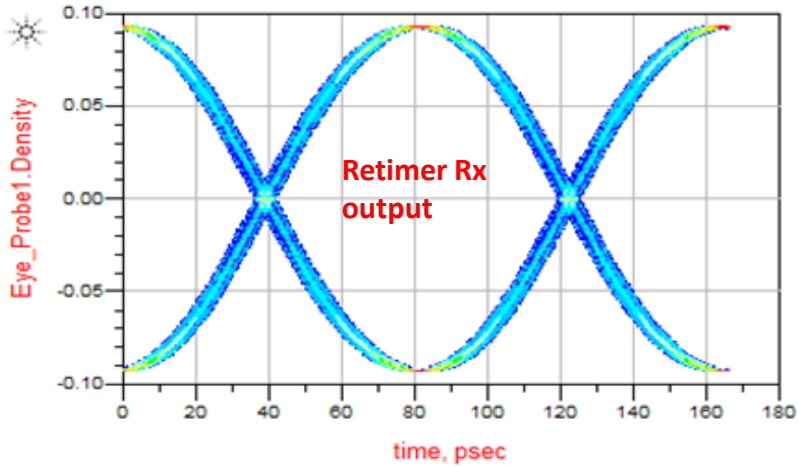
Jitter Transfer Analysis



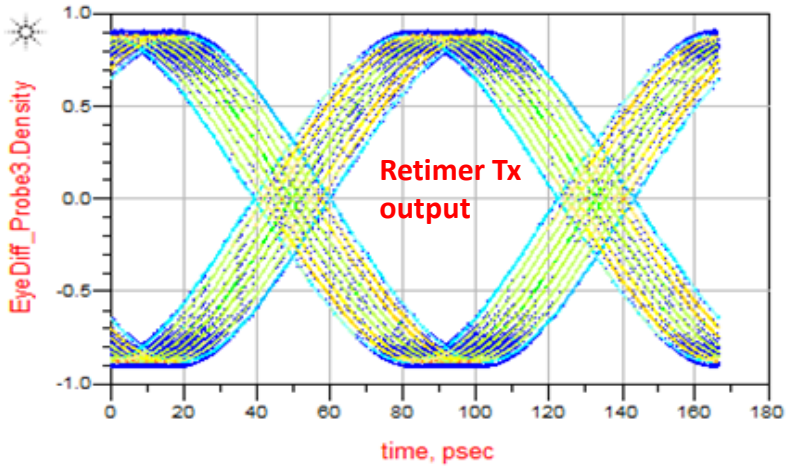
Retimer Tracks Low-frequency Jitter





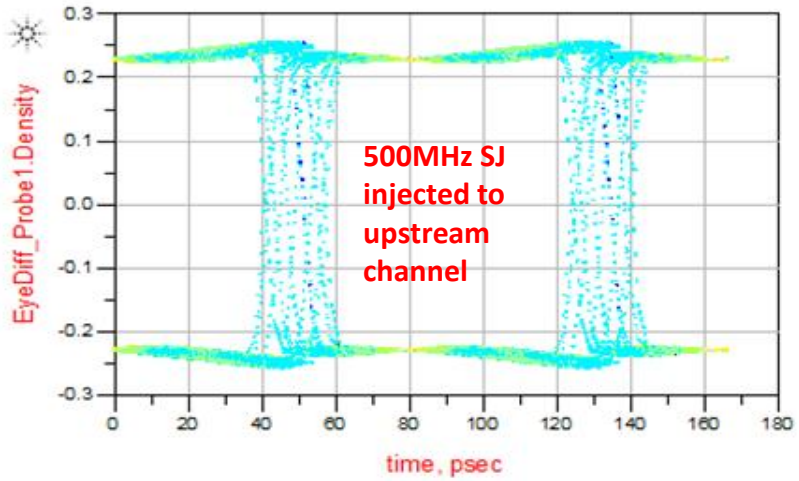


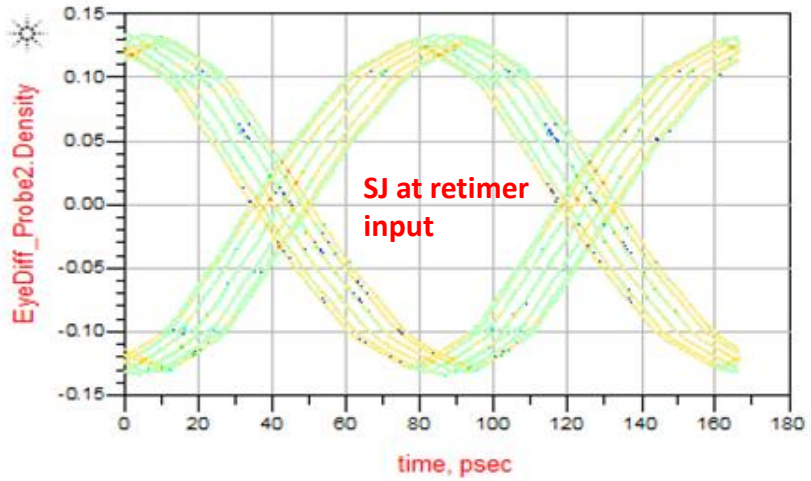
Retimer Rx CDR tracks SJ in clock times

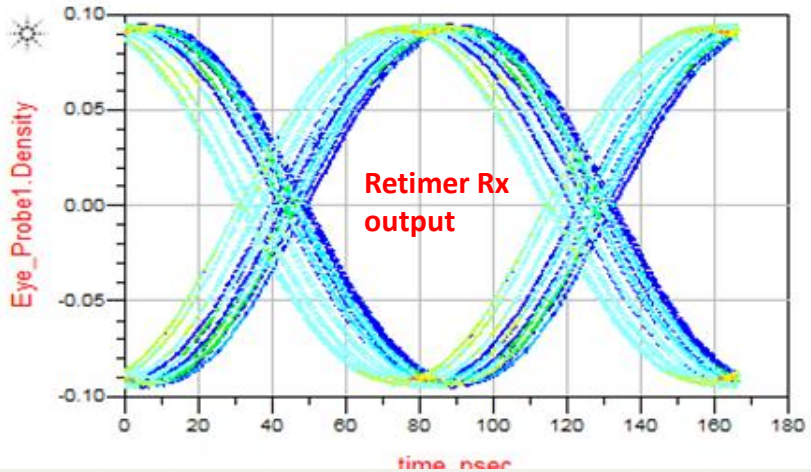


Tracked SJ is passed to downstream channel

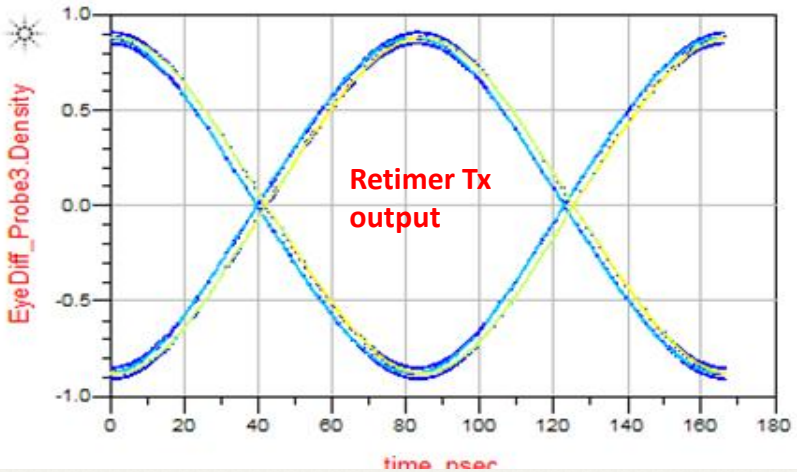
Retimer Filters High-frequency Jitter





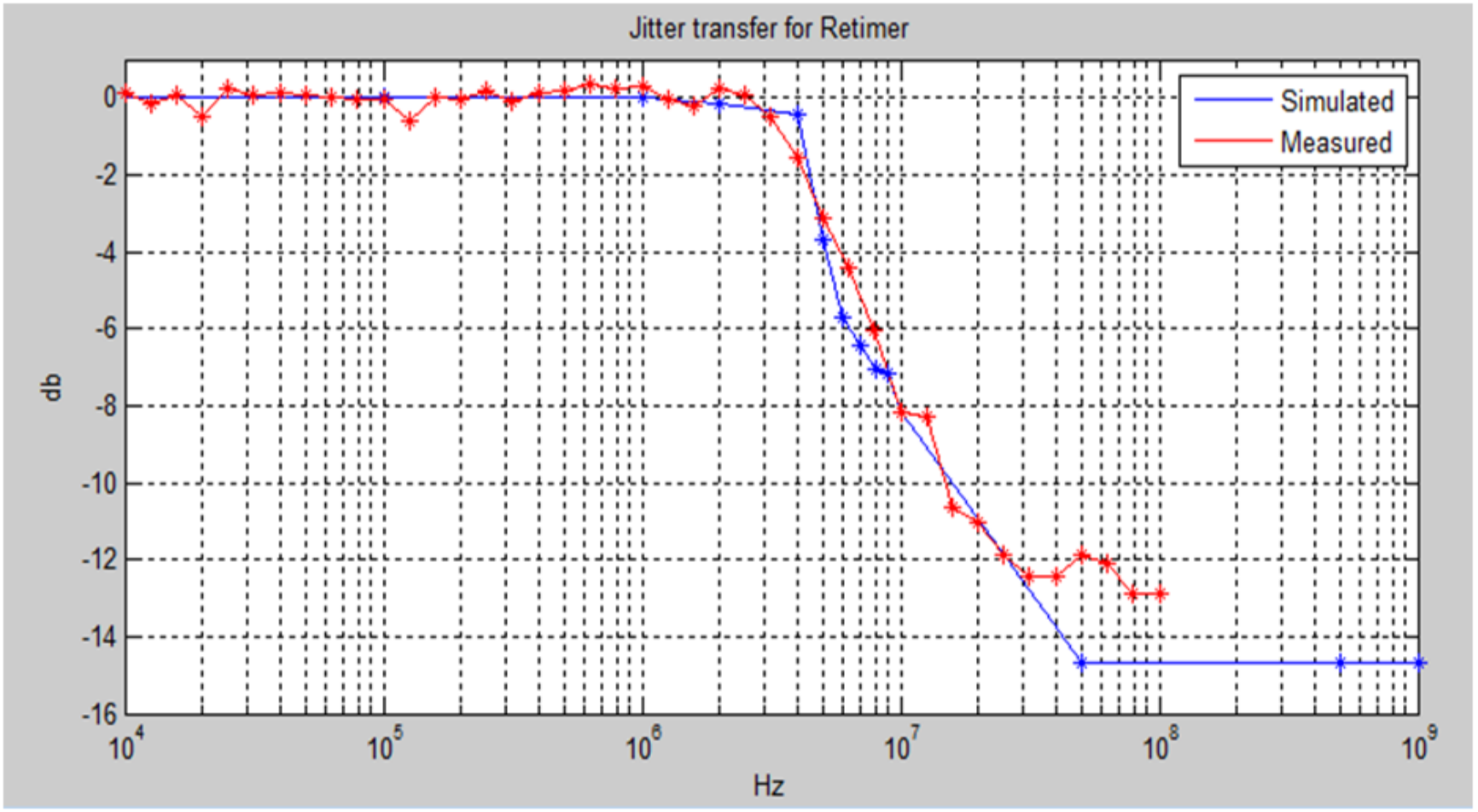


Retimer Rx CDR fails to track SJ



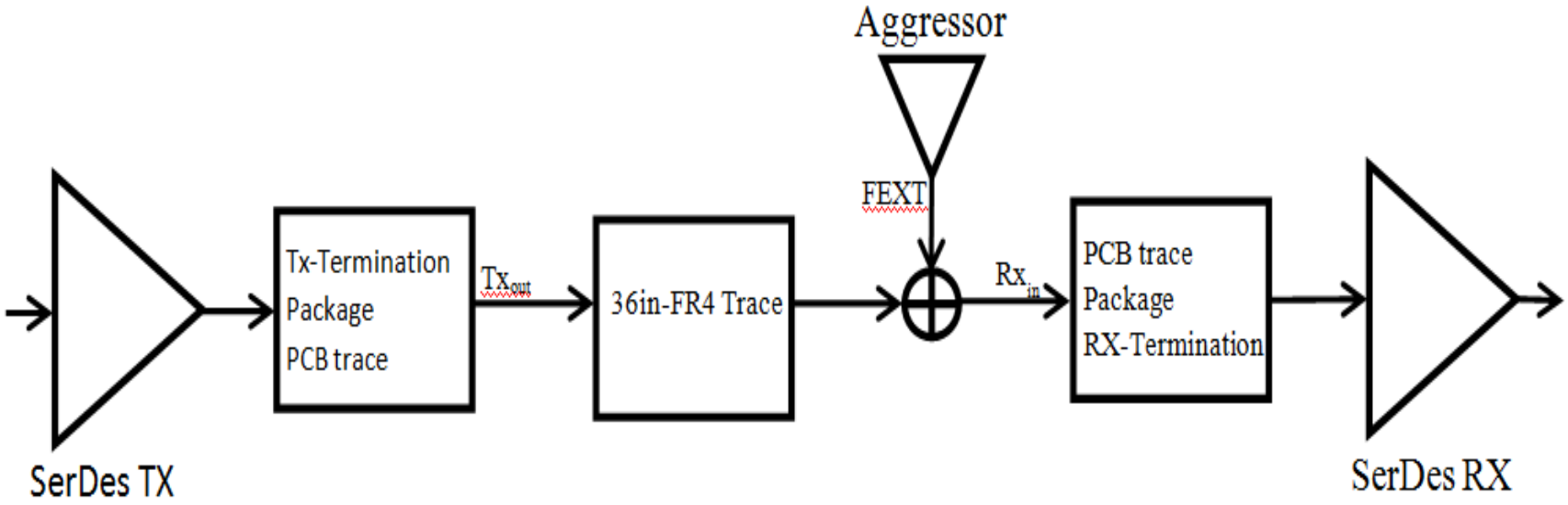
SJ is rejected

Simulated and Silicon Measured Jitter Transfer Curve

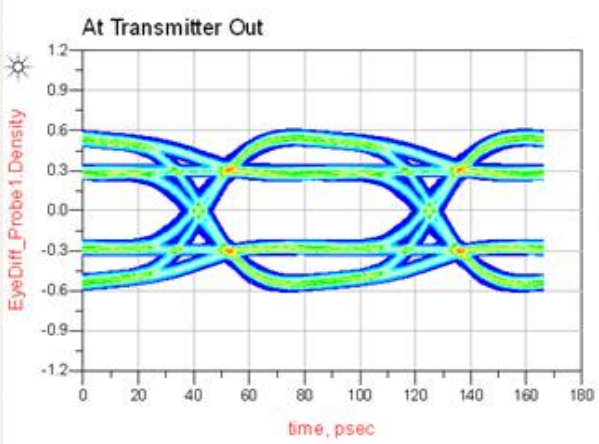


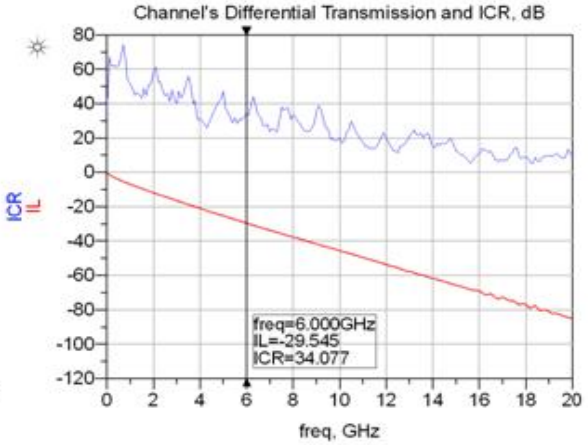
Active Link Analysis Using AMI Model

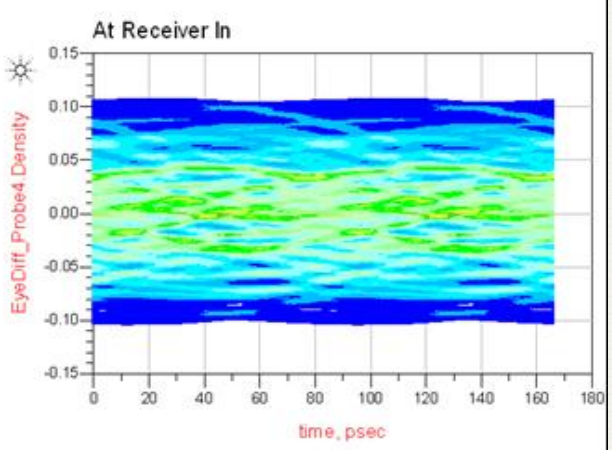
- We first analyze a channel w/o retimer at 12Gbps data rate
- IL=30dB
- ICR=34dB
- BER target is 1e-12

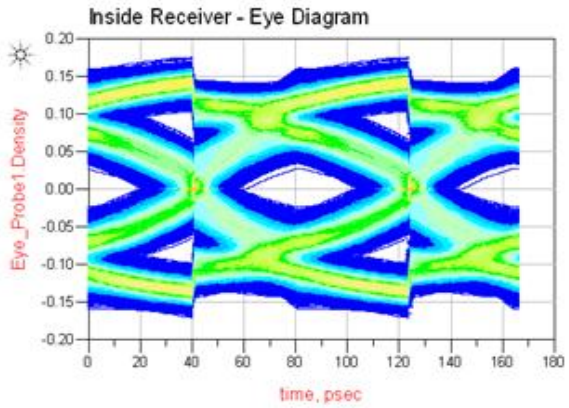


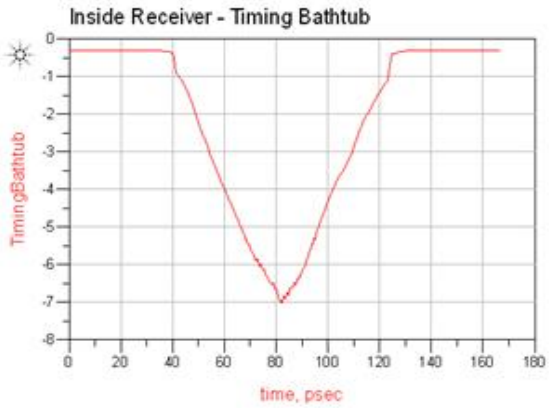
Link Performance w/o Retimer

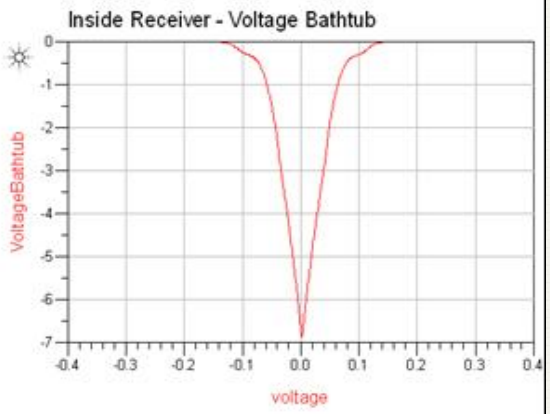






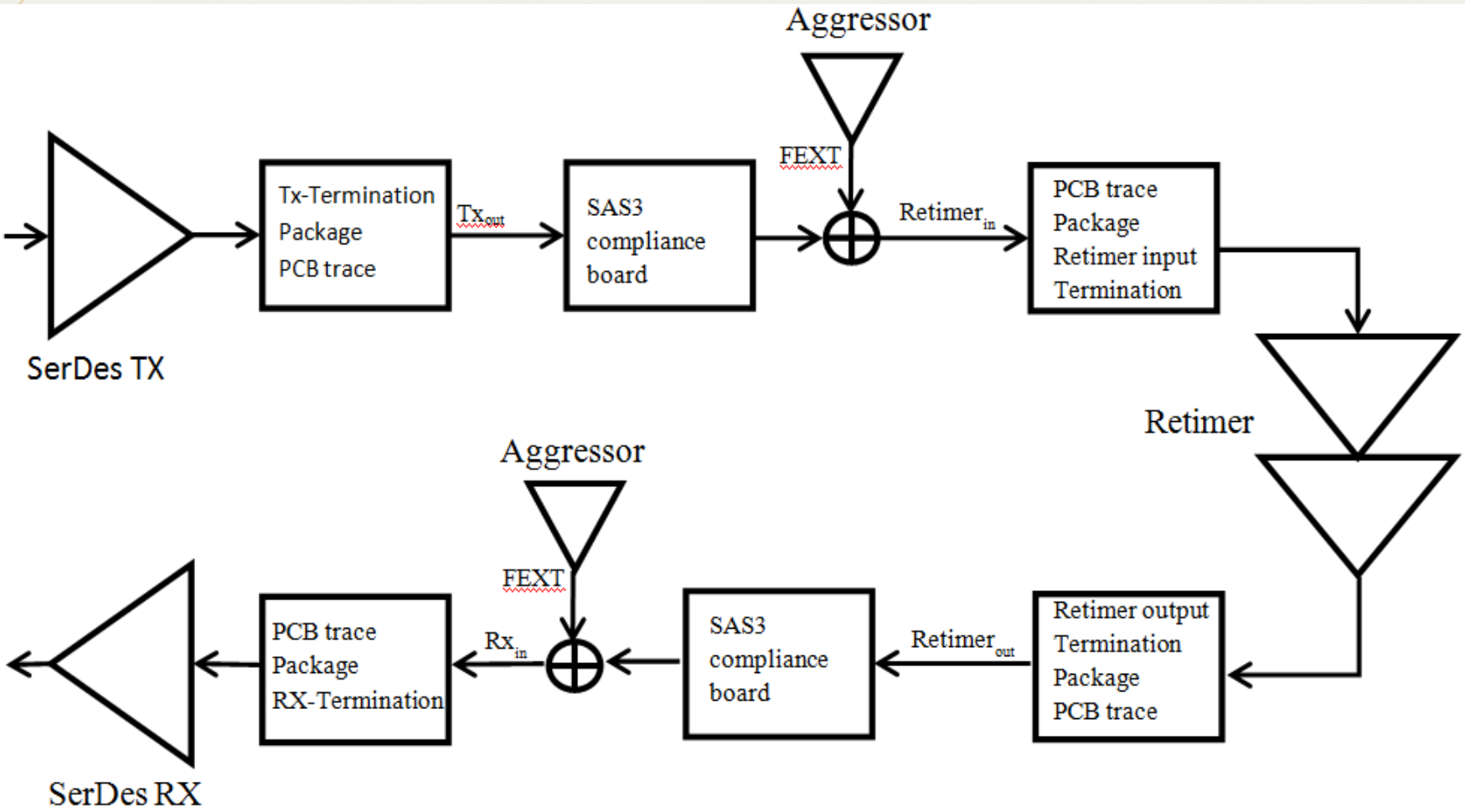




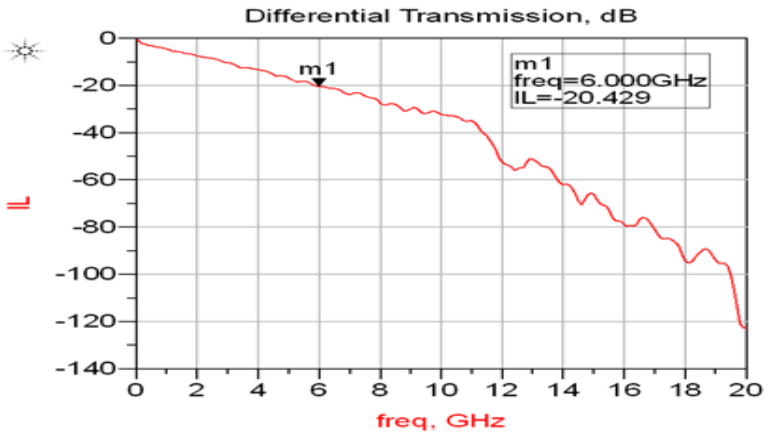


Eye is close at 1e-12 BER

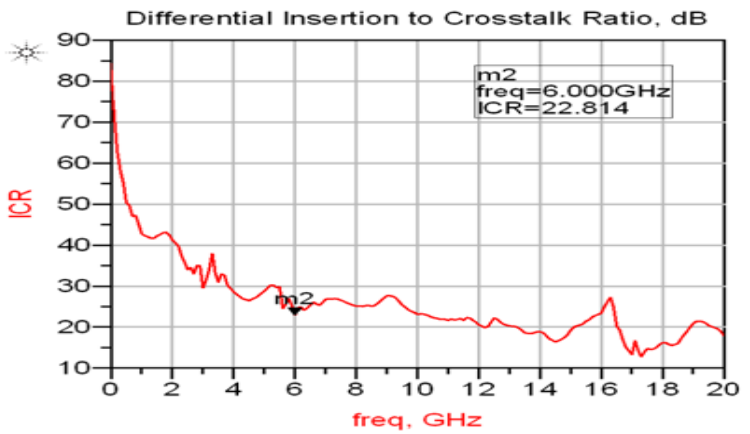
Using Retimer to Improve System Performance



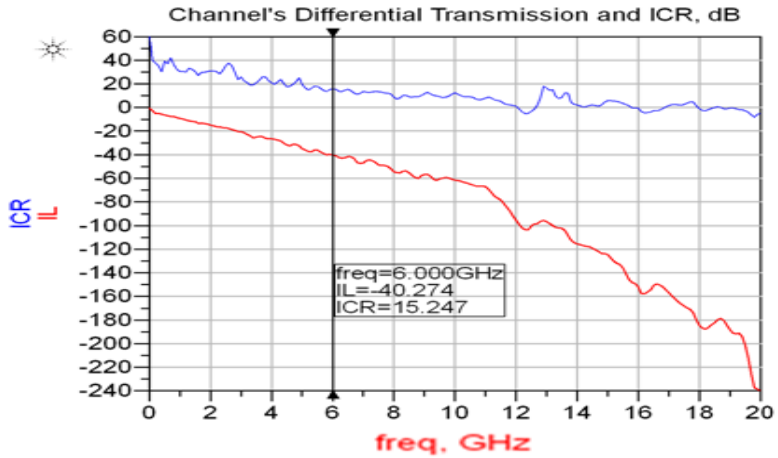
Insertion Loss and ICR of the System



(a) Single compliance board insertion loss



(b) Single compliance board ICR



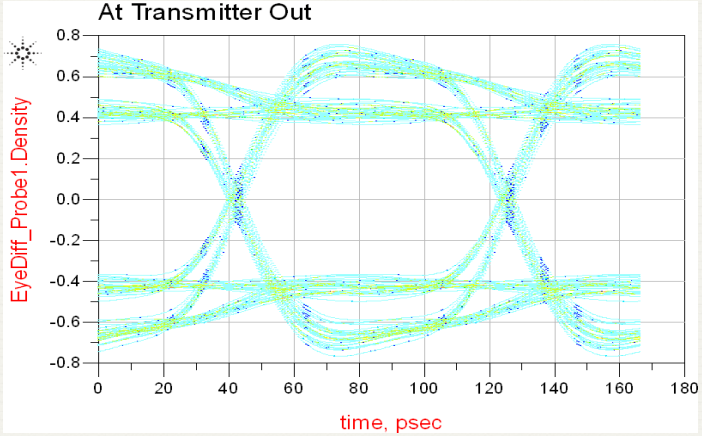
(c) Insertion loss and ICR of two cascaded compliance boards

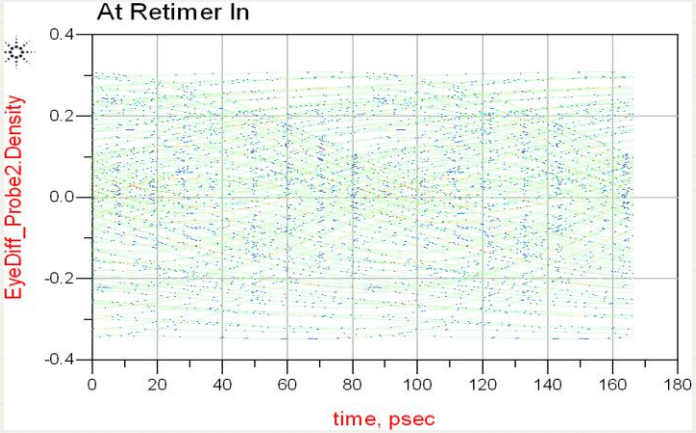
In cascaded boards

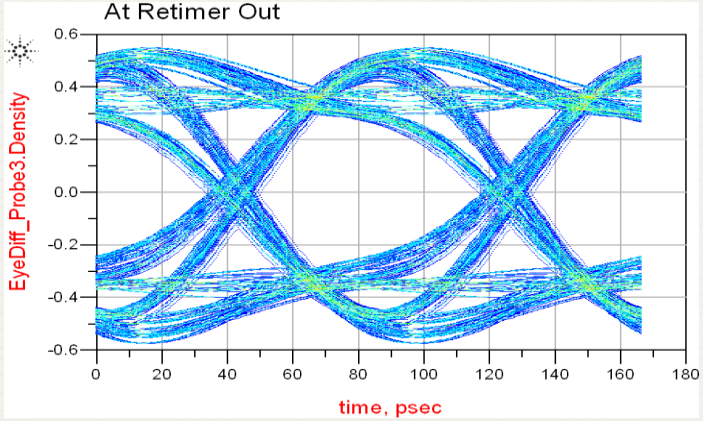
Combined IL=40dB

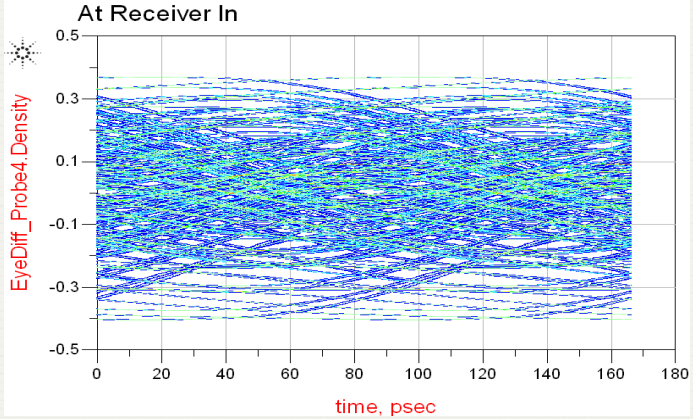
Combined ICR=15dB

Link Performance with Retimer

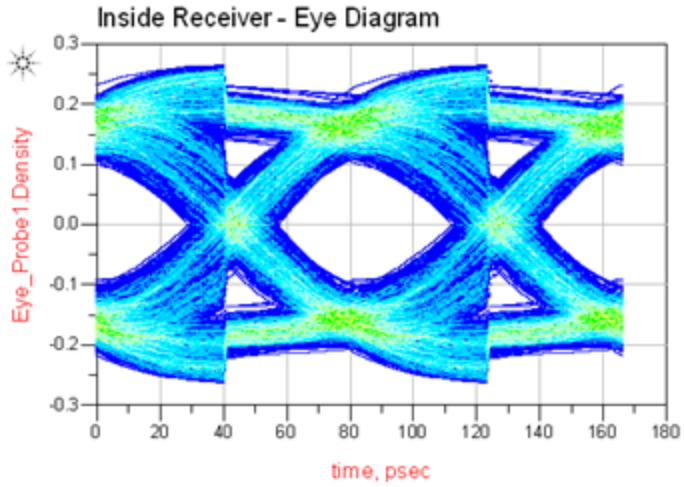


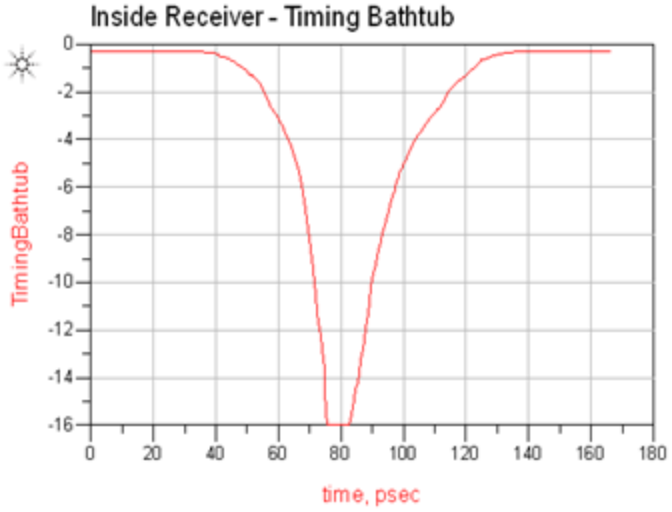


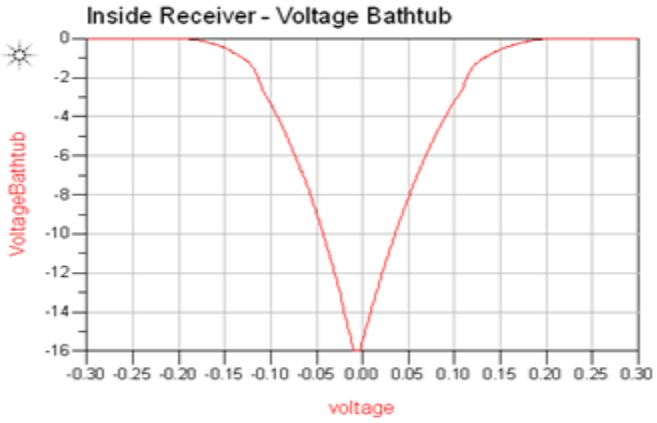




Link Performance with Retimer (cont'd)

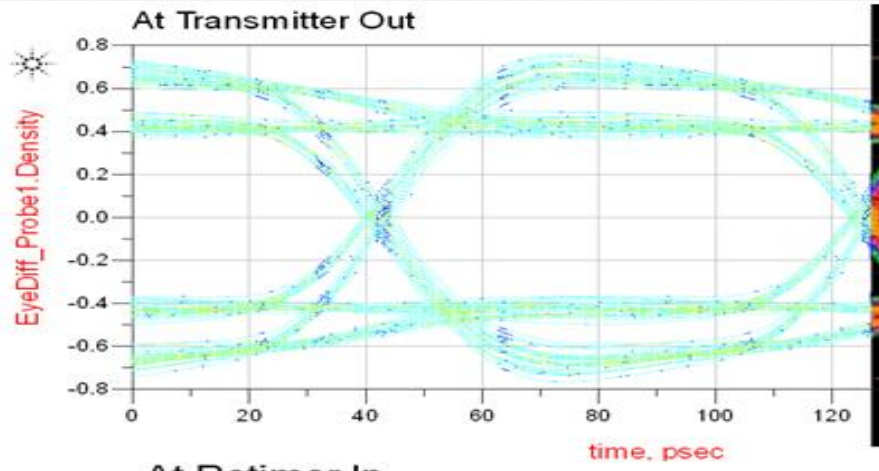


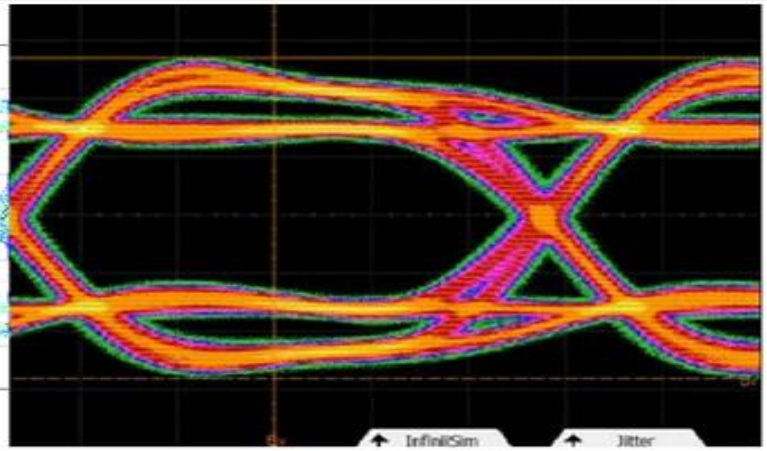


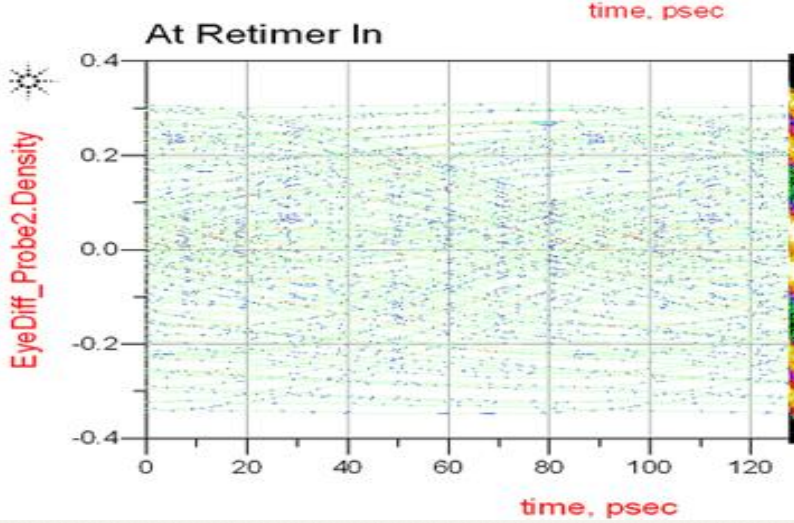


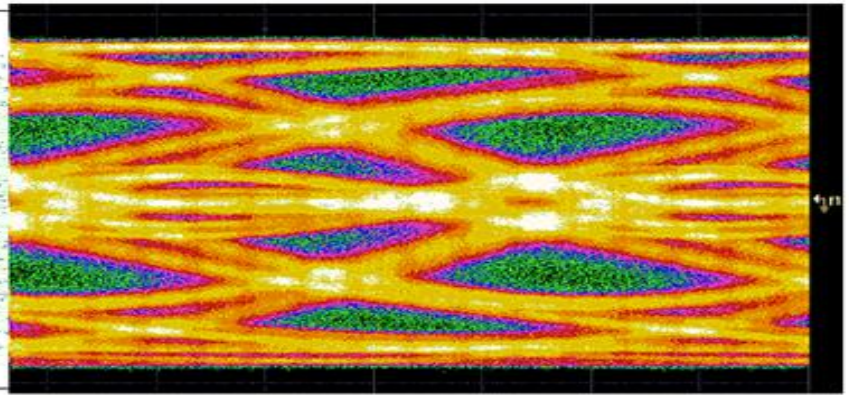
- Eye is open at 1e-12 BER
- Retimer increases system tolerances to IL and ICR by 10dB and 19dB, respectively

Simulation and Silicon Measurement Correlations

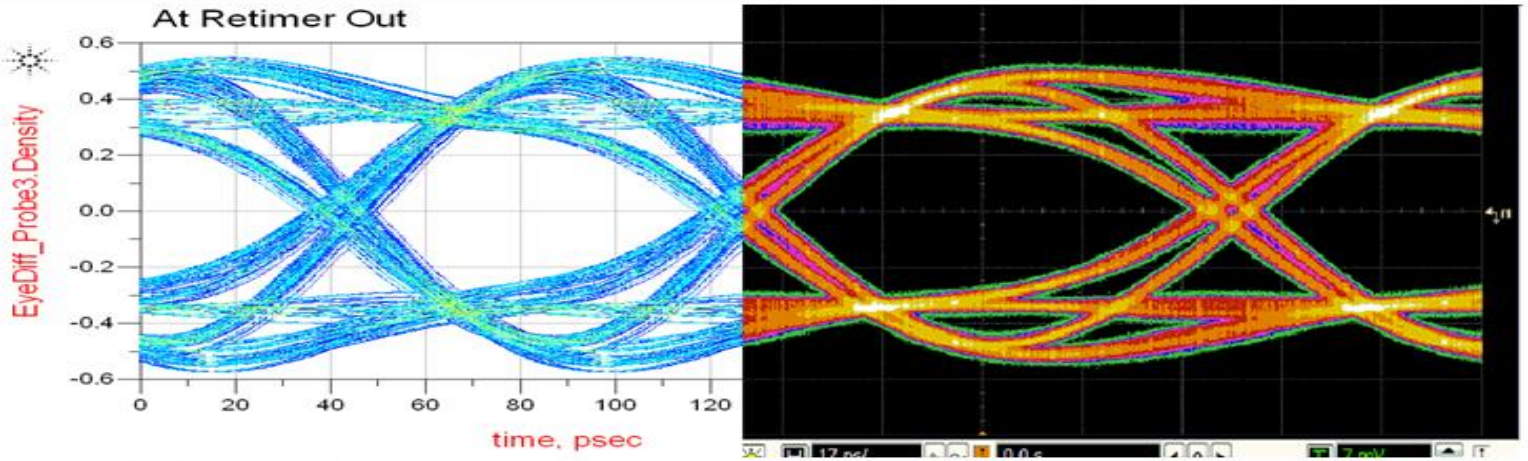


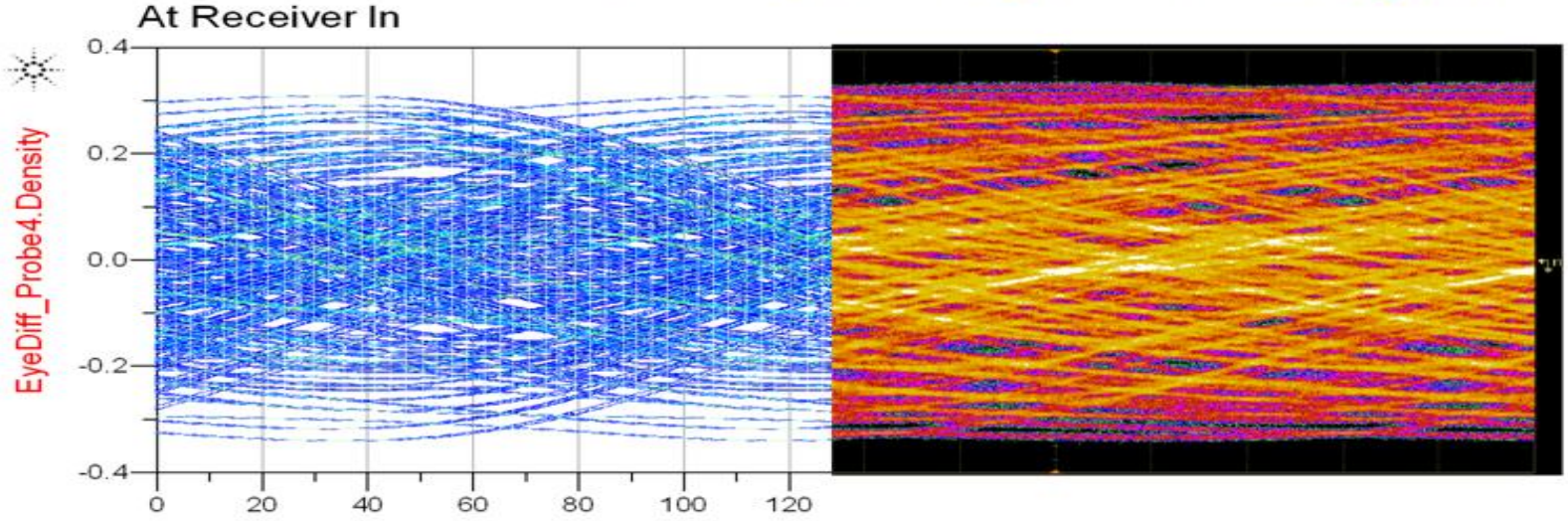






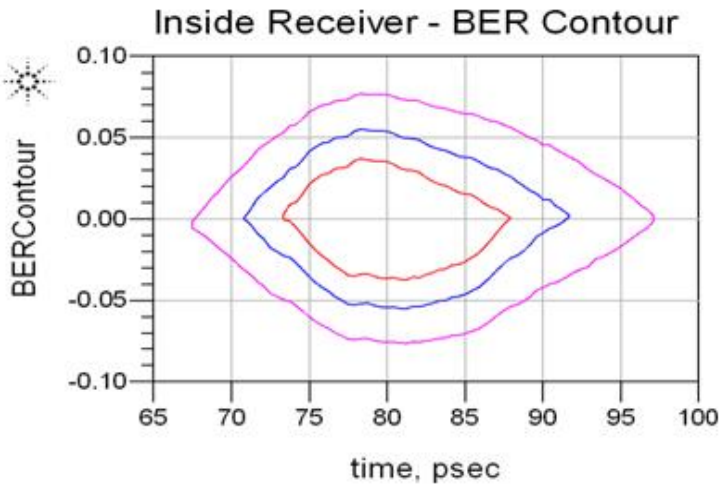
Simulation and Silicon Measurement Correlations (cont'd)





Simulation and Silicon Measurement Correlations (cont'd)

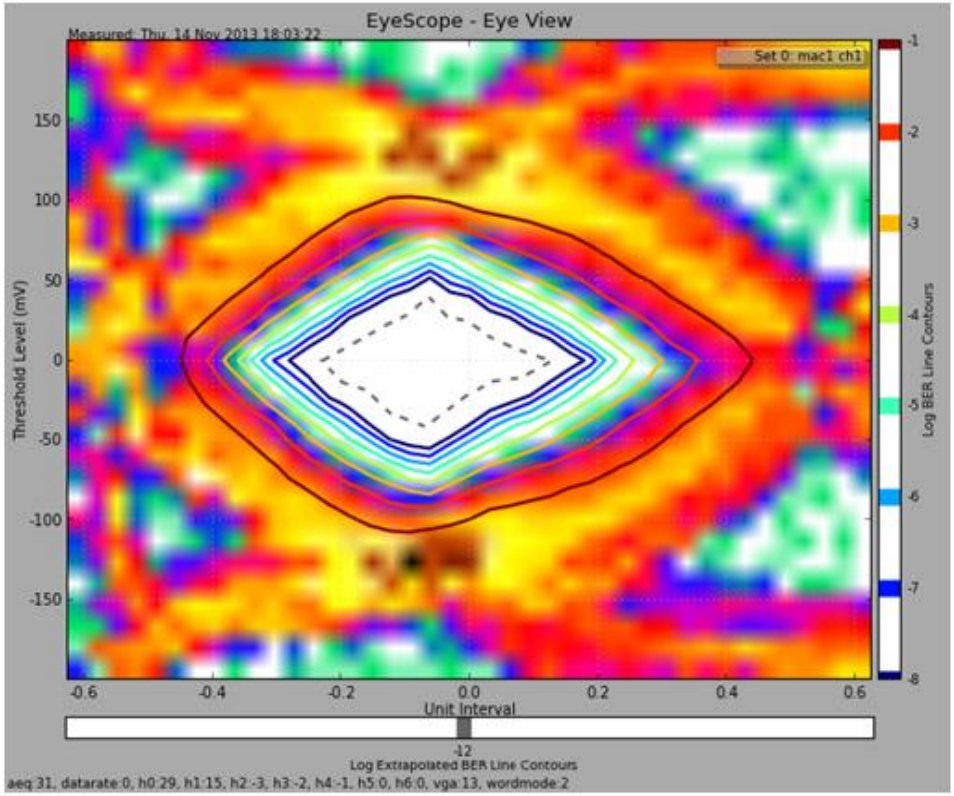
Simulated eye



At BER 1E-12 ; height in mV, width in ps

measurement	Eye_Probe1.Summary
WidthAtBER	1.500E-11
HeightAtBER	0.072

Eye captured by EyeScope inside SerDes



At 1e-12 BER, measured eye height=70mV and width=25ps

Conclusion

- We presented a novel IBIS-AMI modeling approach for developing and simulating Retimer models
- Retimer is shown to be a promising candidate to extend the reach of high-speed serial links
- Retimer AMI model can be used to predict jitter and link performance to ensure first pass manufacture success