

Signal Loop Inductance in [Pin] and [Package Model]

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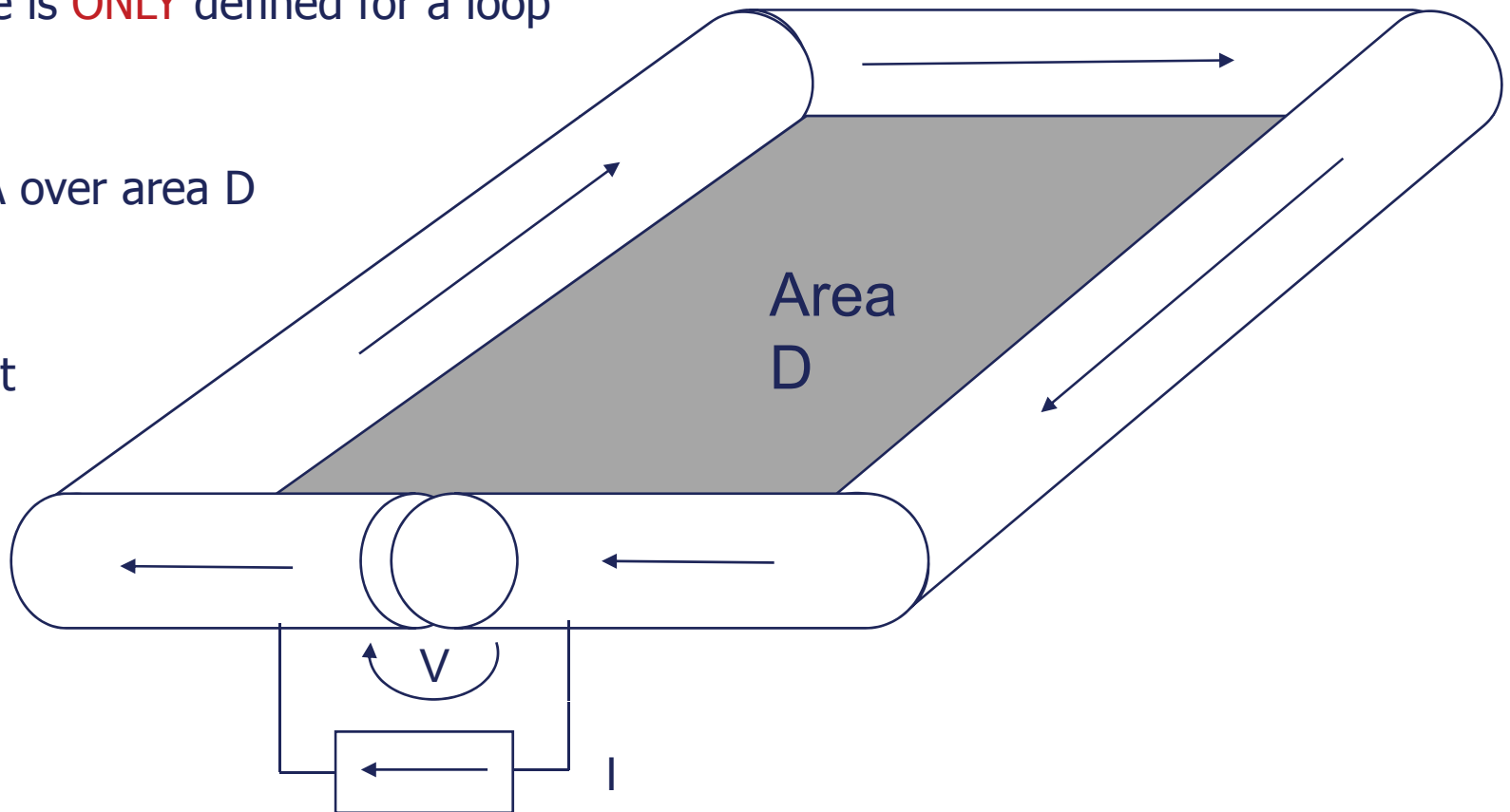
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Overview

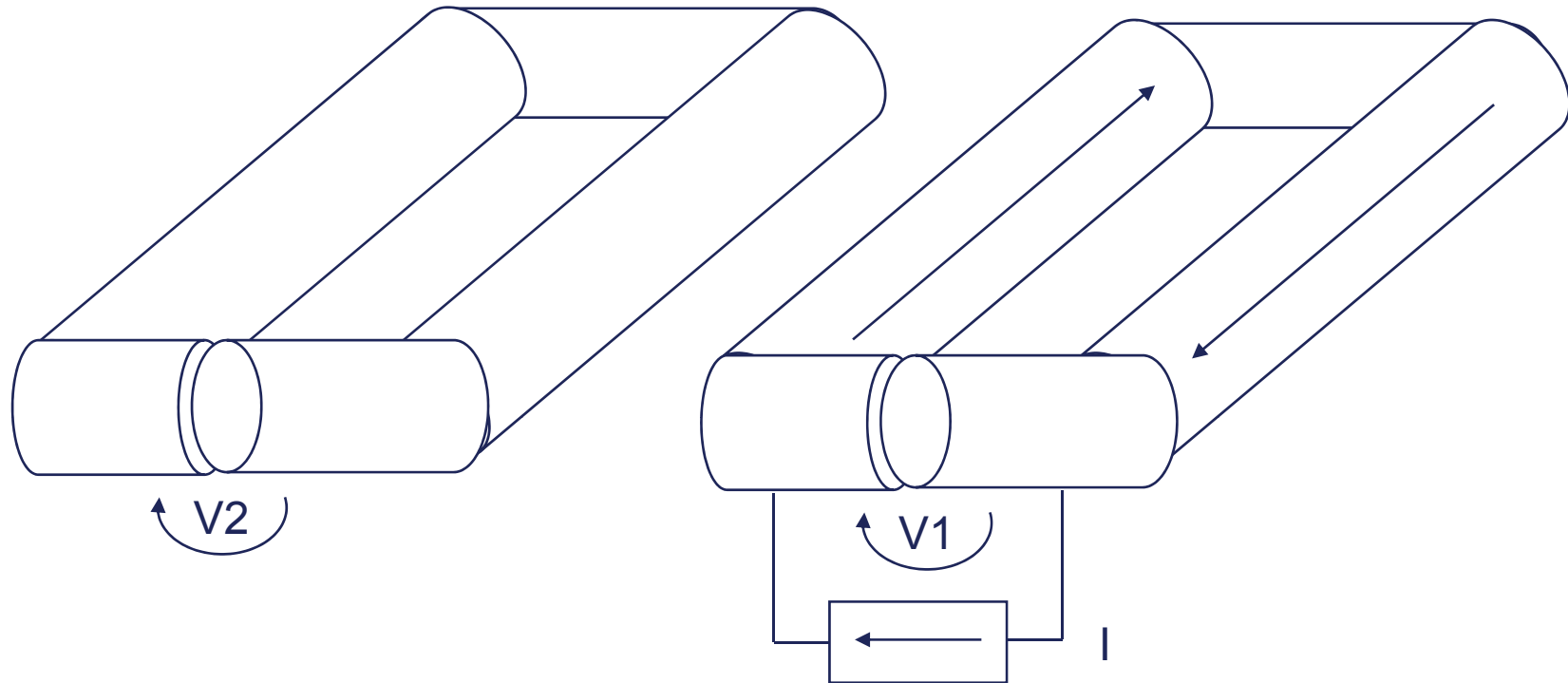
- Inductance terminology
- 3D Field Solver outputs
- Inductance model simulation examples
- Micron's loop inductance analyzer
- Application to IBIS [Pin] and [Package Model]

Definition of Inductance

- Inductance L is magnetic flux through a loop area divided by the current
- Inductance is **ONLY** defined for a loop
- $\Phi = \int \mathbf{B} \cdot d\mathbf{A}$ over area D
- $L = \Phi / I$
- $V = L \, dI/dt$



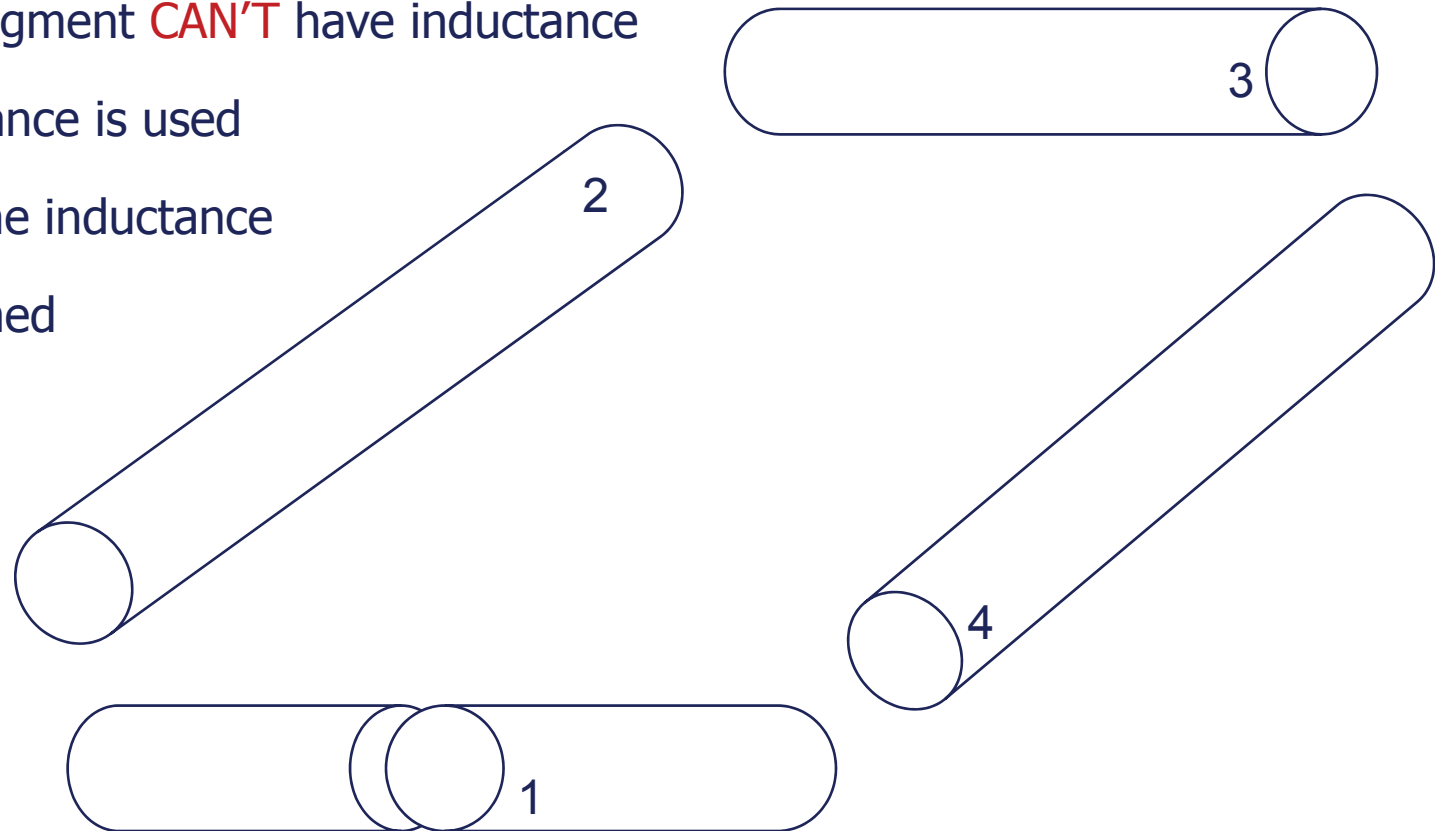
Self and Mutual Inductance



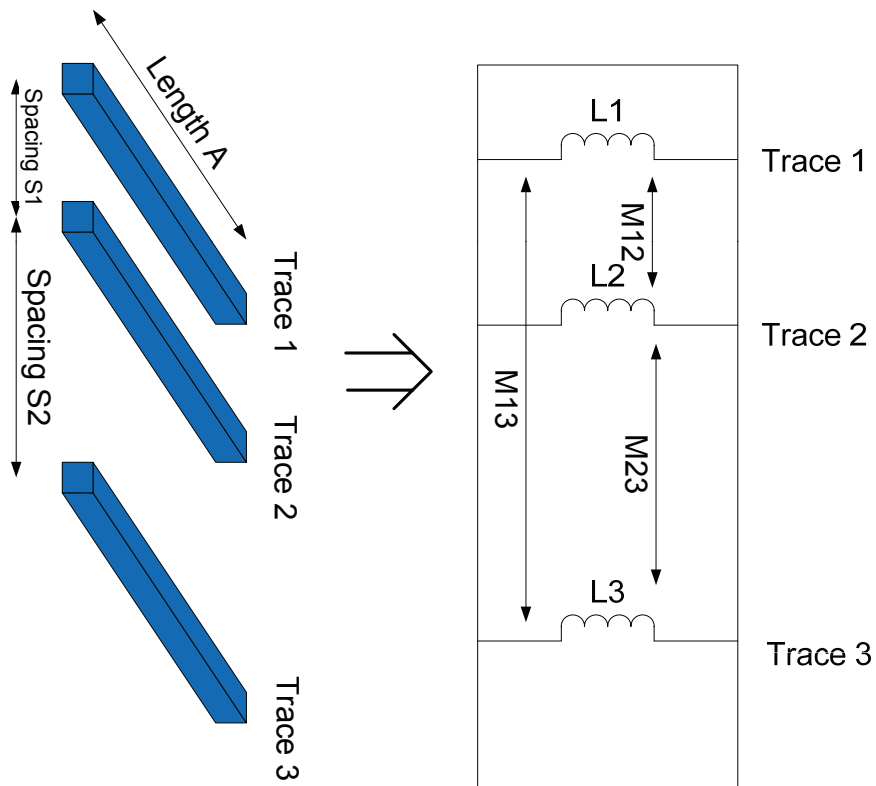
- Self loop inductance generates a voltage V_1 in the driven loop
- Mutual loop inductance generates a voltage V_2 in the adjacent loop
 - Note – current in adjacent loop is 0

Partial Inductance

- Partial Inductances are the Self and Mutual Inductances of the loop segments
- Mathematical construct - They have **NO MEANING** independent of other partial inductances that form a loop
- An isolated segment **CAN'T** have inductance
- Partial inductance is used to calculate the inductance of a loop formed of segments



3D Field Solver Partial Inductances



- 3 Traces in Free Space (no reference plane in structure)
 - Typical for 2 layer packages
- L1, L2, L3 – **Partial** Self Inductances are determined mostly by length, smaller effects from width and height
- M12, M23, M13 – **Partial** Mutual Inductances mainly a function of spacing and length

3D Field Solver Inductance Matrix

	Trace 1	Trace 2	Trace 3
Trace 1	5.16	3.78	0.458
Trace 2	3.78	5.16	0.464
Trace 3	0.458	0.464	5.16

Partial Mutual Inductance

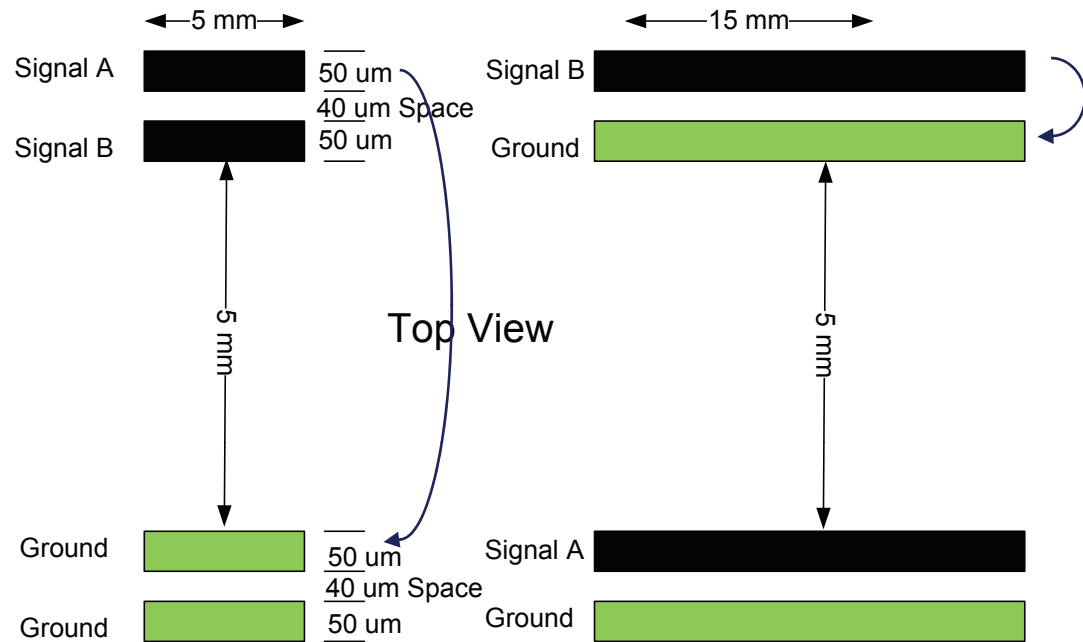
Partial Self Inductance

- ONLY LOOP INDUCTANCE HAS MEANING
- To define loops, the current paths must be defined
- Example: Trace2 is a return path
 - Trace1 to Trace2 loop = $5.16 + 5.16 - 2 * 3.78 = 2.76$
 - Trace3 to Trace2 loop = $5.16 + 5.16 - 2 * 0.464 = 9.39$

Example – 5 mm vs. 15 mm Long Traces

Partial Self Inductance
 -> Case 1 (5mm)
 is much better

Loop Inductance
 -> Case 2 (15mm)
 is somewhat better



	Case 1 - 5 mm long	Case 2 – 15 mm long
Partial Self Inductance	5.16 nH	19.2 nH
Signal A to Gnd Loop Inductance	8.72 nH	7.99 nH

3D Field Solver Inductance Matrix

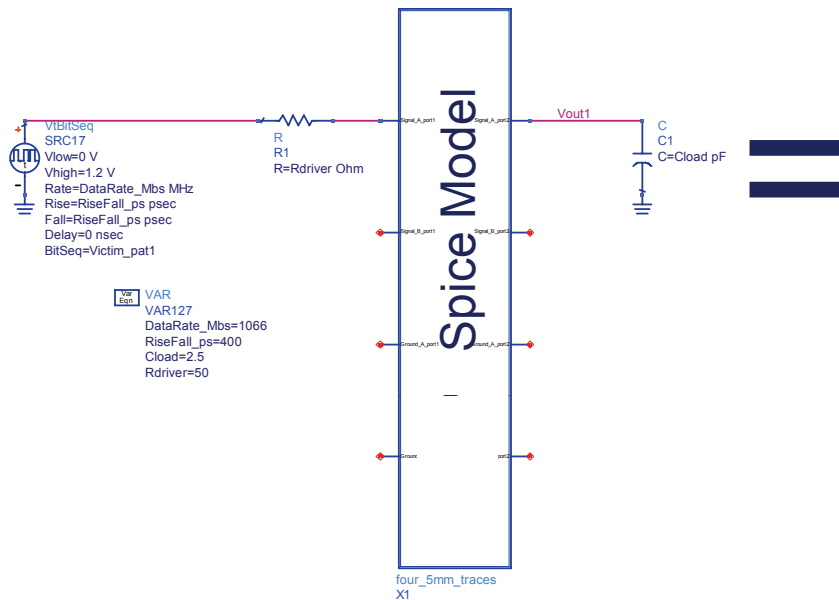
	Signal A	Signal B	Ground	Ground
Signal A	5.16E-09	3.78E-09	4.58E-10	4.52E-10
Signal B	3.78E-09	5.16E-09	4.64E-10	4.58E-10
Ground	4.58E-10	4.64E-10	5.16E-09	3.78E-09
Ground	4.52E-10	4.58E-10	3.78E-09	5.16E-09

Case 1
5 mm Traces

	Signal A	Ground	Signal B	Ground
Signal A	1.92E-08	1.49E-08	3.34E-09	3.30E-09
Ground	1.49E-08	1.92E-08	3.37E-09	3.34E-09
Signal B	3.34E-09	3.37E-09	1.94E-08	1.51E-08
Ground	3.30E-09	3.34E-09	1.51E-08	1.93E-08

Case 2
15 mm Traces

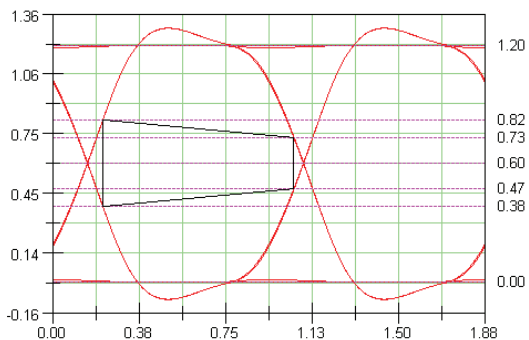
Sims with Global Ground Return Path



This sim creates a non-real loop with the trace as the only Segment. Inductance of **non-real loop** is trace partial inductance

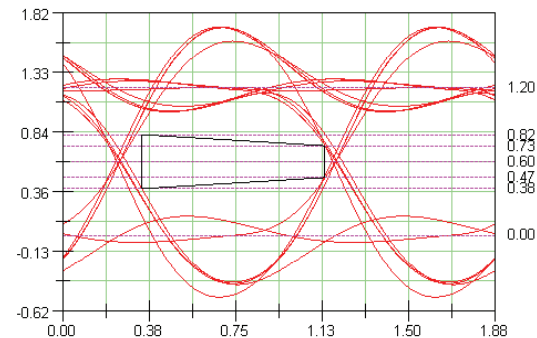
Case 1 5 mm trace (Partial self L=5.16 nH)

AptACDC = 0.828ns Jitter = 2ps MinSlewRise = 3.15V/ns
MaxSlewRise = 3.20V/ns MinSlewFall = 3.15V/ns MaxSlewFall = 3.20V/ns



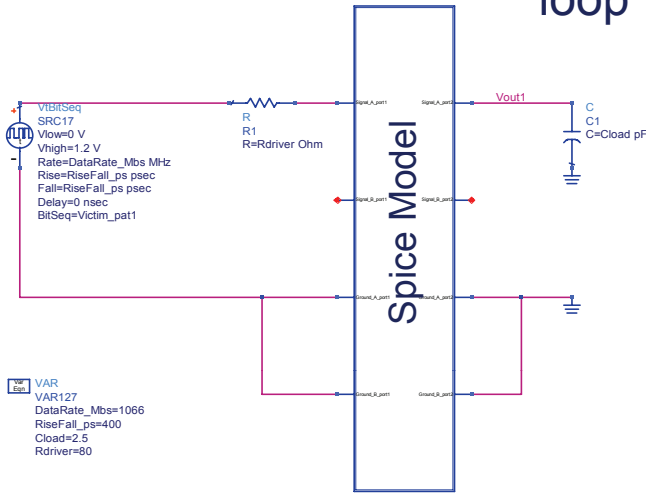
Case 2 15 mm trace (Partial self L=19.2 nH)

AptACDC = 0.791ns Jitter = 47ps MinSlewRise = 2.92V/ns
MaxSlewRise = 3.99V/ns MinSlewFall = 2.89V/ns MaxSlewFall = 4.05V/ns

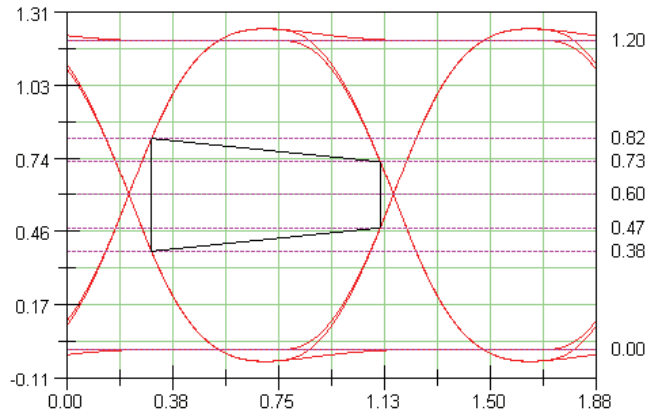


Sims with Return Paths

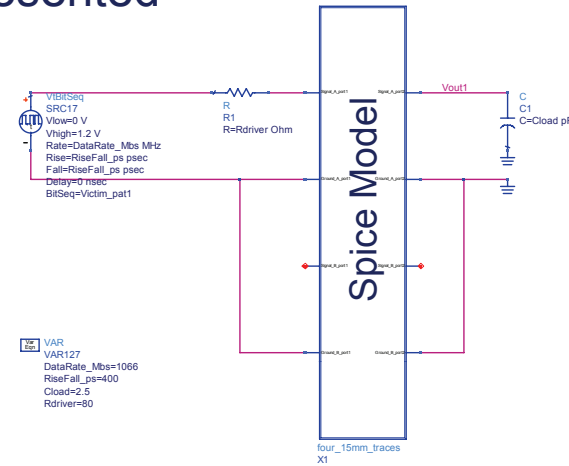
Spice model includes all partial and mutual inductances so correct loop values are represented



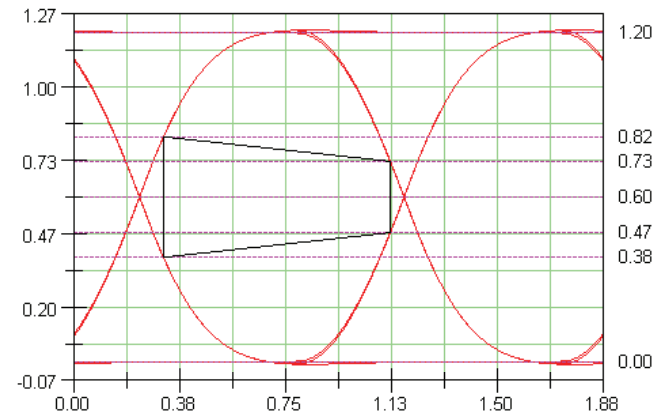
AptACDC = 0.81ns Jitter = 0ps MinSlewRise = 2.70V/ns
MaxSlewRise = 2.74V/ns MinSlewFall = 2.70V/ns MaxSlewFall = 2.74V/ns



Case 1 – 5 mm Trace



AptACDC = 0.803ns Jitter = 1ps MinSlewRise = 2.57V/ns
MaxSlewRise = 2.59V/ns MinSlewFall = 2.57V/ns MaxSlewFall = 2.59V/ns

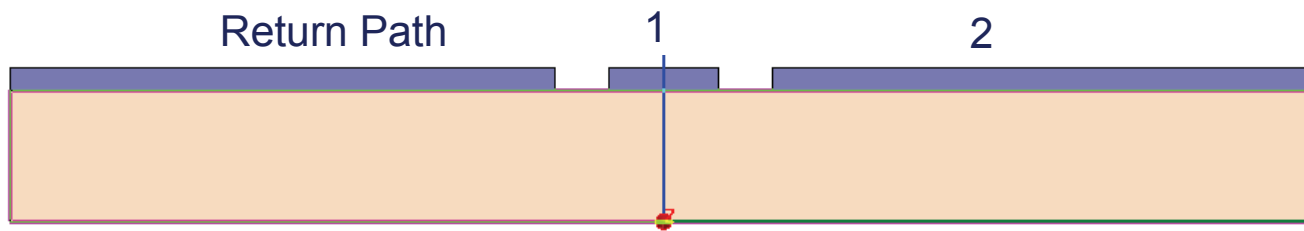


Case 2 – 15 mm Trace

Why Partial Inductances are Misleading

- **Actual test case** comparing various extraction tools
- Question? Which tool gives the correct partial inductances? Is conductor 1's self partial inductance 4.5 or 10.1?
- Answer? **They are all correct!** Partial inductance is only meaningful with respect to other partial and mutual inductances within a loop. Partial inductances can't be compared between tools or even different simulations on the same tool. **Only loop inductances can be compared.** In this case they are all within about 15%.

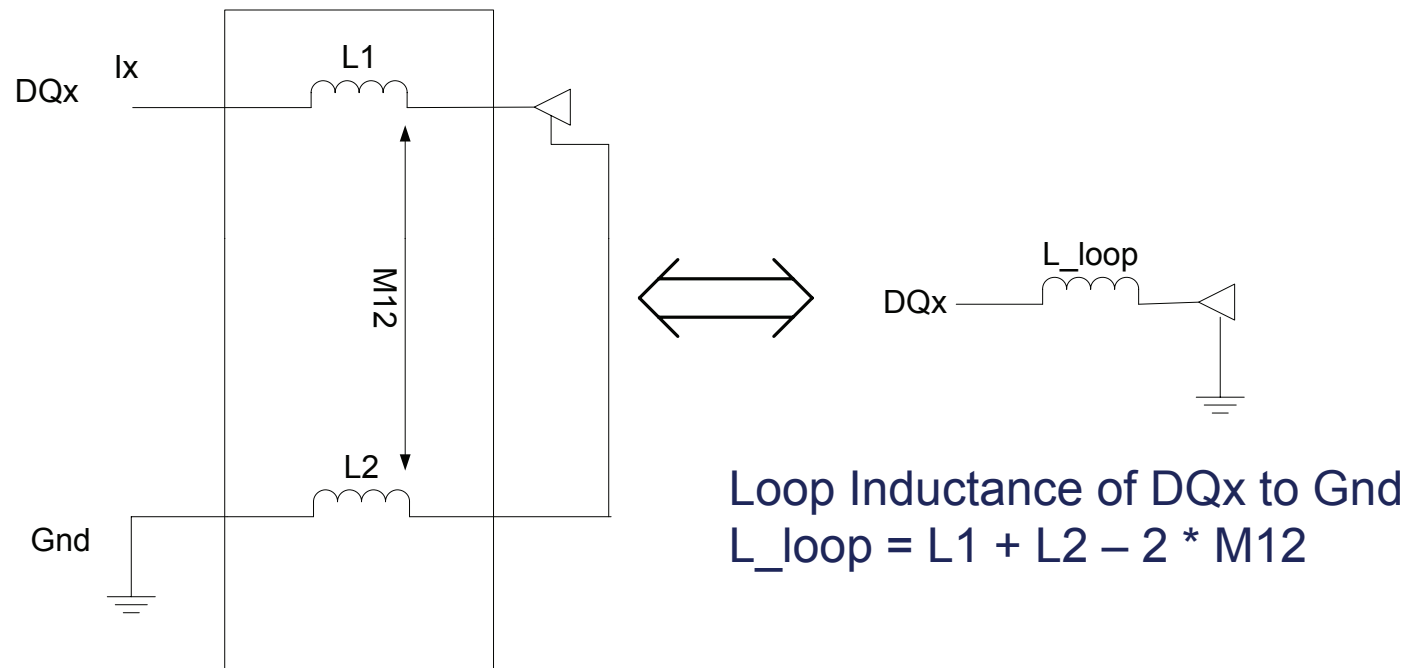
	A	B	C	D
Self Partial 1	5.280	4.533	10.072	10.100
Self Partial 2	5.856	5.375	9.022	9.261
Mutual 1-2	2.929	2.681	7.244	6.900
Loop 1-2	5.278	4.546	4.606	5.561



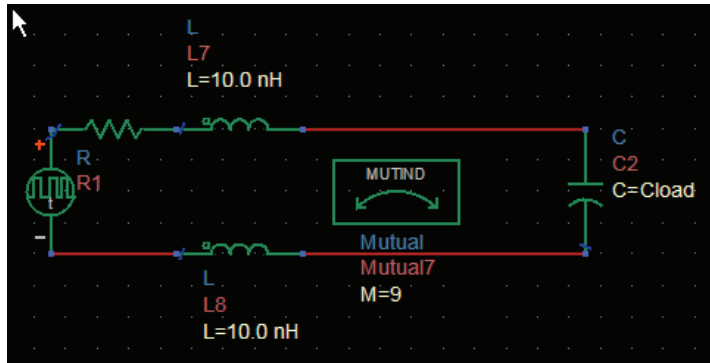
width of center trace	50 μm
width of reference	250 μm
width of gap	25 μm
thickness of trace/ref.	10 μm
height of substrate	60 μm
dielectric constant	4.5
length of trace	10 mm

Signal Loop Inductance Model

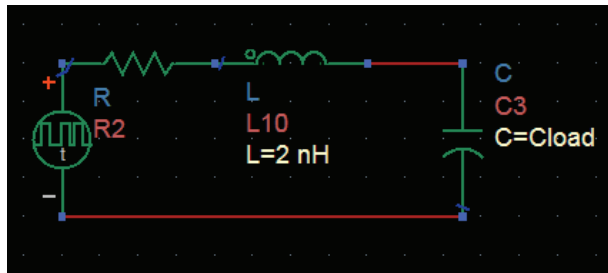
These 2 circuits are equivalent



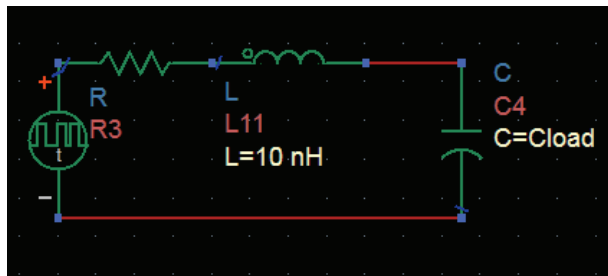
Simulation with 2 Inductors



$$L\text{-loop} = 10 + 10 - 2 \cdot 9 = 2 \text{ nH}$$



$$\text{Single } L=L_{\text{loop}} = 2\text{nH}$$

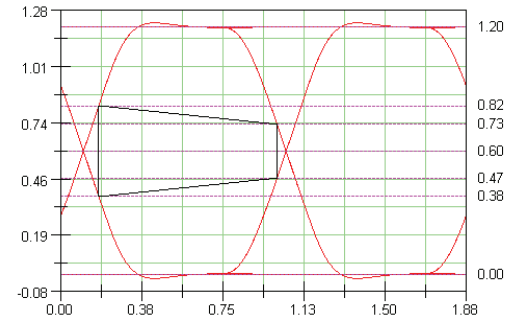


$$\text{Single } L=L_{\text{Partial}} = 10\text{nH}$$

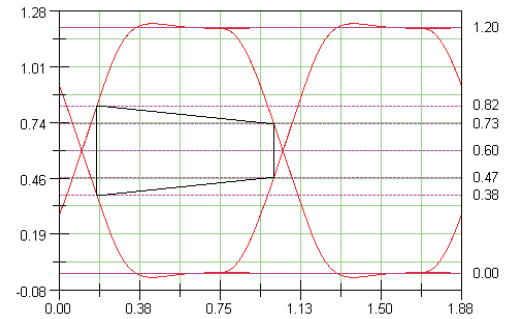
Equivalent Circuits

Incorrect result using only partial inductance and ignoring mutual terms

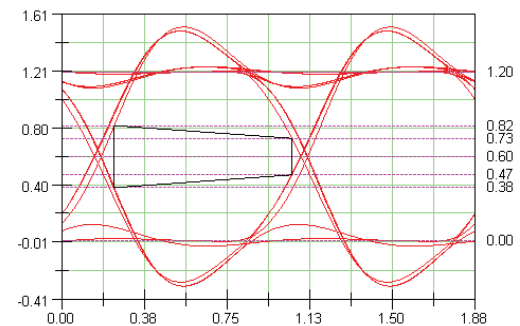
AptACDC = 0.826ns Jitter = 0ps MinSlewRise = 3.10V/ns
 MaxSlewRise = 3.10V/ns MinSlewFall = 3.10V/ns MaxSlewFall = 3.10V/ns



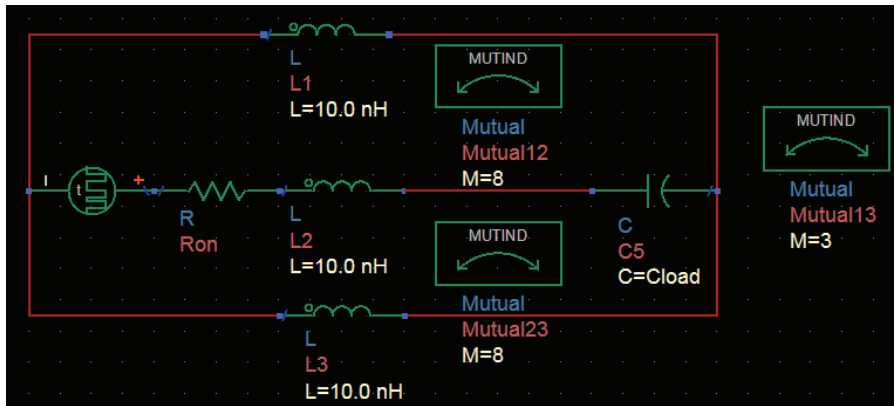
AptACDC = 0.826ns Jitter = 0ps MinSlewRise = 3.10V/ns
 MaxSlewRise = 3.10V/ns MinSlewFall = 3.10V/ns MaxSlewFall = 3.10V/ns



AptACDC = 0.804ns Jitter = 33ps MinSlewRise = 3.18V/ns
 MaxSlewRise = 3.48V/ns MinSlewFall = 3.16V/ns MaxSlewFall = 3.48V/ns

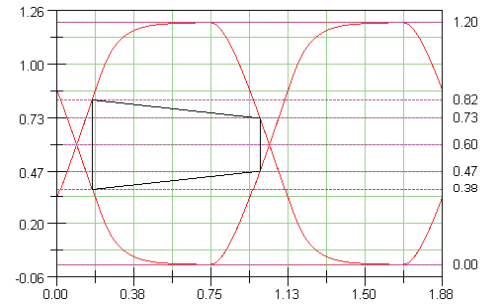


Simulation with 3 Inductors

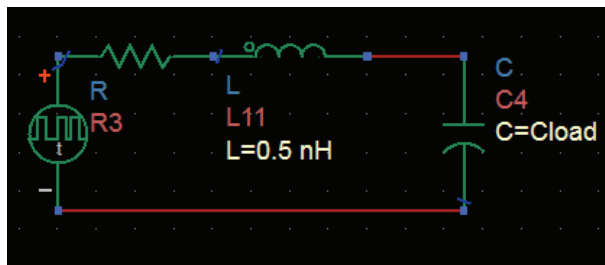


Note: With more than two inductors loop calculation becomes more complex

AptACDC = 0.817ns Jitter = 0ps MinSlewRise = 2.87V/ns
MaxSlewRise = 2.87V/ns MinSlewFall = 2.87V/ns MaxSlewFall = 2.87V/ns



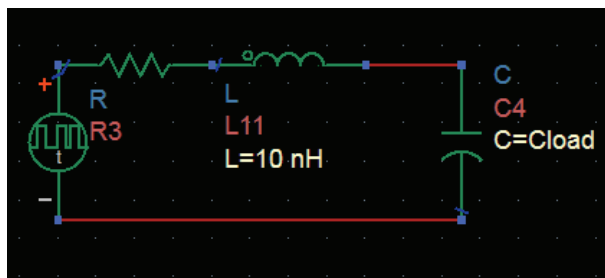
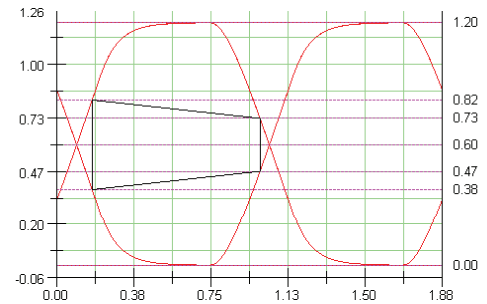
Equivalent loop $L = 0.5 \text{ nH}$



Single $L=L_{\text{loop}} = 0.5\text{nH}$

Equivalent Circuits

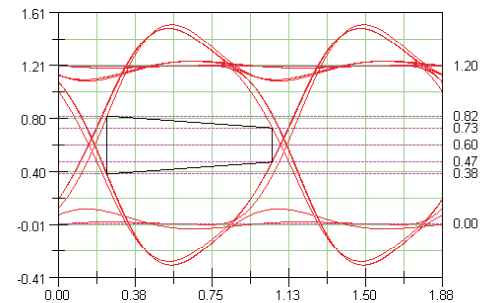
AptACDC = 0.817ns Jitter = 0ps MinSlewRise = 2.87V/ns
MaxSlewRise = 2.87V/ns MinSlewFall = 2.87V/ns MaxSlewFall = 2.87V/ns



Single $L=L_{\text{Partial}} = 10\text{nH}$

Incorrect result using only partial inductance and ignoring mutual terms

AptACDC = 0.804ns Jitter = 33ps MinSlewRise = 3.16V/ns
MaxSlewRise = 3.48V/ns MinSlewFall = 3.16V/ns MaxSlewFall = 3.48V/ns



Application to IBIS [Pin] and [Package Model]

[Pin]	signal_name	model_name	R_pin	L_pin	C_pin
A1	VSS	GND			
A2	DQ15	DQ_18	596.6m	4.09nH	1.61pF
A3	VSSQ	GND			
A7	VDDQ	POWER			
A8	DQ0	DQ_18	751.6m	5.59nH	1.80pF
A9	VDD	POWER			

- Where does the L_pin in the [Pin] list come from?
 - Is it the partial self inductance from a 3D field solver inductance matrix? **VERY LIKELY!**
 - L_loop is what you really want

How do you get L_loop from the inductance matrix?

Micron's Loop Inductance Analyzer Tool

- Excel spreadsheet macro
- Reads in matrix data from several Field Solver tools
- Solves for loop inductance to power, ground, or both
- Correlates well to simulation, best with loop inductance to both power and ground


Signal	Simulator Optimized L Value (nH)	Matrix Analyzer Value (nH)	Delta (%)
DQ0	2.783	2.785	0.08%
DQ1	1.624	1.625	0.09%
DQ2	1.294	1.295	0.08%
DQ3	1.425	1.425	0.05%
DQ4	2.020	2.021	0.04%
DQ5	2.900	2.902	0.05%
DQ6	2.439	2.437	-0.09%
DQ7	2.899	2.904	0.17%

Micron's Loop Inductance Analyzer Tool

- Separate analyses are run for Address/Command and DQs due to separate power and ground return paths
 - VDD and VSS versus VDDQ and VSSQ

Line number	Line Name	Definition
1	U1:A0:112 aPadE<0>	Signal
2	U1:A1:111 aPadE<1>	Signal
3	U1:A2:110 aPadE<2>	Signal
4	U1:A3:109 aPadE<3>	Signal
37	U1:DQ15:21 DqPad<23>	Other
38	U1:LDM:64 DmPad<1>	Other
39	U1:LDQS:65 DqsPad<1>	Other
40	U1:RAS#:117 RasPadEF	Signal
41	U1:SV:138 SVPadsW	Other
42	U1:UDM:34 DmPad<2>	Other
43	U1:UDQS:33 DqsPad<2>	Other
44	U1:VDD:62 vccx	Power return
45	U1:VDDQ:72 vccq	Other
46	U1:VSS:2 gnd	Ground return
47	U1:VSSQ:8 vssq	Other
48	U1:WE#:119 WePadEF	Signal

Problems with [Package Model]

- Sparse_Matrix package models in combination with [Pin Mapping] have all the data necessary to correctly model loop inductance
- Many tools use the Partial Self Inductance term from the [Package Model] inductance matrix when modeling a single pin. This is **NOT** correct.
- So, which is a better single line model?:
 - [Pin] model with the correct loop inductance 
 - [Package Model] with partial self inductance

Conclusions

- Partial Inductance numbers directly from 3D Field Solvers provide minimal information and can be misleading
- For simulations assuming ideal power delivery the appropriate loop self and mutual inductances should be used. The partial self inductances off the diagonal of the inductance matrix should **NOT** be used.
- A sparse matrix [Package Model] can be less accurate than a [Pin] model if mutual inductances to power and ground are not part of the final EDA tool package model

