Measurement and Analysis of Statistical IC Operation Errors in a Memory Module Due to System-Level ESD Noise

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***Abstract*—Voltage noise and operation errors in an integrated circuit (IC) due to electrostatic discharge (ESD) events were measured, validated, and analyzed in this paper. A simplified structure of a laptop personal computer and an IC with a D-type flip-flop were designed and manufactured for the experimental tests. Every signal input to the IC was simultaneously measured during the ESD tests, and validated with the simulated results using a full-wave solver and a simple circuit model. Next, SPICE simulations were conducted using the measured voltages with ESD tests. The output waveforms and the statistical occurrence ratios of the operation failures found from the SPICE simulations were compared with measured values. Furthermore, the effects of decoupling capacitors on the IC operation failures due to ESD were investigated.**

***Index Terms*—Conduction noise, decoupling capacitor (de-cap), dual in-line memory module (DIMM), electrostatic discharge (ESD), error ratio, flip-flop, shielding, soft failure.**

I. Introduction

ELECTROSTATIC discharge (ESD) is increasingly a major electromagnetic compatibility problem and results in malfunctions of various electronic devices such as laptops and mobile phones. Problems due to ESD can usually be categorized as a hard failure at a chip-level or a soft failure at a system level. ESD hard failures at a chip-level occur during integrated circuit (IC) fabrication or assembly and from physical damage inside the IC. ESD soft failures at a system-level represent latch-ups, data corruption, faulty sensor readings, or malfunctions of the operating system that do not involve physical damage [1]. ESD protection devices and countermeasures against hard failures have been intensively developed by the researchers for the semiconductor fabrication process and circuit design [2]–[6]. However, system-level ESD soft failures have very different mechanisms and phenomena from chip-level ESD hard failures, and as such, the solutions are also different. Moreover, as smart mobile and wearable devices are becoming more widely used, the possibility of system malfunctions due to ESD events from contact with the human body are rapidly increasing. Therefore, it is important to pursue in-depth research on precise measurement and analysis of system-level ESD soft failures.

IC soft failures due to ESD can be generated by disturbed IC input voltages, such as data, clock, or power supply nets, on the printed circuit boards (PCBs) of the system. The voltage disturbances at the IC inputs can be also caused by direct field coupling to an IC die, package, or wire-bonds. For analysis of system soft failures, it is important to first obtain accurate measurements.

Transient voltage disturbances on PCBs have been measured in a careful measurement setup to prevent strong common mode noise and electric field coupling induced by the ESD [7]. Impedance parameters in a frequency domain have been also measured for analysis and validation [8]–[10]. Electromagnetic fields generated by ESD can be measured using field sensors or probes [11]–[16] by converting the measured probe voltages to field quantities. Various simulation and modeling techniques have been studied to validate measured voltages and fields due to ESD [11], [17]–[19]. Numerical analysis using the partial element equivalent circuit method was developed to facilitate the analysis of system-level ESD noise coupling [17], [18]. ESD field coupling in relation to PCB ground and metal chassis have been investigated [19]. However, these studies focus on the estimation of coupled noise voltage rather than operation errors caused by the ESD.

In order to analyze and reduce malfunctions due to ESD, it is necessary to analyze and measure the operation errors in the IC and system as well as the noise itself. Research has been conducted to understand the soft failures caused by ESD or electric fast transient at simple digital circuits, such as D flip-flop, ring oscillators, and logic gates [20], [21]. The methods for detecting functional changes in an IC due to ESD or electromagnetic interference were outlined [22]. A behavioral model of a microcontroller input for ESD soft failure simulation was proposed in [23]. The root causes of soft failures at a custom test chip induced by the system-level ESD and transmission-line

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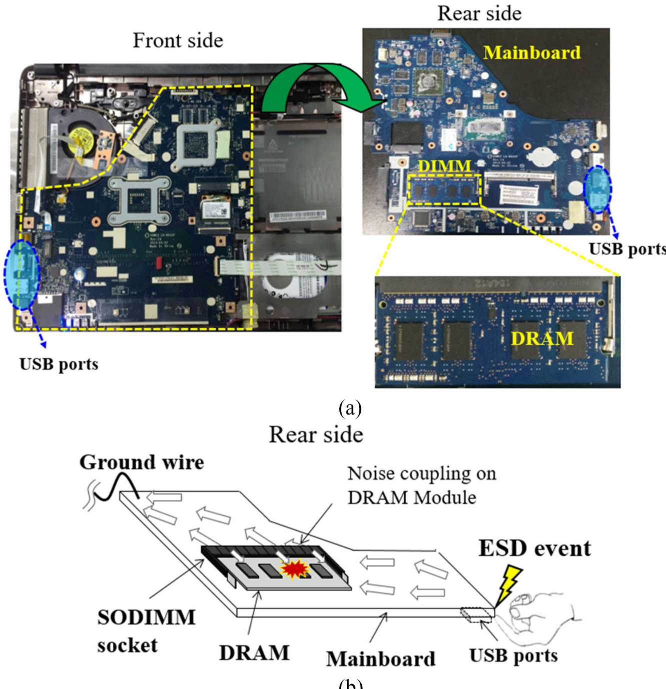


Fig. 1. (a) Mainboard of a real operating laptop PC. (b) Illustration of DRAM operation errors in a laptop PC due to a system-level ESD.

pulse (TLP) were experimentally tested and analyzed in [24]. Hardware and application level manifestations of ESD soft failures were experimentally characterized [25]. In [26] and [27], a system-level TLP probing technique was presented to evaluate soft fail robustness of systems and interfaces. A method for separating local soft failures from distant errors related to noise on the power distribution network was demonstrated [28]. In [29] and [30], the ESD soft failures of a real dynamic random-access memory (DRAM) at several test conditions were experimentally investigated. However, statistical phenomena of logic operation errors at a digital output have not yet been considered.

Fig. 1(a) shows the structures of the mainboard, dual inline memory module (DIMM), and DRAM in a real laptop personal computer (PC). DRAM operation errors can occur at a particular situation that an ESD stress is injected into a ground pin of the universal serial bus (USB) port installed at the side of the mainboard, as depicted in Fig. 1(b). A large ESD current flows into the board and the ground voltage of the mainboard fluctuates, which affects the DRAM operation in the DIMM. The noise voltages at the DIMM in a real operating laptop can be directly measured, but it is almost impossible to validate and analyze them using a full-wave solver due to the complexity of the real system. It is also difficult to reproduce the soft failures in real DRAM operations using SPICE circuit simulations because of the complicated operation states of the DRAM.

This paper presents the design of a simplified mainboard and DIMM structures, which resemble real configurations in a laptop PC. An IC with a simple D flip-flop was also designed and mounted on the simplified DIMM. The flip-flop in the IC operates by the clock and data input signals that are generated at the simplified mainboard. In Section II, the voltages at the clock, data input, data output, and power nets of the IC were simultaneously measured at the DIMM during ESD events. The measurement techniques shown in [7] were applied in the experiments.

A soft failure can be identified by monitoring the deviation of the real flip-flop data output versus the expected one. Since soft failures of a system due to ESD are a stochastic phenomena according to the ESD injection timing, the occurrence ratios of soft failures under repeated multiple ESD tests were recorded for several structures and ESD excitation voltages, respectively. Section III validated the experiments, where the measured noise voltages at the power-ground nets were compared with the simulated results using a full-wave electromagnetic solver in both frequency and time domains. Time-domain noise voltages were obtained from frequency-domain measurements, similar to [8]. The simplified laptop structure was also approximated to a circuit model to understand root causes and the ringing frequency of the ESD-induced noise voltages. The ESD gun body and strap were modeled on the basis of [11]. Next, IC soft failures were modeled using SPICE and then further investigated using the verified model in Section IV. The measured voltages of the clock, data input, and power nets were utilized as the input signal vectors for the IC in the H-SPICE simulations. The simulated data output waveforms of the IC were then compared with the measured waveforms for every repeated multiple ESD test. The occurrence ratios of the soft failures found from the SPICE simulations were also compared with measured ratios. From the SPICE simulations, the measured noise voltages and IC soft failures were completely validated, and the mechanism for soft failures was elucidated. Finally, Section V discusses how to rescue the operations errors from the system-level ESD events. The effects of the amount, number, and distribution of the decoupling capacitors (de-caps) are experimentally demonstrated.

II. Measurements of System-Level ESD Noises and IC Operation Errors on a Simplified Laptop Structure

A. Structures of the Simplified Mainboard, DIMM, and IC

The simplified mainboard has a plane shape similar to the real mainboard, as shown in Fig. 2(a). It consists of a four-layer PCB with an overall size of $220 \times 230\,\mathrm{mm}^2$. The first layer is used for the power island and component mounting, and the second and fourth layers are dedicated to the ground planes. Signal traces are predominantly routed in the third layer. The conductor layers are separated by a FR-4 dielectric material with a thickness of 0.3, 0.1, and 0.1 mm, respectively, from the first to fourth layer. The signal traces were designed to have a characteristic impedance of 50 Ω. The upper-right corner of the ground plane is connected to a large ground plane on the floor through a ground wire. As shown in Fig. 2(a), a 6-V dc voltage was supplied to the main board by an external power supply, which was then converted to 1.8 and 3.3 V using two commercial regulators. A 1.8-V dc is used for the power supply of the fabricated IC in the DIMM, and a 3.3-V dc was for the generator

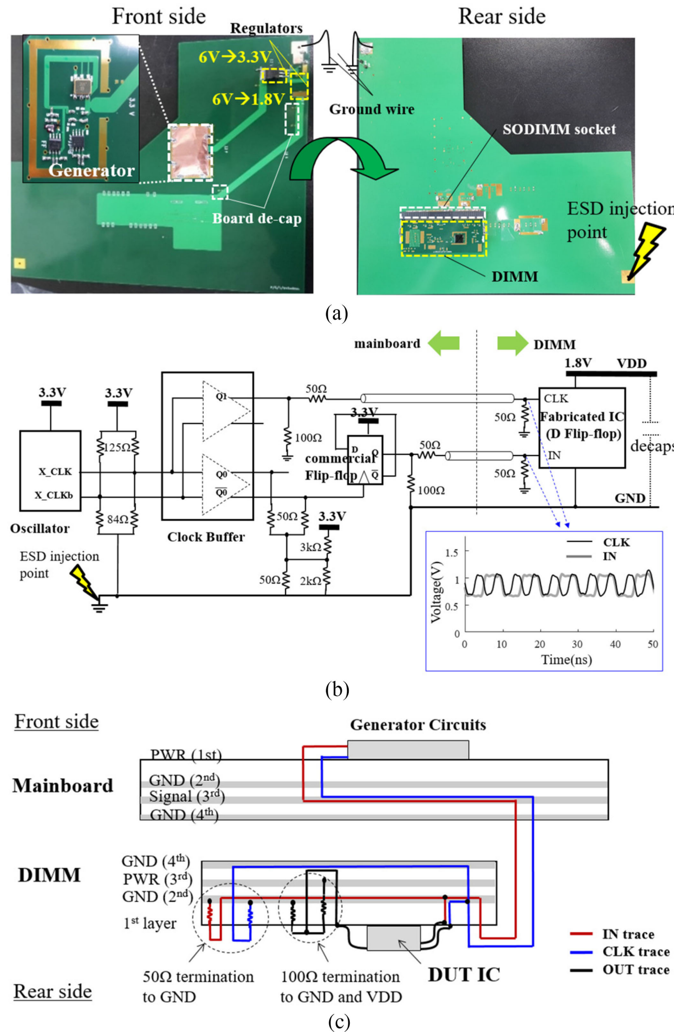


Fig. 2. (a) Photographs of the simplified mainboard. (b) Circuit schematic diagram. (c) Connections between the generator part on the mainboard and the IC on the DIMM.

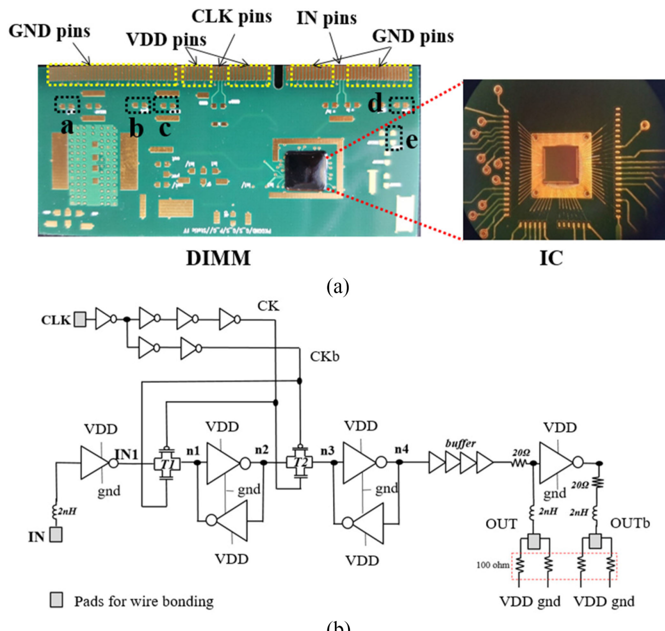


Fig. 3. (a) Photos of the DIMM and IC. (b) Circuit schematic of the D flip-flop in the IC.

circuit part on the mainboard that generates the clock and data input signals for the IC. Multiple de-caps were mounted at both 1.8 and 3.3 V power nets in the motherboard for stable dc supply. The 1.8-V dc power and ground nets for the IC were named as VDD and GND, respectively. As depicted in Fig. 2(b), two D-type flip-flops are utilized in the overall circuit configuration: one as a part of the generator circuit, and another as a part of the device under test (DUT) IC. The generator part provides the proper input signals for the DUT IC, and the behavior of the D flip-flop in the IC under the ESD events is investigated in the experiments. The generator circuit part consists of several commercial components such as a voltage-controlled crystal oscillator with a 200 MHz, clock buffer, and D-type flip-flop. The data input signal for the IC, “IN,” is obtained from a clock divider circuit using the commercial D flip-flop. Since the clock divider is triggered at every negative edge of the CLK, the toggling IN signal has a stable setup/hold time at the positive edges of CLK. The normal waveforms of IN and CLK signals are shown in Fig. 2(b). The IN and CLK signals from the generator part are connected to the IC on the DIMM through the small outline DIMM (SODIMM) socket, as shown in Fig. 2(c). The 1.8-V VDD island and GND planes in the mainboard were also connected to those in the DIMM through multiple VDD and GND pins of the socket. The voltage swing ranges of the IN and CLK were adjusted to proper levels for the 1.8-V IC by using source and load terminations.

When ESD events are excited at the lower left corner of the mainboard where the USB port is located in a real board, operational errors of the generator circuits sometimes occur due to strong electric fields. After the generator part is covered with copper tape and shielded from the direct field coupling, as shown in Fig. 2(a), all functional errors of the generator circuits can be prevented.

Fig. 3(a) shows the geometry of the DIMM and fabricated IC. The DIMM consists of a four-layer PCB with a size of 68 mm $\times$ 30 mm. The stack-up of the DIMM PCB is the same as the mainboard PCB. The layouts of each layer are designed similar to the real DIMM. The IC is directly mounted at the first layer of the DIMM by the chip-on-board assembly. The second and fourth layers are comprised of GND planes and signal traces, and the third layer is occupied by both VDD and GND planes. The fourth layer of DIMM faces the fourth layer of mainboard, as previously depicted in Fig. 2(b). There are a total of 204 pins at the front and back sides of the DIMM PCB for the connection to the socket. The pin assignments are similar to those of the real SODIMM. As shown in Fig. 3(a), 52 pins are dedicated to the GND, and 18 pins at the middle are for VDD connection. The CLK trace is connected to the IC, while running through the first, second, and fourth layers. The end of the CLK trace is terminated to a 50-Ω resistor at the corner of the DIMM. The IN trace is routed through the second layer and connected to the IC, which is then also terminated to a 50-Ω resistor.

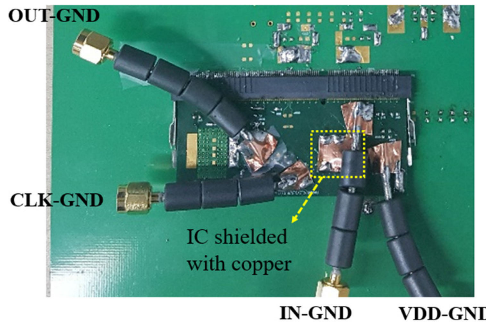


Fig. 4. Measurement setup using four semirigid cables.

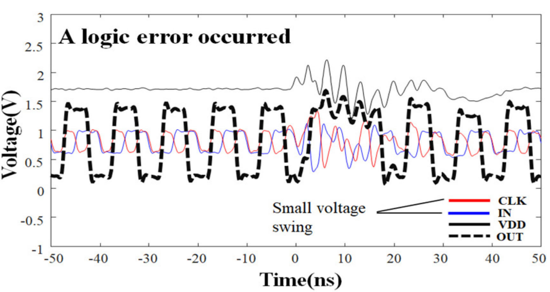


Fig. 5. Example of measured noise voltages due to 5 kV ESD events.

TABLE I
THREE EXPERIMENTAL CONDITIONS

	Case 0	Case 1	Case 2
IC shielding	No	Yes	Yes
DIMM de-cap	No	No	Yes (5 ea)

The schematic diagram of the designed IC is shown in Fig. 3(b), which consists of a typical static D flip-flop. The outputs of the flip-flop, "OUT and OUTb" are center-tap-terminated to the VDD and GND nets using two 100-Ω resistors on the DIMM, respectively. The soft failures, i.e., the operation errors of the flip-flop outputs in the IC were measured and analyzed.

B. Measurements of Noise Voltages on the DIMM and the Statistical IC Errors

For ESD events of 3, 5, and 8 kV, the voltages at the CLK, IN, OUT, and VDD nets with reference to the GND were simultaneously measured using a four-channel real-time oscilloscope with 1 GHz bandwidth. Four thin semirigid coaxial cables with ferrite beads were soldered to each net near the IC on the DIMM, as shown in Fig. 4. The outer grounds of the rigid cables were connected to the GND plane of the DIMM, and the signal pins were connected to the corresponding nets in series with 470-Ω surface-mount-technology resistors in order to create the conditions for high impedance probes [7]. The noise voltages measured at different positions of the same net are a bit different from each other. Since the main purpose of the experiment was to observe IC errors and correlate them with simulations, the measurement positions of the rigid cables were chosen to be sufficiently close to the IC. The maximum length difference between measurement points is about 40 mm, which has the delay difference of 280 ps at a strip line in the FR-4 medium. Because the delay is sufficiently small compared with the 200 MHz CLK period of 5 ns, its effect on observing the soft failures was ignored.

Three experimental conditions according to existence of the IC shielding and DIMM de-caps were tested and compared. As summarized in Table I, neither IC shielding nor DIMM decap were employed in Case 0. In Case 1 and Case 2, the IC is shielded by a copper tape, as shown in Fig. 4. The copper tape is connected to the ground plane of the DIMM and the outer ground of the coaxial cable without touching any signal pins. In Case2, five 10-uF de-caps were additionally employed between VDD and GND nets on the DIMM. The positions for the five de-caps are indicated from "*a*" to "*e*" in Fig. 3(a). The experiments in each case were repeated 50 times. Fig. 5 shows an example of the measured voltage waveforms in Case 1 under the 5 kV contact-discharge mode ESD excitation using EM Test Dito ESD simulator. All waveforms were plotted after multiplying by 10 to compensate for the high impedance probe gain. When the ESD event is excited at 0 s, significant fluctuations occur at every net of CLK, IN, VDD, and OUT. The shapes of the fluctuating noise are similar among those nets. It is worth noting that a large amount of noise also should arise in the GND net with reference to the earth ground, but it is not visible in the measured waveforms, since all the measurements are conducted with respect to the GND net on the DIMM. That is, the voltage fluctuations at the VDD nets represent the differential power-ground noise, which is seen by the IC.

The occurrence of an IC soft failure can be identified by observing the OUT signal, which is the output of the D flip-flop in the IC. In normal operation without a failure, the OUT should toggle at every rising edge of the CLK. When the noise voltages at CLK, IN, or VDD nets are induced at a critical timing with the amount exceeding tolerable levels for the IC operation, an incorrect logic output at the OUT can temporarily occur. The ESD-induced disturbance sometimes results in a soft-failure or sometimes not, depending on the disturbance timing. Fig. 5 corresponds to the case when the logic failures occurred. Among the repeated 50 ESD tests for each case, the number of tests that occurred with logic errors was recorded, and the statistical occurrence ratio of the logic errors was obtained. The measured error ratios of the three cases under the ESD events of 3, 5, and 8 kV are summarized and plotted in Fig. 6. The voltage noise waveforms of Case 0 and Case 1 are very similar, but the error occurrence ratio of Case 1 (26%) is less than that of Case 0 (36%). This is attributed to the reduction of the direct coupling to the wire-bonds and IC die by using the copper shielding. In a real-life system-level ESD, the couplings from relay switching of the ESD gun is nonexistent, but the direct coupling from the charges and currents at the nearby ground planes should be existent. After further employing five de-caps on the DIMM as in Case 2, the voltage noises were drastically reduced and even no errors occurred. Therefore, it is expected that IC shielding or DIMM de-caps can reduce malfunctions of real DRAMs in a real laptop PC induced by ESD events.

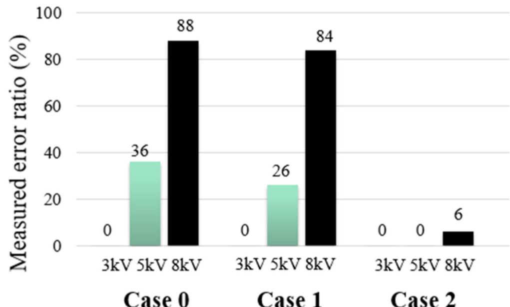


Fig. 6. Error occurrence ratios obtained from 50 measurements for each of the three cases for ESD events of 3, 5, and 8 kV.

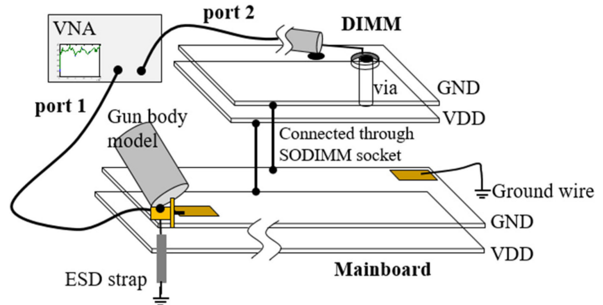


Fig. 7. Schematics of the setup and port conditions for the frequency-domain measurements.

III. Validation and Analysis of the Measured Voltages Using Simulations and Models

A. Validation by Frequency-Domain Measurements and Full-Wave Simulations

Noise voltages measured at the VDD net were validated by frequency-domain measurements using a vector network analyzer (VNA) [8]–[10]. As shown in Fig. 7, port 1 of the VNA was connected to the ESD excitation point using an sub-miniature version A connector, and port 2 was connected to the VDD measurement point using a thin semirigid cable. The signal pin of port 1 was connected to the ESD injection ground pad on the mainboard, and the outer ground was connected to the ESD gun ground strap. In addition, a cylindrical-shape conductor was also connected to the ground of port 1 to implement the selfcapacitance of ESD gun body, which is important for the high-frequency return-path of the ESD current. The size of the cylindrical conductor is similar to the actual gun size. Meanwhile, the signal pin of the rigid cable at port 2 was connected to the VDD net on the DIMM, and the outer ground of port 2 was soldered to the GND net. Although the signal pin of port 1 and the ground of port 2 are connected to the same GND net, the ac signals on them can be isolated from each other, since many ferrite cores were installed on the measurement cables and the distance between the two ports was sufficiently far apart. The transfer impedance, Z_{21}, which represents the ratio of the port 2 voltage due to the port 1 current, is extracted from the measured S-parameters. The ESD injection current was separately measured in a time domain using a commercial current probe (CT1) for a 5 kV ESD event, and its frequency spectra was obtained

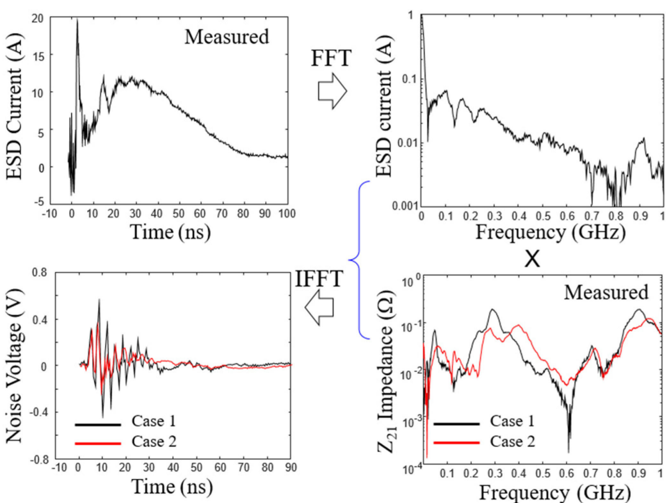


Fig. 8. Procedure for the extraction of the transient noise waveforms from the frequency-domain measurements.

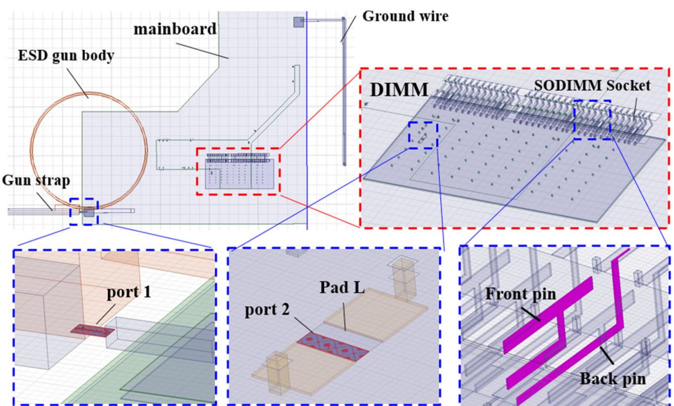


Fig. 9. Structures and port conditions for the frequency-mode HFSS simulations.

by the fast Fourier transform (FFT) calculation. The product of the Z_{21} and the frequency spectra of the ESD injection current results in the spectra of the noise voltage waveform on the VDD net. The noise voltage waveform on the VDD net in time domain is then calculated by the inverse-FFT (IFFT) of the spectra of the noise voltage. The procedure and results are summarized in Fig. 8 for the two experimental cases, Case 1 and Case 2. The results of Case 0 are very similar to those of Case 1, because the ESD injection current and Z_{21} parameter are rarely affected by the IC copper shielding.

For further complete validation of the measured results, the structures of the mainboard and DIMM were also simulated in both frequency and time domains using a full wave solver, Ansys HFSS. Fig. 9 shows the model geometries and port conditions for the HFSS frequency-mode simulations, which are all the same as those for the measurements. An inductance of 150 pH was added at port 2 in the simulation setup to consider parasitic inductances from the soldering part between the cable pin and the pad. The connector pins at the front and back sides of the SODIMM socket were also drawn.

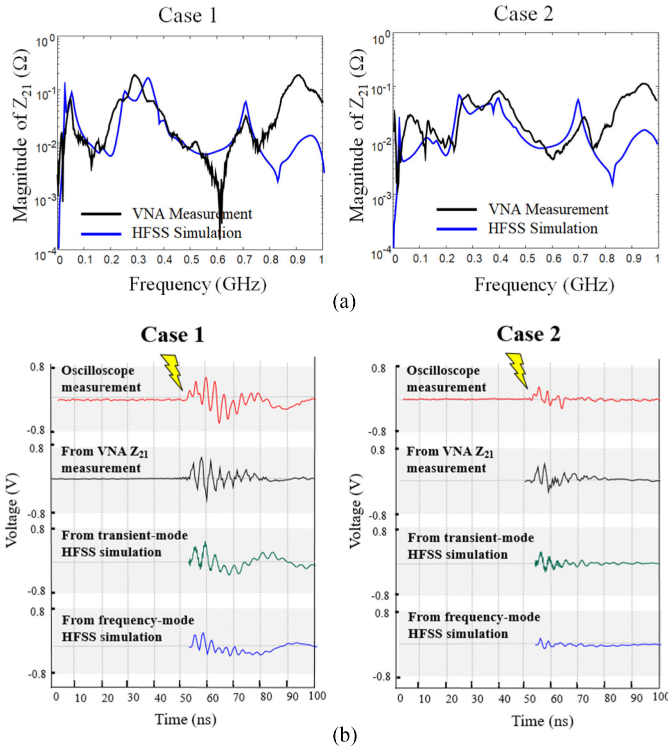
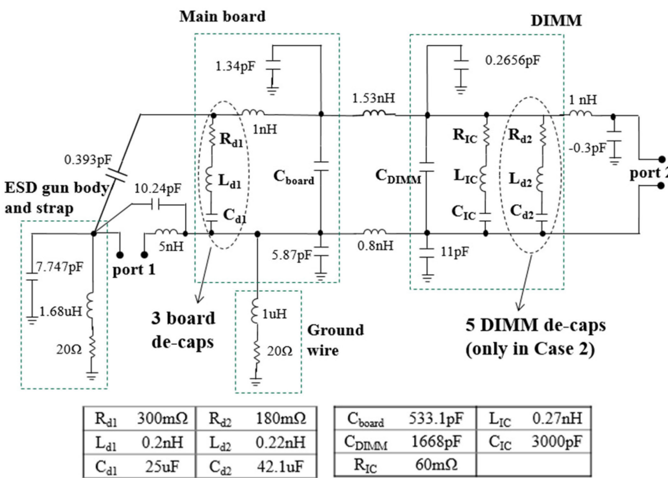


Fig. 10. (a) Comparison between simulated and measured Z_{21} parameters. (b) Comparison between the transient voltage waveforms obtained by the four methods.



R_{d1}	300mΩ	R_{d2}	180mΩ	C_{board}	533.1pF	L_{IC}	0.27nH
L_{d1}	0.2nH	L_{d2}	0.22nH	C_{DIMM}	1668pF	C_{IC}	3000pF
C_{d1}	25uF	C_{d2}	42.1uF	R_{IC}	60mΩ		

Fig. 11. Physics-based equivalent circuit model for the simplified mainboard, DIMM, and IC structures.

In HFSS transient-mode simulations, the model geometries are the same as those in the frequency mode except that the circuit components in the ESD gun are also added. According to the specification for the ESD gun [31], the *R*–*C* components with a value of 150 pF and 330 Ω in series with the ESD step voltage source are applied to the ESD gun excitation point. The voltage fluctuations at the position of port 2 is observed across 520 Ω resistance, which is the input impedance of high impedance probes used in the oscilloscope measurements. The results from the HFSS simulations in both frequency and time domains are compared with the measured results in Fig. 10. The simulated Z_{21} parameters are compared with the measured parameters for Case 1 and 2 in Fig. 10(a). Also, the procedure in Fig. 8 was conducted again based on the simulated data. That is, the transient ESD input currents obtained from the HFSS transient-mode simulations were converted to frequency spectra, which were then multiplied with the Z_{21} obtained from the HFSS frequency-mode simulations. Subsequently, the noise voltages on the VDD net were extracted by the IFFT. In summary, transient voltage waveforms were obtained by four methods:

1) direct transient measurements using an oscilloscope;
2) procedure in Fig. 8 based on the measured data of Z_{21} and ESD injection current;
3) transient simulations using a transient-mode HFSS
4) the procedure in Fig. 8 based on the simulated data of Z_{21} and ESD injection current.

The voltage waveforms on the VDD net obtained using the four methods were plotted for the two cases of Case 1 and Case 2 in Fig. 10(b), which shows sufficient agreement with each other. Although the simulated and measured Z_{21} impedance curves at the high frequencies above 800 MHz do not agree well, the discrepancy has little effects on the calculated time-domain noise waveforms, because the ESD current spectra are predominantly concentrated in the low-frequency range, as shown in Fig. 8. Also, the first impedance peak near 50 MHz shown in Case 1 is significantly reduced in both measured and simulated impedance curves of Case 2, which results in the reduced low-frequency ringing in the noise waveforms of Case 2. The difference between the waveforms obtained from the frequency-mode HFSS simulation and VNA measurement in Case 2 is attributed to the discrepancy between simulated and measured impedance curves below 200 MHz. Consequently, the measurement methods and the simulation models in both time and frequency domains were all validated.

B. Analysis Using Simple Equivalent Circuit Models

Figs. 5 and 6 show that the de-caps on the DIMM greatly reduce VDD noise and operation errors of the IC, but it is still difficult to understand the reason and the mechanism behind the noise reduction. To gain an intuitive understanding of the measured and simulated results, a simplified physics-based equivalent circuit model was established, as shown in Fig. 11. The circuit models were basically built from the physical geometries. The ESD gun body as well as the VDD and GND nets on the mainboard and DIMM were modeled as the selfcapacitance of each conductor plane and the mutual capacitance between them, whose values were extracted using a commercial RLC extractor, Ansys Q3D extractor. ESL, ESR, and capacitance of the de-caps were extracted by a shunt-through measurement technique using the VNA [32]. L_{d1}, R_{d1}, and C_{d1} represent the overall ESL, ESR, and capacitance of three de-caps mounted at the mainboard, respectively, while L_{d2}, R_{d2}, and C_{d2} represent those of the five de-caps mounted on the DIMM in the Case 2. Also, the impedance of the on-chip de-cap designed inside the IC are denoted as R_{IC}, L_{IC}, and C_{IC}. In addition, several parasitic inductances and resistances, which are associated with the pad, ESD gun strap, ground wire, and the socket connector, were also included in the model, whose values are fitted to the

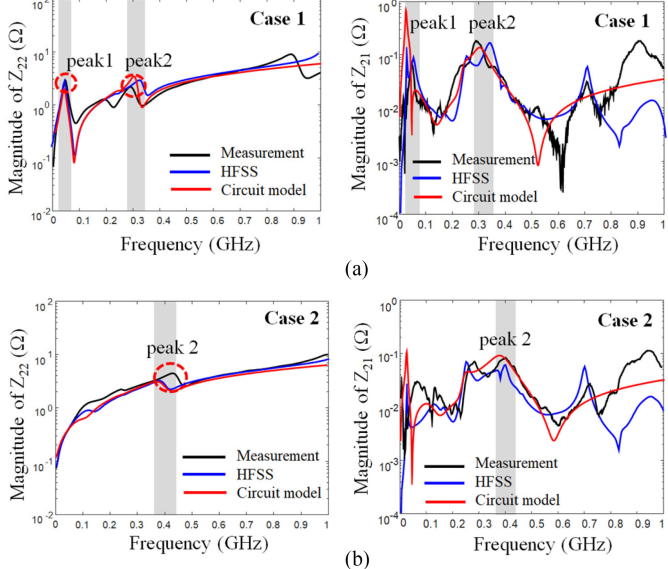


Fig. 12. Z_{22} and Z_{21} parameters obtained from measurements, simulations, and circuit models. (a) Case 1. (b) Case 2.

measured results. The multiple off-chip de-caps were considered in parallel and lumped into one in the circuit model, and their distribution effect was ignored. Actually, the position of the DIMM de-cap also has the considerable effects on the noise voltage and error ratios, as will be seen in the Section V, which cannot be captured in the lumped circuit model.

The Z_{22} and Z_{21} parameters obtained from the circuit model were compared with the results from measurements and HFSS in Fig. 12, which shows acceptable agreement. In Case 1, as shown in Fig. 12(a), there are two peaks in the Z_{22} impedance curves. The main contributors of each resonance peak can be inferred from the sensitivity analysis of the Z_{22} responses. The first peak at about 50 MHz is due to the resonance between the C_{IC} and the inductance path along the socket and the mainboard de-caps. The second peak at about 300 MHz occurs due to the resonance between C_{DIMM} and L_{IC}. When the DIMM de-caps are employed in Case 2, as shown in Fig. 12(b), the first peak in the Z_{22} curve disappears, since the inductance path along the socket and the mainboard de-caps is not visible because of the low impedance path provided by the DIMM de-caps. Also, the frequency of the second peak moves to a higher frequency at around 400 MHz, since the C_{DIMM} resonates in parallel with both L_{IC} and L_{d2}. The high peaks in Z_{21} were also observed at the corresponding resonant frequencies. As discussed in the previous section, the Z_{21} is multiplied with the spectra of ESD injection current to produce the voltage noise spectra. Since the ESD current spectra is predominantly confined at low frequencies below 1 GHz, the high resonance peaks of the Z_{21} below 1 GHz are predominantly responsible for the voltage noise waveforms in Fig. 10. Fig. 10(b) shows that the shapes of the voltage waveforms in Case 1 consist of two kinds of frequency components, whereas those in the Case 2 consist of only the high-frequency component, because the Z_{21} of Case 2 does not have a clear low-frequency resonance. Consequently, using the DIMM de-caps in Case 2, the VDD noise was greatly decreased by the absence of the lower frequency ringing. The ringing due to the second resonance was also reduced and attenuated faster.

IV. Validation and Analysis of Statistical IC Errors Using HSPICE Simulations

In order to validate and analyze the measured results of the IC operation errors, the voltages at the CLK, IN, and VDD nets, which were simultaneously measured under an ESD event, were applied to the inputs for the SPICE circuit simulation. The voltage at every node inside the flip-flop circuit can be obtained from the simulation, and the voltage at the "OUT" node was compared with the measured voltage. These procedures were repeated for the multiple ESD tests, and the error occurrence ratios in the simulations were recorded. The statistical error ratios found in the simulations were also compared with the measured values. Observing the voltage at every internal node of the circuit facilitated identification of the root causes of the operation error in the circuit. Fig. 5 shows that the CLK and IN signals measured at the DIMM had small voltage swings from 0.7 to 1 V. When the signals were applied to the "CLK" and "IN" pads of the flip-flop circuit in Fig. 3(b), which is shown again in Fig. 13 for convenience, the small swing-voltages were changed to full-swing voltages by the inverter buffers in the IC. When an ESD event occurs, the full-swing outputs of the inverter buffers are significantly affected by the fluctuating gate inputs and also by the voltage fluctuations at the VDD nets.

The transient voltage waveforms at all internal nodes under a 5 kV ESD event were obtained from the SPICE simulations, and plotted in Fig. 13. The small swing CLK signal was converted to full-swing voltages at the "*CK*" and "*CKb*" nodes, where several incorrect logic glitches were generated by the ESD event. At the same time, the full-swing voltage at the IN1 node, which was converted from the small swing IN signal, also included incorrect logic glitches. Each temporal logic glitch at the IN1 node was named as "glitch 1" and "glitch 2," as shown in Fig. 13. Glitch 1 was attenuated at the n1 and n2 nodes, but Glitch 2 kept transmitting to the n2 node with a distorted proper logic "1." Subsequently at the next n3 node, proper logic "1" is completely removed, i.e., the narrow high pulses are no longer transmitted, since the T2 switch is turned OFF in the shadow regions due to the *CK* and *CKb* signals. The missing logic state "1" keeps propagating until the final output of the flip-flop, "OUT." The measured "OUT" voltage was also plotted together, and the exact same logic error appears in the measured data, which validates the simulation and measurement results.

The multiple SPICE simulations for the repeated ESD tests identified that the output errors of the flip-flop circuit herein predominantly originated from the first-stage inverter buffers for the CLK or IN signals, which convert the small-swing external signals to full-swing internal signals. Incorrect logic glitches in the input are propagated at unexpected timings by the incorrect switch gating clock due to the ESD. It is also worth noting that "OUTb" seems to have less noises compared to "OUT." It is attributed to that "OUTb" is predominantly remained at the low sate during the soft failure, whereas "OUT" is at the high state. The measured voltage fluctuations represent the differential noises with reference to the DIMM GND net, and, in the HSPICE simulation, the measured signal-to-ground noise is

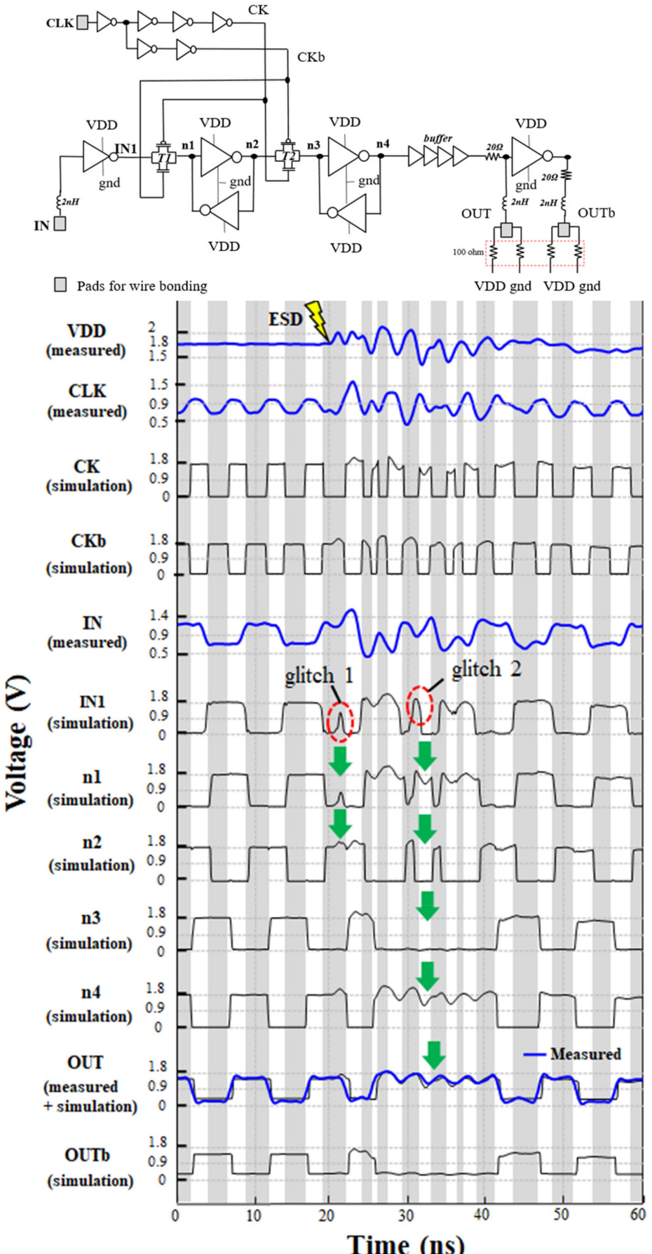


Fig. 13. Voltage waveforms at the IC internal nodes obtained from HSPICE simulation using the measured VDD, CLK, and IN voltages. The simulated "OUT" voltage is compared with the measured one.

entirely excited to the signal line, whereas the voltage of the external GND net is set to 0 V. Therefore, no output voltage fluctuation is supposed to be observed when the output is at the low state having the same voltage as the GND net.

Fig. 14 shows two examples of the simulation and measurement results in the ESD tests for Case 1 structure. As the error occurrence ratios are indicated in Fig. 6, the logic error in the OUT signal stochastically occur in the multiple ESD tests. An error case and a nonerror case are shown, respectively. The CLK, IN, and VDD voltages measured in each ESD test were applied to the SPICE simulation, and the simulated "OUT" signals are compared with measured signals. The simulated "OUT" signals produce very similar waveforms and logic results with the

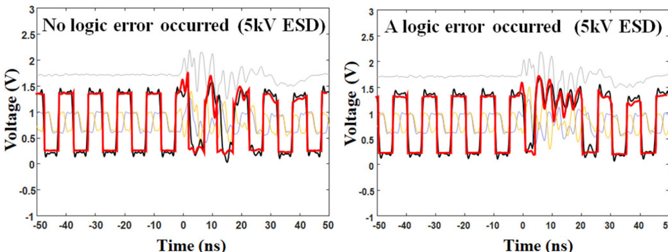


Fig. 14. Two examples of the simulated and measured waveforms in the ESD tests. The simulated "OUT" voltage is compared with the measured voltage.

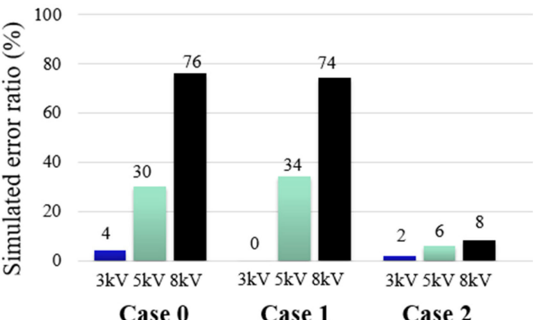


Fig. 15. Error occurrence ratios obtained from 50 instances of HSPICE simulations using the measured VDD, CLK, and IN voltages in Fig. 6.

measured results in most cases. Although the VDD noises in multiple ESD tests in the same condition were very similar each other, the final "OUT" of the IC can be very different according to the ESD timing with regard to the CLK and IN signals. Simulations for all the ESD tests shown in Fig. 6 were repeatedly conducted using the measured CLK, IN, and VDD waveforms, and the error occurrence ratios in the OUT were also recorded. Fig. 15 shows the simulated error ratios, where each percentage represents the error occurrence ratio in the OUT found from the 50 simulations based on the 50 ESD experiments. Because the ESD gun simulator was manually injected by hands, the excitation time of multiple injections is statistically randomized over the IC CLK switching time.

The simulated results in Fig. 15 show a high correlation with the measured data in Fig. 6. Especially in Case 2, the simulated error ratios were drastically reduced, which was similar to the measured results. However, the simulations cannot take into account the effects of the copper shielding in Case 1, since the simulations were conducted only based on the measured voltages on the DIMM. Therefore, no decreasing trends of the simulated error ratios from Case 0 and Case 1 are shown, although the measured error ratios in Case 1 were a bit less than those in Case 0. If the number of tests is increased, it is also possible that the measured error ratios of Case 0 and Case 1 would be statistically even out.

V. Methods for Reduction of IC Soft Failures Due to System-Level ESD

A. De-caps at the DIMM

The impact of an external decoupling capacitance on the ESD propagation paths into an IC was demonstrated in [33]. The

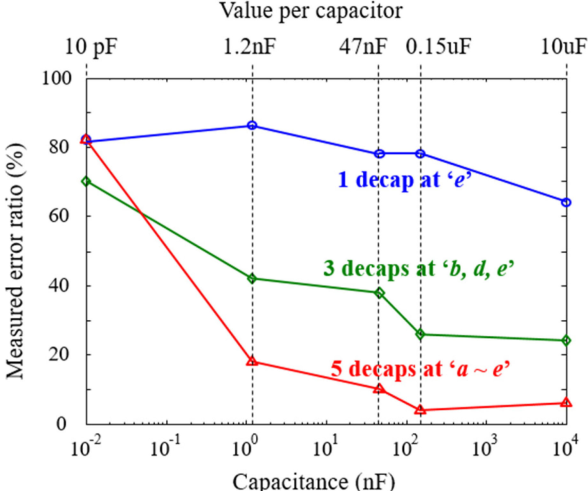


Fig. 16. Measured error ratios depending on the capacitance and number of the DIMM de-caps for 8 kV ESD event.

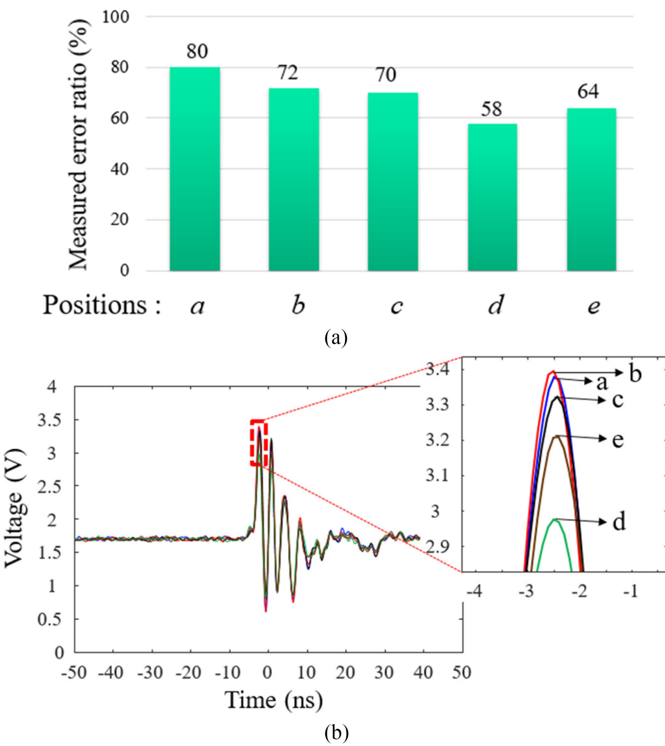


Fig. 17. Dependency on the position of a 10-uF de-cap. (a) Measured error ratios. (b) Measured power-ground noise voltages.

measurements and simulations in this paper also confirmed that the de-caps on the DIMM are very effective in reducing ESD-induced flip-flop logic errors. The effects of the values, numbers, and locations of the de-caps on the logic error and voltage noises were further investigated by the validated measurement and simulation methods. The measured error ratios under 8 kV ESD tests according to the numbers and values of the DIMM de-caps are summarized in Fig. 16. Each error ratio was obtained from 50 repeated measurements. The five possible positions for the DIMM de-caps were previously indicated in Fig. 3(a). A single de-cap is located at position *e*, three de-caps are at positions *b*, *d*, *e*, and five de-caps are at all the positions *a*–*e*. Along with the number of de-caps, five capacitance values: 10 p, 1.2 n, 47 n, 0.15 u, and 10 uF were tested, respectively. The IC is shielded by the copper tape in all experiments.

As a baseline, in the case without any DIMM de-caps, which corresponds to Case 1, the error ratio was 84% for 8 kV ESD tests. Five 10-uF de-caps correspond to Case 2. Comparing the error ratios of the cases employing one de-cap with different capacitance values, the error is only reduced slightly as the capacitance increases. If three or five de-caps are employed, however, the error ratios are quickly reduced as the capacitance increases. Also, the case with one de-cap at the position *e* with 10 uF value has a much larger error ratio than the case with five de-caps at the positions *a*–*e* with 1.2 nF, which has the total capacitance of 6 nF ($= 1.2\text{n} \times 5$). This suggests that not only the increased capacitance is important, but also filtering out the ESD disturbance way before it reaches the victim IC, spatially. Furthermore, the error decreasing ratios seem to be saturated when the value per capacitor is more than 0.15 uF. When a sufficient value of capacitance is utilized, the number of de-caps becomes very important for reducing IC operation errors.

The effect of de-cap positions on the error ratio were also tested, as shown Fig. 17. Only a single 10-uF de-cap was employed on the DIMM de-cap positions *a*, *b*, c, *d*, and *e* in each five test case, respectively. The measured error ratios depending on the de-cap positions are summarized in Fig. 17(a). In each measurement, the voltage between the VDD and GND nets was also measured to investigate the correlation between the error ratios and power-ground noises. Fig. 17(b) shows the measured power-ground noise voltages for the five cases with the different de-cap positions *a*–*e*. As expected, amounts of the peak noises correlate with the error ratios in Fig. 17(a). The cases with the de-cap positions *a*, *b*, and *c* have the more noise voltages and error ratios than those with positions *d* and *e*. This was attributed to the de-cap position *d* or *e* being close to the IC, which suppresses the power-ground noise for the IC more effectively.

B. Discussions

The immunity of an electronic system against the system-level ESD event can be improved by using several techniques. A de-cap is one of the most efficient ESD noise filters, such as a ferrite bead or a transient voltage suppressor [33], [34]. The de-caps are successfully applied to increase the ESD immunity of the D-type flip-flop and the mobile phone in this paper and [35], respectively. The direct field coupling or the ESD current at the wire-bonds of an IC can cause the decoupling of the IC and board power voltage levels, which can result in an unexpected trigger upset [36]. Shielding of an IC or critical I/O paths from the direct electromagnetic fields of ESD zapping can improve the ESD immunity of the system. Because the IC wire-bonds can weaken the ESD immunity of an IC, the IC package that does not employ wire-bonds would be helpful to increase ESD immunity. However, the results of Fig. 6 in this paper show that the IC shielding is not very effective. The low effectiveness of the IC shielding is attributed to the weak direct field

coupling in the test setup. The distance between the zapping point and IC is relatively long. Also, the IC is not placed on the mainboard, where the ESD zapping occurs, but placed on the DIMM. Because the DIMM is sustained above the mainboard by the socket, the field coupling from the ESD-induced charges and currents to the IC on the DIMM would be weaker than that to an IC on the mainboard. More investigations on the effect of the IC shielding in various situations are further required.

As an on-chip solution, inserting a guard-ring between I/O and core blocks inside the IC including memory and logic circuits can also reduce the coupling effects between the blocks, and consequentially increase the system-level ESD noise immunity [37]. Even though the several techniques for ESD noise reduction are utilized, the operating errors still may occur due to the system-level ESD. To rescue a system from a critical malfunction, the on-chip transient detection circuit has been also proposed and combined with the firmware operation to execute the system recovery procedure [38], [39].

VI. Conclusion

In this paper, the statistical operation errors of a flip-flop circuit on a simplified mainboard and DIMM structures due to ESD events were analyzed and validated by full-wave and SPICE simulations. For the analysis and validation of noises and errors, the clock signals, data input, data output, and power nets of the IC were simultaneously measured at the DIMM during ESD events. The measured noise voltages at the power-ground nets were compared with the simulation results using a full-wave electromagnetic solver in both frequency and time domains. Additionally, the power-ground nets of the simplified laptop PC structure was approximated to a simple circuit model to extract the root causes of the ESD noises.

Subsequently, measured voltages in ESD tests were utilized as the input signal vectors for the SPICE simulations to validate and investigate IC statistical soft failures. Simulated data outputs of the IC were then compared with measured values for all repeated multiple ESD tests. The occurrence ratios of the soft failures found from the SPICE simulations were also compared with measured ratios. Output errors of the flip-flop circuit predominantly originated from first-stage inverter buffers, which convert the small-swing external signals to the full-swing internal signals. Furthermore, the effects of de-caps on the soft failures due to ESD were investigated through measurements. Although all the work herein was performed based on a simplified structure of a real laptop, the experiment and analysis methods are very useful for understanding and solving ESD soft failure problems in real complex systems.

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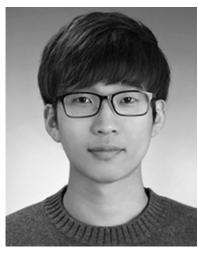

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