Chip-Package-System ESD Simulation Methodology with Chip ESD Compact Model

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ANSYS

UBM Tech

Agenda

- System level ESD Testing
  - EMC Classification
    - What is ESD?

- CPS ESD Simulation Methodology
 - A comprehensive Chip-Package-System (CPS) ESD dynamic methodology

- Modeling for CPS ESD Simulation
  - ESD and ESD Modeling
    - Chip ESD Compact Model
    - ESD Gun Modeling
      - Equivalents Circuit ESD Gun
      - Full 3D ESD Gun with HFSS Transient Solver
    - TVS Diodes, CMF/EMI/ESD Filter
    - Connector and PCB Modeling

- Full 3D Mobile Device ESD Simulation
  - Case Study 1; Micro USB Connector Device on Mobile PCB
    - Understand ESD Propagation on Complex PCB with Connector
  - Case Study 2; Mobile System-level ESD propagation modeling
    - Predict Chip pin V(t) ,ESD propagation Prediction
- Conclusion

System level ESD Testing

- The Mobile system ESD test platform that incorporates
    - All *major components of a converged Device*
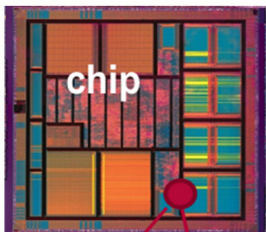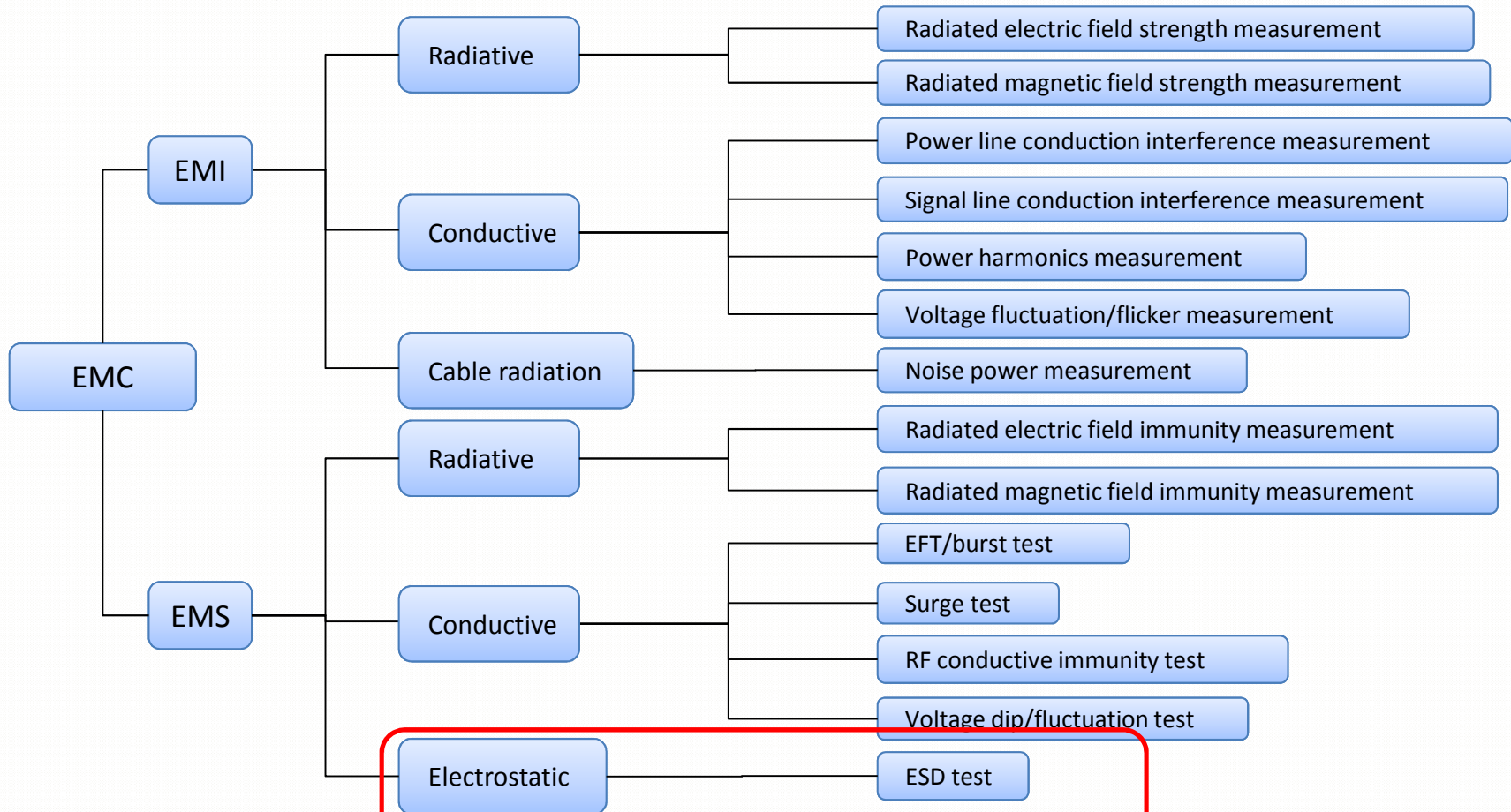
      Chip/Package
      PCB, Connectors
      Housing
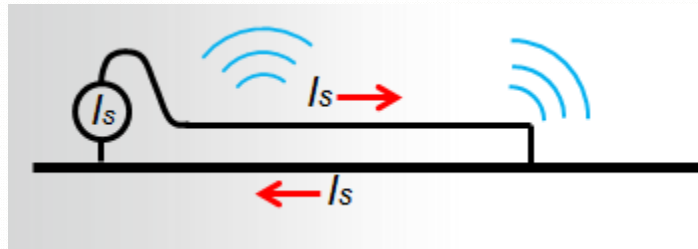   Battery
      Components
      Etc…
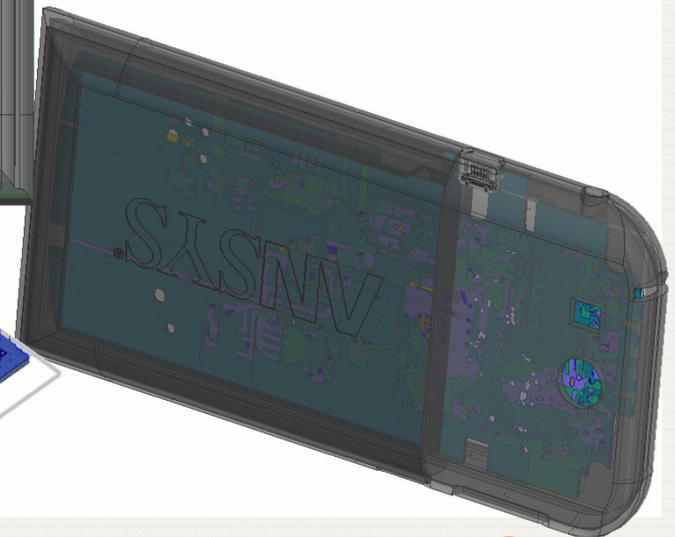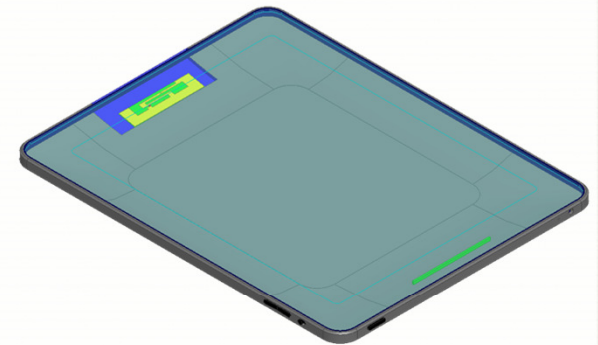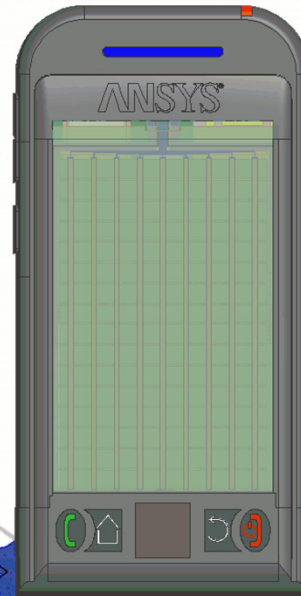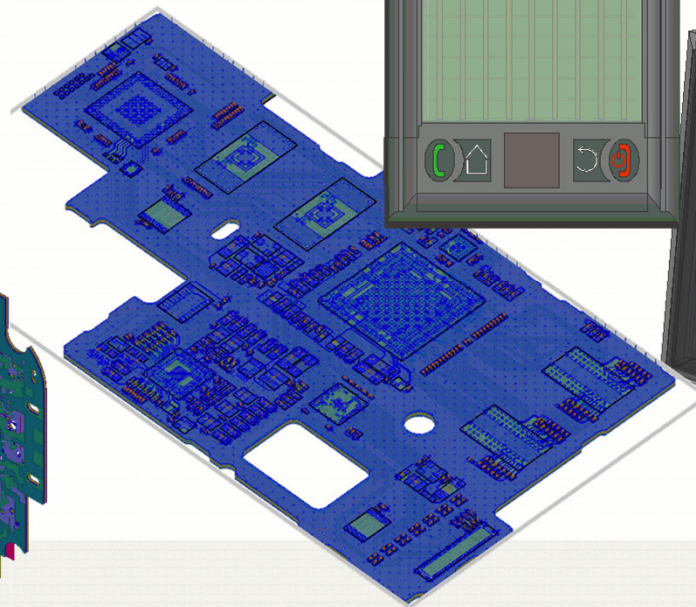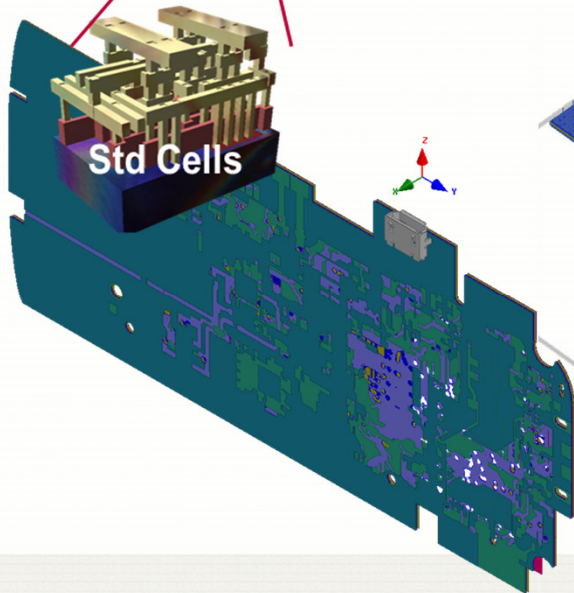
EMC Classification

- Various measurement methods for addressing EMC problems are available for use depending on the product and operating frequency band.

EMC
- EMI
  - Radiative
    - Radiated electric field strength measurement
    - Radiated magnetic field strength measurement
  - Conductive
    - Power line conduction interference measurement
    - Signal line conduction interference measurement
    - Power harmonics measurement
    - Voltage fluctuation/flicker measurement
  - Cable radiation
    - Noise power measurement
- EMS
  - Radiative
    - Radiated electric field immunity measurement
    - Radiated magnetic field immunity measurement
  - Conductive
    - EFT/burst test
    - Surge test
    - RF conductive immunity test
    - Voltage dip/fluctuation test
  - Electrostatic
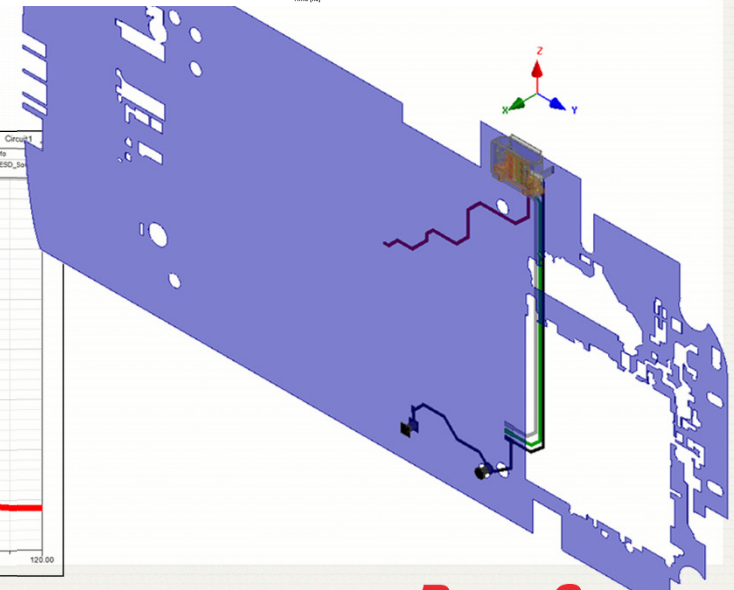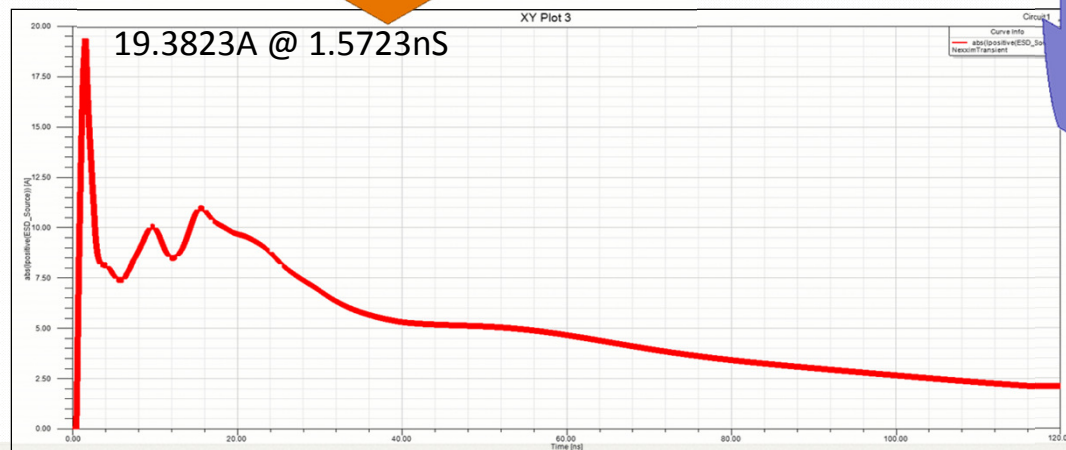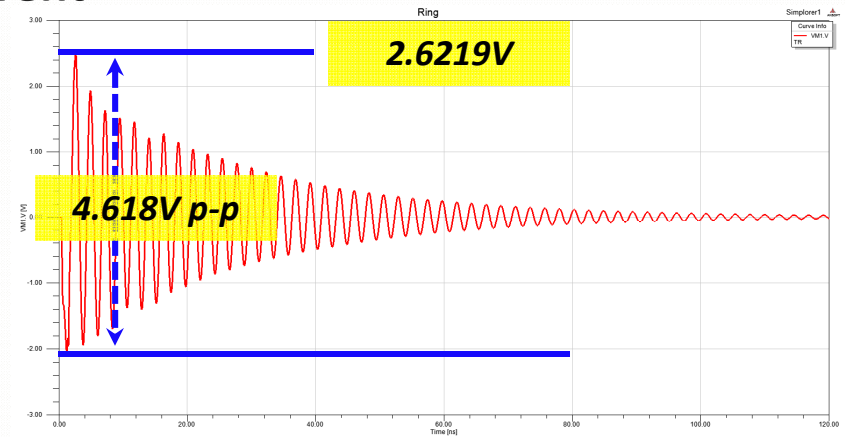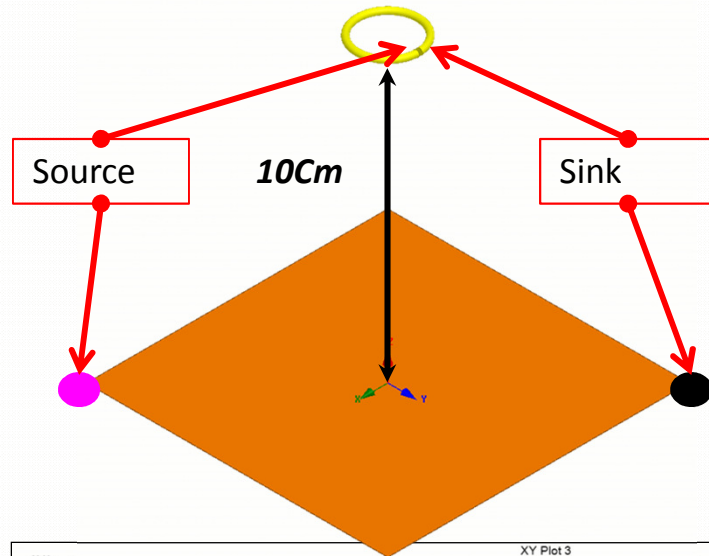   - ESD test

Standard of IEC 61000-4-2

DESIGNCON 2014

What is ESD?

- **Answer is;**
  - **Electrostatic discharge (ESD) is the sudden and momentary electric current** that flows between two objects at different electrical potentials...unwanted currents that may cause damage to electronic equipment. (from *Wikipedia*)

- **Various mechanisms can contribute to the EMS problem**
  - ESD is multi-physics issue
  - Time & Frequency
  - Electro Magnetic Field Coupling
   - magnetic induction, conduction etc.

Electro Magnetic Field Coupling

- **Magnetic Field Coupling**

ESD Injection

I

10 cm

$A = 1\ cm2$

M

$V_p = M\,\dfrac{\partial Ig}{\partial t}$

$V = N\,\dfrac{\partial \phi}{\partial t}$

$\phi = BA$

$\dfrac{\partial \phi}{\partial t} = A\,\dfrac{\partial B}{\partial A}$

$B = \dfrac{\mu_0 I}{2\pi r}$

$\dfrac{\partial B}{\partial t} = \dfrac{\mu_0}{2\pi r}\cdot\dfrac{\partial I}{\partial t}$

$V = \dfrac{N\mu_0 A}{2\pi r}\cdot\dfrac{\partial I}{\partial t}$

$N = 1$

$\mu_0 = 4\pi \times 10^{-7}$

$t = 1ns$

Vp

Solutions: MFC_ESC - Q3DDesign1

Simulation: Setup1 | LastAdaptive | AC RL

Design Variation:

Profile | Convergence | Matrix | Mesh Statistics

☐ Resistance Units: ohm | Matrix | 10 (MHz) | Export...

☑ Inductance Units: pH | Original | ☐ All Freqs

Passivity Tolerance: .0001 | Check Passivity | Equivalent Circuit Export...

	Box1:Rectangle1	Torus1:Source1
Freq: 10 (MHz)		
Box1:Rectangle1	64591	-84.302
Torus1:Source1	-84.302	28617

Close

Vp

Source

Sink

"ESD Phenomena"
ESD Mitigation Techniques by Cyrous Rostamzadeh 2008

Electro Magnetic Field Coupling

- **Magnetic Field Coupling Due to an ESD event**

Source

Sink

*10Cm*

2.6219V

4.618V p-p

19.3823A @ 1.5723nS

Electro Magnetic Field Coupling

- Simplorer Q3D Dynamic Link
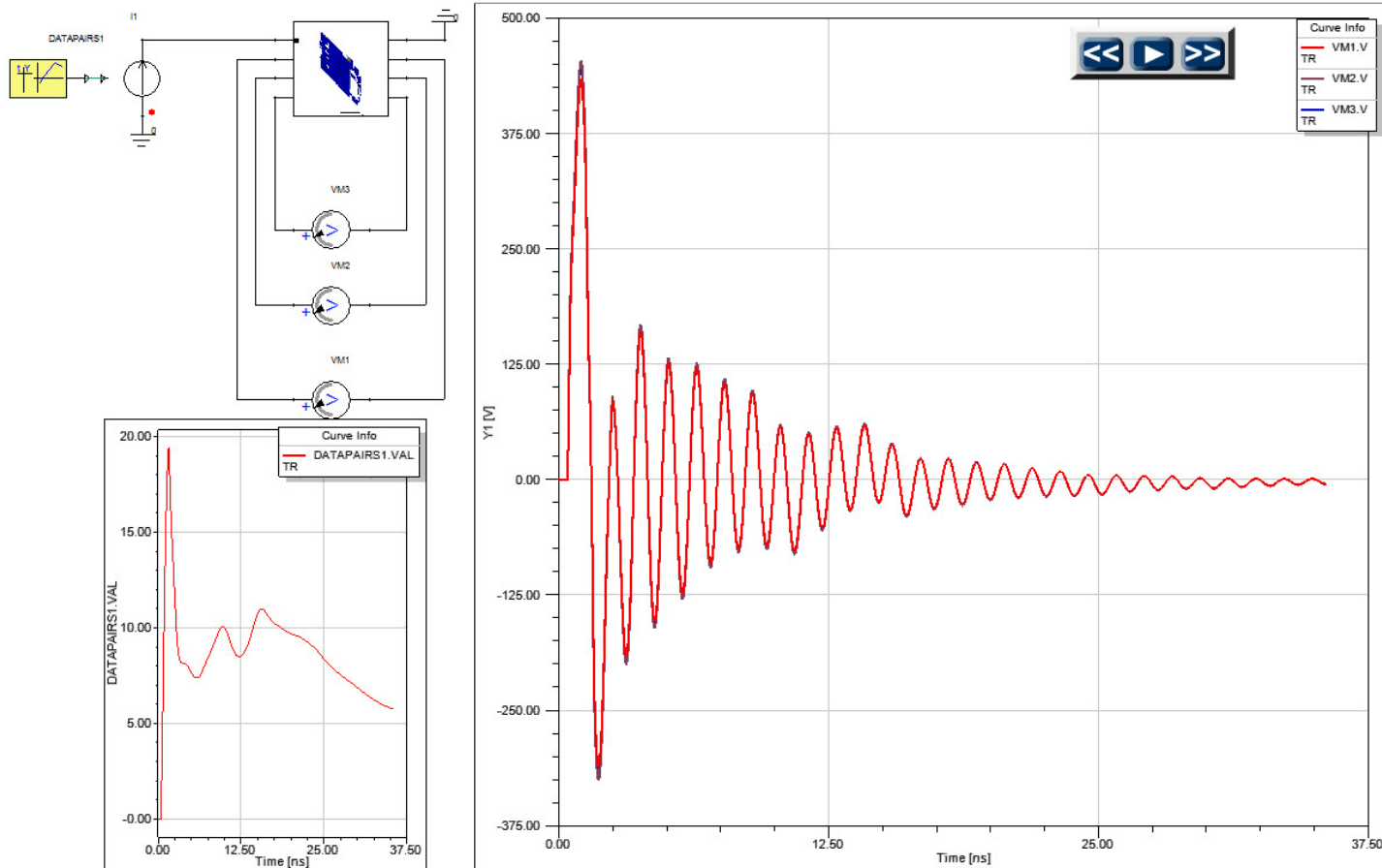
# Electro Magnetic Field Coupling

- **ESD susceptibility map on printed circuit board trace with ESD Protection device**
  - ESD susceptibility map for printed circuit board is presented and the mechanisms that the ESD event couples into the digital devices is demonstrated.

453.68V

400.305V

Simple ESD Protection device = Cap.
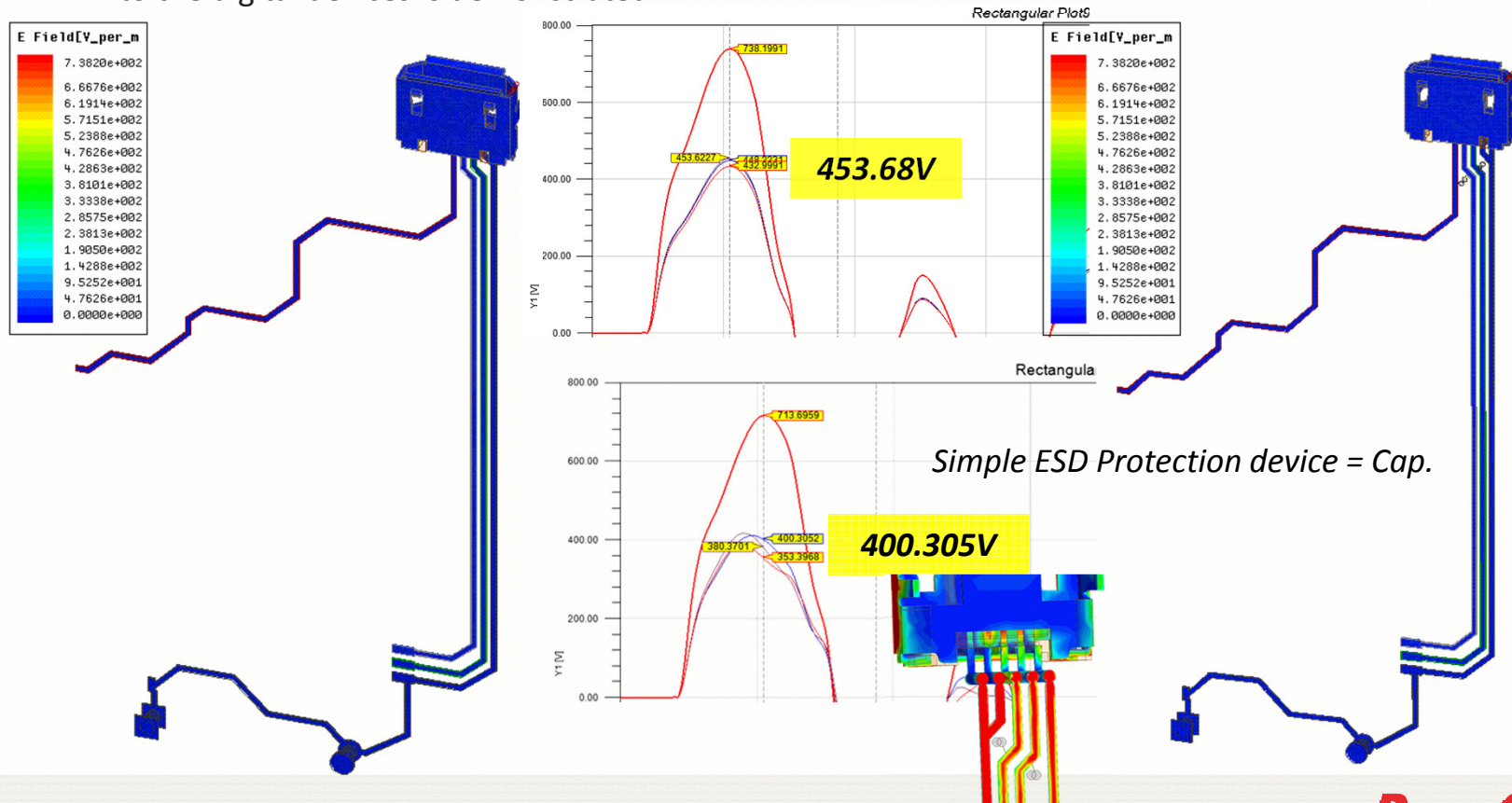
ESD and ESD Modeling

- **Chip ESD Compact Model**
  - Chip ESD Compact Model (CECM) provides a reduced RLC network among ports and per port demanding current for the chip power-on status with a chosen chip operation vector
  - On-chip decaps are modeled including intrinsic device decap, power/ground cap, intentional decap, and effective loading cap
  - On-chip diodes/clamps can be included in the model when generating from RedHawk Pathfinder-S which is on-chip ESD analysis tool
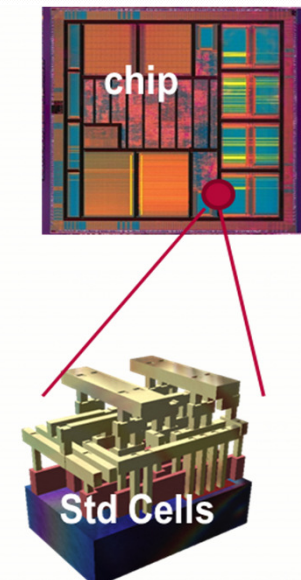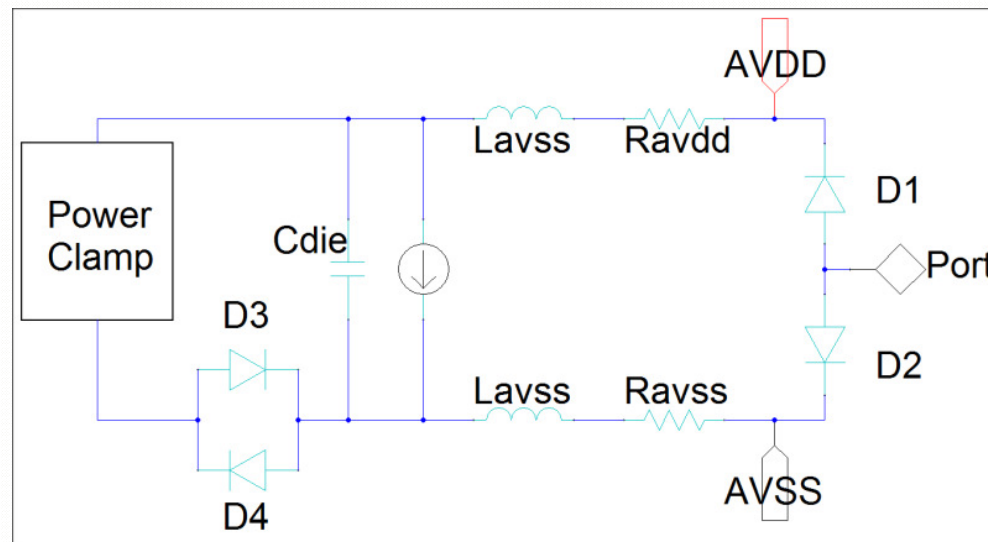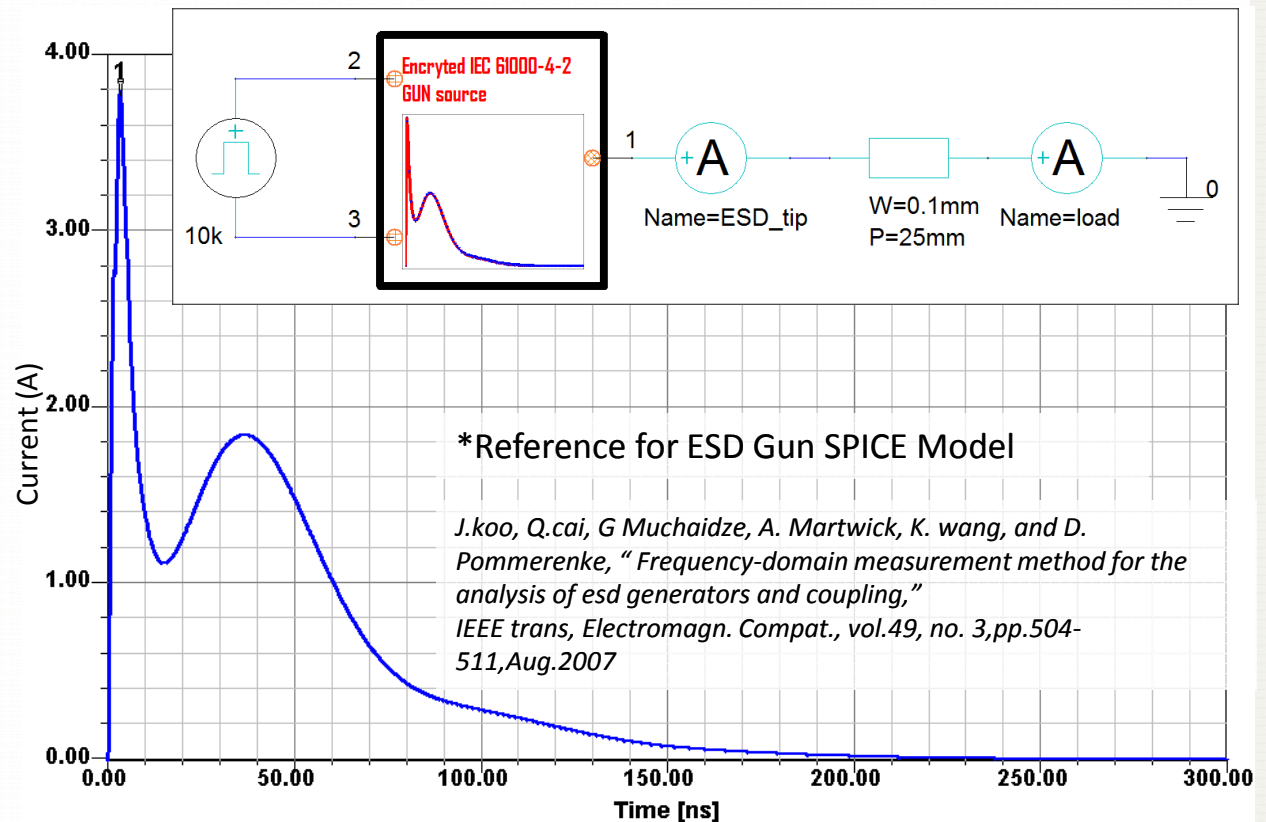
ESD GUN Modeling

- **ESD GUN Modeling**
 - Circuit base ESD Gun Model for Contact Method

Peak current : 3.75 A / kV ±10%

30ns current : 2 A / kV ±30%

60ns current : 1 A / kV ±30%
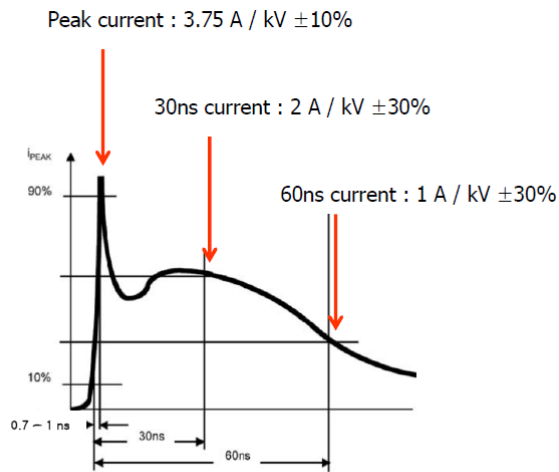
Current waveform of an ESD generator

Standard of IEC 61000-4-2

Encryted IEC 61000-4-2 GUN source

Name=ESD_tip

W=0.1mm
P=25mm

Name=load

10k

*Reference for ESD Gun SPICE Model

J.koo, Q.cai, G Muchaidze, A. Martwick, K. wang, and D. Pommerenke, " Frequency-domain measurement method for the analysis of esd generators and coupling,"
IEEE trans, Electromagn. Compat., vol.49, no. 3,pp.504-511,Aug.2007

Current (A)

Time [ns]

ESD and ESD Modeling

- **ESD GUN Modeling**
  - Circuit base ESD Gun Model for Contact Method
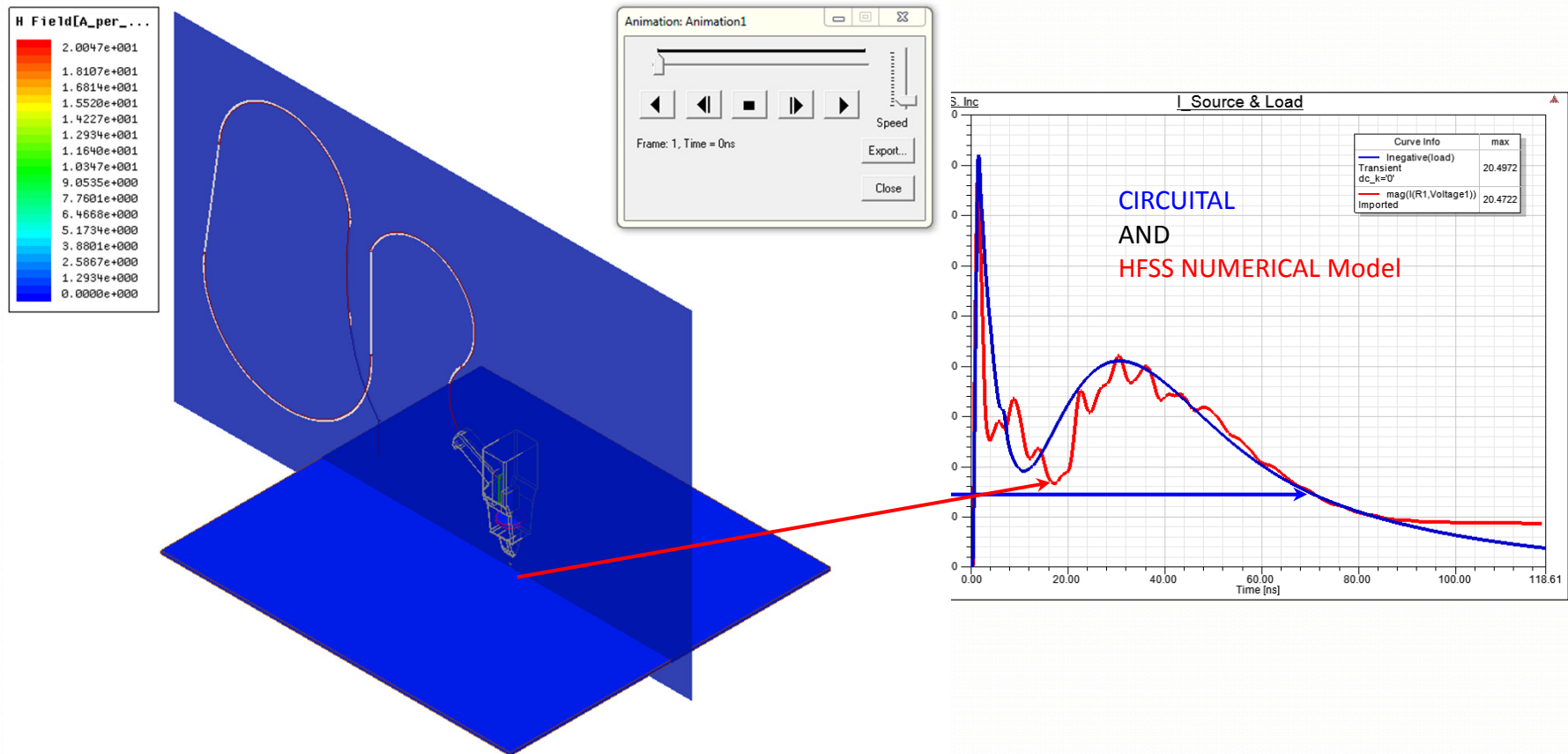   (Between EM test DITO and SPICE model in DesignerSI)
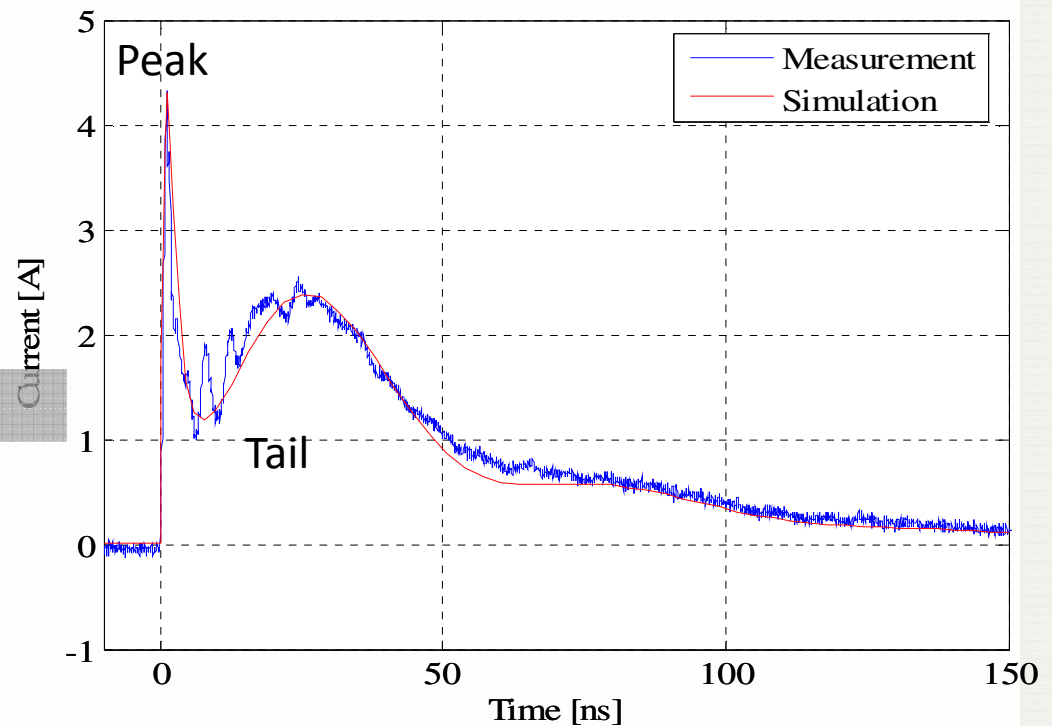
ESD and ESD Modeling

- ESD GUN Modeling
  - Simulation vs. Measurements

HFSS Transient solver
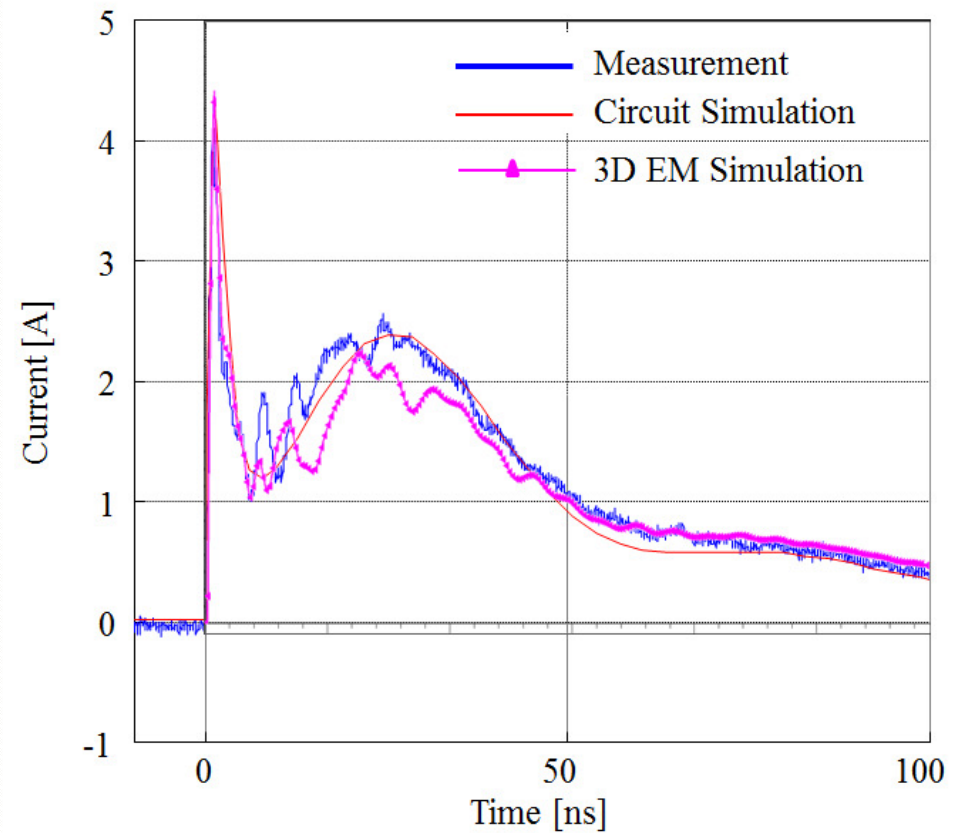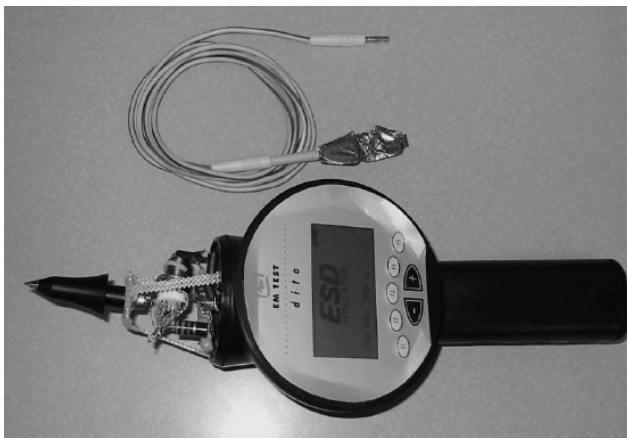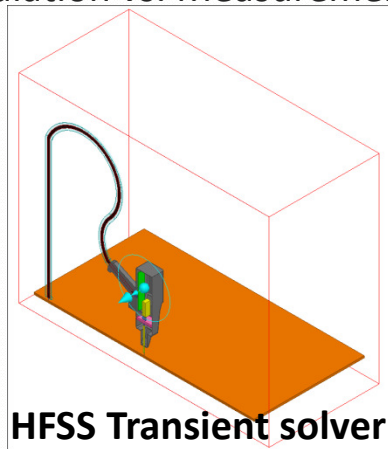
ESD and ESD Modeling

- **ESD Gun**
  - Time-varying Magnetic Field with Discharge Current waveform

CIRCUITAL
AND
HFSS NUMERICAL Model

- **ESD Gun Current propagation**

ESD Current propagation; 0ps to 5ns
10ps frame

0   250   500 (mm)

ESD and ESD Modeling

- **ESD Gun Current propagation**

| 400ps | 430ps | 500ps |

| 530ps | 600ps | 800ps |
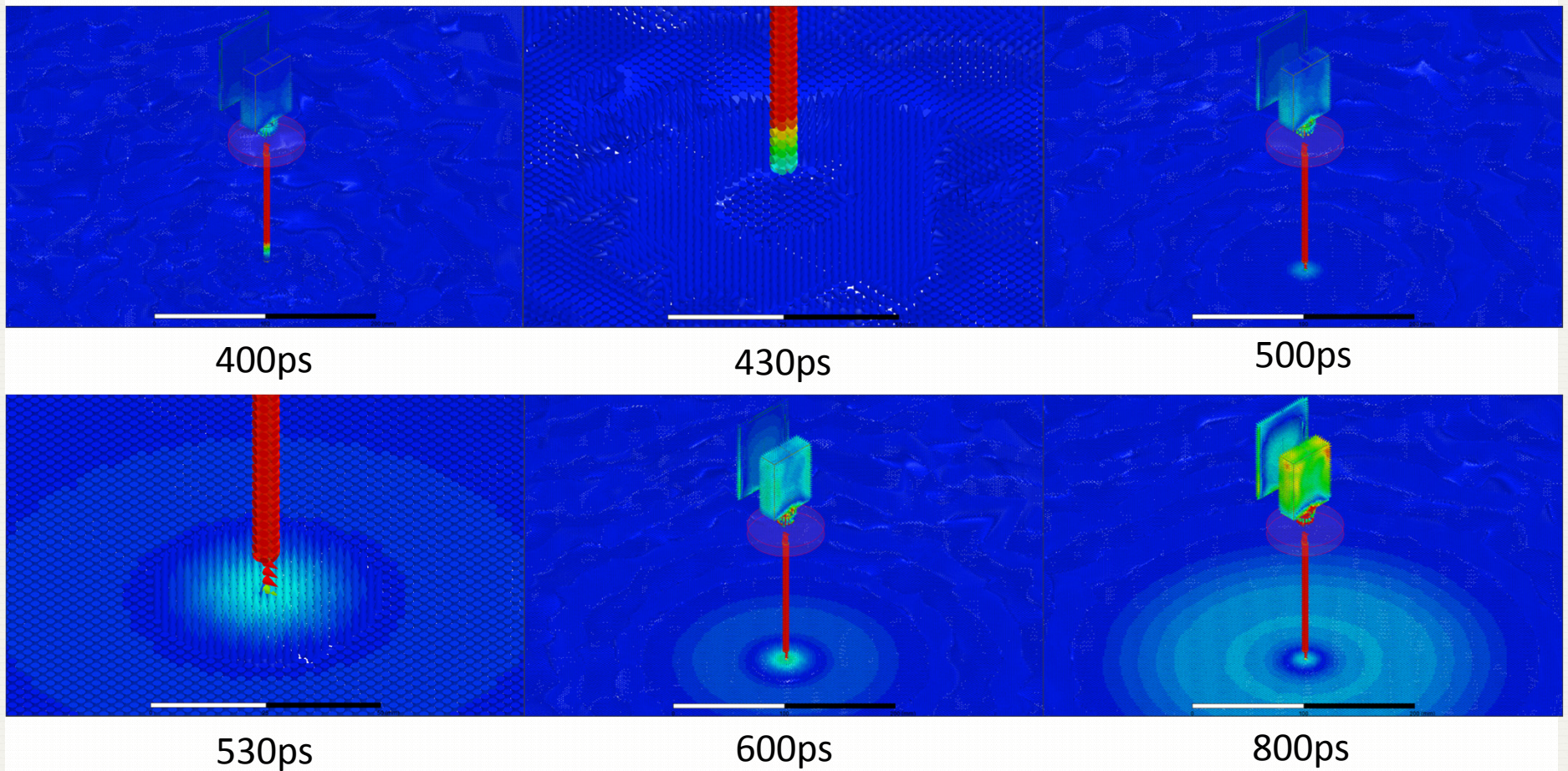
ESD and ESD Modeling

- **5KV ESD Discharge Current waveform**

——— : Simulation

· · · · : IEC 61000-4-2 (5kV)

Applied Voltage (kV)	Peak Current (A) IEC 61000-4-2 (ESD Test)	Peak Current (A) Simulation Results
2	7.5	7.75
4	15	15.5
5	18.75	19.3
6	22.5	23.25

18.75A

19.3A
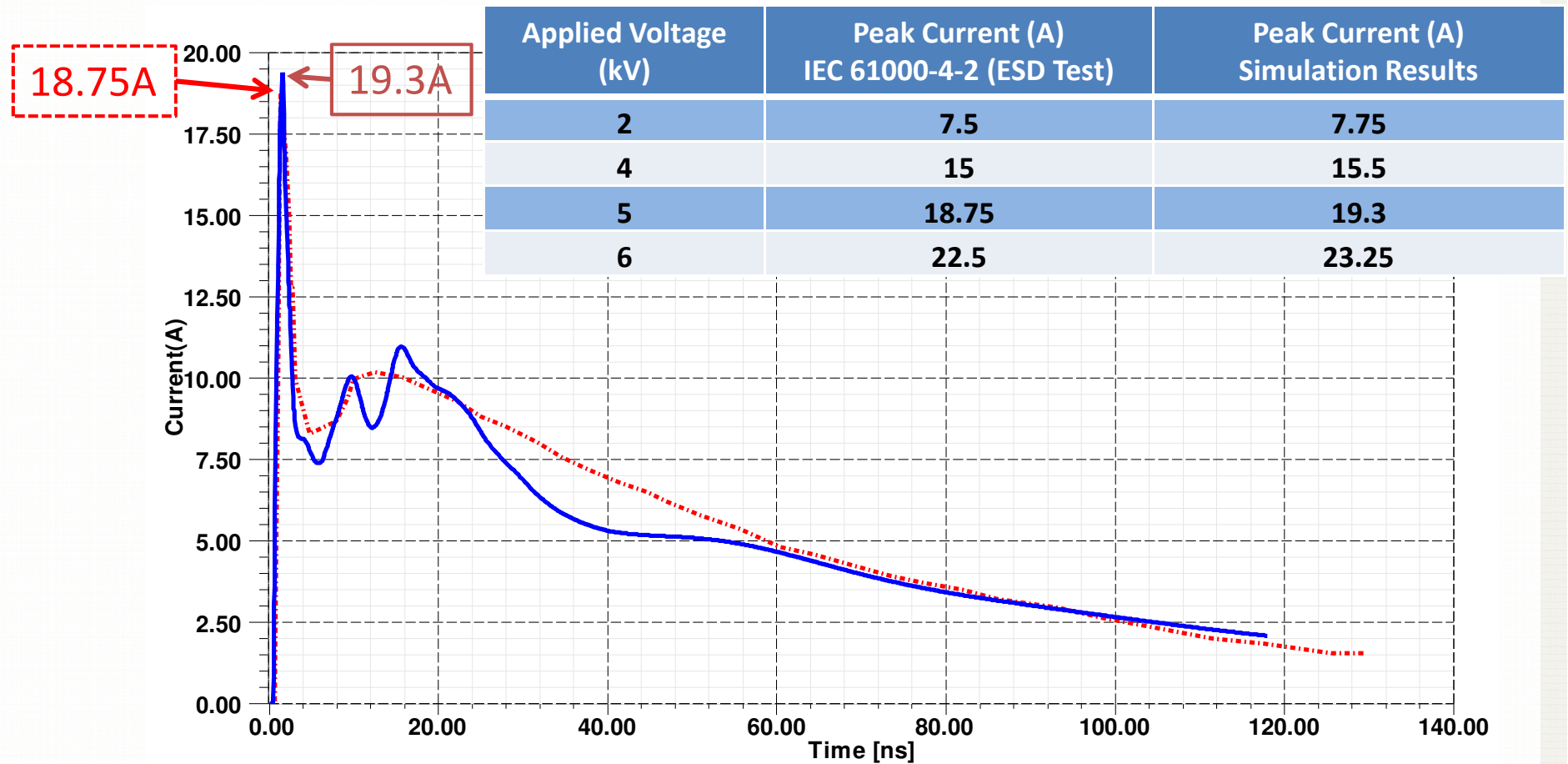
ESD and ESD Modeling

- **TVS Diode Modeling**

  - TVS(Transient Voltage Suppressors) diode modeling parameters

  - DesignerSI library support TVS parameters.
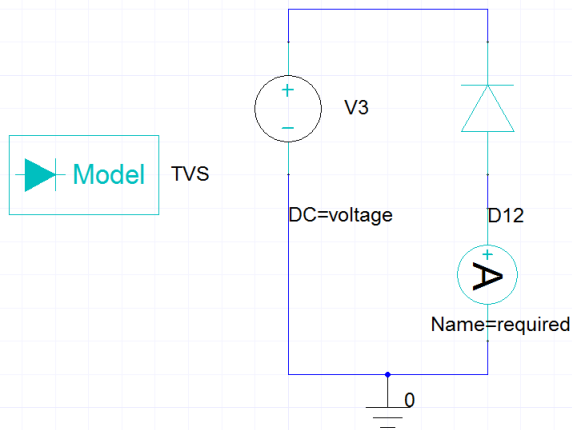
Parameter
IS
BV
VJ
RS
IBV
CJO
TT
M
N
EG

Parameter Values | General | Symbol | Property Displays

○ Value   ○ Statistics

Name	Value	Unit	Evaluated V...	Description
LEVEL	5		5	
ModelName	TVS			Name of device model
IS	2e-012		2e-012	Saturation current per unit area (JS) (A/m^2)
N	1.1		1.1	Emission coefficient
IBV	0.001	A	0.001A	Current at breakdown voltage
BV	9.2	V	9.2V	Magnitude of reverse breakdown voltage
FC			0.5	Coefficient for forward bias depletion capacitance
CJ0	5.6e-011	farad	5.6e-011farad	Zero bias PN junction capacitance
VJ	0.6	V	0.6V	Built-in junction potential
M	0.23		0.23	PN junction grading coefficient

No Snapback effect on this model
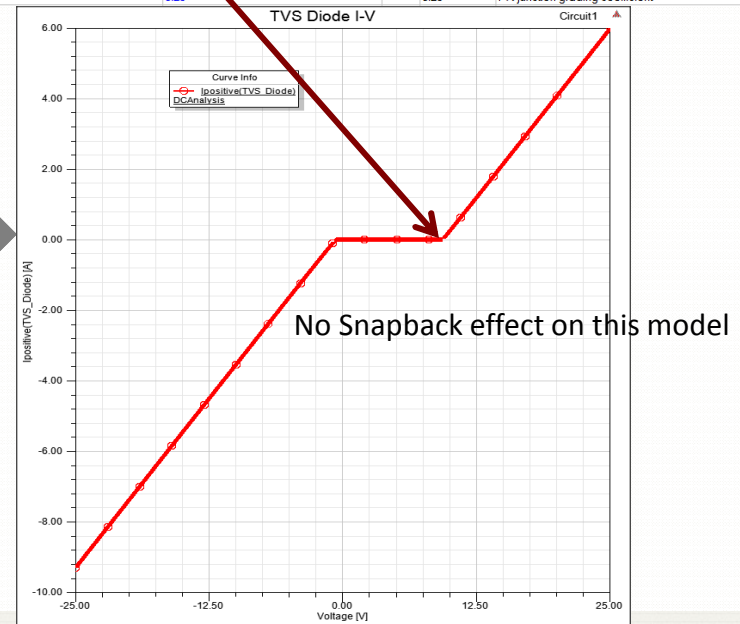
ESD and ESD Modeling

- **TVS Diode Modeling Example**
  - Panasonic Rclamp0821p Spice Model
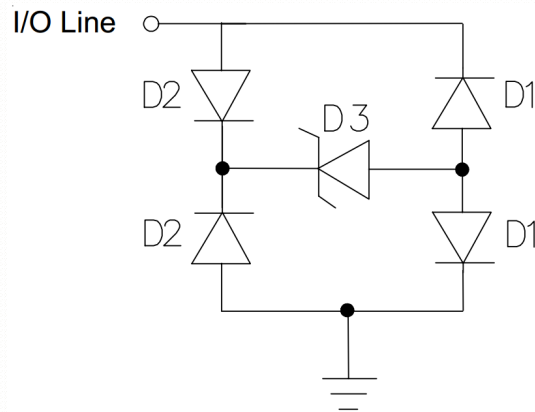
RClamp0821P Spice Model

Table 1 - RClamp0821P Spice Parameters				
Parameter	Unit	D1 (LCRD)	D2 (LCRD)	D3 (TVS)
IS	Amp	1.0E-20	1.0E-20	2.0E-12
BV	Volt	100	100	13.7
VJ	Volt	0.7	0.7	0.6
RS	Ohm	0.458	0.89	0.8
IBV	Amp	1E-3	1E-3	1E-3
CJO	Farad	0.4E-12	0.4E-12	56E-12
TT	sec	2.541E-9	2.541E-9	2.541E-9
M	--	0.01	0.01	0.23
N	--	1.1	1.1	1.1
EG	eV	1.11	1.11	1.11

TVS,
Panasonic Rclamp0821p Spice Model
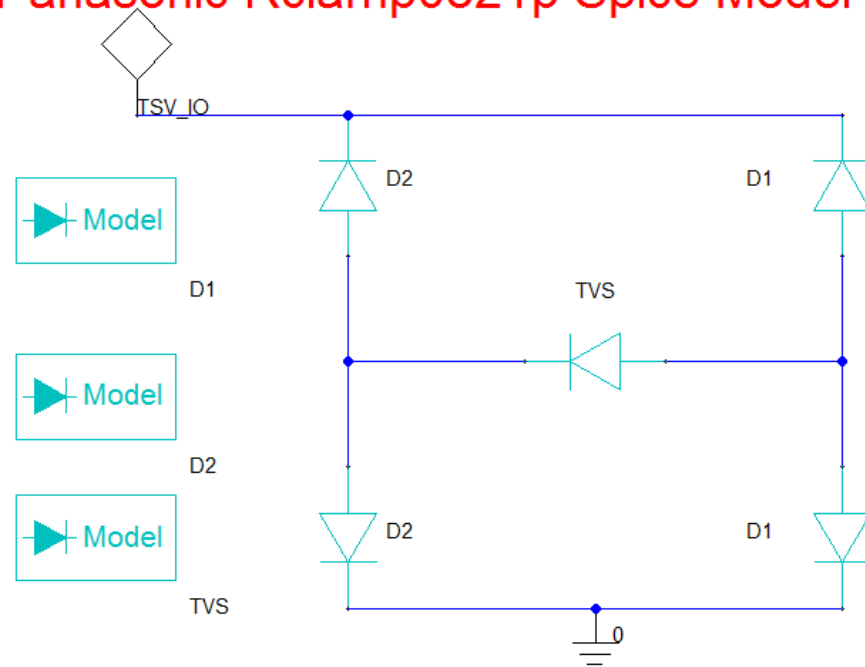
ESD and ESD Modeling

- **ESD Filter Modeling**
  - CMD ESD Filter : Full (Triple) LC block with substrate & diode effects
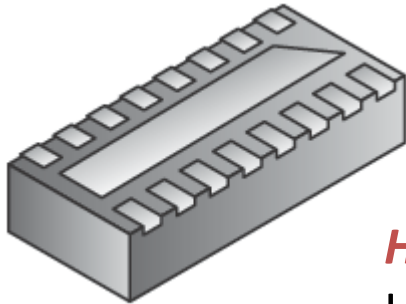
HFSS + Designer Dynamic Link Design
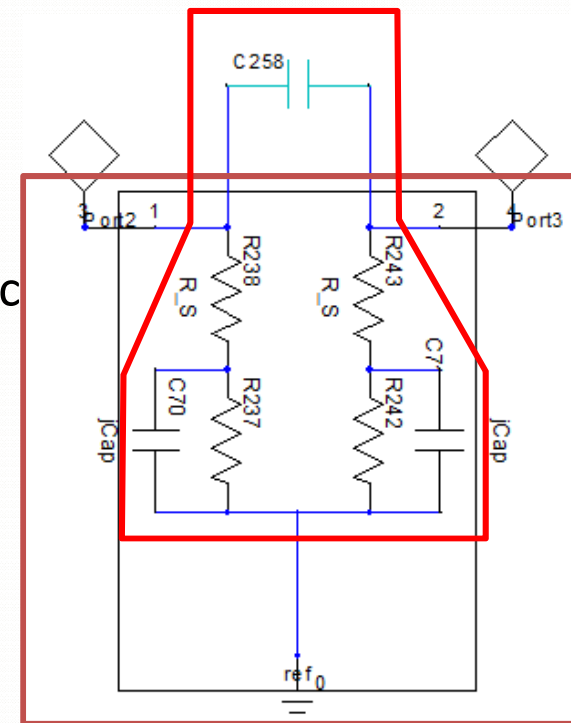
ESD and ESD Modeling

- **ESD Filter Modeling**
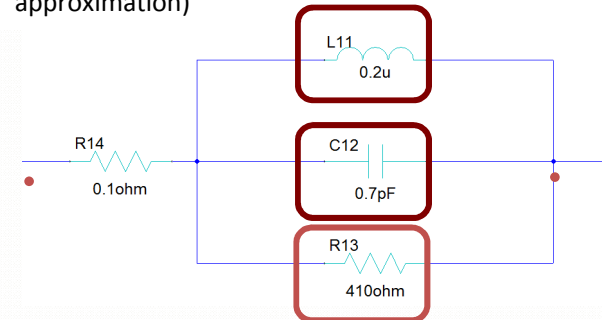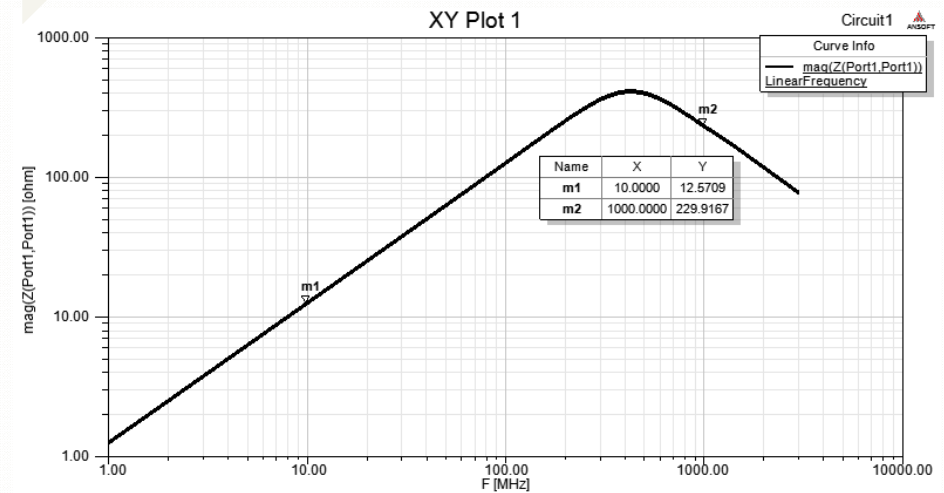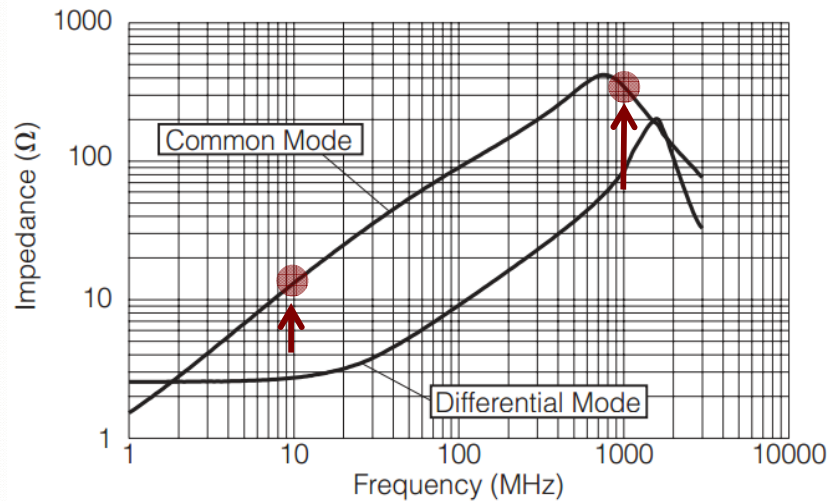 - Simulation vs. ESD Filter Measurement
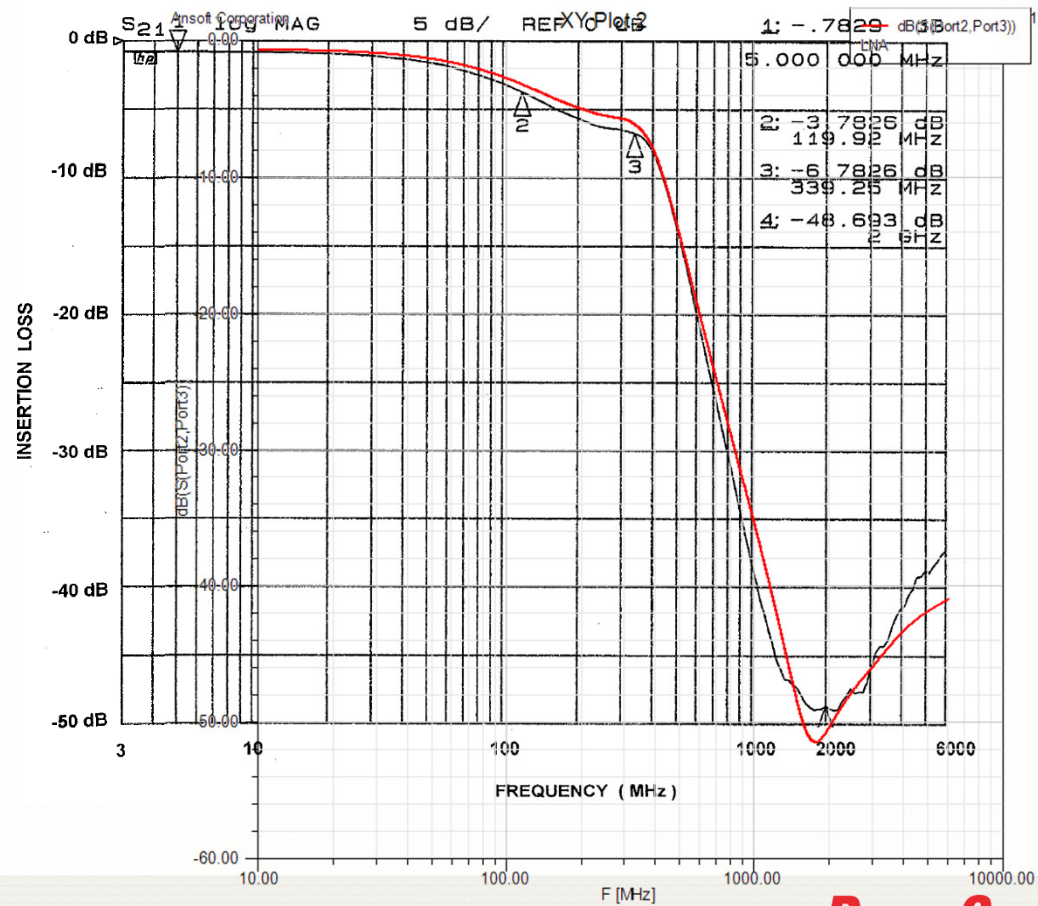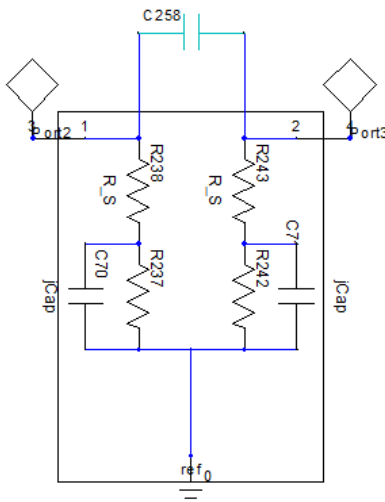
ESD and ESD Modeling

- ## Common mode EMI/Noise Filter Modeling
  - EMI Filter in this simulation will have frequency - dependant equivalent circuit.

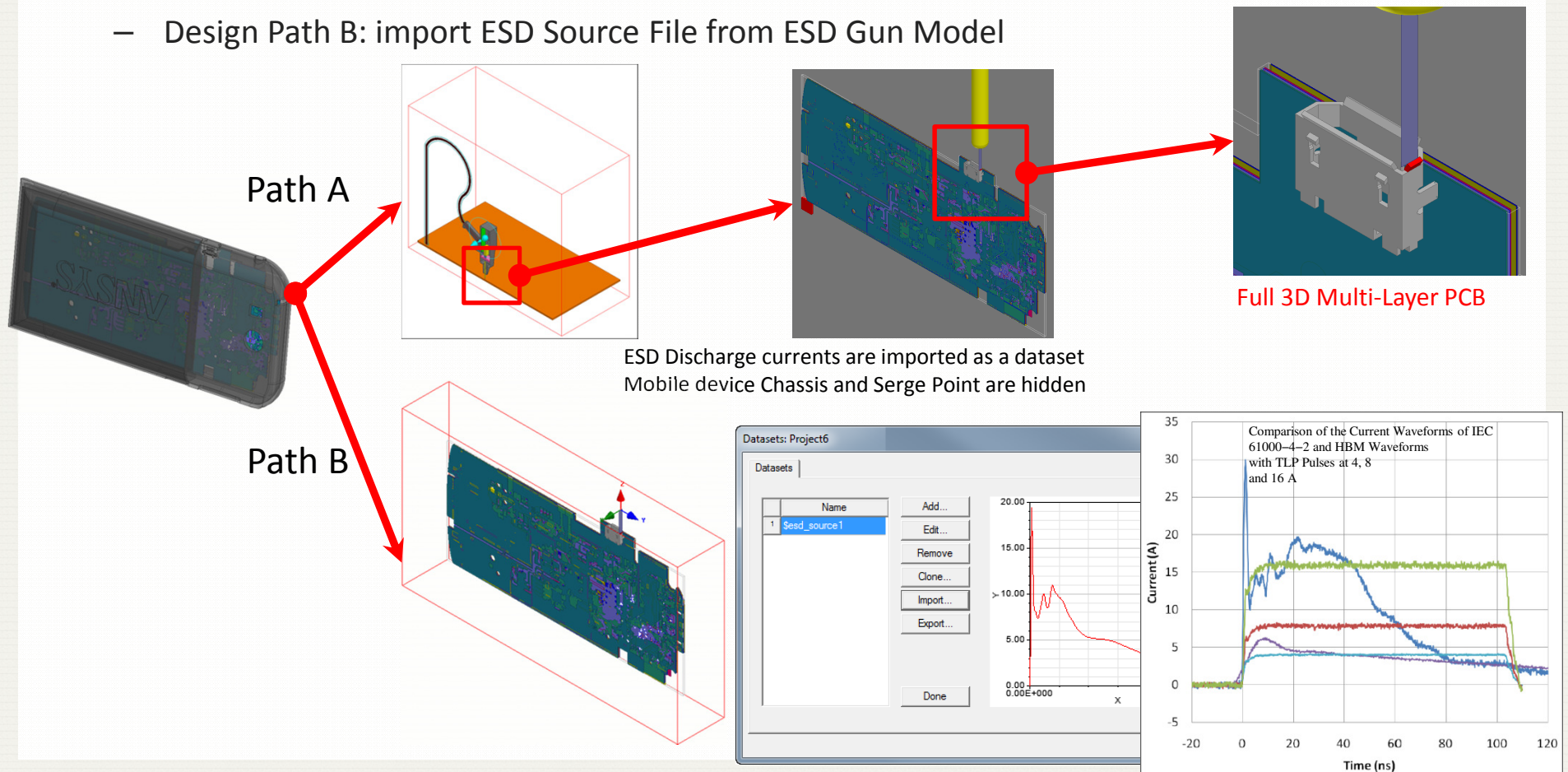Single-ended equivalent model for common mode (Simple approximation)

L11
0.2u

R14
0.1ohm

C12
0.7pF

R13
410ohm

● EXC24CE900U

XY Plot 1

Name	X	Y
m1	10.0000	12.5709
m2	1000.0000	229.9167

Curve Info

—— mag(Z(Port1,Port1))
LinearFrequency

Circuit1

System-level ESD design

- **System-level ESD design**
  - Design Path A: with ESD Gun Model
 - Design Path B: import ESD Source File from ESD Gun Model

Path A

Path B

Full 3D Multi-Layer PCB

ESD Discharge currents are imported as a dataset
Mobile device Chassis and Serge Point are hidden

Comparison of the Current Waveforms of IEC 61000–4–2 and HBM Waveforms with TLP Pulses at 4, 8 and 16 A

Micro USB Connector Device on Mobile PCB

- **Micro USB Connector Device on Mobile PCB**
  - ESD injection on Micro USB Connector
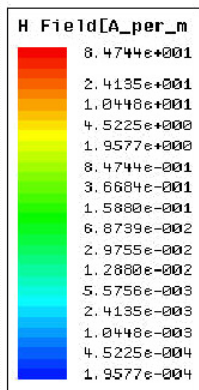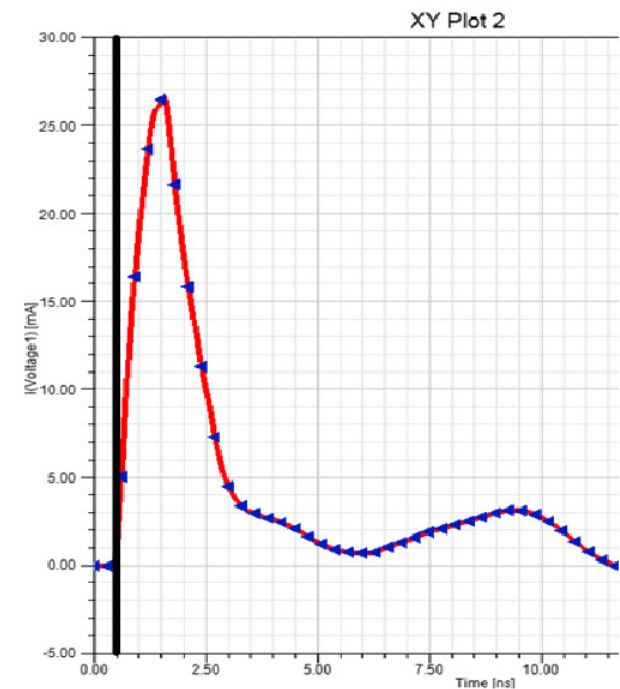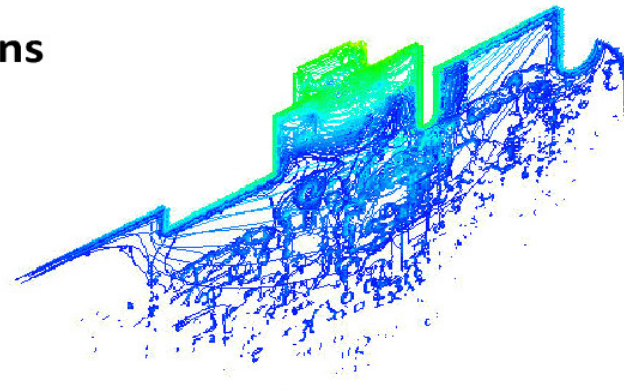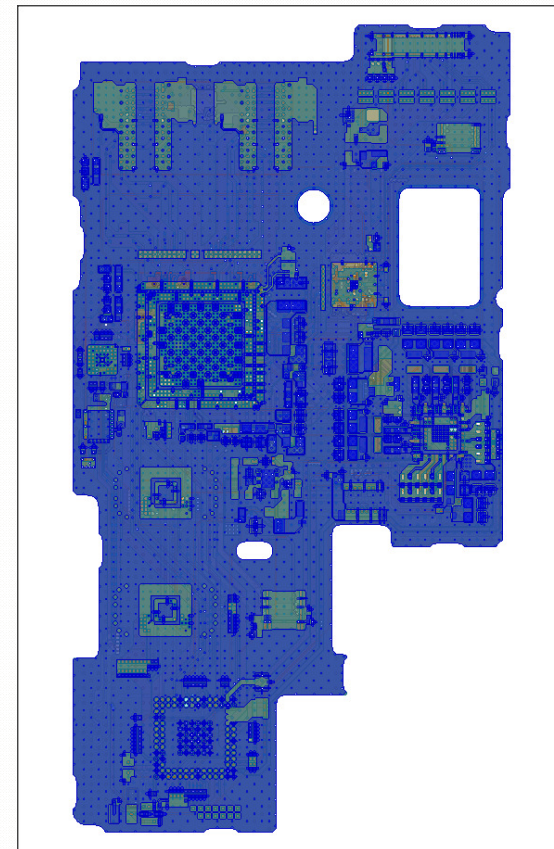
System-level ESD propagation modeling
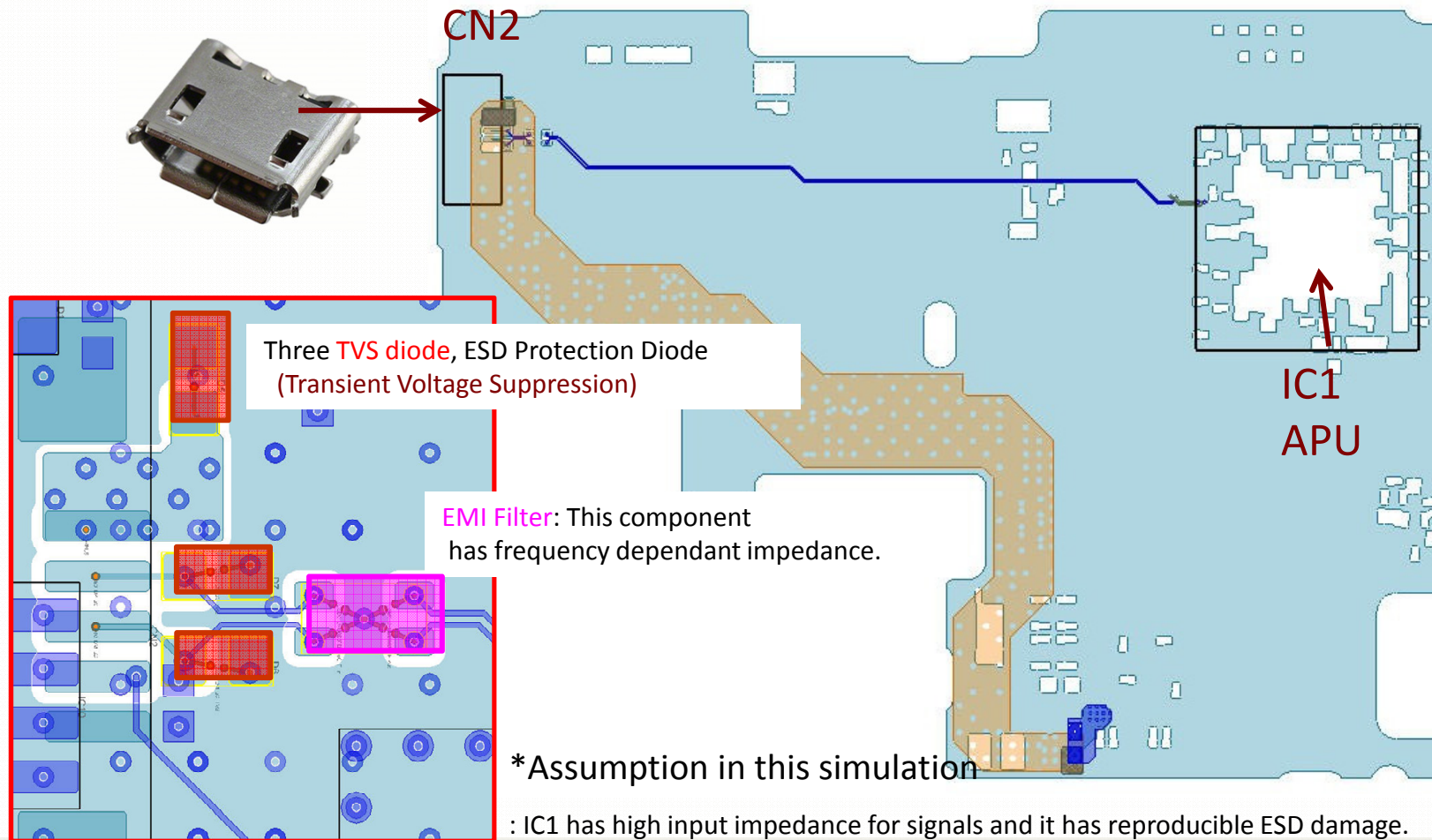
- Mobile System-level ESD propagation modeling

VBAT,   VCC1.2v,   VCC1.8v,   VCC2.9v,   VCC3.3v,   VAP's & Memory Power,   VUSB   And Ground
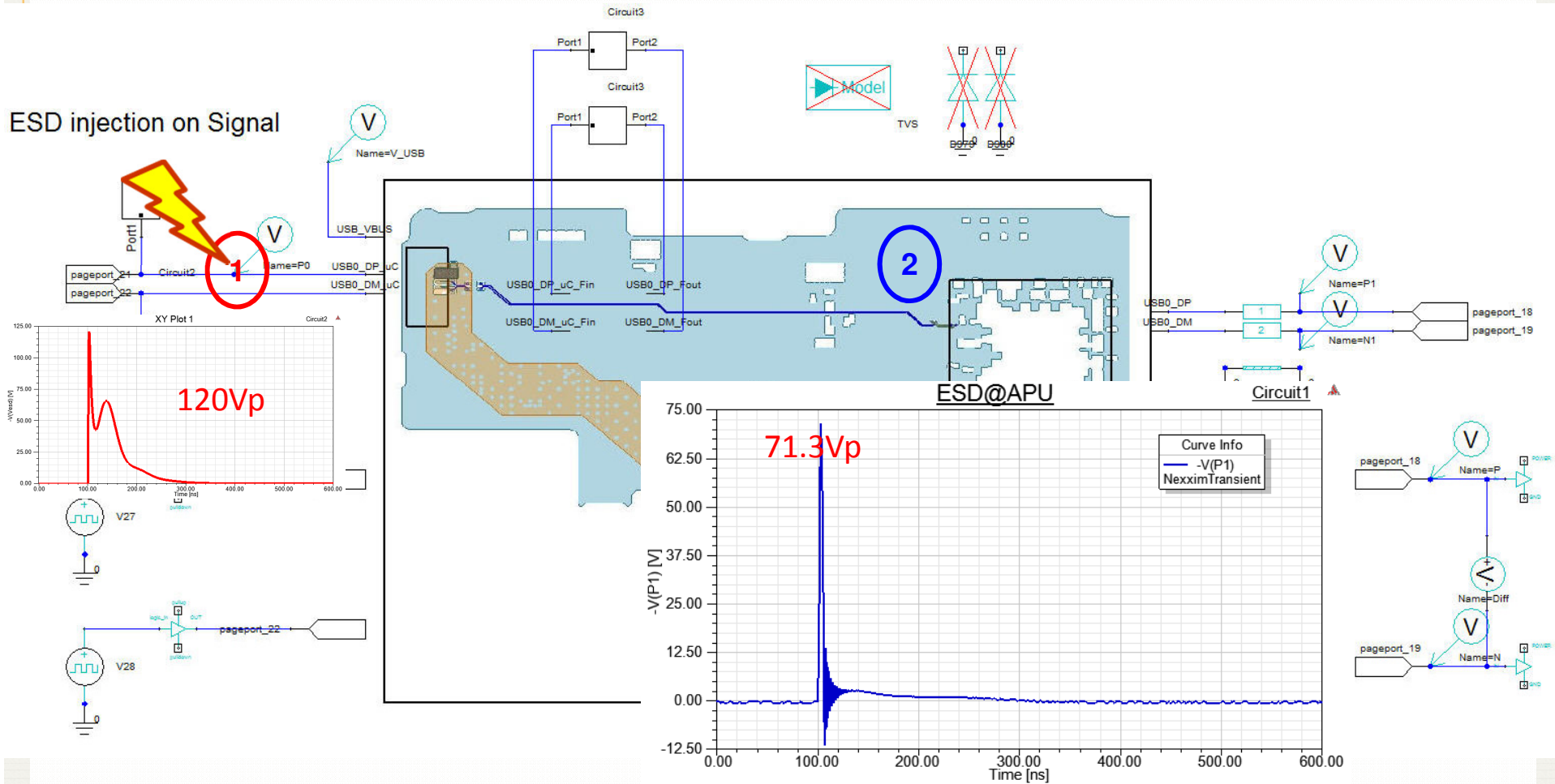
System-level ESD propagation modeling
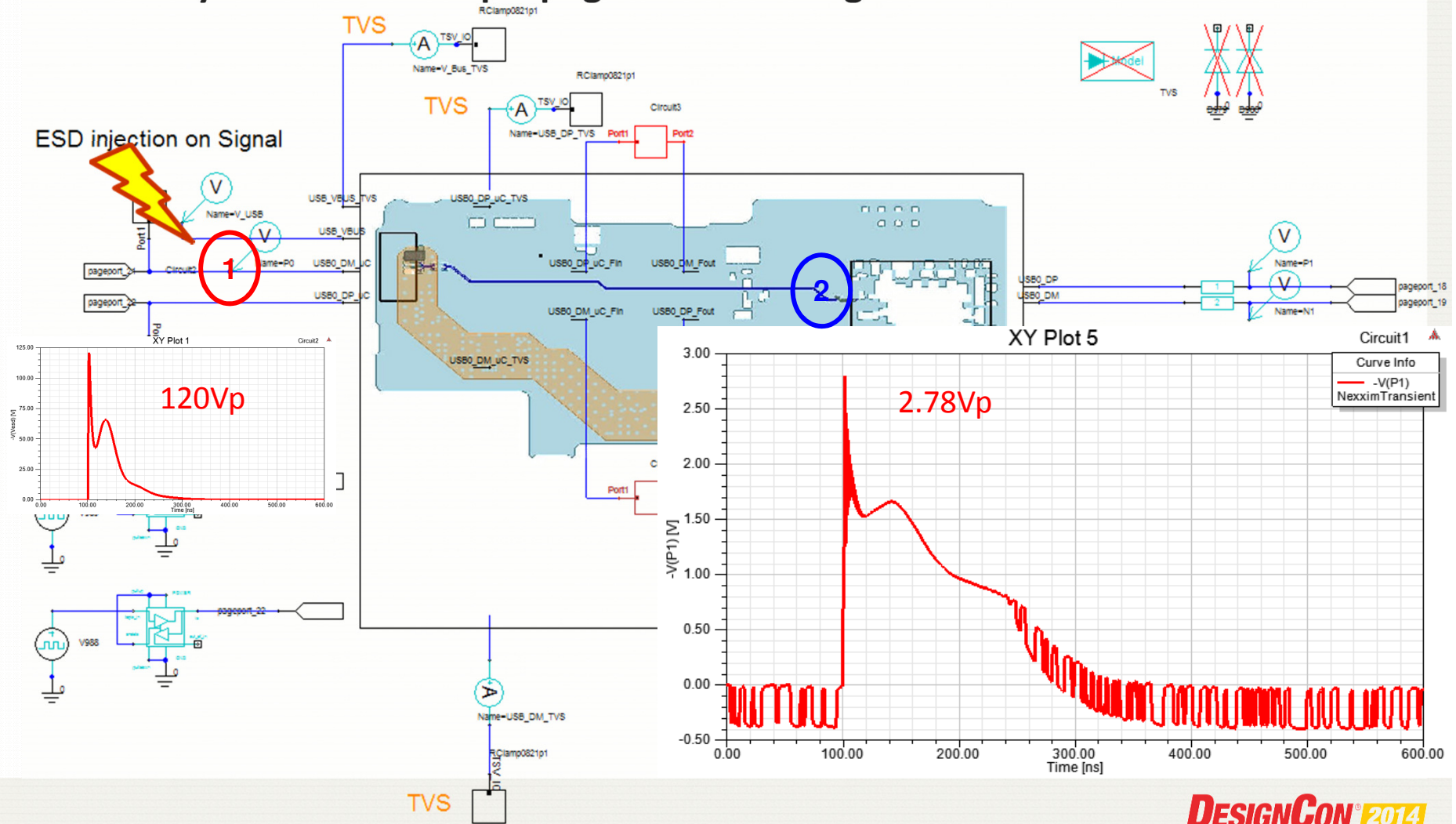
- **Mobile System-level ESD propagation modeling**

CN2

Three TVS diode, ESD Protection Diode
(Transient Voltage Suppression)

EMI Filter: This component
has frequency dependant impedance.

IC1
APU

*Assumption in this simulation

: IC1 has high input impedance for signals and it has reproducible ESD damage.

System-level ESD propagation modeling

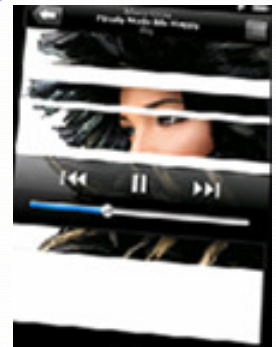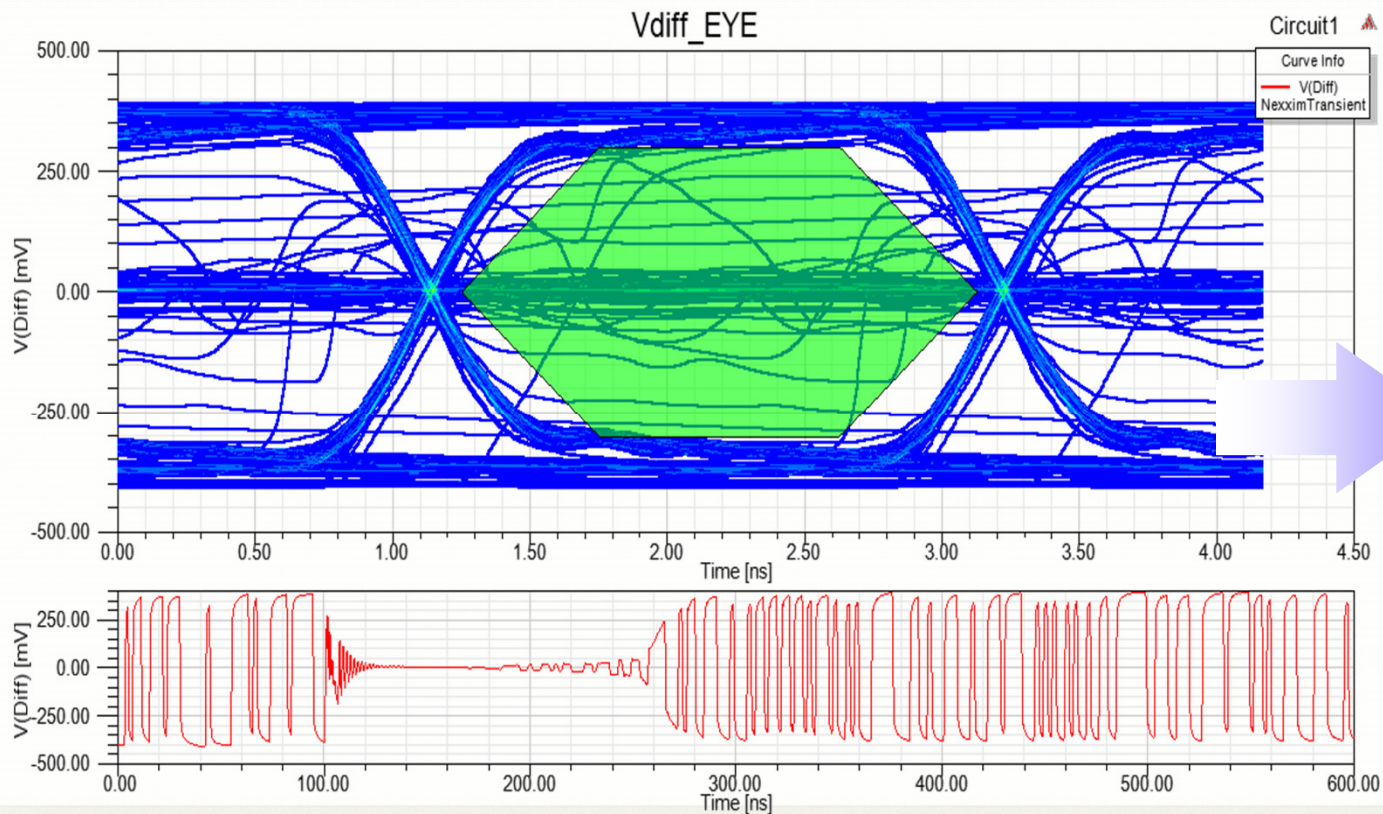- **Mobile System-level ESD propagation modeling**

System-level ESD propagation modeling

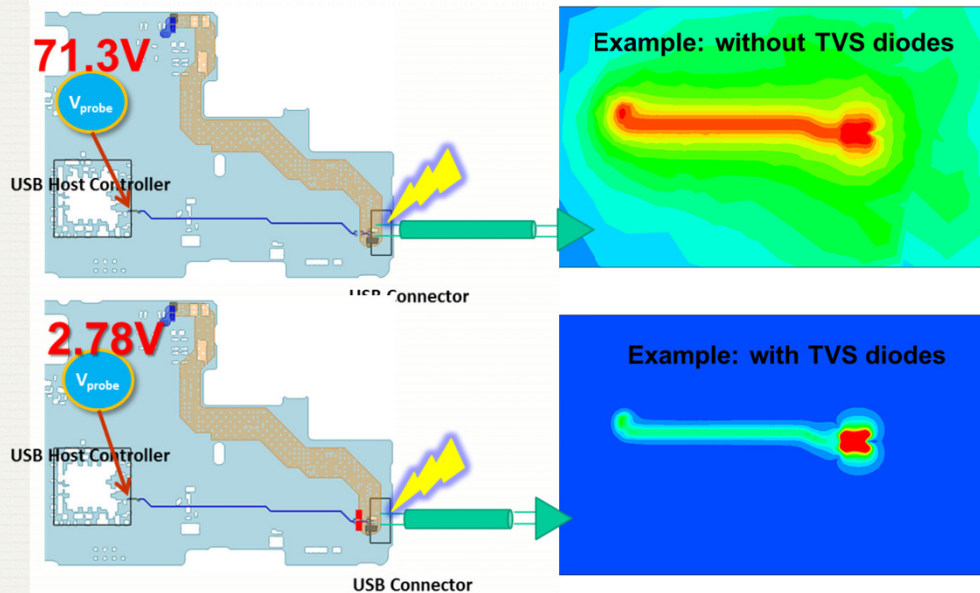- Mobile System-level ESD propagation modeling

System-level ESD propagation modeling

- **Mobile System-level ESD propagation modeling**
  - ESD effect on Signal
    - Soft Error
      - Any error that can be cured by resetting the system (Logical errors: bit error, false reset)
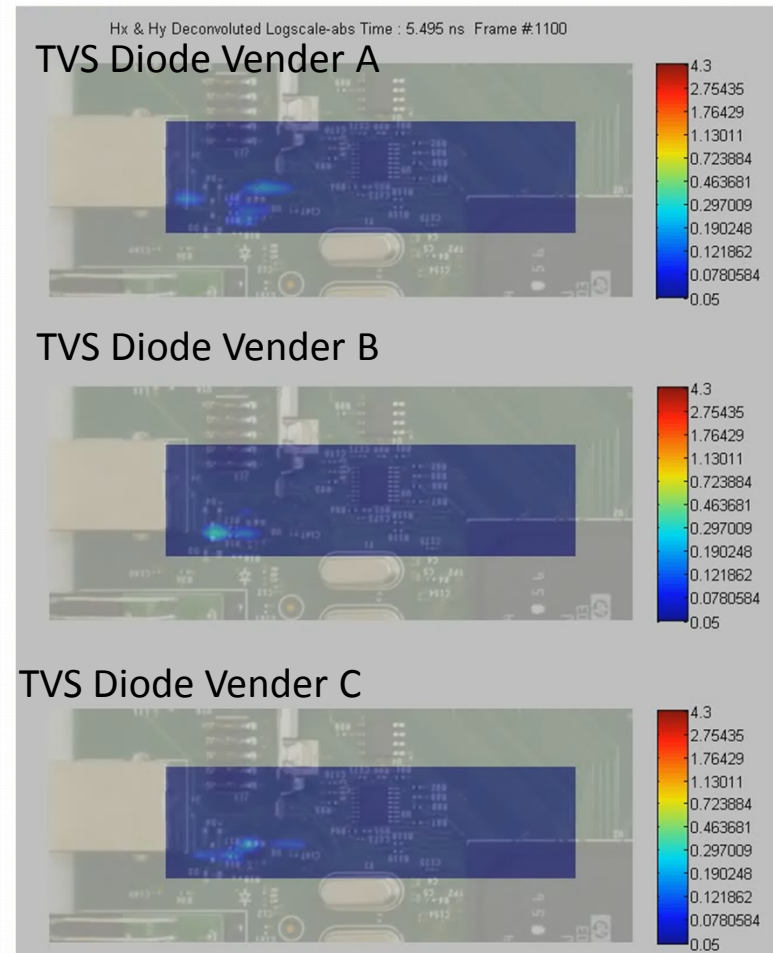
System-level ESD propagation modeling

- **TVS Diode Effect on High-speed USB Signal**
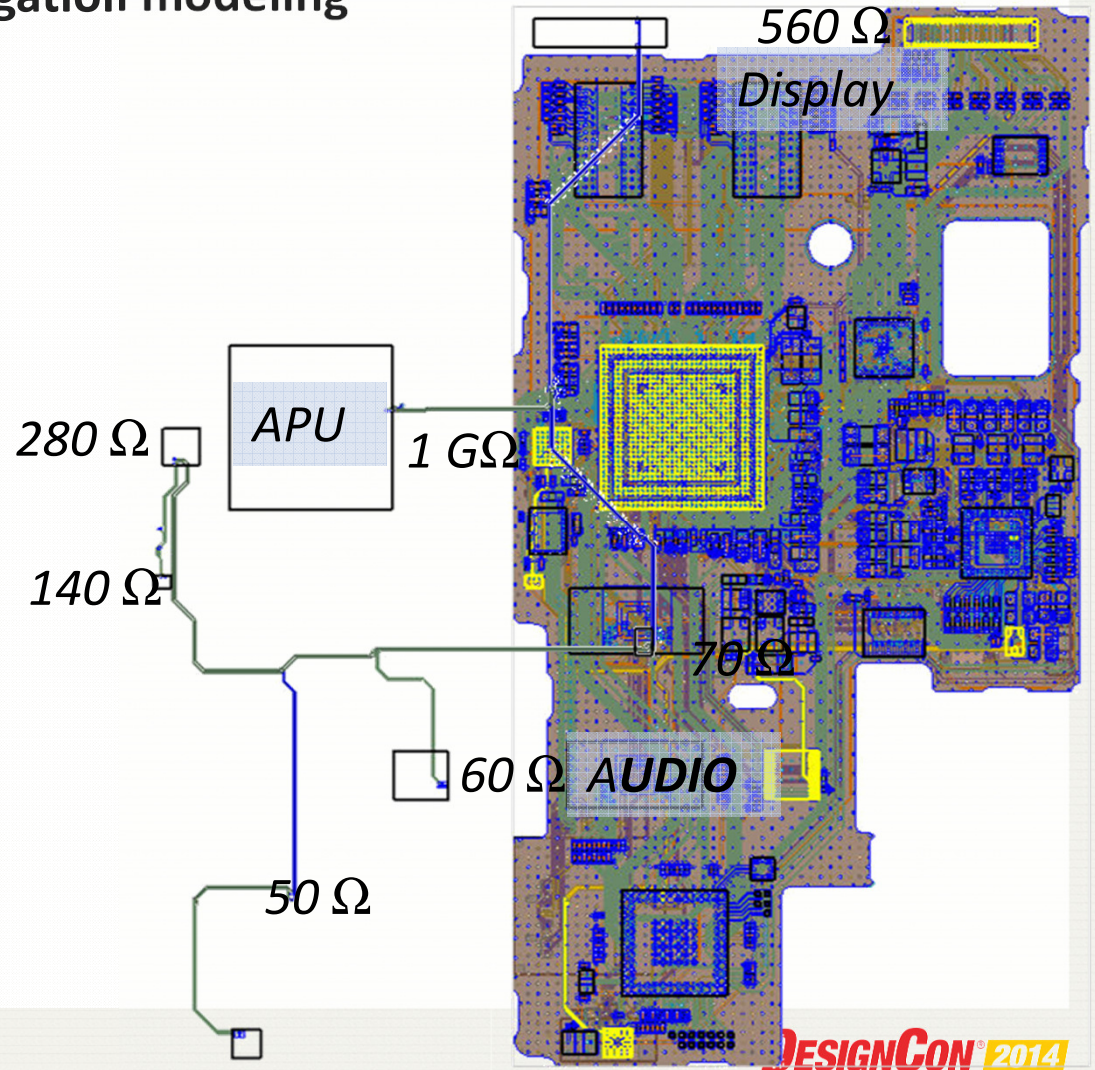 - NF scan Simulation Results

71.3V

2.78V

Example: without TVS diodes

Example: with TVS diodes

NF Scan Measured Example →

Hx & Hy Deconvoluted Logscale-abs Time : 5.495 ns Frame #1100

TVS Diode Vender A

TVS Diode Vender B

TVS Diode Vender C

System-level ESD propagation modeling

- Mobile System-level ESD propagation modeling

560 Ω Display

APU

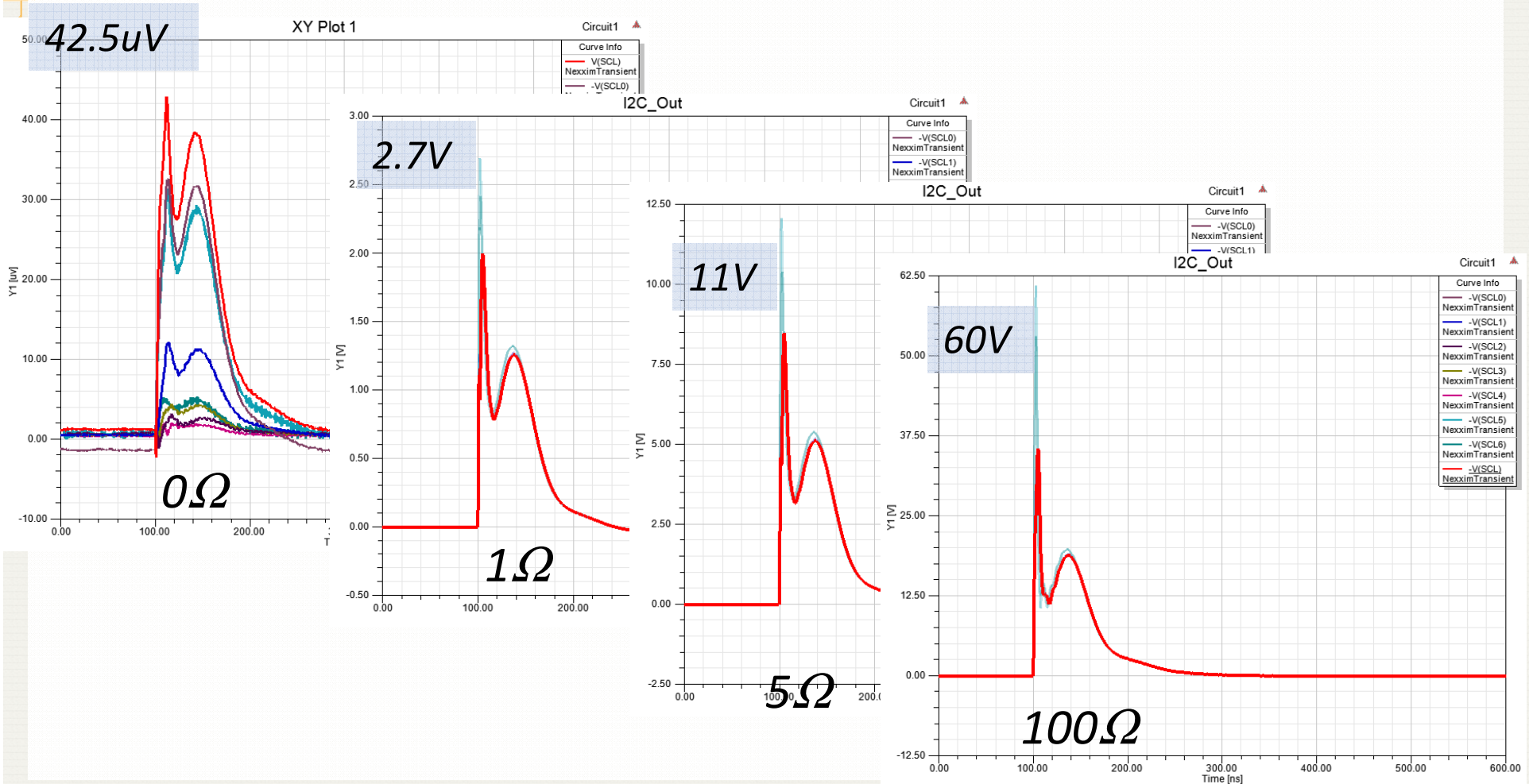280 Ω

1 GΩ

140 Ω

70 Ω

60 Ω AUDIO

50 Ω

System-level ESD propagation modeling

- Reference GND effect(0W, 1W, 5W, 100W)
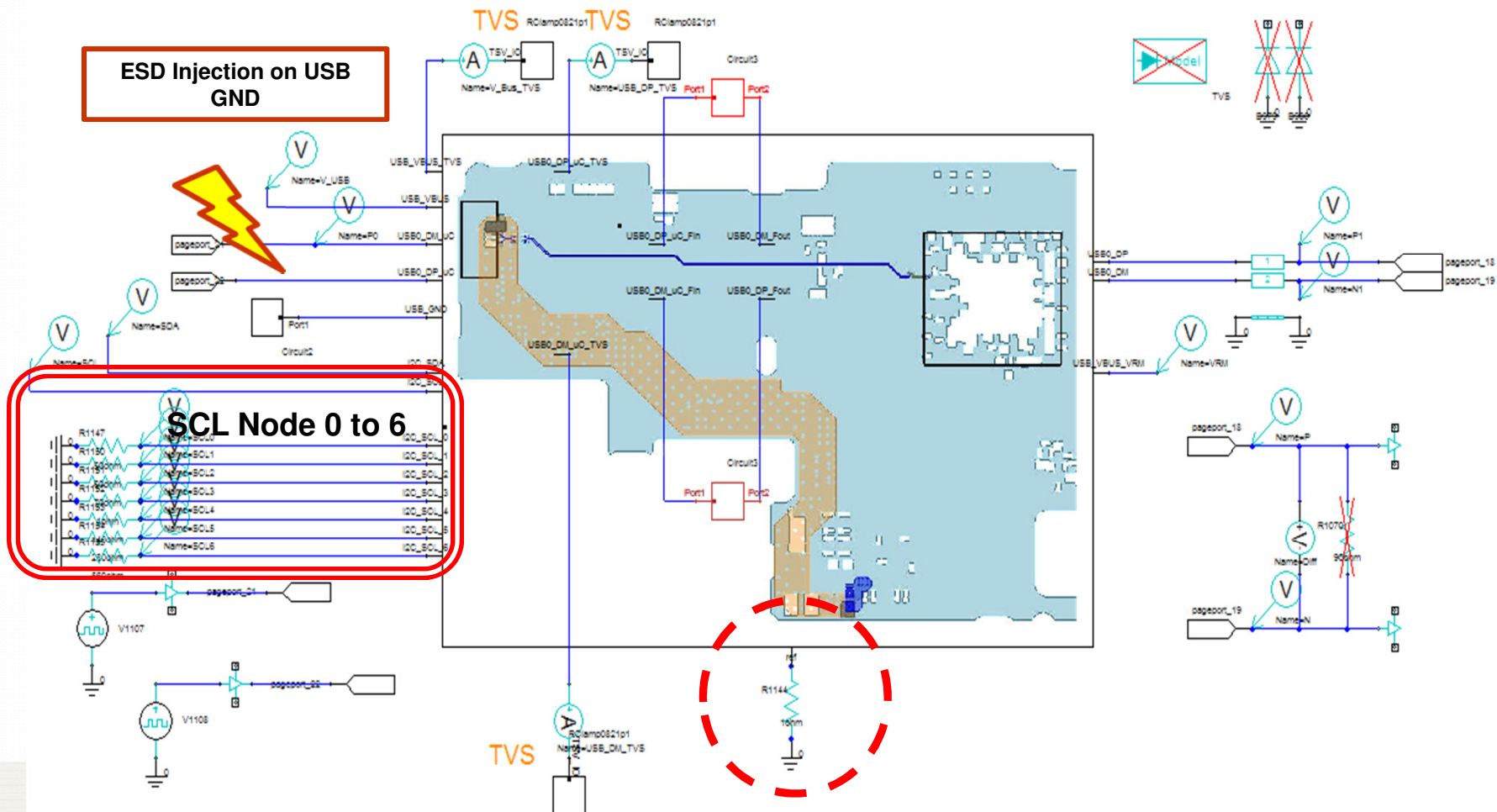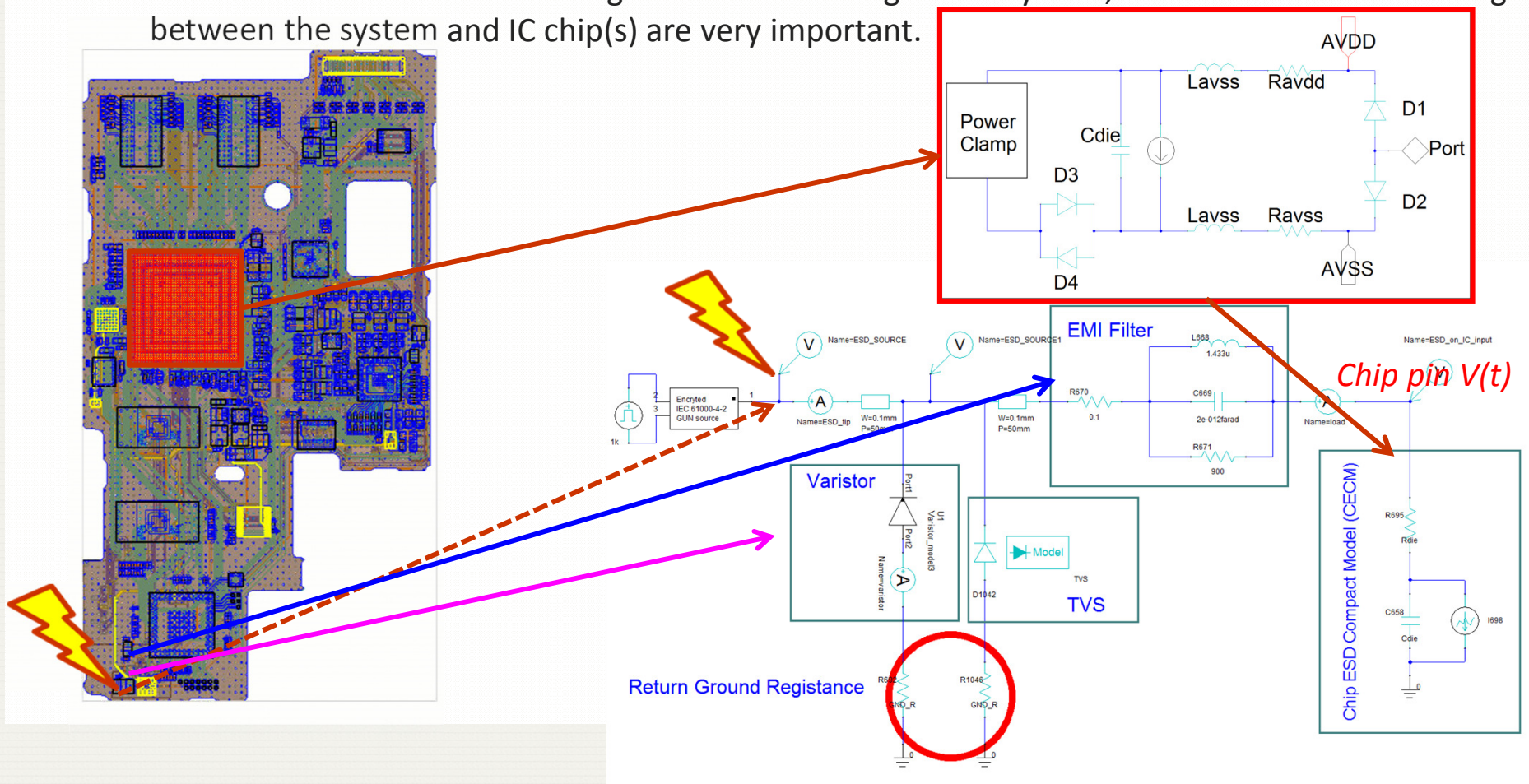
System-level ESD propagation modeling

- Reference GND effect(0W, 1W, 5W, 100W)

System-level ESD propagation modeling

- **Mobile System-level ESD propagation modeling**
  - Outline a comprehensive Chip-Package-System ESD simulation methodology that particularly addresses the interface modeling between the ESD gun and system, and the interface modeling between the system and IC chip(s) are very important.

System-level ESD propagation modeling

- **Chip Pin V(t) Response w/ Different Cdie**
  - Chip pin V(t) response with different chip Cdie to provide guidance on the effectiveness of ESD protection on PCB (or system)
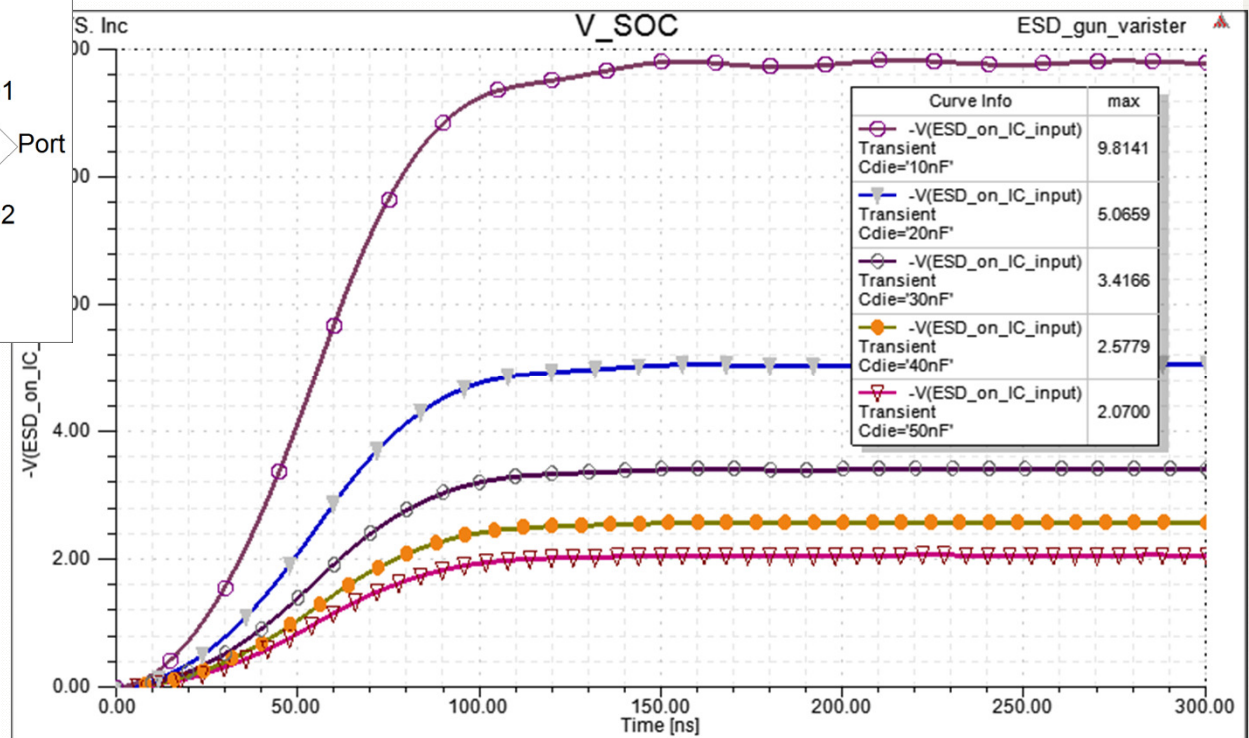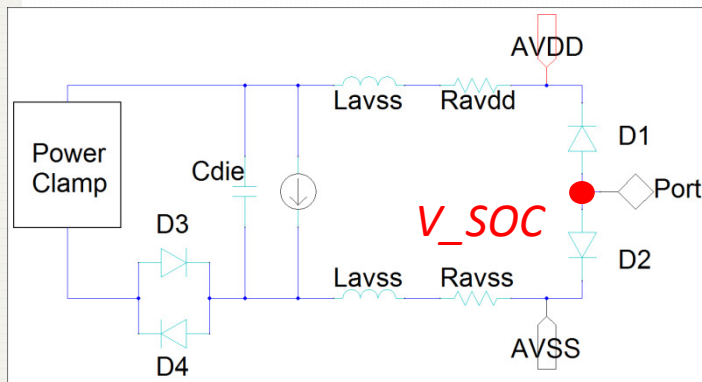
Conclusion

- Comprehensive study for ESD events by using "Chip-Package-System ESD Analysis "

  - "Frequency dependent component such as Common Mode Filter & TVS Diode with I-V characteristics" can be modeled and used as a part of system-level ESD simulation.

  - Chip pin V(t) and I(t) curve are identified based on chip Cdie, Rdie value in CECM Model.

  - 3D EM solver provides the robustness in analyzing transition of spike current with visualization.

- ESD zap gun measurement result correlates well with simulated zap current waveform