A Test Structure for the EMC Characterization of Small Integrated Circuits

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***Abstract*— This paper deals with the measurement methods used to evaluate the electromagnetic (EM) emission of integrated circuits (ICs) as well as their susceptibility to EM interference. In particular, the micro stripline method, which is prescribed by the International Electrotechnical Commission (IEC 62132-8), is considered and its limitations for the characterization of ICs encapsulated in small packages are highlighted. Wanting to address such issues, a new EM guiding structure that shows an enhanced coupling with the device under test in the frequency range 800 MHz–3 GHz is proposed. A circuit model of the test structure based on lumped elements that allows one to perform circuit analysis with SPICE-like simulators is proposed. It can also be used to check the effectiveness of the test bench before setting it up. The model has been validated comparing the scattering parameters obtained from simulations with those resulted from measurements carried out on a real test structure, which was designed and fabricated for this purpose.**

***Index Terms*— Electromagnetic compatibility (EMC) and interference, EM coupling, EM radiation effects, integrated circuit (IC) radiation effect, measurement standards, measurement techniques, modeling.**

I. Introduction

RECENT advances in semiconductor technology have made possible the implementation of most functions performed by electronic modules at the integrated circuit (IC) level. This has significantly reduced the number of components, but has brought also to address development and qualification issues at the IC level rather than at the module level. For example, the compliance to electromagnetic compatibility (EMC) limits, as defined by the International Standards [1], nowadays can be obtained using ICs compliant to EMC limits defined at the IC level. In this contest, the methods used to evaluate the EM emission delivered by an IC and its susceptibility to the EM interference (EMI) play a key role, and this explains the interest on this topic.

In the last decades, the problem of measuring the EMC performance of ICs have been addressed by several authors. In [2], a GHz transverse electromagnetic cell (GTEM) cell is used to measure the susceptibility of a field programmable analog array IC to radiated EMI. In that work, the device under test was mounted on a printed circuit board (PCB), which was inserted into a GTEM. The EM field induced by an RF source feeding the GTEM couples with the PCB interconnects causing DUT operation failures. In such a test, the EMC performance of the IC depends on the test board features (PCB interconnects, passive elements and parasitics), and the wiring connecting the test board to the GTEM technical panel. In other words, if the same IC had been inserted in another test board with different features, its EMC performance would have been much different. Other authors faced the topic from a different perspective: instead of measuring the EMC performance at the system or module level, they embedded a sampler into the DUT to provide an external acquisition board with the samples needed to reconstruct the disturbance waveform at the chip level. This solution applies regardless of the module which the DUT is a part of, but as a drawback the DUT must include a part of the measuring circuits [3].

Over the years, several measurement techniques were developed and some of them were chosen and optimized to be included in the IEC and SAE standards [4]–[7]. Among them, those dealing with the measurement of EM emissions are presented in [4]. This document is made up of eight sections, each one describing a measurement technique suitable to evaluate either conducted or radiated emissions. From their introduction, such methods have been reviewed and improved to address specific issues. For instance, Musolino [8] showed that the IC conducted emission can be measured using a directional coupler embedded in the same test board hosting the device under test (DUT). Other authors focused on the test structure used to perform radiated EMC tests.

Radiated emission tests were originally carried out using the mini TEM cell [9], [10] but its limited bandwidth and the poor coupling with the DUT had led to develop the IC stripline [11], which became a standard afterward [4]. Similar considerations hold for the methods used to measure the susceptibility of ICs to EMI [5]. Conducted susceptibility tests are usually performed referring to the direct power injection (DPI) method, which prescribes to apply the interference to one DUT's pin at time while monitoring the device outputs. The interference level must be increased until the operation failures occur or a maximum interference level is reached. In addition, this method has been the object of investigations aimed to reduce the complexity of the test setup and to improve repeatability. In [12], it is shown that the directional coupler and the power meter needed to measure the RF power injected into the IC can be replaced by a sense resistor and an amplifier included in the test board. However, it is worth

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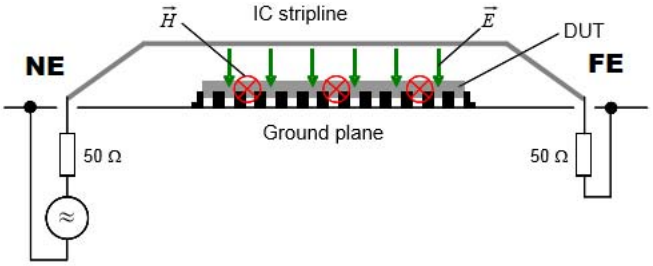

Fig. 1. Cross-sectional view of the stripline as shown in IEC 62132-8 [5].

noticing that the DPI method is appropriate to investigate the cause of failure but it is not for reproducing real operating conditions, in which the IC is affected by the interference at all pins, simultaneously.

This last case is usually covered referring to radiated susceptibility test methods like those presented in [5]. In such tests, the IC is exposed to the EM field propagated by the guiding structure, so that its nominal signals are corrupted by the interference collected by the IC package interconnects. The guiding structures for injecting the interference are the same used for measuring the IC radiated emission. In particular, the IC stripline described in IEC 62132-8 is made up of a properly shaped metal plate running over the test board ground layer. The IC under test is placed between the top metal plate and the PCB ground layer, and its terminals (pins) are connected through vias to the ancillary circuits, which are needed to make the DUT work. The stripline is designed to propagate the TEM mode only and to show 50-Ω characteristic impedance in the frequency range of interest. Therefore, to minimize the impedance mismatch, the near-end (NE) termination of the stripline is driven by a 50-Ω RF source and the far-end (FE) one is loaded by a 50-Ω resistor. This structure has been extensively investigated by several authors [11], [13]–[16], who showed among others, how the IC package lead frame affect the stripline mismatch, thus, the results of susceptibility and emission tests. In particular, they showed that the larger the package is, the greater the coupling of the IC active components with the stripline will be. Therefore, two identical ICs (silicon die) encapsulated in two packages of different sizes show different levels of susceptibility to EMI. In light of the above considerations, the results of EMC tests carried out on different devices can be compared to one another only if they are encapsulated in the same package, show the same pinout and perform the same functions.

Over the time, the size of IC packages has decreased dramatically, as it is clearly shown in Fig. 2. The strong demand for ICs showing the smallest feasible packages is a topical issue, given the miniaturization of consumer devices, with even more functionalities (e.g., smartphones and tablets). Furthermore, small size packages reduces the impact of parasitics on the IC electrical performances [17]. And vice-versa, this trend toward the miniaturization has made the IEC 62132-8 standard less and less effective because the stripline-to-DUT coupling, which is exploited in such tests, decreases with the package

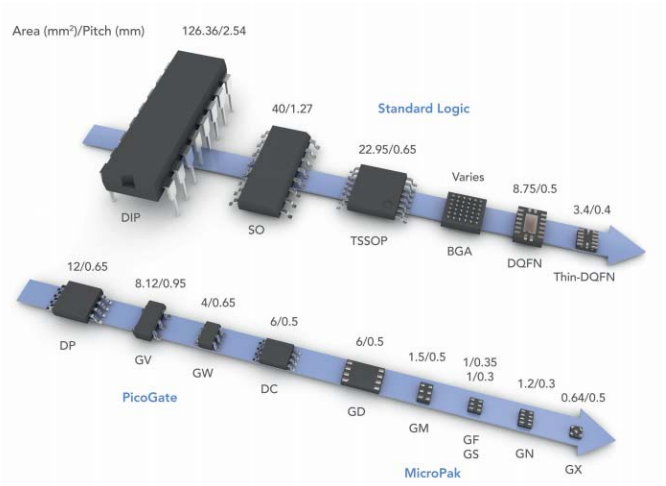

Fig. 2. IC package evolution.

shrinking. In view of these considerations, this paper proposes a new coupling structure that can be inserted in the stripline to address this problem. The paper is organized as follows. Section II reviews the IC stripline method described in IEC 62132-8 and introduces a new solution suitable for small packages. A circuit model of the proposed structure suitable to perform circuit analysis with SPICE-like simulators is presented in Section III. Finally, the experimental characterization of the proposed solution and the validation of the extracted model are presented in Sections IV and V. Concluding remarks are drawn in Section VI.

II. Microstripline With Enhanced Coupling

According to IEC 62132-8, the IC stripline should be designed to propagate the TEM mode up to 3 GHz and to show a 50-Ω characteristic impedance. It should be fed by a 50-Ω RF source and matched at the opposite end by a 50-Ω load. Furthermore, its VSWR should be lower than 1.25 in the frequency range of interest with the DUT not inserted into the structure [5]. The stripline looks like a microstrip line with air as dielectric, which is shaped to show the above-mentioned features and to host an IC. This is the reason why its central body is usually sized referring to [5], therefore its characteristic impedance can be expressed as

$$Z = \frac{120 \cdot \pi}{\frac{w}{h} + 2.42 - 0.44 \cdot \frac{h}{w} + \left[1 - \frac{h}{w}\right]^6} \tag{1}$$

where h is the distance of the top conductor from the ground layer in the central region and w is the width of the top conductor in the same region.

The design of the two tapered regions connecting the stripline central body to its terminations is aimed to keep the longitudinal resonances above the maximum operating frequency of the cell, i.e., 3 GHz. This task is usually accomplished performing EM simulations.

Concerning the electric coupling of the guiding structure with the IC package, it depends on the parasitic capacitances between the package interconnects and the stripline top plate,

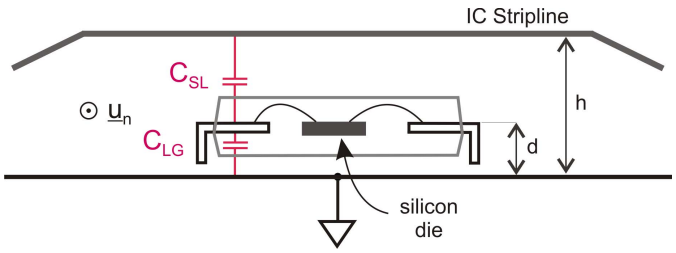

Fig. 3. Stripline to IC package coupling.

but also on the parasitic capacitances between the package interconnects and the ground layer underneath. Based on this, if the stripline is excited by an RF source, the voltage at the IC terminals due to the capacitive coupling is proportional to the ratio d/h, where d is the lead to ground and h is the top plate to ground distance as shown in Fig. 3.

Furthermore, the magnetic coupling should be also taken into account. This is due to the mutual inductance among the current loops at package level and the main loop of the stripline, which comprises the stripline itself, the NE and the FE terminations and the ground layer of the test board. Such mutual inductances can be expressed as

$$M_{1,2} = \frac{\Phi_{1,2}}{i_1} \tag{2}$$

where $\Phi_{1,2}$ is the flux of the magnetic field vector $\vec{B}_1$ concatenated with the generic package loop S_2. It is given by

$$\Phi_{1,2} = \int_{S_2} \vec{B}_1 \cdot \vec{u}_n dS \tag{3}$$

so, the interference level is proportional to the area of the secondary loops (S_2).

As a consequence, the lower the package size, the lower the magnitude of disturbances induced at the IC level through the stripline. Aiming to increase the DUT-to-stripline coupling without affecting the VSWR of the structure, this paper proposes to mount the DUT on a small carrier whose metal traces show a better (and well defined) coupling with the stripline. Furthermore it allows the connection of the DUT terminals to the ancillary circuits needed to make the DUT work. The structure presented hereinafter is suitable to perform either susceptibility or emission tests on packaged ICs as well as on bare dies. It is composed of a metal strip and a two-layer 100 mm × 100 mm test board (the same prescribed in [4]). The NE and the FE terminations of the stripline are connected to two SMA connectors that allow the connection to the test setup. The DUT and its carrier are mounted on the test board, which is just underneath the metal strip, as it is shown in Fig. 4. The IC terminals are connected to the auxiliary components and to the measurement instrumentations through the metal traces laid on the IC holder and through the related vias. The proposed structure is shown in Fig. 4, and the dimensions resulted from the design and the optimization, which was carried out with Microwave Studio (an EM simulator) [18], are listed in Table I. According to the simulation results, the coupling between port 5 and port 1, as defined in Fig. 4, is that shown in Fig. 5. It is greater than −25 dB above 800 MHz.

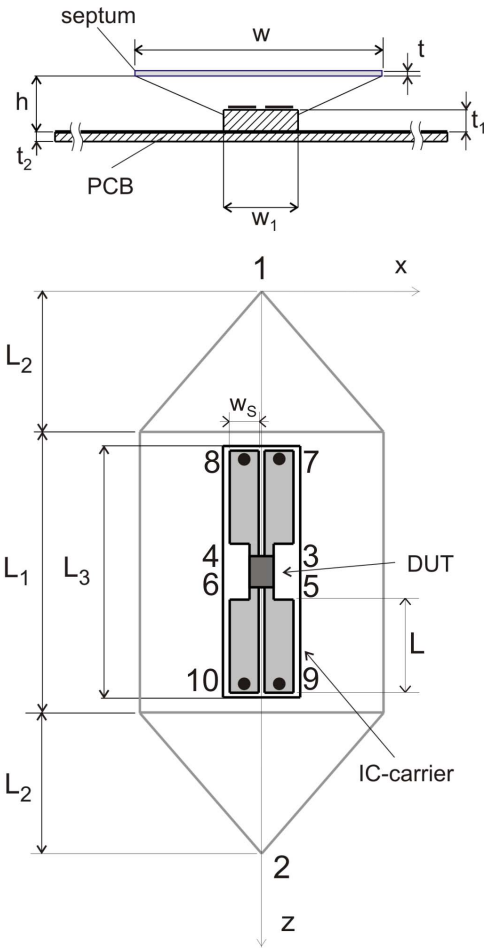

Fig. 4. IC Stripline including the DUT carrier.

TABLE I
GENERAL IC STRIPLINE DIMENSIONS

Parameter	Value [mm]
L_1	30
L_2	15
w	30
t	0.2
t_2	1
h	6
L_3	28
w_1	8
t_1	2.4
L	10
w_s	3

III. MODEL OF THE STRIPLINE

This section presents a circuit model of the guiding structure, which is made up of the stripline itself and the IC carrier. For modeling purposes, the structure is divided into three parts,

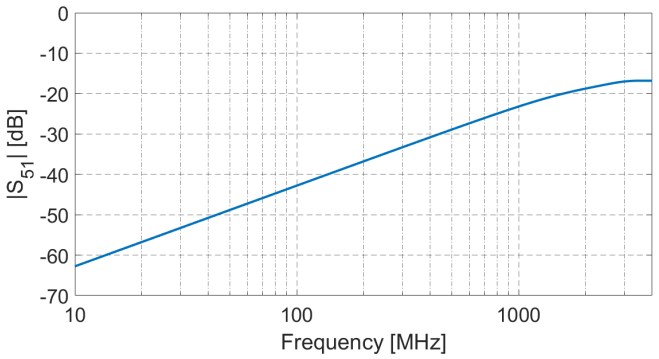

Fig. 5. Magnitude of S_{51} versus frequency obtained from EM simulations.

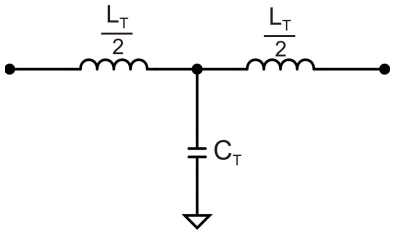

Fig. 6. Elementary cell used to model the tapered region.

TABLE II
PERUNIT-LENGTH PARAMETERS OF THE TAPERED REGION

Interval	z(mm)	No. of sections	$L_{\mathbf{T}}$(nH/m)	C_{T}(pF/m)
1	0-1	1	148	75
2	1-2	1	156	71
3	2-6	4	160	69
4	6-15	9	163	68.3

the central body and the tapered regions, which are assumed to be identical.

A. Model of the Tapered Regions

As mentioned earlier, the tapered regions are needed to connect the central body of the stripline to the terminations and to avoid the generation of higher order modes. Such regions are usually designed referring to a linear tapering, i.e., (w/h) is constant along the z-axis. This keeps constant the characteristic impedance along the z-axis.

A circuit model of the tapered regions has been derived referring to the microstrip line modeling presented by Hammerstad–Jensen–Kirschning in [19] and [20]. The structure has been divided into N sections all equal to each other, meaning the same length along the z-axis, each one represented by the T-cell shown in Fig. 6. The model parameters have been calculated using the expressions shown in [19]. In that model, the thickness of the metal strip t is taken into account only if $t/w > 0.1$. Moving from port 1 (port 2) toward the central body, the parameters change. They have been approximated with two ladder functions (one for C_T and another for L_T), whose respective values are listed in Table II. The values for each interval are those calculated for the central cell.

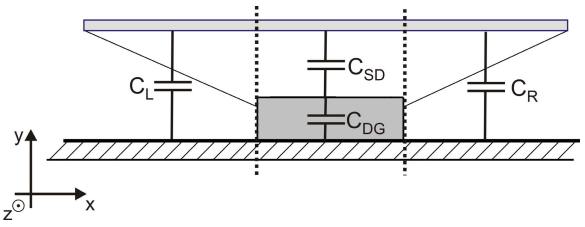

Fig. 7. x-y cross section of the proposed guiding structure—main body.

TABLE III
CENTRAL REGION P.U.L. PARAMETERS

Parameter	Value
L_{S} (nH/m)	170
$C_{\mathrm{L}} = C_{\mathrm{R}}$ (pF/m)	28
C_{SD} (pF/m)	19.7
C_{DG} (pF/m)	127

B. Model of the Central Body

In addition, the model of the central region has been derived cascading a set of elementary cells. The per unit length (p.u.l.) inductance L_S and the p.u.l capacitance have been calculated referring to the expression shown in [19] and [20]. In particular, given that the dielectric constant is not uniform over the x-y cross section (see Fig. 7), the p.u.l. capacitance has been calculated as follows. The central region has been divided into three subregions, and each one has been analyzed independently. The overall p.u.l. capacitance has been evaluated as

$$C_{\mathrm{SG}} = C_L + C_R + \frac{C_{\mathrm{SD}} C_{\mathrm{DG}}}{C_{\mathrm{SD}} + C_{\mathrm{DG}}} \tag{4}$$

where C_L and C_R are the p.u.l. capacitances of the side regions. Their value was calculated as

$$C_L = C_R = \epsilon_0 \frac{(w - w_1)}{2h} + C_{\mathrm{fr}}. \tag{5}$$

C_{fr} is the fringing capacitance whose model can be found in [22].

C_{SD} and C_{DG} are the p.u.l. capacitances of the central region as shown in Fig. 7. In particular,

$$C_{\mathrm{SD}} = \epsilon_0 \frac{w_1}{(h - t_1)} \tag{6}$$

$$C_{\mathrm{DG}} = \epsilon_0 \epsilon_r \frac{w_1}{t_1} \tag{7}$$

where ϵ_0 is the vacuum permittivity and ϵ_r is the relative one. The dielectric considered hereinafter is FR4 having $\epsilon_r = 3.9$.

The model parameters of the body region are listed in Table III.

C. Stripline to Microstrip Coupling

In addition, the coupling (parameters $K_{\mathrm{SM}}, C_{\mathrm{SM}}, and C_{\mathrm{MG}}$) between the metal traces connected to the DUT pins and the micro stripline have been evaluated using the expressions given in [19] and [20]. In particular, C_{SM} has been calculated assuming the stripline top plate as the reference plane [21].

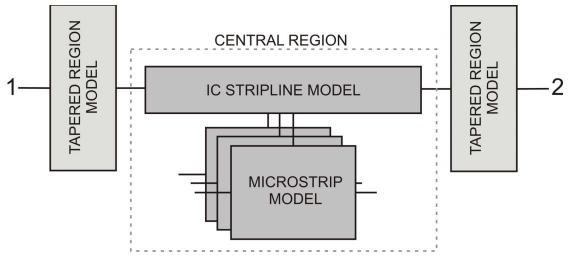

Fig. 8. Block diagram of the proposed model.

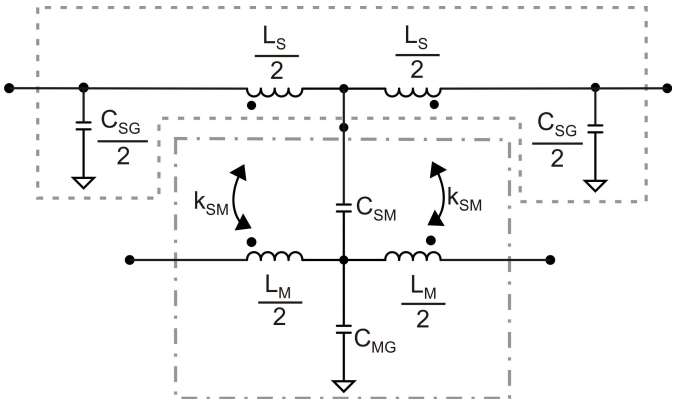

Fig. 9. Elementary cell used to model the central body. Elements enclosed by the dash-dotted line are those related to the IC carrier.

The inductive coupling is modeled by an ideal transformer whose coefficient k_{SM} has been calculated referring to the magnetic coupling between the micro stripline loop along the z-axis and those of the microstrips belonging to the IC carrier. Furthermore, the mutual coupling among the microstrips of the IC carrier has been evaluated referring to the approach shown in [22], which defines the even mode (C_e) and the odd mode (C_o) p.u.l. capacitances, the p.u.l. mutual capacitance C_m, and the p.u.l mutual inductance (M). Such parameters can be calculated as

$$C_M = \frac{1}{2}[C_o(\varepsilon_r) - C_e(\varepsilon_r)] \tag{8}$$

$$M = \frac{\mu_0 \varepsilon_0}{2}\left(\frac{1}{C_e(\varepsilon_r = 1)} - \frac{1}{C_o(\varepsilon_r = 1)}\right) \tag{9}$$

thus, the inductive coupling is given by

$$k_{\mathrm{MM}} = \frac{M}{L_M}. \tag{10}$$

L_M is the self-inductance of the microstrip [22].

To sum up, the geometrical dimensions, as listed in Table I, are the input parameters needed to calculate L_M, C_o, and C_e, which in turn are used to obtain M, k_{MM}, and C_M. Furthermore, it is worth mentioning that in case of multiconductor microstrip (more than two) the general approach presented in [23] can be used.

D. Complete Model

The block diagram shown in Fig. 8 provides a general view of the developed model. It is made up of the elementary models described so far, each one represented by an equivalent circuit. The equivalent circuit representing each tapered region is shown in Fig. 6 while that used for the central region is in Fig. 9.

The proposed model has been validated performing scattering parameter measurements on the test structure presented hereinafter.

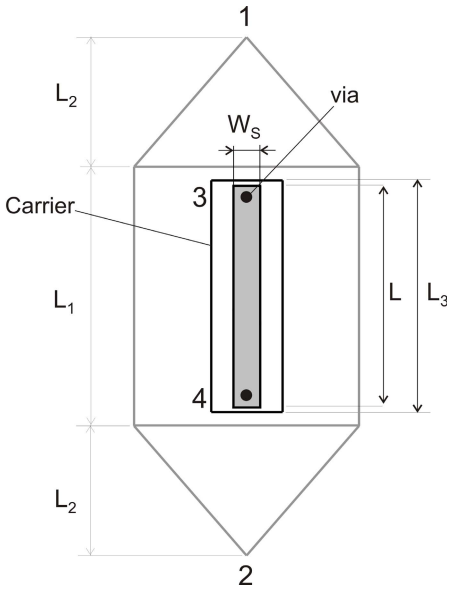

Fig. 10. IC stripline including the microstrip top view.

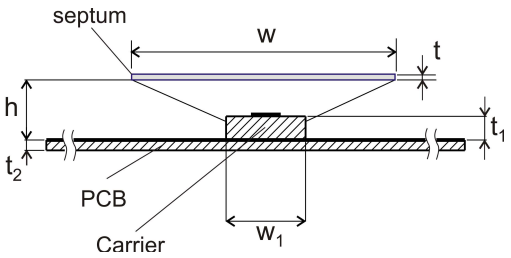

Fig. 11. IC stripline including the microstrip cross-sectional view.

TABLE IV
STRIPLINE MODEL PARAMETERS

Parameter	Value
L_{S} (nH/m)	170
C_{SG} (pF/m)	67

IV. Model Validation

Aiming to validate the model presented in Section III, a stripline comprising a microstrip line as shown in Fig. 10 (top view) and Fig. 11 (cross section) was considered. The structure is similar to that shown in Fig. 4; thus, its dimensions are those listed in Table I except for $L = 27$ mm. The parameters of the stripline model obtained from the above-mentioned expressions are listed in Tables III–V. Based on that, a prototype was fabricated and experimentally

TABLE V
IC CARRIER PARAMETERS

Parameter	Value
L_{M} (nH/m)	364
C_{MG} (pF/m)	93
C_{SM} (pF/m)	38.5
k_{SM}	0.2

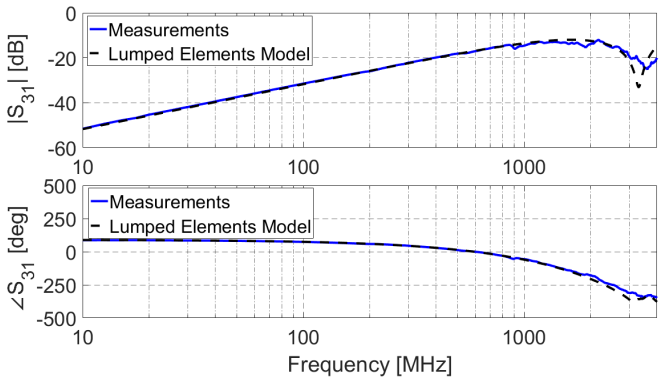

Fig. 12. Scattering parameter S_{31} obtained from measurement (continuous) and simulation (dashed).

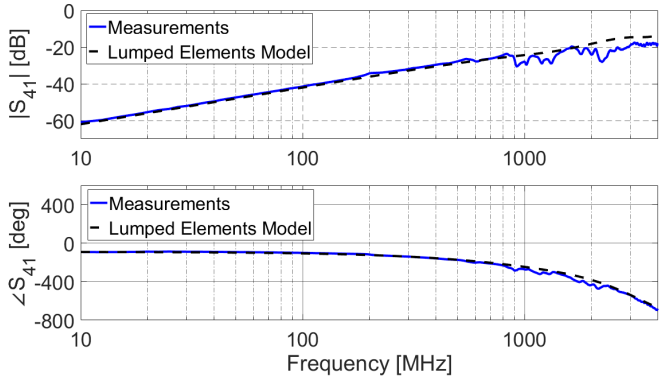

Fig. 13. Scattering parameter S_{41} obtained from measurement (continuous) and simulation (dashed).

characterized using a 6-GHz two-port vector network analyzer. Some of the results obtained from such measurements are shown by continuous lines in Figs. 12 and 13. Those obtained from the simulation in the frequency domain of the proposed model are shown by dashed lines.

The number of cells needed to model each block has been calculated to meet

$$n_{\mathrm{cells}} > \frac{30\ fl}{v_{\mathrm{ph}}} \tag{11}$$

where l is the length of each block, f is the maximum operating frequency, and v_{ph} the phase velocity. In particular, the results shown in Figs. 12 and 13 were obtained with 30 cells for each section.

The model presented in Section III allows one to perform simulations aimed to check the test bench for measuring either the EM emission or the EM susceptibility of a given IC. For

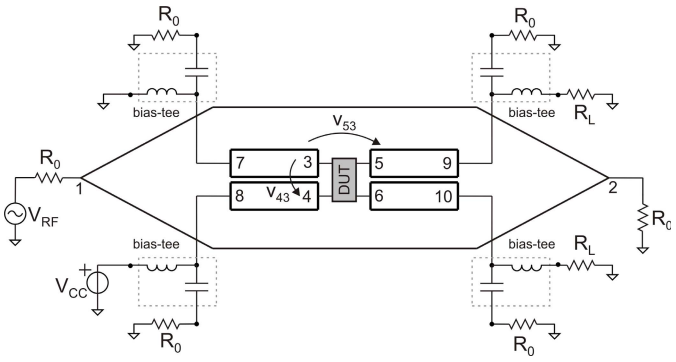

Fig. 14. Circuit representing the test setup used to perform radiated susceptibility tests.

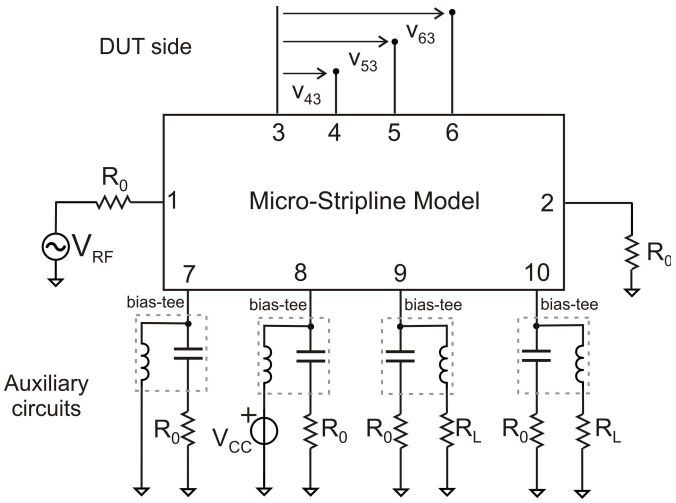

Fig. 15. Example of circuit used to perform the susceptibility analysis of an IC.

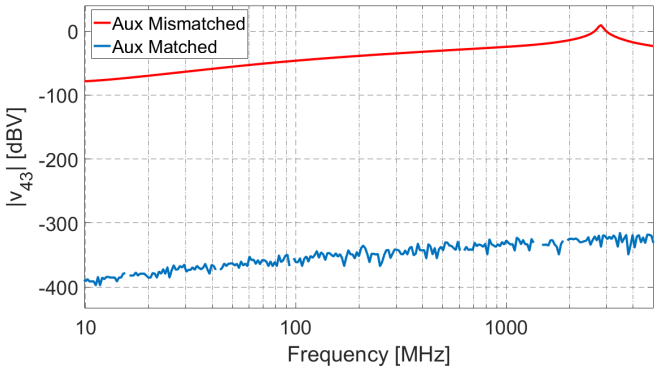

Fig. 16. v_{43} is the voltage induced between terminals 3 and 4 by a unit 50-Ω RF source feeding the stripline at port 1. The continuous line was obtained from a frequency domain **simulation** carried out with ports 7 shorted and the remaining ports matched. The dashed line was obtained with ports 7–10 matched.

instance, wanting to check the consistency of a susceptibility test setup, the incident power to be applied to the micro stripline to obtain a given level of interference at the DUT ports can be evaluated through the analysis of the equivalent circuit comprising the above-presented model, the auxiliary circuits, and the equivalent circuit of the instruments. An

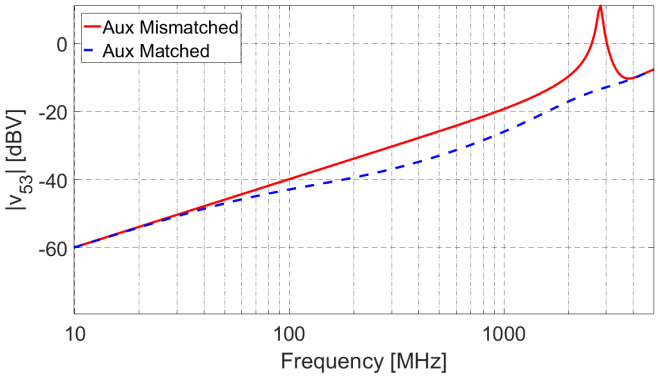

Fig. 17. v_{53} is the voltage induced between terminals 3 and 5 by a unit 50-Ω RF source feeding the stripline at port 1. The continuous line was obtained from a frequency domain simulation carried out with ports 7 shorted and the remaining ports matched. The dashed line was obtained with ports 7–10 matched.

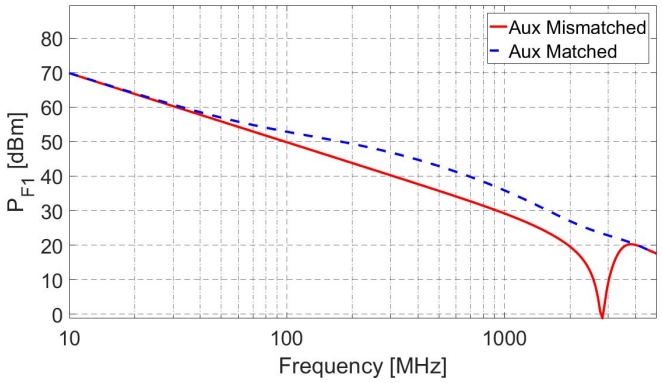

Fig. 18. RF source incident power needed to obtain $v_{53,\text{open}} = 1\,\text{V}$ over the frequency range of interest.

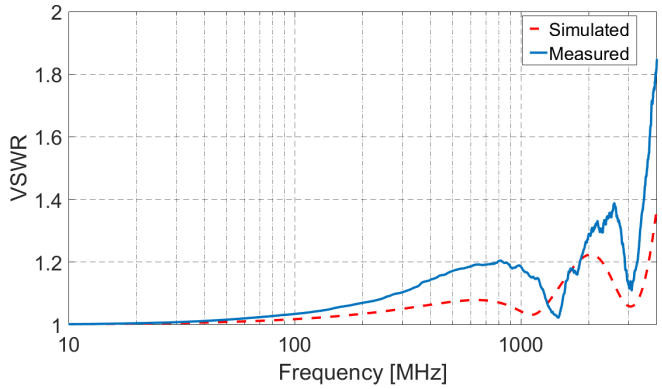

Fig. 19. VSWR of the guiding structure sketched in Fig. 4 obtained from measurement (continuous line) and from simulation (dashed line).

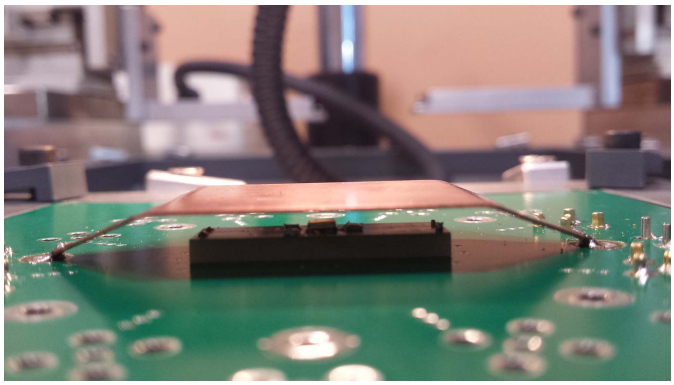

Fig. 20. Photograph of the prototype.

example of that is given in Fig. 14. A DUT featuring four terminals is mounted on its carrier and both are placed into the micro stripline. The DUT carrier terminals (7–10) are connected to the auxiliary circuits while the micro stripline is driven by a 50-Ω RF source at port 1 and it is matched at port 2. The schematic view of the test setup used for such analyses is shown in Fig. 15. The model of the micro stripline is connected to the RF source (port 1), to the 50-Ω load (port 2) and to the auxiliary circuits, but without the DUT model, i.e., with ports 3–6 left open. The voltages induced at these ports when port 1 is fed by a 50-Ω unit source was evaluated performing simulations in the frequency domain. The voltage between terminals 3 and 4 and that between terminals 3 and 5 (ports 7–10 are assumed to be matched) obtained from these analyses are shown in Figs. 16 and 17, respectively. The voltages obtained with port 7 mismatched (R_0 replaced by a short circuit for this port only) are shown by dashed lines. $|v_{43}|$ is about zero over the whole frequency range for matched auxiliary ports (dashed line) and it increases significantly otherwise (continuous line). About the RF source feeding the cell, the incident power needed to obtain certain magnitude for v_{53} is given by

$$P_{\text{F1}}(f) = \left(\frac{|v_{53}(f)|}{\sqrt{2}|A(f)|}\right)^2 \frac{1}{R_0} \tag{12}$$

where $P_{\text{F1}}(f)$ is the incident power at port 1 and $A(f) = (v_{53}/V_{\text{RF}})$. $R_0 = 50\ \Omega$ is the micro stripline matching resistance. Therefore, as far as the matched configuration is concerned, the power level needs to obtain $v_{53,\text{open}} = 1\,\text{V}$ in the frequency range of interest is that shown in Fig. 18.

V. Measurement Results

The test structure shown in Fig. 4, whose dimensions are listed in Table I, was fabricated and assembled with the aim to perform susceptibility tests on an MEMS microphone encapsulated in a tiny BGA-like package (dimensions: $3 \times 4 \times 1.5$ mm). The VSWR of the guiding structure resulted from the measurement of the reflection coefficient at port 1 is shown in Fig. 19 by continuous line, that obtained from simulations by dashed line. The difference between the two plots can be ascribed to the assembly tolerances. Furthermore, aiming to check the effectiveness of the proposed structure, an MEMS microphone encapsulated in a tiny BGA-like package (dimensions: $3 \times 4 \times 1.5$ mm) was considered. A sample was mounted into the proposed IC stripline (a photo of the test structure is shown in Fig. 20), and another sample was mounted into a IC stripline compliant to IEC 62132-8 [5] without the DUT carrier. In this latter case, the DUT was mounted on the test board directly.

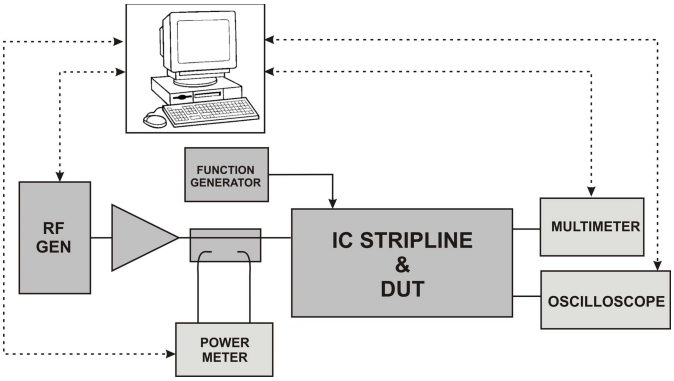

Fig. 21. Measurement test setup.

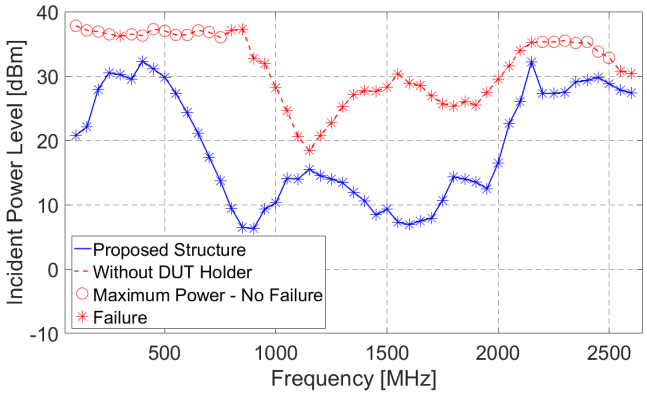

Fig. 22. Measurement results. RF power level needed to make the output voltage exceed the susceptibility criterion versus frequency. Stars indicate the frequencies at which failures occurred and circles point out those at which the maximum available power was reached without recording any failure.

The susceptibility to radiated EMI was evaluated for both samples using the test setup shown in Fig. 21, which allows the measurement of the baseband output voltage when the RF interference is applied to port 1. The RF source chain included a 10-W wideband RF amplifier fed by an RF source. The forward and the reverse power were monitored with a two-channel power meter connected to a bidirectional coupler.

In such tests, the dc offset induced by the radiated RFI at the microphone output was monitored and failures recorded whenever its magnitude exceeded 1 mV (susceptibility criterion). Measurements were carried out for a set of frequencies in the range 10 MHz–2.6 GHz obtaining the results shown in Fig. 22. The results obtained with and without the DUT carrier are shown by the blue-continuous line and the red-dashed line, respectively. In the same plot, stars and circles indicate the frequencies at which failures occurred (stars) and those at which the maximum available power delivered by the RF amplifier was reached (circles) without recording any failure. By these plots, it can be concluded that the level of RF power needed to induce an error of 1 mV with the DUT carrier is much less than that needed without it. Therefore, higher disturbance magnitude can be induced at the IC terminals or, from a different perspective, a smaller RF amplifier can be used to feed the stripline.

VI. Conclusion

Through this paper, it has been shown that the micro stripline prescribed in the international standard IEC 62132-8 can be modified in order to perform radiated susceptibility or emission tests on ICs encapsulated in small packages or bare dies, whose antenna efficiency is poor up to several tens GHz. Aiming to that, the original IC stripline was critically assessed to find out the design parameters to leverage on, in order to increase the stripline-to-DUT coupling. To this purpose, a new guiding structure showing more than −25 dB coupling in the range 800 MHz–3 GHz was designed, prototyped, and experimentally characterized. In such a structure, the DUT is mounted on a small antenna (the DUT carrier), which is also used to bias the DUT and to monitor its signals.

Furthermore, a circuit that models the stripline itself and its coupling with the DUT carrier was derived then validated performing measurements on a prototype, which was developed specifically to this purpose.

The effectiveness of the proposed approach was checked by comparing the results of susceptibility tests carried out on an MEMS microphone mounted on the DUT carrier and on the test board directly.

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