Determining Equivalent Dipoles Using a Hybrid Source-Reconstruction Method for Characterizing Emissions From Integrated Circuits

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***Abstract*—An efficient emission model for radiation problems in integrated circuits (ICs) is required at the early phase of industrial design. Traditional source-reconstruction methods rely exclusively on near-field scanning and lack the flexibility needed to handle varying IC work conditions. The proposed hybrid model can build a physical connection to the IC's inherent electric properties; therefore, after simple parameter adjustments, it can be applied to any mode of operation. The complete model consists of two sets of equivalent dipoles; one is converted directly from the current/voltage information distributed along the IC package, while the other initially is solved from linear equations that describe the relationship between the dipoles and scanned fields. Then, they are multiplied by a scaling factor to adapt to varying IC work conditions. The emission behavior of an 8-bit commercial microcontroller was reasonably simulated in full-wave solver under various working conditions. The proposed hybrid equivalent source model correctly predicted the simulated reference fields at each operation mode. The feasibility and flexibility of the proposed modeling method have been well validated.**

***Index Terms*—Current/voltage distributed in integrated circuit (IC), equivalent dipoles, integrated circuit (IC) emission, modeling.**

I. Introduction

ELECTROMAGNETIC (EM) field emissions from high-speed digital electronic devices have become a critical industrial design concern. The emission fields must be predicted for both early phase design and postoptimization. One of the most straightforward and accurate prediction methods is to perform a full-wave simulation with an EM solver [1] [2]; however, this method requires fully detailed 3-D geometries of the emitting source components and the coupling environment, resulting in long computation times and high computation hardware requirements. Thus, the focus has turned to developing a simplified and efficient model for evaluating the emitting EM field. Most models are based on near-field scanning along a surface above the device under test (DUT).

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According to Huygens's equivalent principle in EM theory [3], any emitting source below a sufficiently large near-field scanning surface can be replaced by appropriate equivalent sources, which can generate the same tangential field components on the scanning plane as the actual sources. This principle theoretically makes it possible to perform a near-field to far-field transformation and to establish equivalent sources below (or on) the scanning surface. Multiple methodologies for performing near-field transformations exist. One is to decompose the near field into plane-waves using 2-D Fourier transform; the expanded spectrum-domain fields allow a transformation from the scanning plane to a higher plane or far-field region [4]. Another approach is to build equivalent current sources (electrical or magnetic) on the scanning surface and then calculate the radiated field with integral equations of Green's function [5], [6]. The limitations of this near-field transformation are obvious: the field beneath the source plane cannot be predicted, the physical radiation sources cannot be easily reflected, and most importantly, these methods are difficult to handle IC radiation models that may be used in different working/load conditions of IC. For example, if a radiation model is extracted when the IC operates without a heat sink using the Huygens' sources, the extracted model is not valid when the same IC operates in a different system where a heat sink is further applied. Obviously the EM fields near the IC have changed due to the heat sink, which is a scatter.

The other typical method employed to model equivalent sources uses a set of electrical and magnetic dipoles placed on the *xy* plane to replace the actual source. The transfer coefficient between one dipole and its emitting field can be found analytically [7] [8]; then, a set of linear transformation equations can be established to relate the fields on the scanning plane and the equivalent dipoles at the DUT. In [9] and [10], a uniformly distributed electrical dipole array was used as the equivalent source; the dipoles were positioned and oriented on the *xy* plane (i.e., current vector's polar angle $\theta = 90^\circ$ in spherical coordinates). In these studies, magnetic near-field measurements were necessary for solving the linear equations to obtain the current value and orientation angle of the electrical dipoles. A simpler approach that only requires vertically oriented magnetic dipoles (i.e., infinite small current loop laid in the *xy* plane) was introduced in [11]. Theoretically, it is sufficient to use just one of the scanned magnetic field components (Hx, Hy, or Hz) to calculate

the current value in the loop elements; however, the accuracy of the prediction results cannot be guaranteed. Later, the work in [9] and [10] was extended to a complete model that uses both electrical and magnetic dipoles as the equivalent sources and requires both the E-field and H-field to be scanned [12]. The above methods apply the least squares method to solve the linear equations; however, due to the ill-conditioned transformation matrix, the solution can be sensitive to disturbances during the measurements. Some other optimization techniques, such as the Levenberg–Marquardt algorithm, can improve the numerical conditioning at the cost of increasing the computation time [13]. In [14], the least squares method and the regularization technique were combined to avoid ill-conditioned matrices and to obtain dipoles with physical meaning.

Some optimization methods determine the proper locations for the recovered dipoles automatically, rather than fixing a uniformly distributed dipole array. The genetic algorithm and an extended metaheuristics method were applied in [8] and [15]. Several techniques utilize knowledge of the geometry of the emitting device and the approximate current-flowing paths to help locate the positions of the dipoles, as noted in [16]–[19]. With the location constraints, these methods can provide more accurate recovered sources than the uniformly distributed dipole array; the total number of unknown variables during the calculation can be reduced significantly.

All of the approaches discussed thus far rely on near-field scanning data, rather than the electric parameters inside the emitting components (e.g., current and voltage distribution of the IC). The recovered equivalent sources are only available for the specific IC (or device) working conditions and load conditions under which the near-field scanning was performed; if the conditions change, near-field scanning must be performed again, and the complete source-reconstruction procedure must be conducted again to determine the new available equivalent sources. This kind of nonflexibility is caused by the lack of a direct connection between the electric properties of emitting components and the emission/radiation characteristics.

In this paper, an efficient hybrid model is proposed to establish equivalent sources of the IC, with a physical connection to the IC's inherent electric properties. The equivalent dipoles were obtained in two ways: by directly converting the current and voltage distributed inside the IC's package to magnetic and electrical dipoles, with knowledge of the lead-frame geometry; and by utilizing the least squares and regularization techniques [14] to obtain the dipole array from near-field data, and then employing a scaling factor on this portion of dipoles so that a direct "bridge" was built to relate the component's electric properties with the emission dipoles. The complete hybrid model is based on the proper combination of these two approaches; it can be built as a straightforward and flexible function of the current/voltage characteristics of the chip. The current/voltage can be obtained easily by taking measurements or by performing circuit simulations based on integrated circuits EM models (ICEM) or input/output buffer information specification (IBIS) models under various operating conditions, such as different running programs, input/output (IO) load impedances, or power supplies [20].

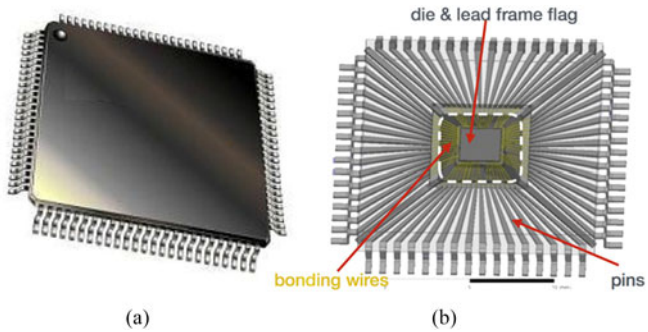

Fig. 1. Illustration of QFP IC: (a) general looking; and (b) 3-D model.

II. Architecture and Methodology of the Hybrid Model

According to the linear properties of the EM field radiating mechanism, one emission component can be divided into several smaller portions whose contributions on radiated fields will be combined to obtain the total EM-field distribution. For a typical quad flat package (QFP) chip (see Fig. 1), the IC's radiation source can be separated into two major parts; one is associated with the lead-frame pins and bonding wires (BW), and the other is associated with the die or lead-frame flag (a piece of square metallic sheet beneath the die, represented as the region within the white square in Fig. 1). The radiation from the lead-frame flag may be as substantial as that from the lead-frame pins/BW, especially on electrical field radiation.

A. Modeling of Lead-Frame Pins and BW

Generally, the physical emission sources can always be represented by six types of infinitely small dipoles [7], which are electrical dipoles at *x, y, z* directions (P_x, P_y, P_z), and magnetic dipoles at *x, y, z* directions (M_x, M_y, M_z). The infinitely small electrical dipoles are a current line with an infinitely small length; the infinitely small magnetic dipoles are equivalent to an electric current loop with an infinitely small radius, and its orientation is normal to the loop surface. In terms of IC radiation, three types are directly in relation to the physical emission sources of the IC. The lead-frame structure leads the current flowing with the pins and BW in a horizontal direction, and consequently the returning currents beneath the pins and BW are generated. At the same time, the voltage distributed along the pins can cause displacement currents in the vertical direction. These conductive and displacement currents serve as the physical sources for generating the EM field. According to the dipole moment definition, the current loops (formed by the horizontal conductive currents and their returning currents) can be represented by the magnetic dipole moments M_x and M_y. The vertical displacement current can be represented by the electric dipole moment P_z. Thus, a straightforward relationship between these equivalent dipoles and IC physical radiation sources can be found.

Looking closely at the package pins of the IC that carry currents as illustrated in Fig. 2, a current loop is formed by the

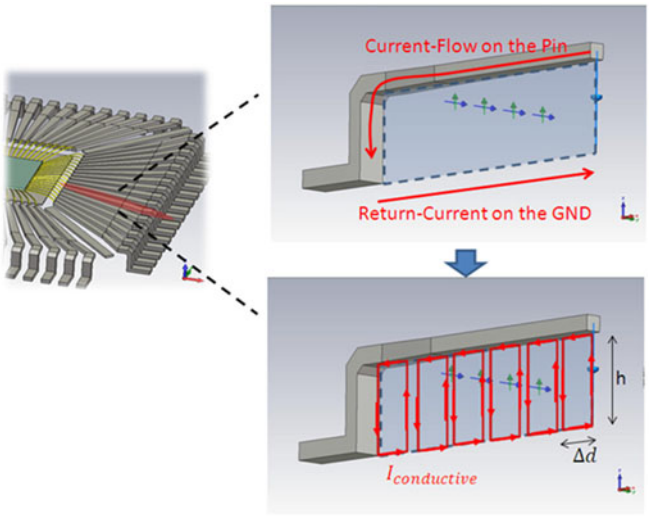

Fig. 2. Current loop(s) associated with the pin.

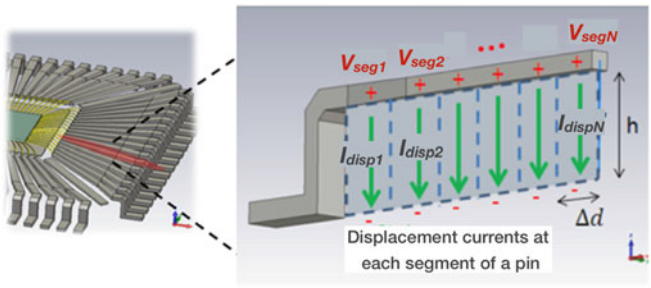

Fig. 3. Vertical displacement currents associated with the pin.

conductive current flowing in the pin and its returning current on the ground plane at the opposite direction, as labeled with the red arrows in Fig. 2. This large current loop can be further segmented into several small subloops of relatively small geometrical size compared with the wave length of interest. Due to its small electrical size, each subloop can be approximated as an infinitely small electrical current loop, which is equal to an infinitely small magnetic dipole oriented perpendicularly to the loop plane.

In [21], the magnetic dipole element $I_m l$ representing each subloop was determined using the following equation:

$$\mathrm{I}_m l = jS \cdot 2\pi f \cdot \mu \cdot I_0 \tag{1}$$

where $S = \mathrm{h}\cdot\Delta\mathrm{d}$ is the area of the subloop, f is the frequency of interest, μ is the permeability constant, and I_0 is the constant electric current in the subloop. Considering a typical IC size, such as $1.5 \times 1.5\, textmm^2$, the length of the IC pins plus the BW is much smaller than the wavelength in gigahertz; additionally, the pin-to-ground capacitance is usually less than 0.5 pF. Thus, the current along a single pin and its associated bonding wire can always be considered as constantly distributed. Therefore, each subloop shares the same constant electric current value, including the magnitude and phase. The loop stands vertically on the ground plane, so the corresponding magnetic dipole only consists of $\hat{x}$ and $\hat{y}$ direction components; the dipole's position is the center of the subloop. The radiate d field from this magnetic dipole then can be obtained either from analytical equations [3] or commercial full-wave software [2], [22].

Due to the parasitic inductance of the pins and the impedance of their external end load, the current flowing on the pin will result in voltage distributed along the pin. The displacement current, which is associated with the time-varying electric charge on the pin, exists from the pin to the ground, as shown in Fig. 3. Similar to the segmentation of the subloops, after dividing a pin into *N* segments, the voltage within one segment is treated as a constant value, and the capacitance per segment is approximately calculated according to the whole pin's pin-to-ground capacitance and the total number *N* of segments. With the knowledge of the segment voltage and segment capacitance, the displacement current for each segment in Fig. 3 can be expressed as follows:

$$I_{\mathrm{disp}} = j2\pi f \cdot Q_{\mathrm{seg}} = j2\pi f \cdot V_{\mathrm{seg}} \cdot C_{\Delta d} \tag{2}$$

where f is the frequency of interest, Q_{set} is the electric charge related to this segment, V_{seg} is the voltage of one segment of the pin, and $C_{\Delta d}$ is the pin-to-ground capacitance per segment.

As the height from the pin's surface to the ground plane is usually very small, no more than 1 mm, it is reasonable to consider the vertical directional displacement current line for each segment as an infinitely small electric dipole along the $\hat{z}$ direction. From [7], the electric dipole element of each segment is described as follows:

$$I_e l = l_{\mathrm{disp}} \cdot h = j2\pi f \cdot V_{\mathrm{seg}} \cdot C_{\Delta d} \cdot h \tag{3}$$

where h is the height from the pin's surface to the ground plane, which is usually smaller than 1mm. The z-axis position of this dipole is set as the middle point between the pin's surface and the ground plane. The radiated field from this electric dipole then can be obtained from analytical equations [3] or from commercial full-wave software [2], [22].

B. Modeling of the Lead-Frame Flag Beneath the Die

The lead-frame-flag beneath the silicon die also plays an important role on generating radiation fields. In real integrated circuit design, the impedance between power net and ground net and the impedance between ground net and lead-frame-flag are usually very small at high frequency, due to the large inherent capacitance; consequently, in the case of strong switching current along with IC power/ground pins, the voltage drop from lead-frame-flag to the ground plane of the application board can be sufficiently large for generating strong emission. At the meantime, the radiation from the conductive currents crossing the die is not always ignorable if the die's geometry size is relatively large.

In order to represent the radiation contribution from the die and lead-frame-flag, a uniformly spread dipole array on *xy* plane is used as the equivalent sources. At each location grid, three types of dipoles are used, vertically orientated electric dipoles and horizontally orientated magnetic dipoles along $\hat{x}$ and $\hat{y}$ directions. It is difficult to determine the physical current flows

related to each dipole; therefore, scanned near-field data are necessary to determine the initial dipole array set.

The relationship between dipole elements and their emitted fields can be found in [3], [7], [8], and [14]. The fields at each point can be considered as the superposition of all of the dipole sources; thus, a set of linear equations can be built, as follows:

$$\begin{bmatrix} [E_x]_{M\times 1} \\ [E_y]_{M\times 1} \\ [H_x]_{M\times 1} \\ [H_y]_{M\times 1} \end{bmatrix} = T1_{4M\times 3L} \begin{bmatrix} [P_{z\_\mathrm{DIEflag}}]_{L\times 1} \\ [M_{x\_\mathrm{DIEflag}}]_{L\times 1} \\ [M_{y\_\mathrm{DIEflag}}]_{L\times 1} \end{bmatrix} + T2_{4M\times 3P} \begin{bmatrix} [P_{z\_\mathrm{pinBW}}]_{P\times 1} \\ [M_{x\_\mathrm{pinBW}}]_{P\times 1} \\ [M_{y\_\mathrm{pinBW}}]_{P\times 1} \end{bmatrix} \quad (4)$$

where M is the total number of scanning points for the field; L is the total number of unknown dipoles for modeling the die and lead-frame flag; P_{z_DIEflag}, M_{x_DIEflag}, and M_{y_DIEflag} represent these dipole elements; P is the total number of dipoles for modeling the pins, and BW; P_{z_pinBW}, M_{x_pinBW}, and M_{y_pinBW} are the dipole elements that have been calculated from the pins' current/voltage; and T1 and T2 are the transformation matrices for the unknown and known dipole sets, respectively.

Obtaining the unknown dipoles (i.e., P_{z_DIEflag}, M_{x_DIEflag}, and M_{y_DIEflag}) requires scanning the near fields under one of the IC working conditions (i.e.,

$$\begin{bmatrix} [E_x]_{M\times 1} \\ [E_y]_{M\times 1} \\ [H_x]_{M\times 1} \\ [H_y]_{M\times 1} \end{bmatrix}\Bigg)$$

, as well as calculating the dipoles for the pins/BW (i.e.,

$$\begin{bmatrix} [P_{z\_\mathrm{pinBW}}]_{P\times 1} \\ [M_{x\_\mathrm{pinBW}}]_{P\times 1} \\ [M_{y\_\mathrm{pinBW}}]_{P\times 1} \end{bmatrix}\Bigg)$$

using the process described in Section II-A. With enough information, the die/flag dipoles can be solved accurately and with real physical meaning by employing the least squares approach combined with the regularization technique in [14].

The die/flag dipole array that is solved here can simply be multiplied by a complex-valued scaling factor to adapt the changes in the working conditions of the IC. This process will be described in detail in later sections.

C. Hybrid Combination of Two Groups of Dipoles

After obtaining the dipoles for the pins/BW and for the die/lead-frame flag, the two groups of dipoles are added together to complete the emission model. Considering the model's flexibility for handling any possible changes in the IC's operating conditions, the modeling procedure has two stages, the initial stage and the changing stage.

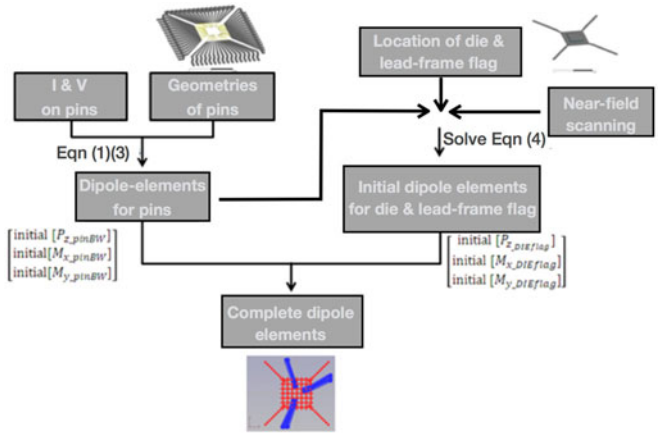

Fig. 4. Work flow for the initial stage of proposed hybrid modeling.

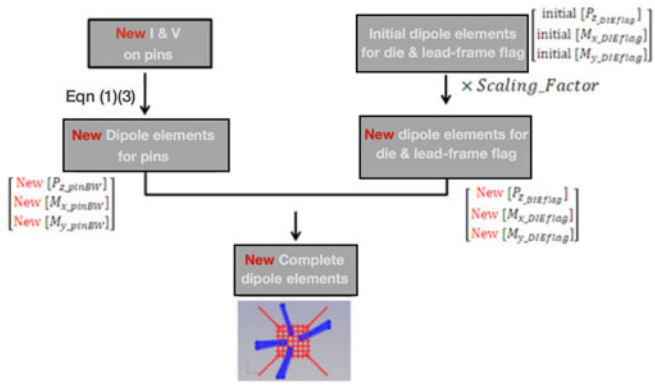

Fig. 5. Work flow for the changing stage of the proposed hybrid modeling.

In the initial stage, any working condition can be selected to initiate the modeling. As shown in Fig. 4, information pertaining to the voltage, current, and geometry will help in calculating the equivalent dipoles of the pins and BW. Then, these calculated dipoles are utilized in conjunction with the near-field data to solve the dipoles of the die and lead-frame flag. Finally, the two parts of the dipoles are combined to complete the model. Near-field scanning and the procedure for solving linear equations only need to be performed once, during the initial stage; these complicated procedures need not be repeated to model any further changes in the operating conditions.

In the changing stage, as shown in Fig. 5, the new current and voltage under the new work condition are used to generate the new equivalent dipoles for modeling the pins and BW. The necessary geometric information and related capacitance/inductance extracted in the initial stage allow the new dipoles to be established easily and quickly. Then, the dipoles of the die/lead-frame flag previously solved in the initial stage are utilized again after being multiplied by a scaling factor. This is based on a reasonable assumption that the physical radiation sources of the die/lead-frame flag (i.e., crossing currents on the

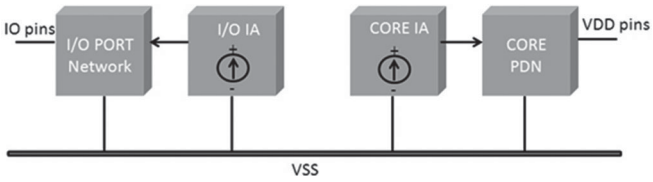

Fig. 6. Illustration of IC's ICEM architecture.

die or voltage drop of the lead-frame flag) have a constant distribution and that the absolute value of these emitting sources is linearly proportional to the currents flowing along the power delivery network (PDN) pins of the IC.

The procedure for practically determining the scaling factor is as follows. After changing the IC's working condition or IO loading condition, the changes on the PDN current can be quantified by the ratio of new currents flowing in the power/ground pins to the previous currents in the power/ground pins (those recorded during the initial stage). This ratio factor is a complex value that includes the magnitude change and the phase shift. The change ratio reflects the voltage change of the lead-frame flag and the change of the currents crossing the substrate; thus, this ratio is used directly as the scaling factor by which the initial dipoles of the die/lead-frame flag will be multiplied.

III. Applications on a Commercial Microcontroller

To verify the results of the hybrid modeling method and to illustrate the guidelines for employing this approach, we selected a commercial microcontroller as the application example.

A. The QFP Commercial Microcontroller

The chosen application target was an 8-bit microcontroller mainly used in washing machines, with a 64-pin QFP. There were two power pins and three ground pins in total, with 54 general purpose input/output (I/O) pins distributed among six I/O ports. In this setup, software selectable pull-up on I/O ports can be enabled. Our first task was to simulate the IC's emission caused by its internal activity (IA) source using a full-wave EM solver [2]. Then, a dipole-based hybrid model was established to adaptively predict the IC's emitting near field under various operating conditions. Finally, the hybrid model's results were verified with the direct full-wave EM solver's results which serve as an accurate reference.

In the example, the IA current for the digital core's PDN and for the I/O driver network typically were treated as separate sources in the ICEM modeling procedure, as shown in Fig. 6; thus, during the emitting-behavior full-wave simulation, two irrelevant current sources of 500 MHz were used as the on-die stimulation sources, driving the power/ground nets, and a pair of IO pins, respectively.

In Fig. 7, the digital core's PDN pins and a selected pair of I/O pins are marked in the IC package with a size of 14×14 mm^2. The die and the lead-frame flag were relatively small. Their edge length is no larger than 5 mm, as shown in Fig. 8. In actual design, the power and ground nets on the die often are formed

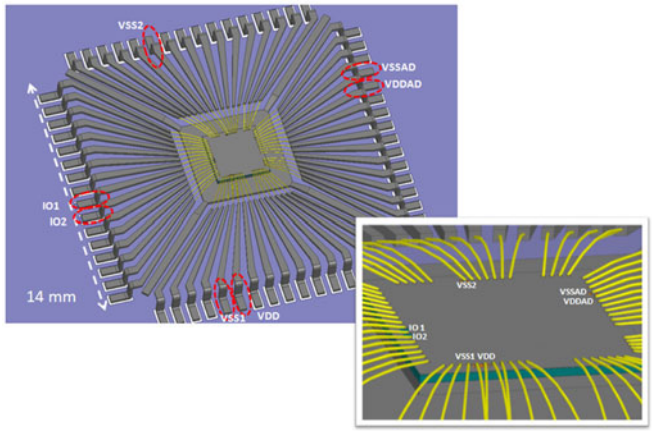

Fig. 7. PDN pins/BW and I/O pins/BW within the package structure.

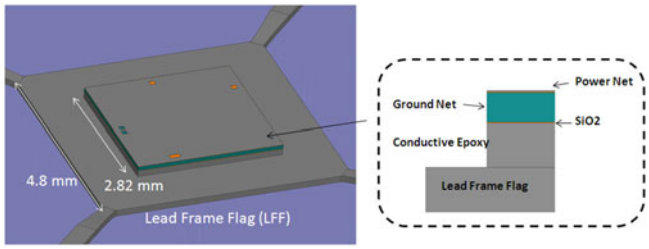

Fig. 8. Lead-frame flag structure and die above the flag.

TABLE I
Important On-Die Capacitance Values

	Capacitance Description	Capacitance Value
1	Power-net on die to ground-net on die	1 nF
2	Ground-net on die to lead-frame flag	112 pF
3	Lead-frame flag to return plane	1 pF

by metallic mesh grid with a high density or even solid planes; thus, we used two solid planes to represent the power/ground net on the die. The thickness and permittivity of the dielectric layer between the power/ground nets were selected so that the power-ground capacitance was close to our measured actual value. Table I lists some important capacitance values. In the full-wave simulation, the two separate IA current sources were placed between the on-die power and ground planes, and between the I/O pads and the on-die ground planes.

A huge de-coupling capacitance always exists on the test board, so we assumed that the impedance between the power/ground pin's external end and the return plane could be ignored at 500 MHz. We connected these power/ground pins directly to the perfect electrical conductor (PEC) return plane in the full-wave simulations. A 5 pF capacitor and a 300 Ω pull-up resistor were used as I/O pin external load-termination.

The microcontroller can have quite different electric properties under varying operation programming. We focused on two programing conditions: CORE program and PORT program. When running the CORE program, the digital CORE was

TABLE II
CURRENTS ON EACH PIN @ CORE PROGRAM

@ 500 MHz	VDD	VDDAD	VSS1	VSS2	VSSAD	IO1	IO2
Magnitude (A)	0.0576	0.0522	0.0473	0.0193	0.0437	0	0
Phase (Degree)	48.5	48.1	-131.5	-132.3	-131.6	0	0

TABLE III
VOLTAGES ALONG WITH EACH PIN @ CORE PROGRAM

@ 500 MHz	VDD_A	VDD_B	VDDAD_A	VDDAD_B	VSS1_A	VSS1_B	VSS2_A	VSS2_B	VSSAD_A	VSSAD_B
Magnitude (V)	0.0619	0.3065	0.0574	0.2965	0.0484	0.2074	0.0270	0.1775	0.0435	0.1894
Phase (Degree)	-42	-42	-42	-42	138	138	138	138	138	138
	IO1_A	IO1_B	IO2_A	IO2_B						
Magnitude (V)	0	0	0	0						
Phase (Degree)	0	0	0	0						

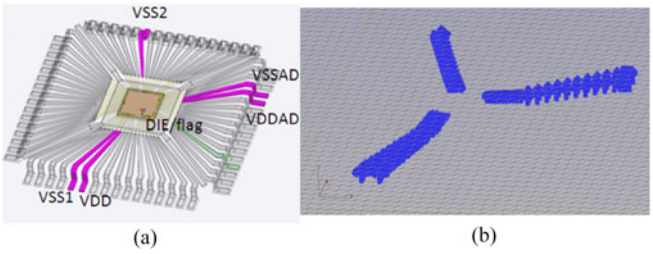

Fig. 9. Five PDN pins: (a) 3-D model; (b) dipole elements in relation.

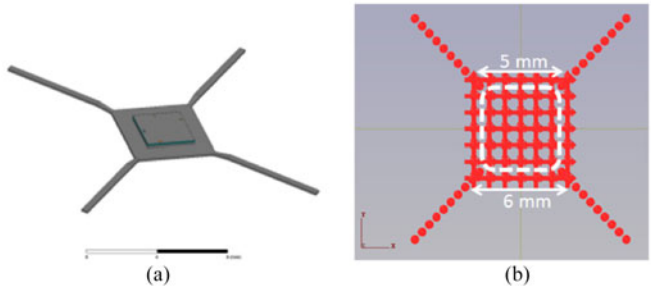

Fig. 10. Lead-frame flag and die: (a) 3-D model; (b) dipole elements in relation.

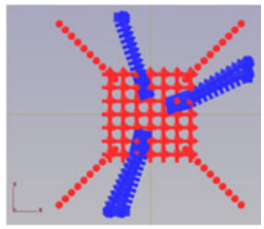

Fig. 11. Complete dipole elements for IC running CORE program.

in high-performance mode, but the I/O driver was turned OFF. When running the PORT program, the performance of the digital core decreased slightly, while the IA for the I/O port was turned ON.

B. Modeling Results for Different Working Conditions

1) CORE Program: We began our modeling procedure with the CORE program condition, which served as the initial stage defined in Fig. 4.

First, the equivalent dipoles for the pins/BW were built based on the necessary current/voltage information. When running the CORE program, the only emitting sources were the five PDN pins (i.e., two power pins and three ground pins); the current/voltage of these five pins were recorded in Tables II and III. In Table III, "XX_A" and "XX_B" (XX is the pin's name, e.g., VDD, VDDAD, etc.) represent the recorded voltages at two nodes along the pin; the voltage at each small pin segments then was estimated by linear interpolation based on the voltage on these two nodes. The equivalent dipoles for these five pins/BW then were determined according to (1) and (3), as shown in Fig. 9.

Next, the equivalent dipoles for the die/lead-frame flag were calculated according to the linear (4). We used the direct full-wave simulated fields in HFSS (which is a commercial full-wave simulation tool) to replace the practical scanned fields in order to verify the proposed modeling methodology while avoiding measurement error. A 40 mm x 40 mm observation plane placed 3 mm above the PEC return plane was chosen. As shown in Fig. 10, the positions of the unknown lead-frame-flag dipoles were fixed in relation to the square-shaped frame flag and the four corner bars. At each grid of the square-shaped dipole array, vertical electric dipoles and horizontal magnetic dipoles (x and y direction) were assigned, while at each node of the corner bars, only vertical electric dipoles existed due to the lack of conductive current flowing on the corner bars.

A complete model then was built by combining the two groups of dipoles, as shown in Fig. 11. We then used a commercial method-of-moments (MOM) based EM solver, EMC Studio [22], to calculate the EM fields generated from our calculated equivalent dipoles. The resulting radiation fields on the same observation plane 3 mm above the PEC plane were predicted.

Figs. 12–15 compare the reference field pattern (by HFSS) and our hybrid model's field mapping in terms of components E_x, E_y, H_x and H_y, as well as the 2-D curves along the cross lines at the strong-field region. These comparison figures show good agreement between the reference field and our predicted field. Of course, the die/lead-frame-flag dipoles are only suitable for this CORE program mode; for other operation modes, the dipoles must be adjusted by a scaling factor, which will be introduced later.

2) PORT Program: When the PORT program was running, the digital core's performance weakened, so the IA source for the CORE had a lower magnitude. In the meanwhile, the I/O drivers were turned ON. Tables IV and V list the new current and voltage values on pins.

Following the work flow of the "changing stage," the new equivalent dipoles for the pins/BW can be regenerated quickly by the new current/voltage value according to (1) and (3). For

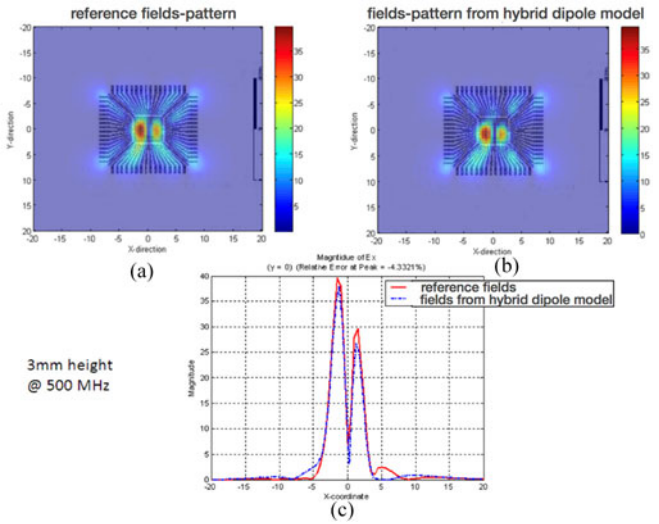

Fig. 12. E_x fields radiated from IC running CORE program: (a) reference field-pattern by full-wave simulation; (b) fields-pattern calculated by hybrid dipole model; (c) fields comparison along $y = 0$ mm cross line.

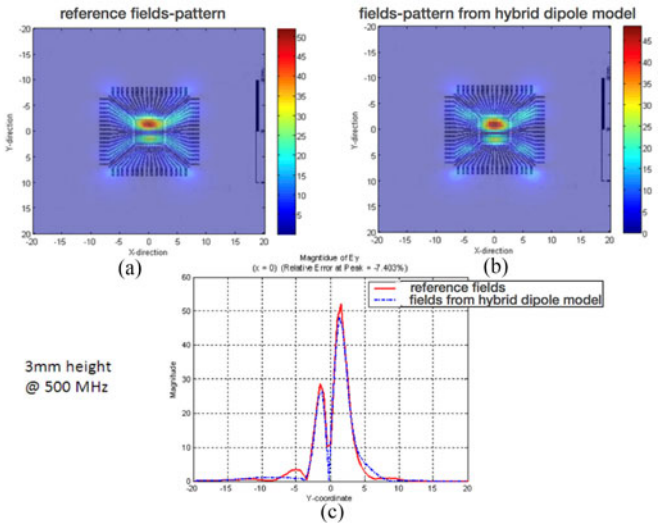

Fig. 13. E_Y fields radiated from IC running CORE program: (a) reference field pattern by full-wave simulation; (b) fields pattern calculated by hybrid dipole model; (c) fields comparison along $x = 0$ mm cross line.

the die/lead-frame-flag dipoles, the near field does not need to be scanned again; instead, the new frame-flag dipoles are estimated by simply multiplying a scaling factor onto the original dipoles. The scaling factor can be estimated from

$$SF_{\mathrm{PWR}} = \frac{I_{\mathrm{VDD}}{}' + I_{\mathrm{VDDAD}}{}'}{I_{\mathrm{VDD}} + I_{\mathrm{VDDAD}}} = 0.41 \cdot e^{j\left(-\frac{37}{180}\right)\pi} \tag{5}$$

$$SF_{\mathrm{GND}} = \frac{I_{\mathrm{VSS1}}{}' + I_{\mathrm{VSS2}}{}' + I_{\mathrm{VSSAD}}{}'}{I_{\mathrm{VSS1}} + I_{\mathrm{VSS2}} + I_{\mathrm{VSSAD}}} = 0.41 \cdot e^{j\left(-\frac{63}{180}\right)\pi} \tag{6}$$

where I_{VDD} and I_{VDDAD} are the power pin currents in Table II; $I_{\mathrm{VDD}}{}'$ and $I_{\mathrm{VDDAD}}{}'$ are the power pin currents in Table IV; I_{VSS1}, I_{VSS2}, and I_{VSSAD} are the ground pin currents

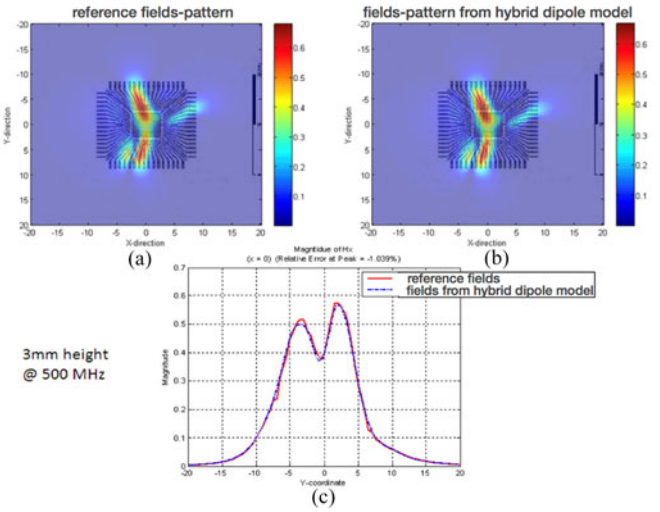

Fig. 14. H_x fields radiated from IC running CORE program: (a) reference field pattern by full-wave simulation; (b) fields pattern calculated by hybrid dipole model; (c) fields comparison along $x = 0$ mm cross line.

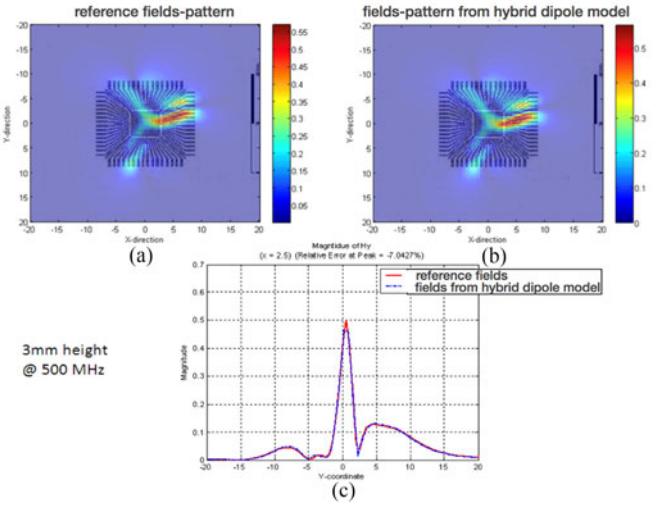

Fig. 15. H_y fields radiated from IC running CORE program: (a) reference field pattern by full-wave simulation; (b) fields pattern calculated by hybrid dipole model; (c) fields comparison along $x = 2.5$ mm cross line.

TABLE IV
CURRENTS ON EACH PIN @ PORT PROGRAM (COMMON-MODE)

@ 500 MHz	VDD	VDDAD	VSS1	VSS2	VSSAD	IO1	IO2
Magnitude (A)	0.0232	0.0218	0.0189	0.0094	0.0174	0.0094	0.0096
Phase (Degree)	12	10	169	146	172	-90	-90

in Table II; and $I_{\mathrm{VSS1}}{}'$, $I_{\mathrm{VSS2}}{}'$, and $I_{\mathrm{VSSAD}}{}'$ are the ground pin currents in Table IV. Taking the average, the final scaling factor was chosen as $0.41 \cdot e^{j\left(-\frac{50}{180}\right)\pi}$ to generate the new lead-frame-flag dipoles. Thus, the complete dipole model for the PORT program was established in this "changing stage," as shown in Fig. 16.

TABLE V
VOLTAGES ALONG WITH EACH PIN @ PORT PROGRAM (COMMON-MODE)

@ 500 MHz	VDD_A	VDD_B	VDDAD_A	VDDAD_B	VSS1_A	VSS1_B	VSS2_A	VSS2_B	VSSAD_A	VSSAD_B
Magnitude (V)	0.0259	0.1350	0.0237	0.1277	0.0203	0.0973	0.0130	0.0847	0.0179	0.0862
Phase (Degree)	-73	-65	-76	-69	71	58	56	56	75	61
	IO1_A	IO1_B	IO2_A	IO2_B	IO_load_1	IO_load_2				
Magnitude (V)	0.578	0.478	0.578	0.478	0.6	0.6				
Phase (Degree)	12	14	12	14	11.5	11.5				

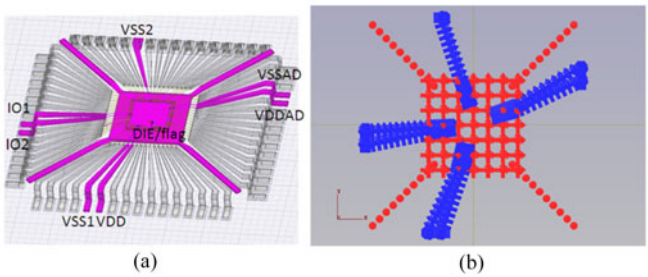

Fig. 16. IC running PORT program: (a) 3-D model; (b) complete dipole elements in relation to active pins, die, and lead-frame flag.

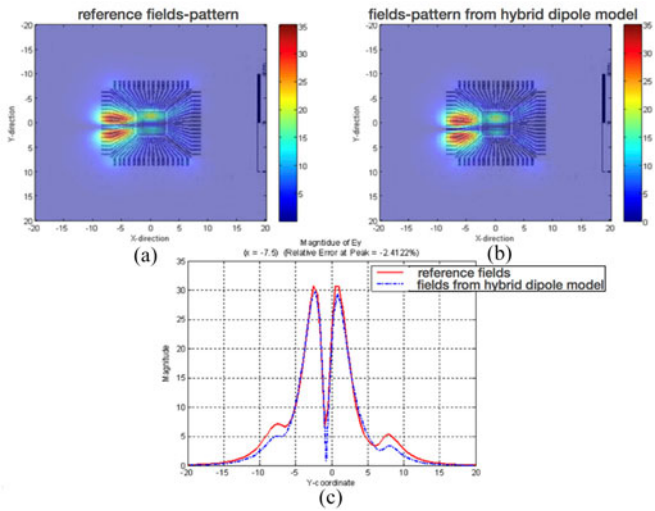

Fig. 17. E_y fields radiated from IC running PORT program: (a) reference field pattern by full-wave simulation; (b) fields pattern calculated by hybrid dipole model; (c) fields comparison along $x = -7.5$ mm cross line.

Figs. 17 and 18 show the plots of the four horizontal components of the E_y and H_y fields (at 3 mm above the return plane) with the reference data (directly simulated in HFSS) and the modeled data (by inserting modeled dipoles into EMC Studio). The I/O pins exhibited large load impedance, indicating that the E-field came primarily from the I/O pin rather than from the lead-frame flag. The Hy field distribution also directly reflected the strong currents caused by the I/O activity. The similarity between the reference data and our predicted data proves the feasibility of the proposed hybrid model for use under changing IC working conditions.

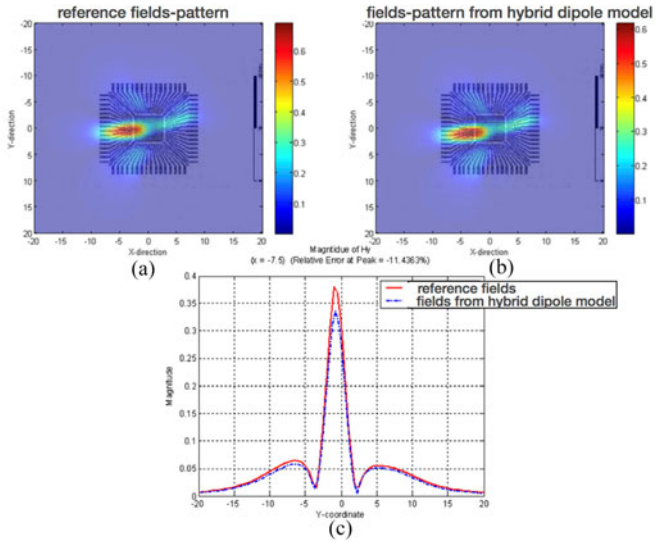

Fig. 18. H_y fields radiated from IC running PORT program: (a) reference field pattern by full-wave simulation; (b) fields pattern calculated by hybrid dipole model; (c) fields comparison along $x = -7.5$ mm cross line.

IV. CONCLUSION

In order to accurately and quickly build an IC emission model suitable for various IC operating conditions, an equivalent dipole-based hybrid modeling method was proposed and verified. This hybrid model is a straightforward function of the IC's electric properties, which are the current and voltage parameters of the pins. The model consists of two groups of equivalent dipoles. One set of dipoles represents the radiation from pins and BW, which can be converted directly from the current and voltage information within the package. The other set of dipoles, based originally on the near-field data under one working condition, mimics the contributions from the die and the lead-frame flag beneath the die. This set can be adjusted quickly using a linear scaling factor to satisfy any other operating conditions. The accuracy and flexibility of the hybrid model were validated by internally exciting a commercial microcontroller under three different operation modes. In the validation cases, the necessary current and voltage information was obtained by monitoring the full-wave simulation results. In terms of practical application, the current of the pin can always be measured by current probes or predicted if an ICEM model is available; the voltage along the pin can be simulated easily in circuit solver if at least one of the associated currents is known.

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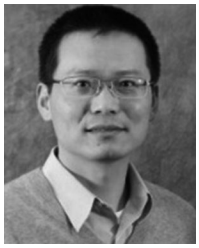

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