Modeling Injection of Electrical Fast Transients Into Power and IO Pins of ICs

Ji Zhang, Jayong Koo, *Student Member, IEEE*, Richard Moseley, *Member, IEEE*, Scott Herrin, *Member, IEEE*, Xiang Li, David Pommerenke, *Senior Member, IEEE*, and Daryl G. Beetner, *Senior Member, IEEE*

***Abstract*—A SPICE-based model of a microcontroller was developed to investigate its immunity to electrical fast transients (EFTs). The model includes representations of the on-die power delivery network, the ESD protection clamps, and the I/O driver circuits. Several measurement approaches were developed to characterize the linear and nonlinear components within the model. EFTs were injected into pins of the microcontroller to verify the accuracy of the proposed model. General purpose I/O were tested in several configurations (i.e., pull-up-enabled input, logical-high output, and logical-low output). The model was able to predict the voltage waveform and maximum voltage at each pin within 5∼6% of the measured values. A parasitic bipolar junction transistor associated with the output driver was found to have a critical impact on the noise coupled to the power bus. The simplicity and accuracy of this model shows its promise for understanding and predicting immunity issues in integrated circuits.**

***Index Terms*—Electromagnetic interference, integrated circuit (IC) design, measurement, modeling, power distribution.**

I. Introduction

WHILE electromagnetic immunity problems may be caused by a variety of mechanisms, the ultimate point of failure in a modern digital device is typically an integrated circuit (IC). System designers are increasingly demanding that ICs undergo rigorous immunity testing, in the hopes of preventing immunity problems before they occur. Models which help the designer predict and understand immunity issues with the IC would be more useful than simple test results, but such models are difficult to construct and are rarely available, even to the IC manufacturer. Developing these IC immunity models has received growing attention in recent years [1].

A variety of tests exist for characterizing the immunity of ICs, including methods which couple energy to the IC through electric or magnetic fields or through direct injection to the pins [2], [3]. Direct injection methods, which conductively couple electrical energy to the pins of the IC, have the advantage that immunity can be quantified on a pin-by-pin basis and the level of energy seen by any one pin is well defined. While experimental tests are able to report the injected power level at which a failure was observed, they fail to improve the understanding of the failure mechanism. An accurate immunity model, however, not only helps to predict the level of a failure but improves the understanding of the failure mechanisms.

The IC electromagnetic model (ICEM) [4], [5] was originally developed to predict electromagnetic emissions from ICs. This model includes a detailed description of the power delivery network, which can be used for immunity analysis if nonlinear effects and I/O drivers are included. [6], [7]. The core of a typical ICEM model is a lumped-element representation of the IC power delivery network consisting of resistors, inductors, and capacitors associated with the package lead-frame, on-die interconnect, and on-die decoupling capacitance [8], [9]. Nonlinear elements, like transistors, are not typically part of the model, though their presence is implied in the on-die decoupling and possibly in an on-die current source or an impedance between the power and return supply nets [10], [11]. While nonlinear elements are rarely needed for emissions models, where voltage variations are relatively small, nonlinear elements can be critical to immunity, where node voltages may exceed the power supply voltage and electrostatic discharge (ESD) protection circuitry may be triggered.

A model is developed in this paper to predict the voltage and currents within an 8-bit microcontroller during direct-injection of electrical fast transients (EFTs). The model is based on an ICEM-like model developed in [12] and [13], but is extended to adequately deal with both positive and negative EFTs to the power supply and to fully comprehend the I/O ring and ESD protection circuitry. The improved model can accurately predict the impact of both positive and negative EFT pulses injected onto power pins and positive EFTs onto I/O pins. The model allows for three possible configurations of the I/O: input with pull-up enabled, and output driven either logically high or driven logically low.

The development and validation of the IC immunity model is presented in the following paper. The architecture of the model will be presented first, along with measurement techniques for determining the values of components that are part of this model. Circuit models for the I/O are also presented, including the modeling of nonlinear parasitics that are not typically included in readily available I/O models. The model is validated by comparing the measured and predicted voltage waveforms on power and

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J. Zhang is with the Cisco Systems, Inc., San Jose, CA 95134 USA (e-mail: jz7r9@mst.edu).

D. Pommerenke and D. Beetner are with the Electromagnetic Compatibility Laboratory, Missouri University of Science and Technology, Rolla, MO 65401 USA (e-mail: daryl@mst.edu; davidjp@mst.edu).

J. Koo is with the Intel Corporation, Folsom, CA 95630 USA (e-mail: Jayong.koo@intel.com).

R. Moseley, S. Herrin, and X. Li are with the Freescale Semiconductor, Inc., Austin, TX 78735 USA (e-mail: rsjp60@freescale.com; Scott.Herrin@freescale.com; B34810@freescale.com).

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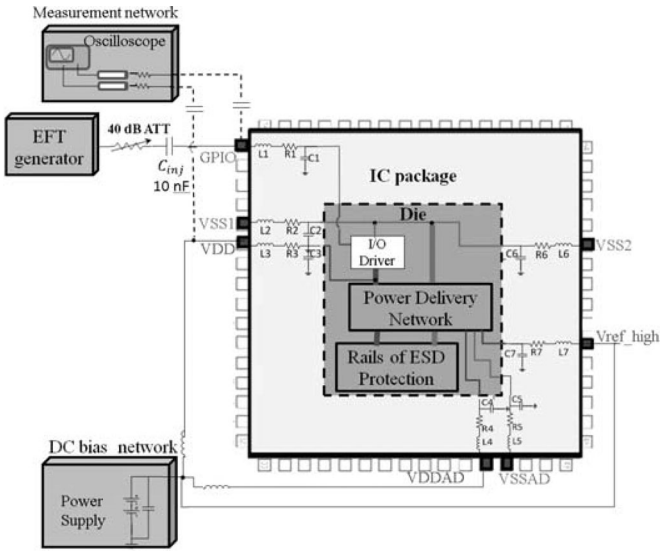

Fig. 1. EFT immunity model for the IC and test setup.

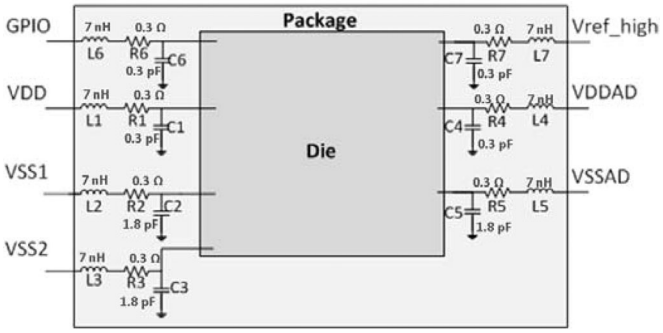

Fig. 2. IC package model.

I/O pins during direct injection of EFTs. The results demonstrate the potential of this model to help predict and understand IC immunity issues.

II. EFT Immunity Model

The model was developed for both the IC and experimental test setup, as shown in Fig. 1. Each part of this model is discussed in the following sections.

A. Model of the IC

The model for the IC includes a model of the package, the on-die power delivery network, ESD protection circuitry, and the I/O drivers.

1) IC Package: The package was represented using a simple lumped element model as shown in Fig. 2. A lumped element model is appropriate given the limited frequency bandwidth of an EFT pulse (i.e., a bandwidth of a few hundreds of MHz for a pulse with a risetime of several nanoseconds as defined by IEC 61000–4–4 [15]). The 8-bit microcontroller studied here had 64 pins, including 54 general-purpose I/O, one power and two return pins for the microcontroller core (VDD, VSS1, and

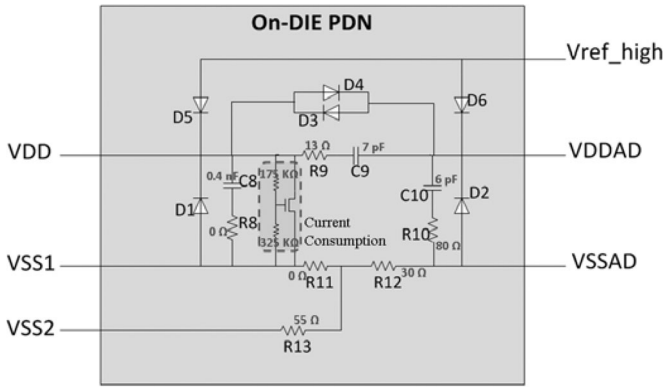

Fig. 3. On-die power delivery network.

VSS2), one power and return pin for the A/D converter (VDDAD and VSSAD), and one V_{ref_high} pin which is the voltage reference high input for the A/D converter. While all the power and reference pins are shown in Fig. 2, only one general purpose I/O pin is shown for clarity. All 64 pins are present in the model. Lumped inductances also include mutual inductances to neighboring pins. Mutual capacitance between pins was ignored since its impact was small.

2) On-Die Power Delivery Network: The architecture of the on-die power delivery network was developed intuitively from a basic knowledge of the IC layout topology and on experimental and simulated measurements, as opposed to automatically extracting the model from detailed layout information using an IC CAD tool. A complete description of the model development process can be found in [12], [13]. Essentially, a first-order circuit model was developed from basic knowledge of the power delivery network—for example, that the on-die power delivery network could be modeled with a resistor and capacitor, that power for the core and for the A/D converter should only be coupled capacitively and through an ESD-protection structure like a diode, that all VSS pins should be connected at least resistively, or that the package can be described at low frequencies by a simple LRC circuit. Measurements of the impedance looking into the pins of the IC were then made using a network analyzer to determine the values of linear components in the model. Nonlinear devices were characterized using an *I–V* curve tracer. Measurements and simulations of impedances associated with the IC were compared and the first-order model was modified, when necessary, to better predict measured results.

The resulting lumped element model of the power delivery network is shown in Fig. 3. The capacitors C8-C10 and resistors R8-R10 represent the coupling between power and ground rails and the resistance of the power delivery networks. The resistance of the substrate, which indirectly connects all return pins, is represented with resistors R11-R13. Diodes D1-D6 allow nonlinear coupling between the power and return rails. These diodes are either added intentionally, as part of the ESD protection circuitry, or result naturally from parasitics within the CMOS circuitry.

Power consumed during IC activity is normally represented using a current source that is independent of the power supply voltage. An EFT on a power or return pin, however, may

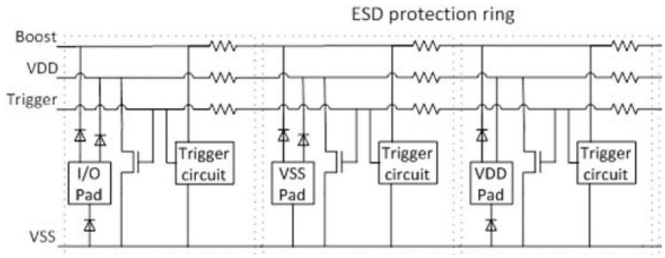

Fig. 4. ESD protection circuitry implemented in the I/O ring [14].

substantially change the power supply voltage and the resulting current or power consumption. To account for the nonlinear change in current with supply voltage while maintaining the goal of keeping the model simple, power consumption was represented using an NFET between VDD and VSS. The NFET was forced into saturation using a resistor divider. This resistor divider configuration allows the current consumption to change with power supply voltage. NFET parameters and resistor values were determined experimentally to replicate the average current consumed by the IC. While this configuration predicts average rather than dynamic current, which peaks on clock edges, the average current was found to be sufficient to predict the overall impact of an EFT, since the dynamic switching did not cause large fluctuations in the current or voltage at the IC pins. It should be noted that the impact of the current consumption on results was relatively small for this IC, so the NFET model for current consumption was not thoroughly tested. Other models, such as a voltage-dependent resistor or voltage-controlled current-source, may work as well or better.

3) ESD Protection Circuitry: The ESD protection network was designed to detect high-voltages and rapidly rising signals at I/O or on the power supply and to activate clamps to safely divert ESD currents and prevent unacceptably large voltage drops across IC components. The ESD protection circuitry was implemented in the I/O ring of this microcontroller as shown in Fig. 4 [14]. Each I/O pad or power/GND pad contains at least one NFET power clamp and a local trigger. The overall I/O ring contains many of these clamps and triggers. While it may be possible to infer this circuitry from external measurements, inferring the circuit characteristics is difficult without some a priori knowledge. For the model presented here, we used a SPICE model of the ESD protection circuitry obtained from the IC manufacturer.

4) I/O Drivers: The initial structure of the I/O pads is shown in Fig. 5. General purpose I/O contain a pull-up FET, an input buffer, and an output buffer. A rough representation of internal circuitry was also included in the model, though the internal circuitry has minimal influence on the impact of the EFT. The parameters for this model were determined both from SPICE circuits available from the manufacturer and from measurements. After investigation, it was found that a parasitic bipolar junction transistor (BJT) had to be added to this model to correctly account for I/O current during an EFT event, as will be discussed in a later section. ESD protection circuitry is not shown in Fig. 5, since it was already show in Fig. 4.

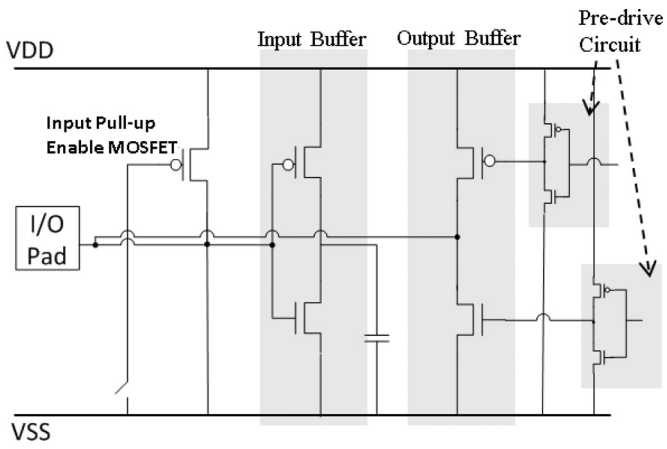

Fig. 5. Model of a general purpose I/O cell.

B. Disturbance Source

The EFT generator was modeled as a transient voltage source in series with a 50-Ω impedance. The voltage source supplied a waveform mimicking the standard EFT pulse [15], amplified by an appropriate gain to provide peak-voltages up to 2000 V.

C. Power Supply and Coupling Paths

The EFT generator, an oscilloscope, and a dc power supply were connected to the IC through coaxial cables and through coupling capacitors or inductors. A 15-nF capacitor and a 40-dB high-voltage attenuator were placed between the EFT generator and the IC in both the test setup and simulation model to limit the size of the EFT seen at the IC. The dc power supply was connected to the VDD and VDDAD pins through a 47-nH inductor and a ferrite. The inductor and ferrite were used to isolate the supply from the IC (and the overall test) at EFT frequencies. The oscilloscope was connected to the pins under test through a 1-nF capacitor and a 475-Ω SMT resistor. The impedance of this series RC connection was sufficiently large to minimize the impact of the oscilloscope on the measurement. The impact of the coaxial cables and the connections to the IC were minimal at EFT frequencies, and therefore were ignored.

III. Extraction of Model Parameters

With the exception of the ESD protection circuitry, the characteristics of model components were determined experimentally by measuring S-parameter and voltage–current (*V–I*) curves.

A. IC package and On-Die Power Delivery Network

The values for components within the IC package and on-die power delivery network were found using the methods described in [12], [13]. RLC parameters were found by making S-parameter measurements looking into or between pins of interest. Other pins were left unconnected (floating) to force the current to flow along a particular path through the IC. Measurements were made at all power and return pins to fully describe the network. Diodes between supplies were similarly

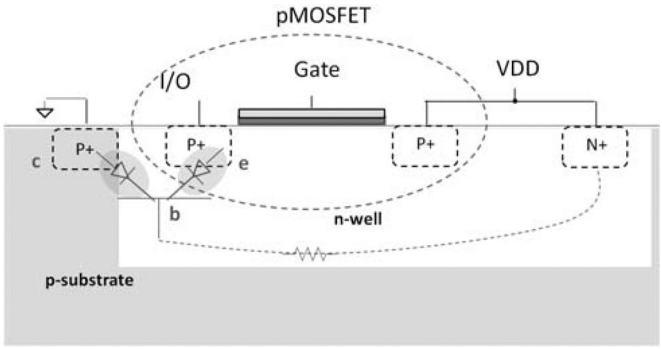

Fig. 6. Parasitic PNP BJT is formed by the PFET drain, the n-well, and the p-type substrate.

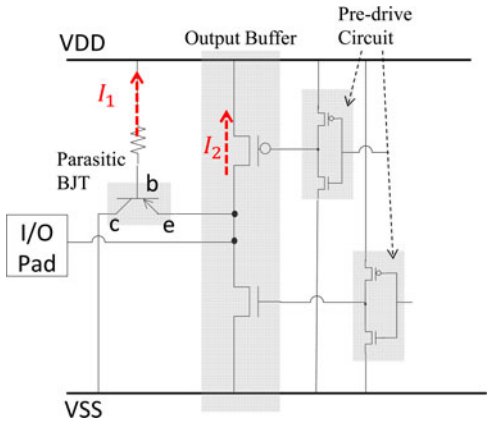

Fig. 7. I/O cell including the parasitic BJT.

characterized from *V–I* curves measured between power and return pins.

B. Establishing Accurate I/O Driver Models

The I/O model depends on the I/O configuration. Three configurations were studied: input with pull-up enabled, output driving a logical high, and output driving a logical low.

1) Output Driving Logical High or Driving Logical Low: As shown in Fig. 5, a typical output buffer includes a PFET and NFET to control the logical high or low of the output signal. In the output high mode, the PFET in the output driver is turned on, while the NFET is turned OFF. In the output-low mode, the PFET is OFF, while the NFET is ON. The "input pull-up enable PFET" used for the input driver is turned off while in output mode. Parameters for the output-driver FETs and the ESD protection diodes connected to the I/O pad in Figs. 4 and 5 were available from the manufacturer. Experimental measurements, however, showed that only modeling the FETs and protection diodes was insufficient to predict current and voltages during a positive EFT. In addition to the nonlinear components connected to the pad shown in Figs. 4 and 5, there is also a parasitic PNP BJT between the pad, VDD, and the substrate (VSS). The standard pMOSFET SPICE model will not account for the shunt current produced by this parasitic BJT. The role of this BJT was critical to accurately predicting results during a positive EFT.

The BJT is formed by an n-well in a p-type substrate as shown in Fig. 6. The n-well is connected to the power supply (e.g., VDD) and the p-type substrate is connected to VSS. A parasitic PNP BJT is formed from p-diffusion in the n-well (i.e., forming the BJT emitter from either the drain of the PFET or the diode anode), the nwell (BJT base), and the p-type substrate (BJT collector). The placement of this BJT in the overall I/O model is shown in Fig. 7. The substrate-resistance is included in the BJT model. Fig. 7 does not include the input gate (shown in Fig. 5), since it has minimal impact on results. The BJT is activated when the I/O pad voltage becomes larger than the value of VDD, forward biasing ESD protection diode which makes up the emitter/base junction. When current flows across this junction and the collector-emitter junction is properly biased (as it will be when power is applied to the IC), the BJT will be turned "ON" and current will flow from the I/O pad to both the VDD and VSS rails. This BJT becomes important when predicting the response of the IC to large over-voltages at the I/O pins [14].

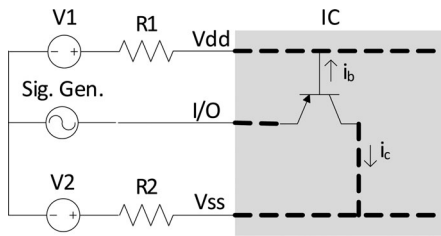

Fig. 8. Setup for measuring the gain of the parasitic PNP BJT.

The characteristics of the parasitic BJT were determined through a set of current and voltage measurements. One such measurement is illustrated in Fig. 8. A signal generator was used to provide a slow-varying input voltage on the I/O pin (the emitter of the parasitic BJT), while a dc bias was provided on the VDD and VSS pins (the base and collector pins, respectively). The voltage drop across R1 and R2 was measured with an oscilloscope to determine the base and collector currents, i_b and i_c respectively, and the relationship between them. Similar measurements were made to determine other BJT characteristics, such as the voltage/current relationship between the emitter and base (I/O pin and VDD), and others. During the measurement, the I/O pin was disabled so all driving FETs connected to the pin were turned OFF and the only low-impedance path from the I/O pad to the VDD bus was through this parasitic BJT. An example measurement result is shown in Fig. 9. The value of the BJT gain, β, was determined from these measurements to be approximately 2. Since the base of the BJT is lightly doped, there is a noticeable relationship between the gain and the collector current. The presence of this parasitic BJT is further validated later in the paper when measured and simulated results are compared using IC models with and without this BJT present in the model.

A parasitic NPN BJT, not shown in Fig. 6, is also created by the ESD protection diode or output NFET connected to VSS. In this case, the n-type material of the diode cathode or NFET

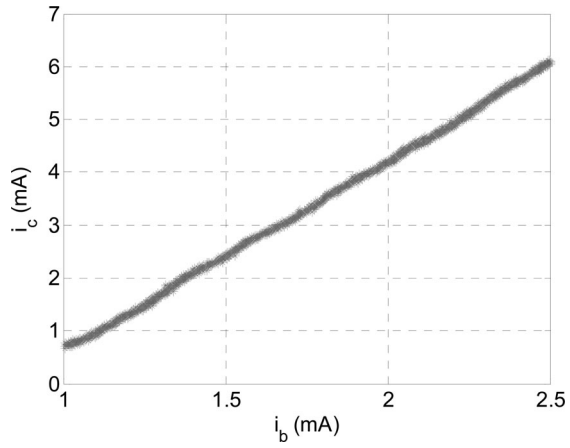

Fig. 9. Collector versus emitter current for the parasitic PNP BJT.

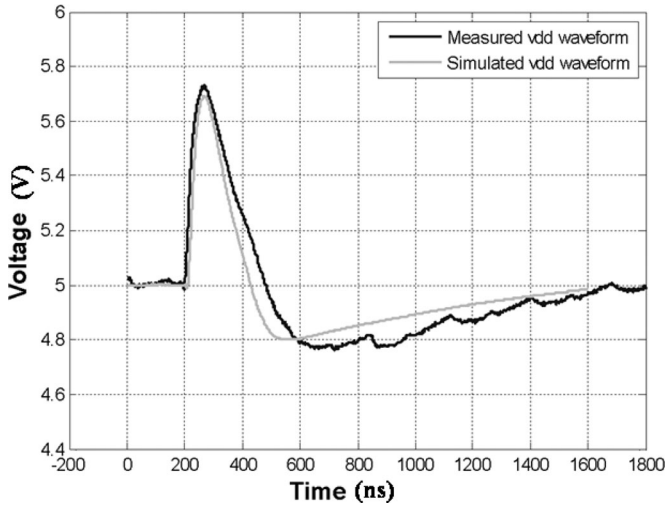

Fig. 10. Waveform on the VDD pin during a positive 200-V EFT injection to the VDD pin.

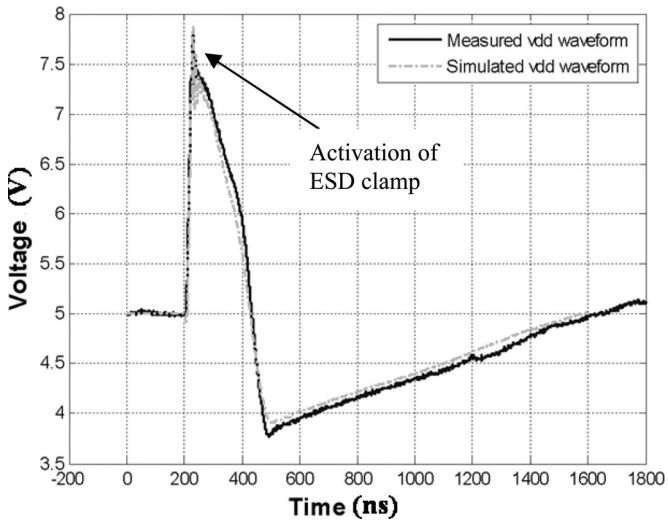

Fig. 11. Waveform on the VDD pin during a positive 1600-V EFT injection to the VDD pin.

drain connected to the I/O pin forms the emitter, the p-substrate connected to VSS forms the base, and a nearby n-well, which is connected to VDD, forms the collector. This parasitic BJT can be activated when the I/O pad becomes sufficiently negative relative to VSS to forward bias the base–emitter junction. The process for accounting for this parasitic BJT is similar to the process used for the BJT in Fig. 6, but was not studied here since negative EFTs were not applied to the I/O.

2) Input With Pull-Up Enabled: In this mode, the output buffer is turned OFF and has minimal impact on the circuit. The pull-up FET can be modeled as a resistor or using a nonlinear FET model. While a resistive model works well for small voltage swings, a more accurate nonlinear FET model is preferred for the large voltage swings seen with an EFT. Both methods were tested, as shown later in this paper. The characteristics of this FET were derived from information supplied by the manufacturer and from S-parameter measurements between the I/O pad and VDD.

IV. Model Validation

The model was validated by injecting positive and negative EFT pulses into IC power pins and positive EFTs into I/O pins. The measurement setup is shown in Fig. 1.

A. EFTs on Power Pins

Both positive and negative EFTs were injected into the VDD pin. While EFTs may also occur on the VSS pins, a negative EFT on a VDD pin is roughly equivalent to a positive EFT on a VSS pin, so additional tests on the VSS pin were not conducted. EFT tests were not performed on power for the A/D converter or for V_{ref_high}, since the supplies for these pins are typically much better isolated from EFT-like events than power for the core. Tests were performed when the microcontroller was powered at 5 V.

1) Positive EFTs: Tests were performed with EFT generator voltages ranging from 200–1600 V. Decoupling capacitors were removed from the PCB to increase the EFT energy conducted into the IC. The resulting voltage was measured at the VDD pin. Example waveforms are shown in Fig. 10 for a 200-V EFT and Fig. 11 for a 1600-V EFT. As shown in these figures, the rise- and fall-time of the EFT waveform is slowed by the on-die decoupling capacitance (around 1.4 nF). At 200 V, the waveform is similar to the waveform at the EFT generator (except for a slower rising edge). At 1600 V, the ESD protection circuitry will be triggered and the coupled voltage on the VDD net will be clamped. The impact of the ESD protection circuitry can be observed in Fig. 11, where it causes a sharp "spike" in the VDD voltage at roughly 200 ns, as the voltage rise rapidly above 7.5 V but then rapidly decreases again to 7.5 V and lower after the power clamp is triggered. The peak voltage observed at the VDD pin as a function of the voltage settings at the EFT generator is shown in Fig. 12. The slope is not constant due to the triggering of nonlinear diodes and power clamps. Measured

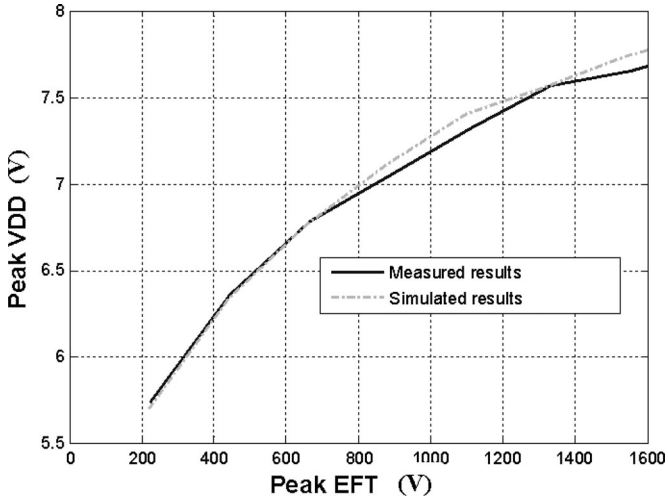

Fig. 12. Peak voltage on VDD pin versus EFT generator voltage.

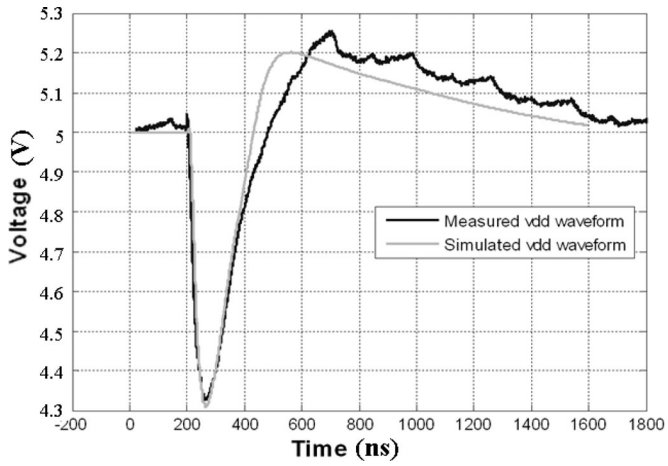

Fig. 13. Waveform on the VDD pin during a negative 200-V EFT injection to the VDD pin.

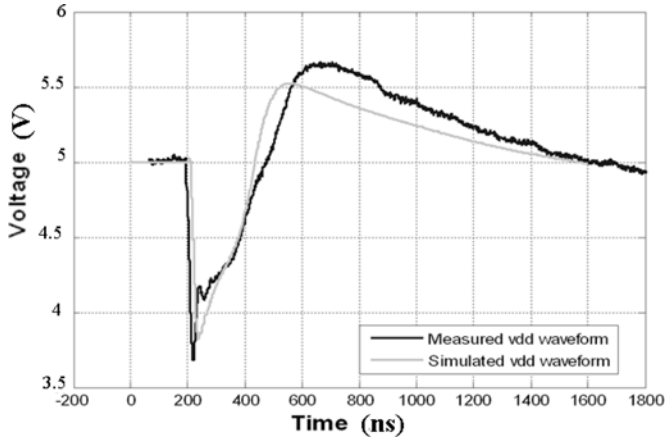

Fig. 14. Waveform on the VDD pin during a negative 600-V EFT injection to the VDD pin.

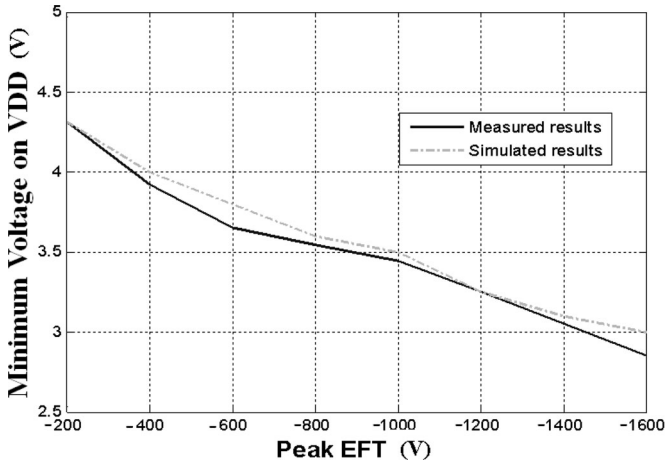

Fig. 15. Minimum voltage on VDD pin versus EFT generator voltage.

and predicted values compare within 2.7% (i.e., 200 mV) in each case.

2) Negative EFTs: A small negative EFT at the VDD pin does not trigger a significant nonlinear response in the IC, as illustrated in Fig. 13 when the EFT generator was set to -200 V. A large negative pulse, however, can turn on the diode between the V_{ref_high} pin and the VDD pin (i.e., D5 in Fig. 3), as shown in Fig. 14. In our test setup, V_{ref_high} was conductively connected to a μF level bulk decoupling capacitor associated with the 5-V voltage regulator. Once the voltage on VDD falls by more than a diode turn-on voltage below V_{ref_high}, the diode will turn ON and the capacitor on V_{ref_high} will provide charge to VDD to help prevent an additional voltage drop on VDD. The voltage drop across parasitics associated with the diode and package, as well as the limited size of the capacitor, however, will prevent the voltage from being clamped exactly to within a diode-drop of 5 V (e.g., to 4.3 V). The minimum voltage seen on the VDD pin is plotted as a function of the negative EFT voltage in Fig. 15. Measured and simulated values were within 5.5% in each test.

B. EFTs on I/O

Positive EFTs were injected to general purpose I/O when the I/O were set as inputs and when they were set as outputs.

1) Input Mode: In this mode, the output driver is turned-off and the input pull-up enable PFET is turned-on to make the default input a logical high. Current may be conducted from the I/O pin to the VDD rail through either the input pull-up enable PFET or the ESD protection diode. Thus, an EFT at an I/O pin may also create a disturbance on the VDD rail. This disturbance is illustrated in Fig. 16, which shows the voltage waveforms on the I/O pin and VDD pin when the EFT generator was set to positive 800 V and the EFT was applied to the I/O pin.

Fig. 17 shows the peak voltages at the I/O pin and the VDD pin as a function of the EFT generator voltage when injecting a positive EFT to the I/O pin. Results are shown both when approximating the input pull-up enable PFET as a resistor and (more correctly) as a FET. The advantage of the FET model becomes clear under a high-voltage EFT excitation where nonlinear effects are more important. Peak voltages are estimated within less than 1.5% using the FET model. As shown in the

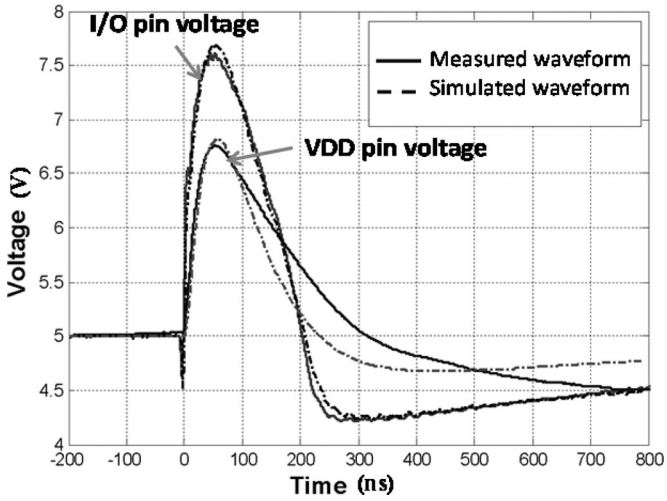

Fig. 16. Waveform on the VDD and I/O pins during a positive 800-V EFT injection to the I/O pin. The I/O pin was in input mode.

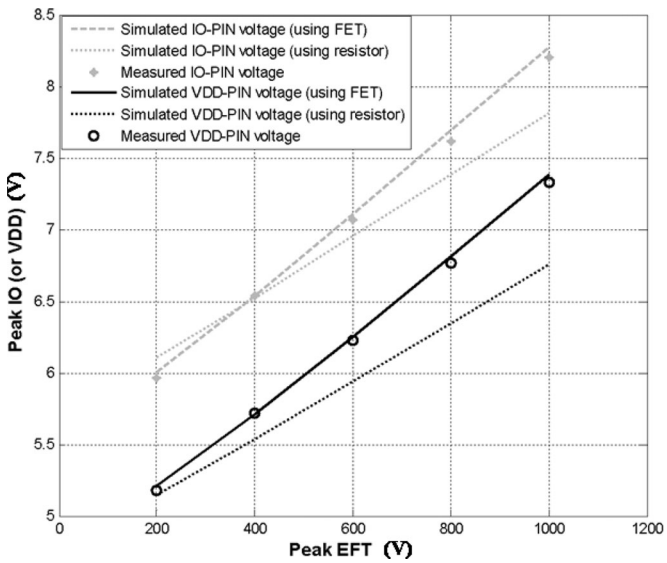

Fig. 17. Peak voltage on the VDD and I/O pin versus EFT generator voltage when injecting to an I/O pin in input mode.

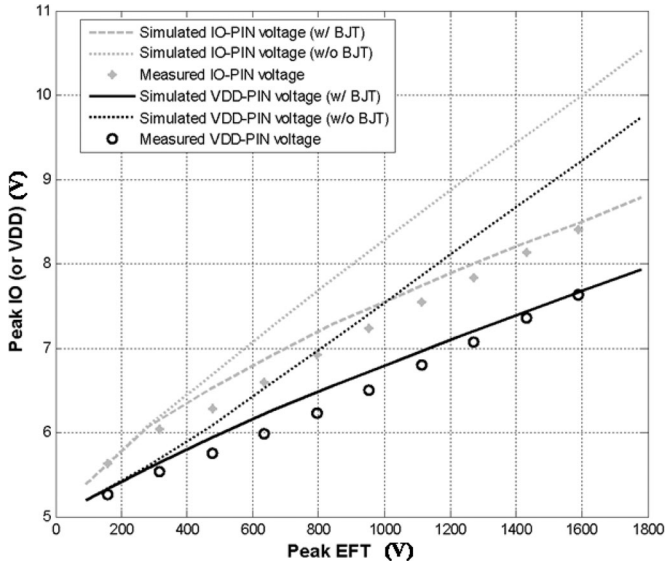

Fig. 18. Peak voltage on the VDD and I/O pin versus the EFT generator voltage when injecting to an I/O pin in output high mode.

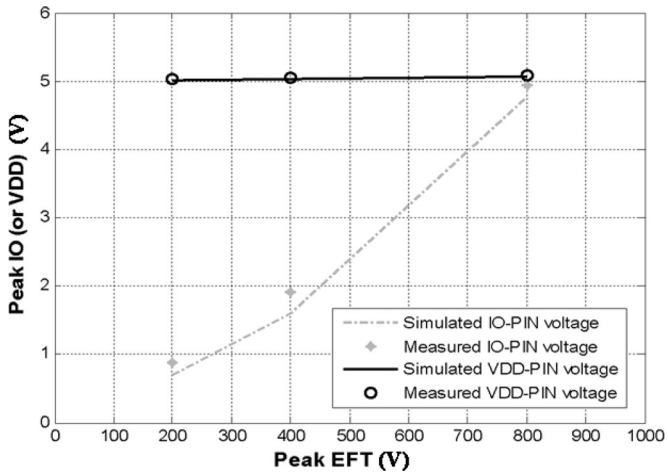

Fig. 19. Peak voltage on VDD and I/O pin versus EFT generator voltage when injecting to an I/O pin in output low mode.

figure, the voltage difference between the VDD pin and I/O pin is clamped to less than 0.8 V by the diode between them.

2) Output Logical-High: When generating an output high, the I/O pad is connected through a PFET to the VDD rail. A positive EFT will cause current to be injected through the PFET and the ESD diode to the VDD rail of the IC. Current will also be shunted to VSS through the parasitic BJT.

Fig. 18 shows the peak voltage on the I/O pin and the VDD pin as a function of the EFT generator setting, when injecting EFTs to the I/O pin in output high mode. Simulated results are given both with and without the parasitic BJT included in the model. If the BJT was not included, there was a poor match between simulated and measured data, especially when injecting high voltage EFTs, validating the need to include this parasitic within IC immunity models. As shown in Fig. 18, the parasitic BJT may change the simulated result by as much as 1.8 V (22%). After adding the parasitic BJT, the predicted and measured peak voltages agreed within less than 3.3%.

3) Output Logical-Low: When generating an output low, the I/O pin is connected to the VSS rail through the pull-down NFET. ESD protection circuitry or diodes are not turned on for reasonable values of EFTs. The I/O input looks primarily resistive. As a result and as illustrated in Fig. 19, the voltage at the I/O pin is roughly linearly proportional to the voltage at the EFT generator and there is minimal change in the voltage on the VDD pin with the EFT.

V. Conclusion

A relatively simple model was developed to predict the voltage and currents on the I/O pins and the power delivery

network of a commercial microcontroller during an EFT event. The model of the power delivery network was constructed based on an intuitive understanding of the IC layout and using external measurements to determine values of component parameters. A critical part of this model was an accurate description of the I/O and the ESD protection circuitry. For the study presented here, much of the I/O and ESD protection circuitry was made available from the IC manufacturer. In cases where this level of information is not available, a reasonable model of the I/O might be developed using IBIS models or using measurements [16], [17], assuming the ESD protection structures are relatively simple (e.g., diodes or snapback structures to VDD/VSS). More complicated structures, like the trigger circuit in the boost bus design, may be challenging to infer without a priori information. A critical part of the I/O model was a parasitic PNP BJT between the I/O pin, VDD, and VSS. This BJT allows significant current to be shunted from the I/O pin directly to the VSS bus during a positive EFT event. A similar parasitic NPN BJT may be important during negative EFT events. This NPN BJT may be characterized using similar methods to those used for the PNP BJT.

Using the methodology presented here, one can develop a model which accurately predicts the voltages or currents within the die. The presented model was able to accurately predict the voltage on the I/O or VDD pins within 5–6% (less than 200 mV) of the measured values in all tests. This model might be used in system-level tests to better evaluate the immunity of an IC than traditional IC-EMC models, like the traditional ICEM or LECCS models, which typically do not include nonlinear effects or simplify these effects for the prediction of emissions. More importantly, this relatively simple model can lead to a better understanding of the mechanisms behind immunity problems and how to fix them.

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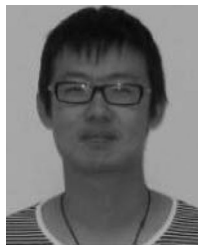
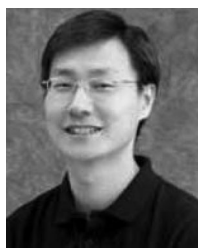


Ji Zhang received the B.S. and M.S. degrees in electronic engineering from Tsinghua University, Beijing, China, in 2005 and 2008, respectively. He received the Ph.D. degree from the Electromagnetic Compatibility Laboratory at the Missouri University of Science and Technology, Rolla, MO, USA, in 2013.

He is currently working for Cisco Systems Inc. His current research interests include the immunity of integrated circuits (ICs) to electrical fast transient events and electrostatic discharge events, IC power delivery network modeling, reconstruction of emission sources, modeling/optimization for high-speed series-link channel, and power integrity of board and ASIC package.



Jayong Koo (S'06) received the B.S.E.E. degree from Chung-Ang University, Seoul, Korea, in 1996, the M.S.E.E. degree from Yonsei University, Seoul, in 1998, and the Ph.D. degree in electrical engineering from the Missouri University of Science and Technology, Rolla, MO, USA, in 2008.

From 1998 to 2004, he was with LG Electronics, Seoul, Korea for four years and with Dacom, Korea for two years. In 2008, he joined Intel Corporation, Hillsboro, OR, USA. His current research interests include signal & power integrity, radio-frequency interference, and electromagnetic compatibility.

Richard Moseley (M'09) received the B.S.E.E. degree from Texas A&M University, College Station, TX, USA, in 1981.

In 1981, he joined Motorola, and in March 2005, he joined the electromagnetic compatibility engineering team as an Applications and Systems Engineer. He is currently a Senior EMC Engineer with the Microcontroller Solutions Group, Freescale Semiconductor, Inc., Austin, TX, where he is engaged as an Electromagnetic Compatibility Test and Validation Engineer.

Scott Herrin (M'99) received the B.S. degree in physics from Mississippi College, Clinton, MS, USA, in 1994, and the M.S. degree in electrical engineering from Texas A&M University, College Station, TX, USA, in 1999.

From 1992 through 1994, he was with Advanced Microelectronics. Since 1997, he has been a Member of the technical staff at Freescale Semiconductor, Inc., Austin, TX, where he has been engaged in analog circuit design.

Xiang Li received the B.S. degree in electronic information engineering from Jilin University, Changechun, China, in 2007, the M.S. degree in electrical engineering from Missouri University of Science and Technology, Rolla, MO, USA, in 2010.

She is currently an Electromagnetic Compatibility Engineer working for Freescale Semiconductor, Inc., Austin, TX, USA. Her current research interests include the radiated emission and immunity of integrated circuits (IC), conducted emission and immunity of the IC, electrostatic discharge event modeling, and crosstalk within harness bundles.

David Pommerenke (SM'03) received the Ph.D. degree from the Technical University Berlin, Berlin, Germany, in 1996.

He was with Hewlett Packard for five years. In 2001, he joined the Electromagnetic Compatibility Laboratory, Missouri University of Science and Technology, Rolla, MO, USA, where he is currently a Professor. He has authored or coauthored more than 200 papers and is inventor on 13 patents. His current research interests include system-level ESD, electronics, numerical simulations, electromagnetic compatibility measurement methods, and instrumentations and measurement/instrumentation ESD and electromagnetic compatibility.

Dr. Pommerenke is an Associate Editor for the IEEE TRANSACTIONS ON ELECTROMAGNETIC COMPATIBILITY.

Daryl G. Beetner (S'89–M'98–SM'03) received the B.S. degree in electrical engineering from Southern Illinois University, Edwardsville, IL, USA, in 1990. He received the M.S. and D.Sc. degrees in electrical engineering from Washington University in St. Louis, St. Louis, MO, USA, in 1994 and 1997, respectively.

He is currently a Professor and the Chair of Electrical and Computer Engineering at the Missouri University of Science and Technology (formerly called the University of Missouri—Rolla), Rolla, MO, USA. He conducts research with the Electromagnetic Compatibility Laboratory at Missouri Science and Technology, Rolla, MO, on a wide variety of topics including electromagnetic compatibility at the chip and system level and detection and neutralization of explosive devices.

Dr. Beetner is an Associate Editor for the IEEE TRANSACTIONS ON INSTRUMENTATION AND MEASUREMENT.