Enabling World's first over 4.4Gbps/pin at sub-1V LPDDR4 Interface using Bandwidth Improvement Techniques

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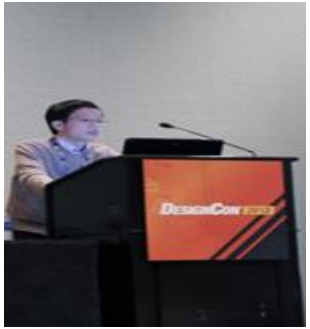
Jinho Choi, Kwanyeob Chae (Samsung)

SPEAKERS



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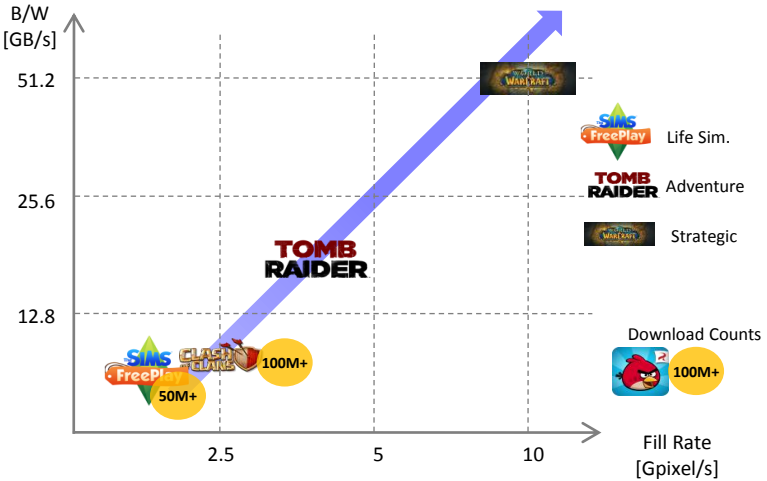
Previous DesignCon

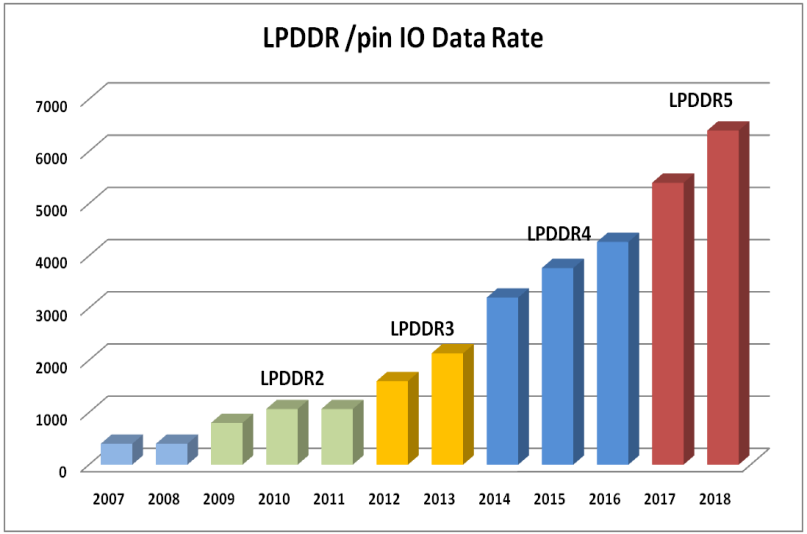
Outline

- **Technical Trend**
- **Valid Window Margin(VWM)**
- **Proposed LPDDR4 Interface:**
  - Low C_{IO} Multi-V_{OH} level Driver and Receiver
  - Duty Adjustment Scheme
  - Asymmetric Rise/Fall time Control Scheme
  - On-die De-cap. Estimation
  - Clean Data Strobe(DQS) Signal
- **DQS Cleaning Method**
- **Test Results**
  - Valid Window Margin(VWM)
- **Conclusion**

Memory Interface Speed Trend

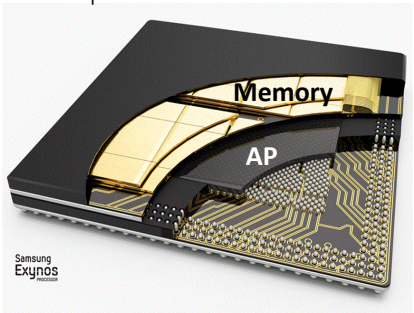
- **Future AP must have GPU performance to run high spec. PC games**
- **Double the bandwidth every other year**





Design Challenges

- **On-chip**
  - Logic speed ↑, Gate counts ↑
  - IR drop↑, Dynamic Voltage Drop(DvD) ↑
  - Clock path jitter ↑, duty distortion ↑
- **Off-chip**
  - PKG size ↓
  - Cross talk ↑
- **Process**
  - Process uncertainty↑
- **Memory**
  - Timing parameter variation ↑
  - Density ↑



- **Purpose of DDRPHY**

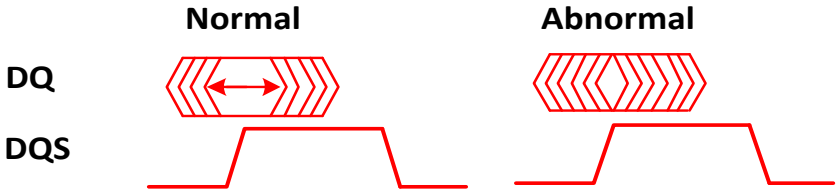
Maximize the valid window margin under P/V/T variations, thereby providing reliable memory access

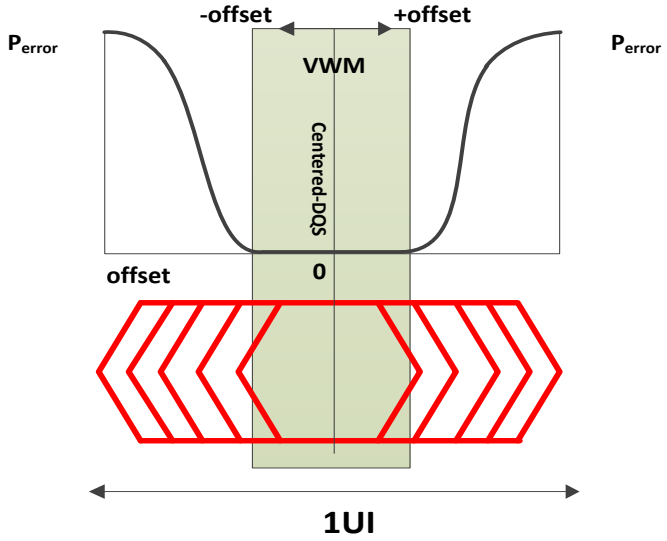
PHY makes DQS edge is centered at DQ window at memory or PHY

If not, the probability of bit-flip error increases

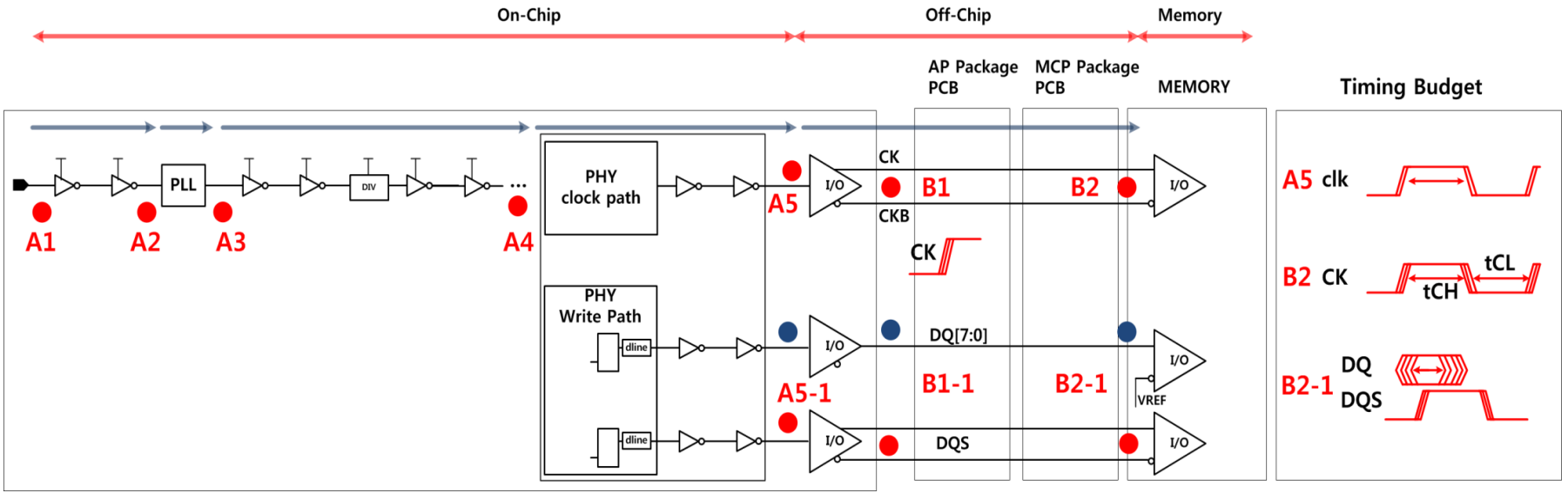
➔ **Hard to meet timing requirement on controller side**

What is Valid Window Margin(VWM)





WRITE Mode VWM



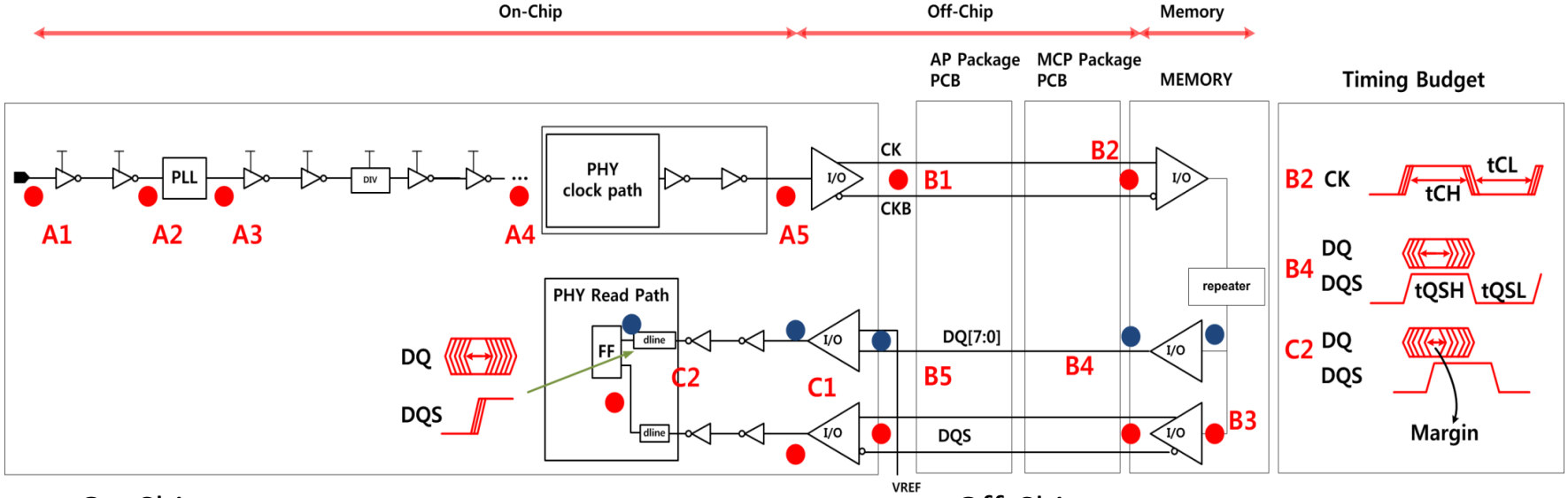
On-Chip

- Reference clock jitter (A1-A2)
- PLL jitter (A3)
- Clock network jitter (A3-A5)
- Clock network duty (A3-A5)

Off-Chip

- Off-Chip clock jitter (A5-B2)
- Off-Chip clock duty (A5-B2)
- Off-Chip eye open ((A51-1)-(B2-1))

READ Mode VWM



On-Chip

- Reference clock jitter (A1-A2)
- PLL jitter (A3)
- Clock network jitter (A3-A5)
- Clock network duty (A3-A5)
- Read path jitter (B5-C2), Read path duty (B5-C2)

Off-Chip

- Off-Chip clock jitter (A5-B2)
- Off-Chip clock duty (A5-B2)
- Off-Chip eye open (B3-B5)

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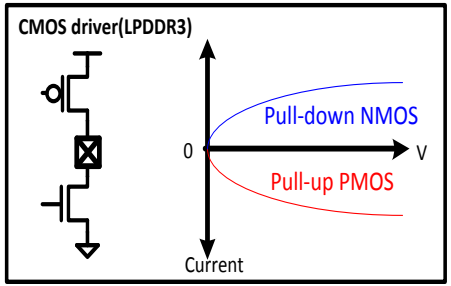
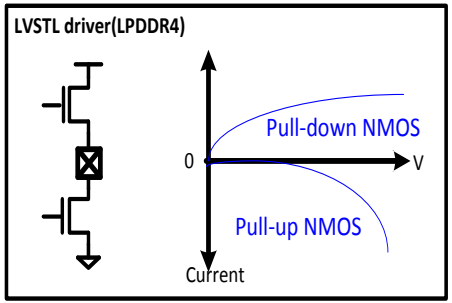
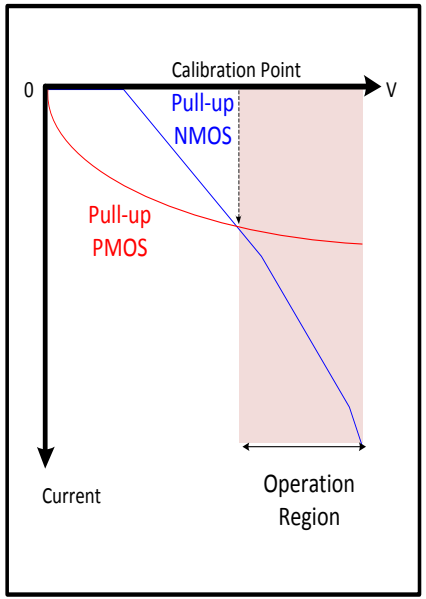
LPDDR4 Signaling and Multi-V_{OH} Driver

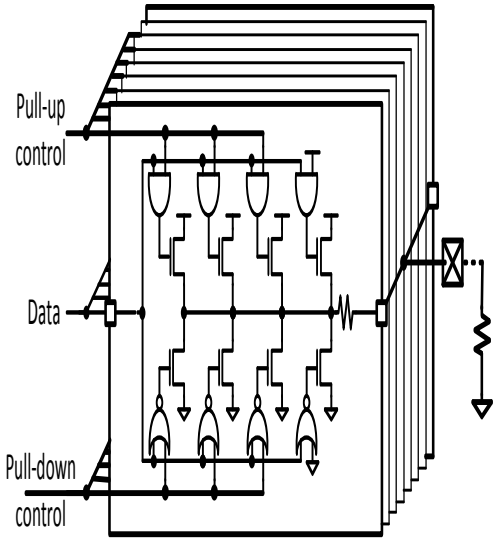
- Difference Between LPDDR3 and LPDDR4

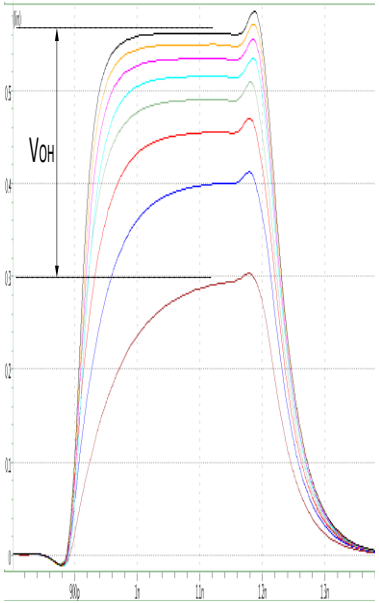




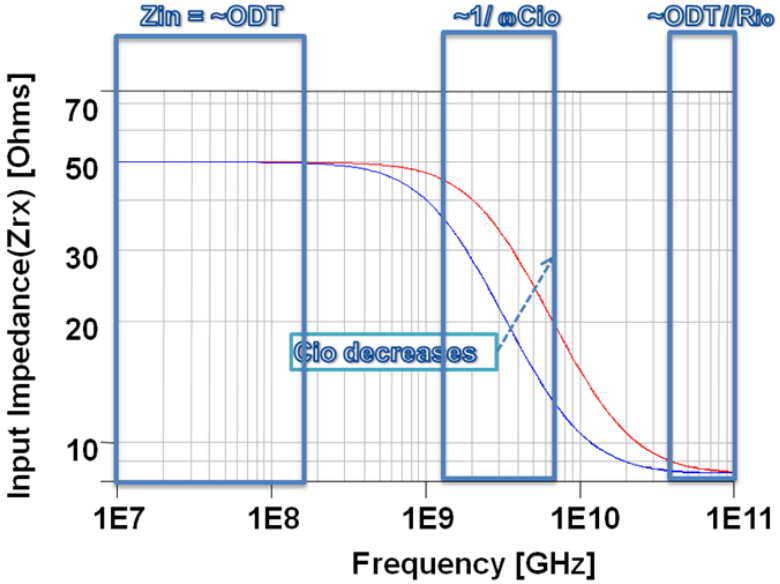


- Multi-V_{OH} Driver

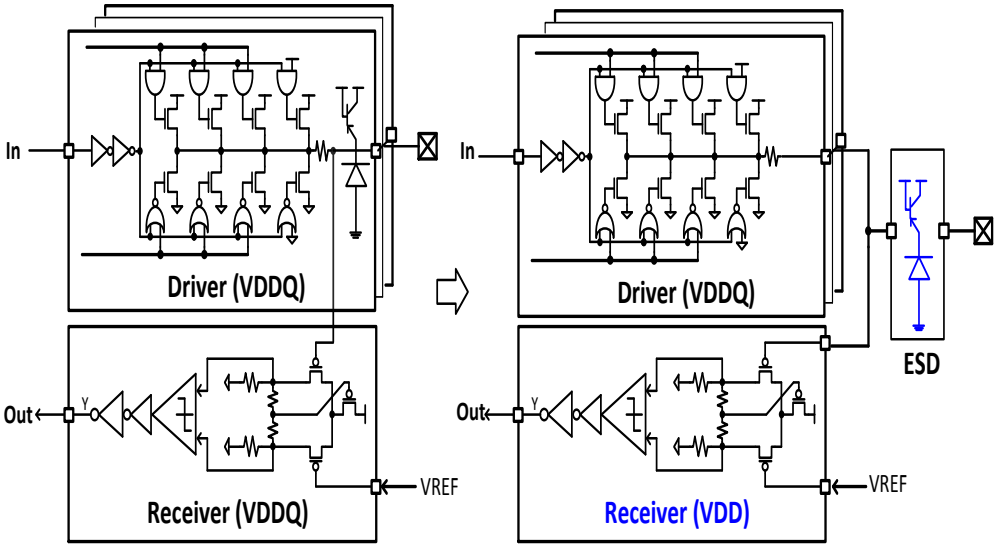




Low Cio Transceiver



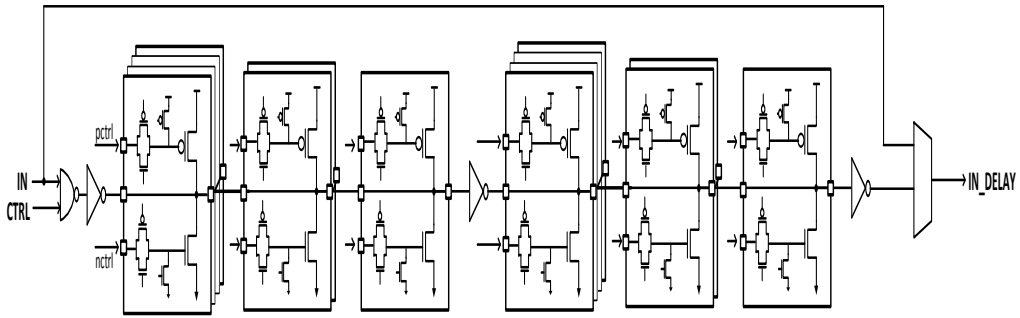
[Source: DesignCon2013]



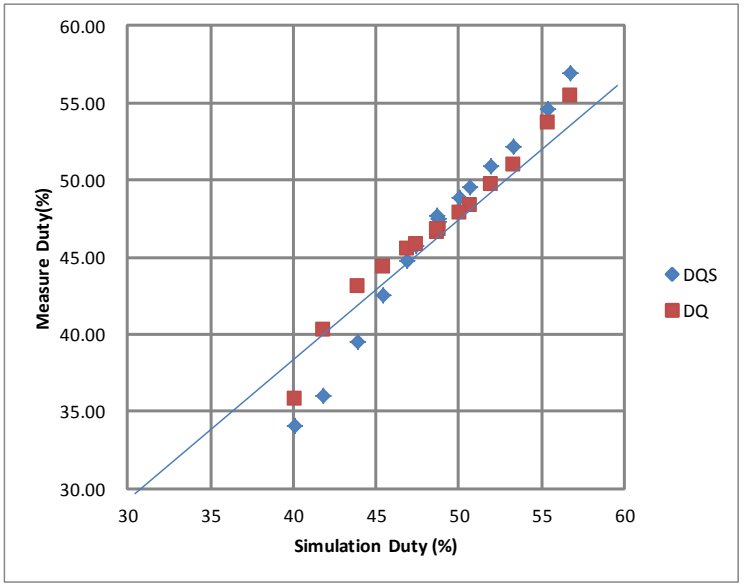
Proposed Transceiver Block

Duty Adjustment Scheme(1)

The duty control block is located at the first stage of I/O and it consists of two CMOS inverter group which is composed by the different kinds of strength pull up and down transistors.

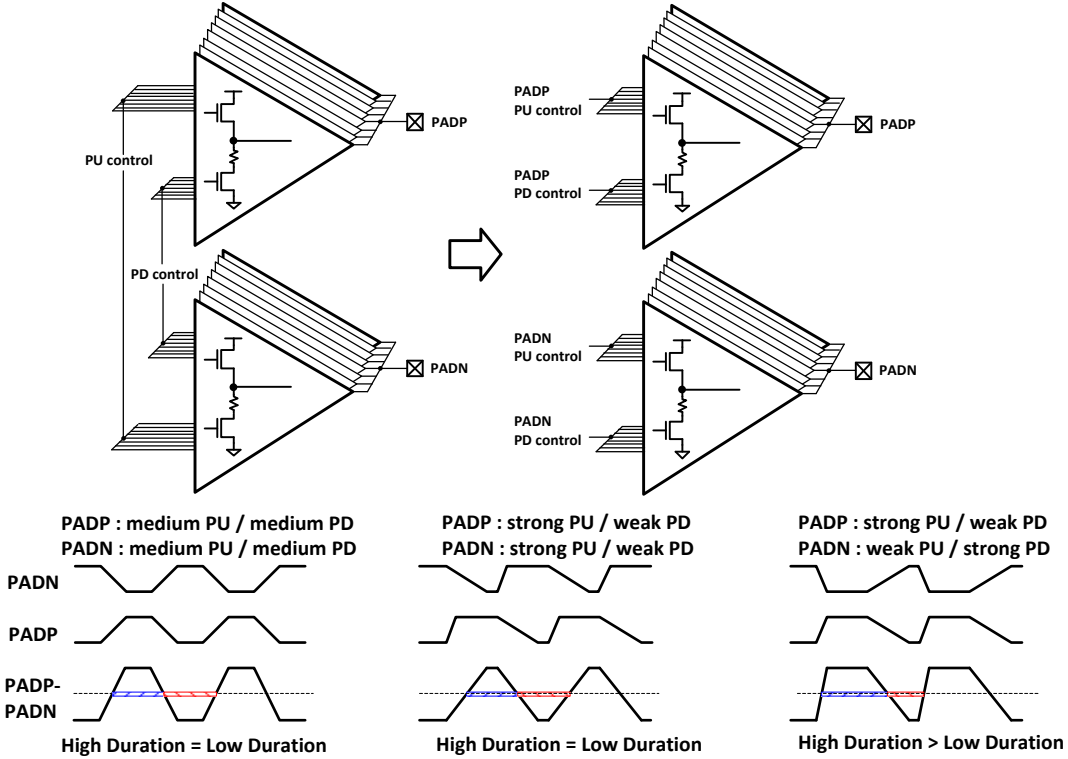


Driver Duty Control Scheme



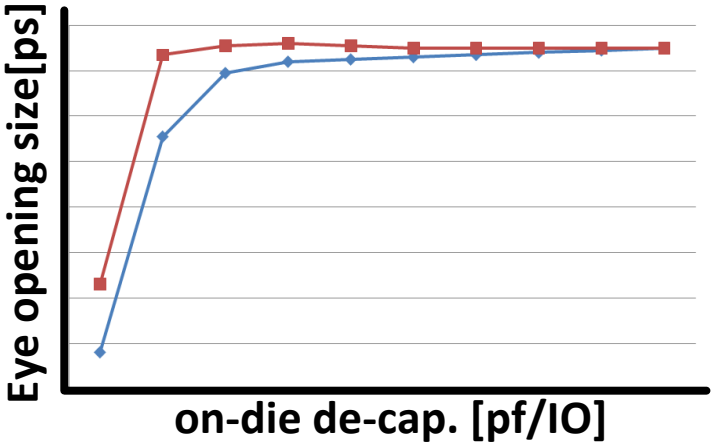
Duty Ratio Range

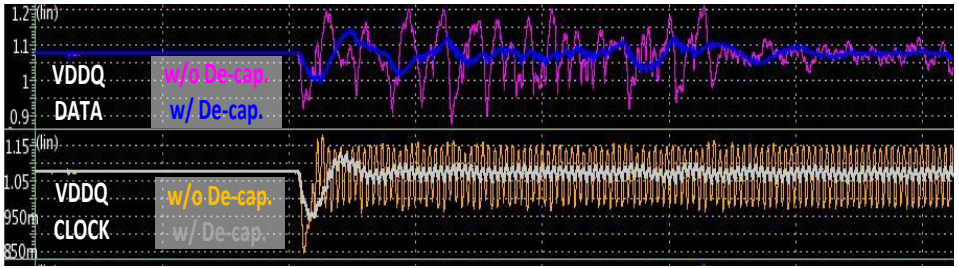
Duty Adjustment Scheme(2)



Asymmetric pre-driver control scheme for DQS(or CLK) PAD can be adjust rise/fall time of PADP and PADN independently.

On-Die De-Cap. Estimation





It is very critical to achieve cost-effective PDN design with optimized on-die power delivery network including de-cap and power/ground grids. Also to reduce SSO noise in weak Power Delivery Network (PDN) condition such as POP package environment, On-die de-cap insertion is considered, but adding on-die de-cap increases the chip size as one of negative sides.

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- Test Results
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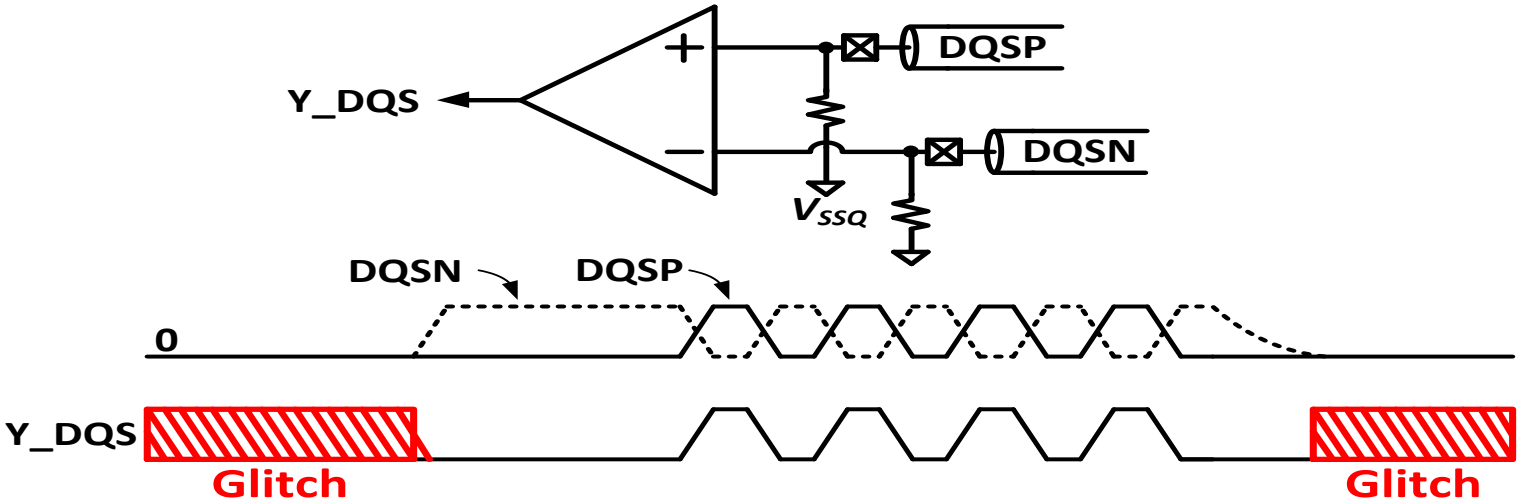
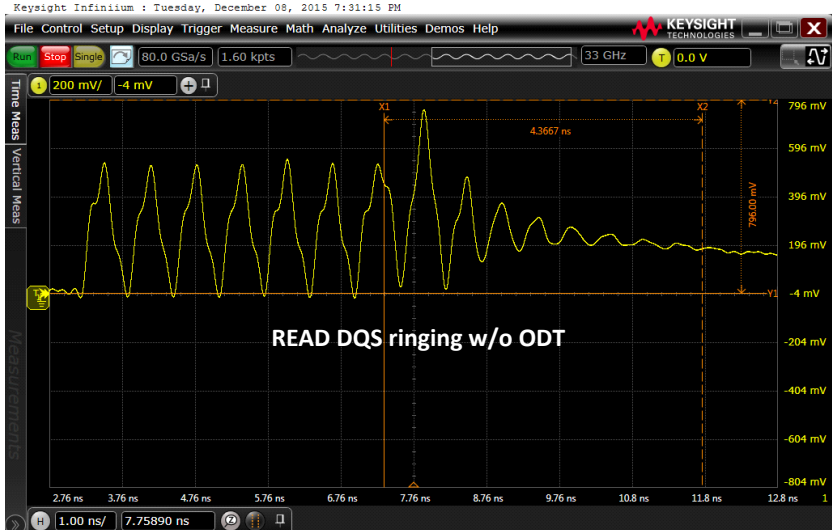
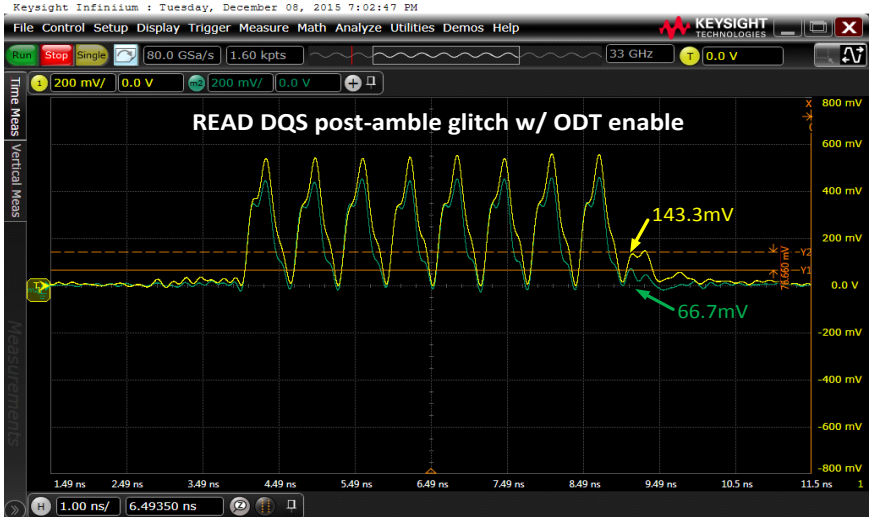
READ DQS Glitch



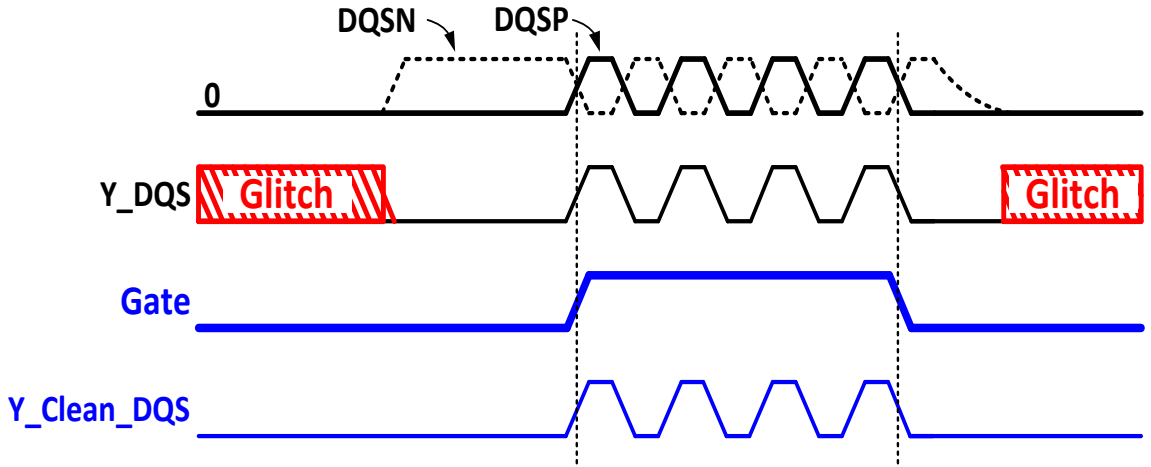
- Y_DQS used for clock in read-FIFO
- At idle state (DQSP=DQSN=0)
  - ➔ Glitch occurs on DQS receiver output (Y_DQS)
  - ➔ READ FAIL

READ DQS Measurement





Remove DQS Glitch



- During READ operation,

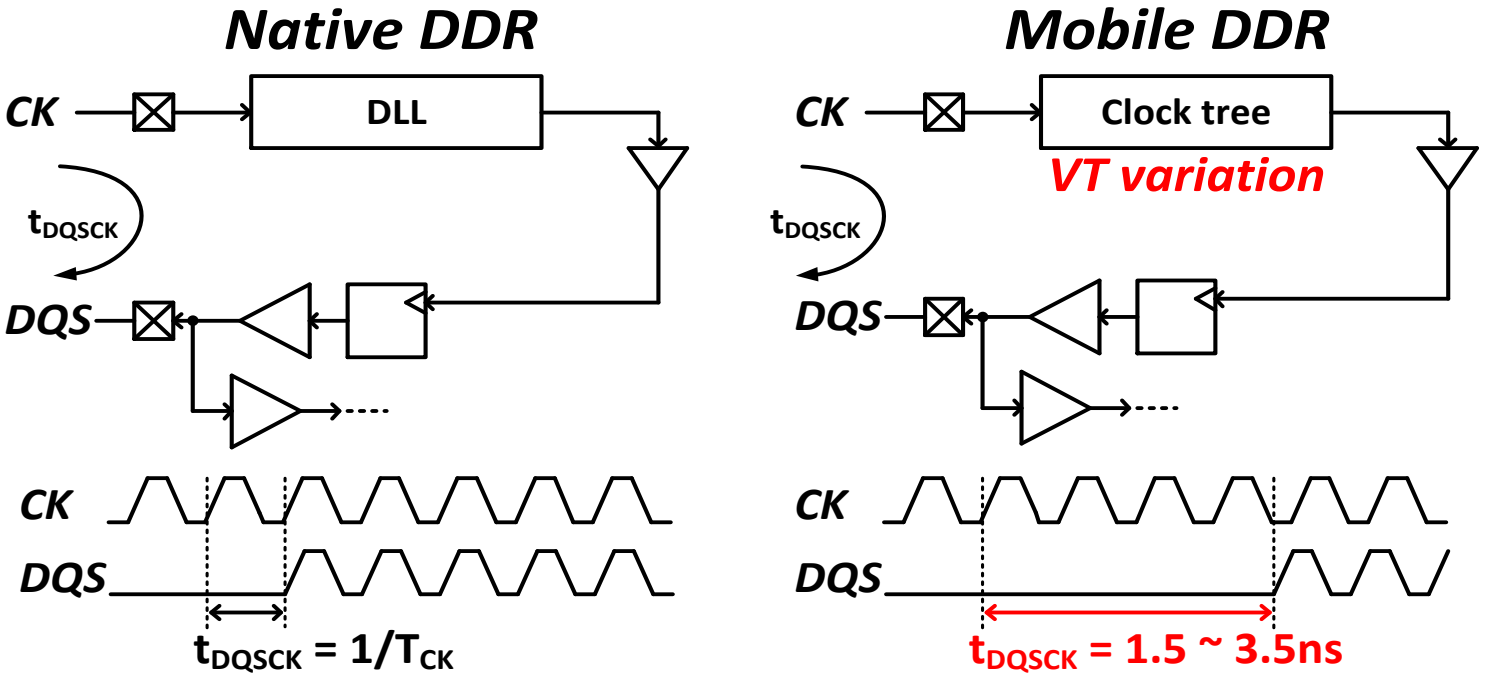
  ➔ glitch occurs on Y_DQS at idle state (DQSP=DQSN=0)

- Initial gate training,

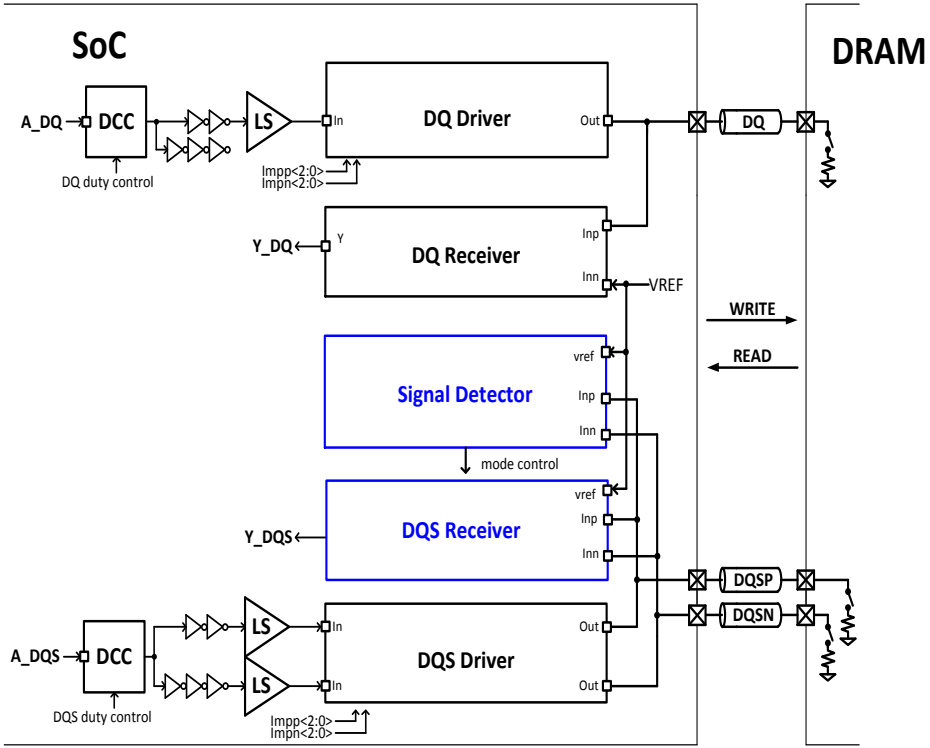
  ➔ generate optimized gate pulse to filter out glitch

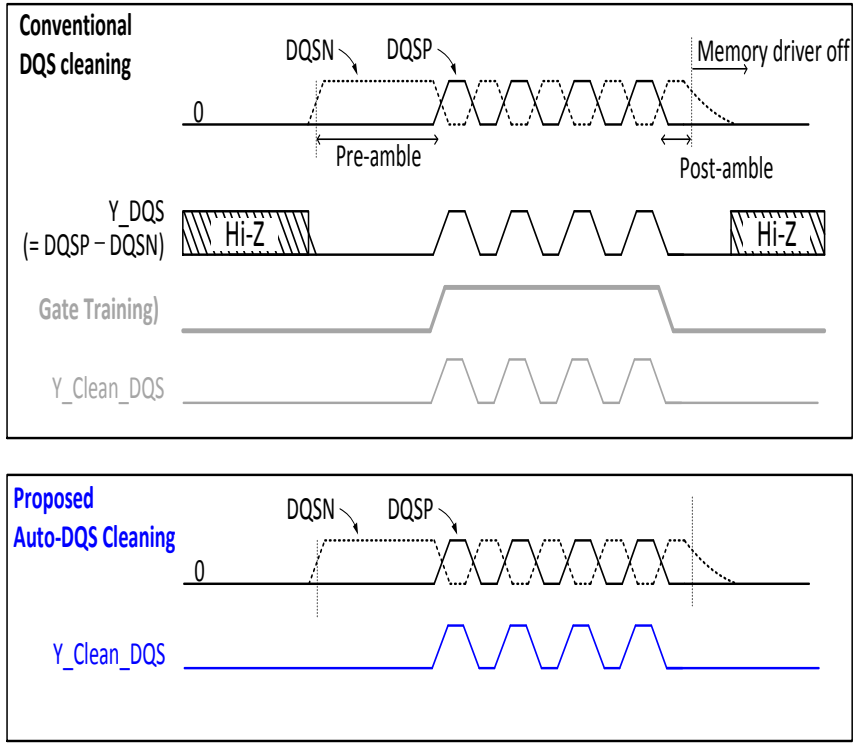
DQS2CK Variation in Mobile DDR

- Large DQS2CK variation in mobile DDR due to absence of DLL



Proposed DQS Cleaning Method





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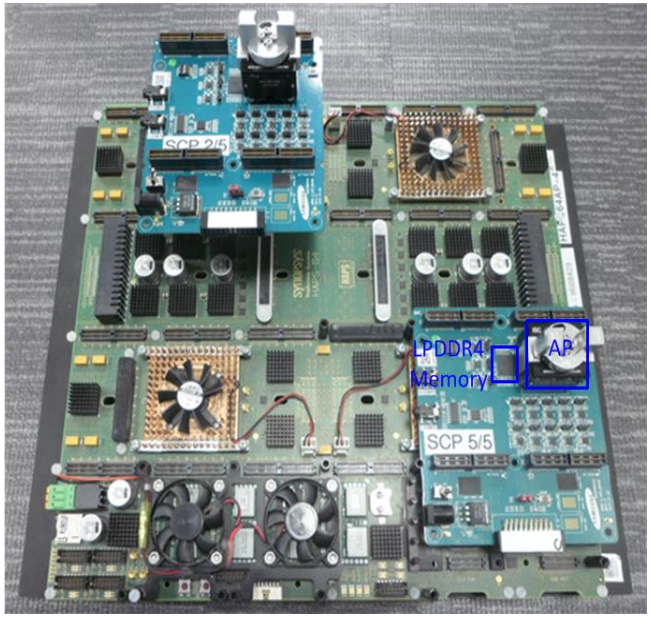
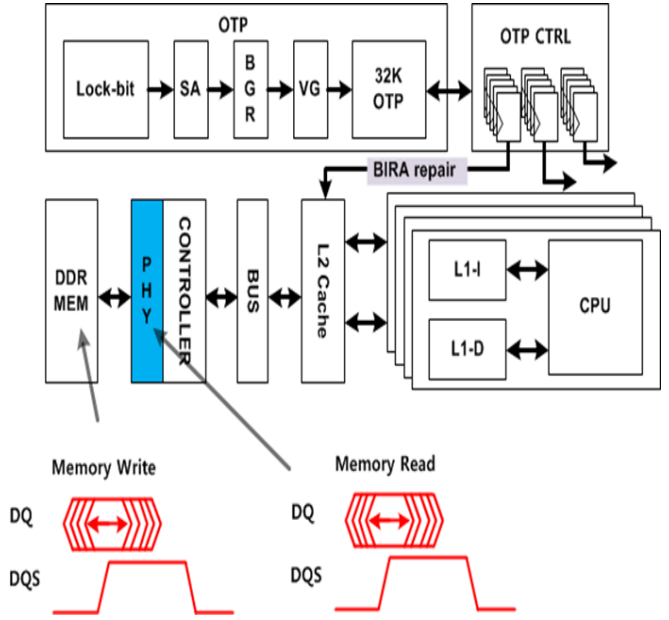
Test Environment



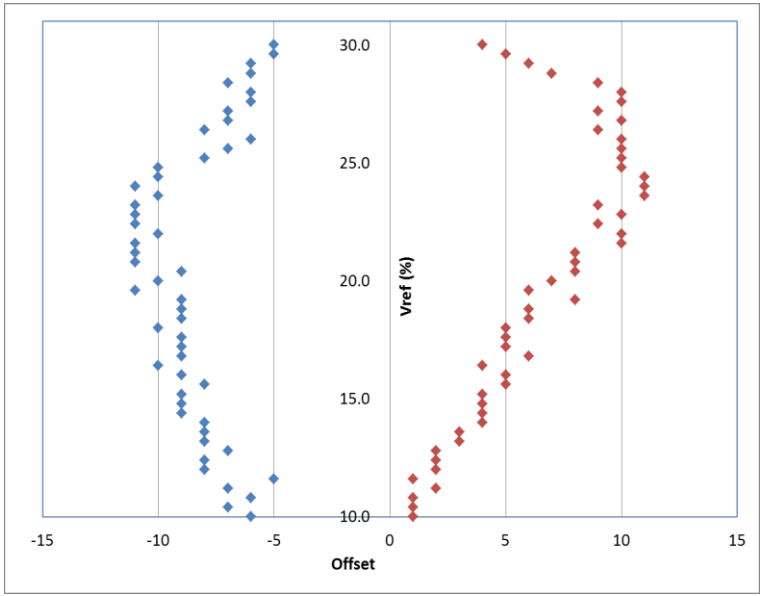
Test Board



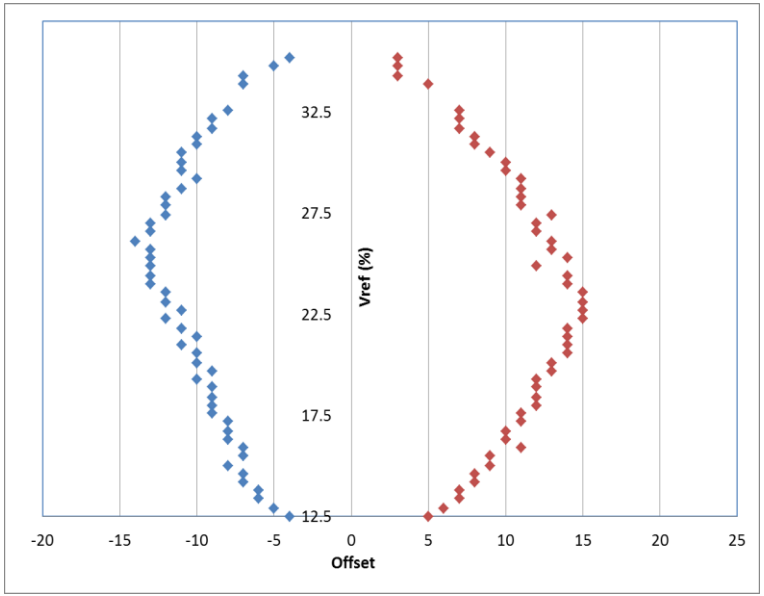
Test Chip

Test Results

- Memory RAED/WRITE operation over 4.4Gbps with sufficient timing margin

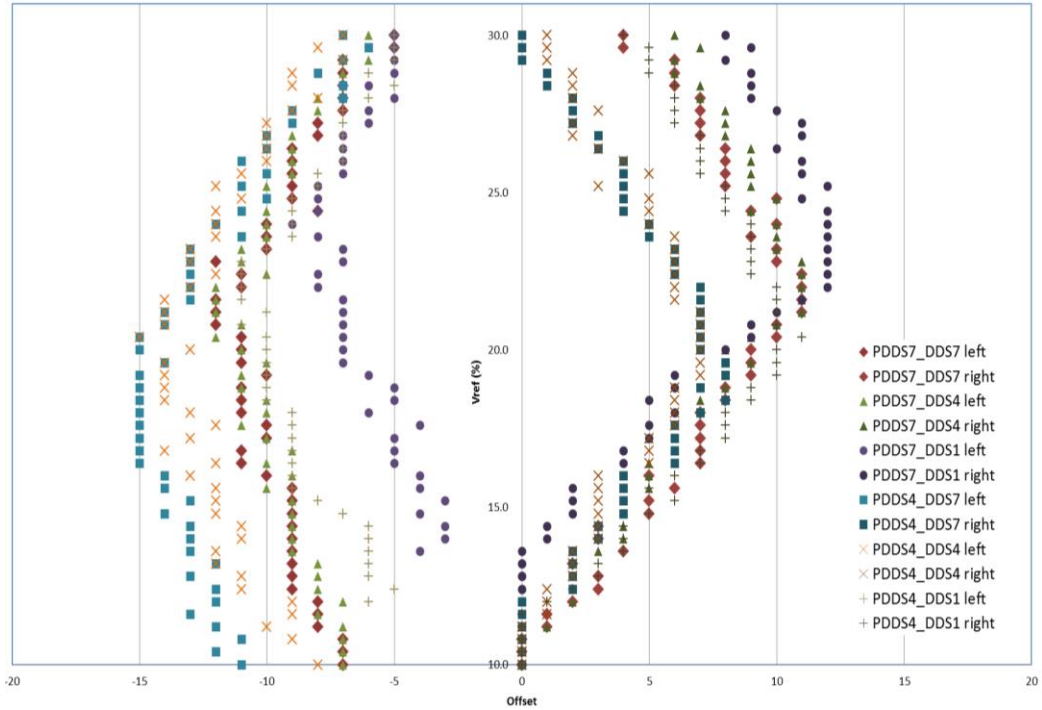


WRITE VWM @4420Mbps



WRITE VWM @4420Mbps

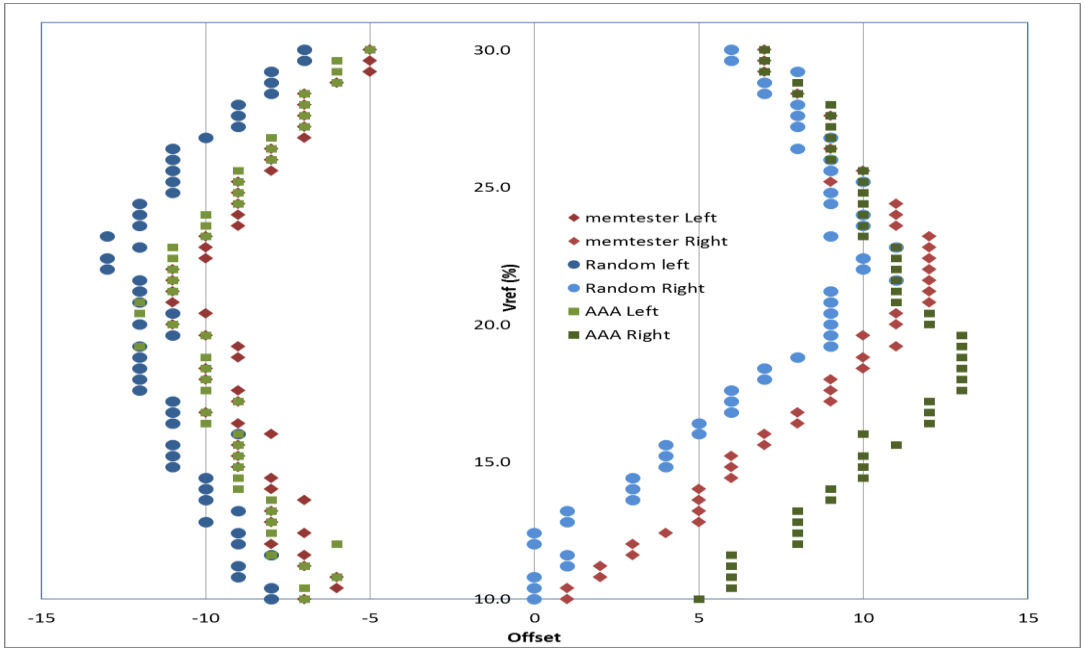
Test Results



- **Driving Strength Dependency**
  - PDDS : pull-up driving strength
  - DDS : pull-down driving strength
  - Good VWM size: PDDS7-DDS7, PDDS7-DDS4, PDDS4-DDS7
  - DDS setting should be deiced VWM and power consumption

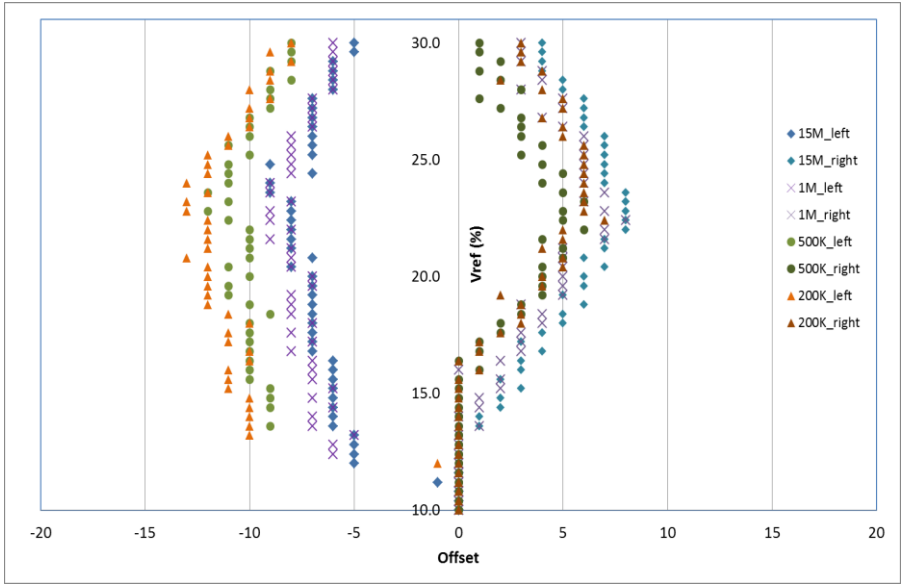
Test Results

- **Pattern types affects VWM size and offset**
- **Memtester pattern was used to measure VWM**



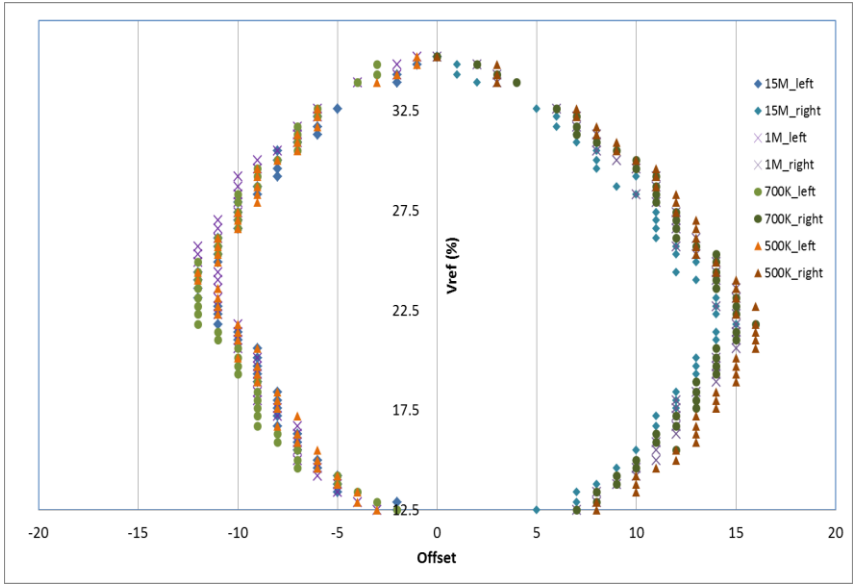
Test Results

- **Optimal test pattern size**
  - WRITE : 500KB



WRITE

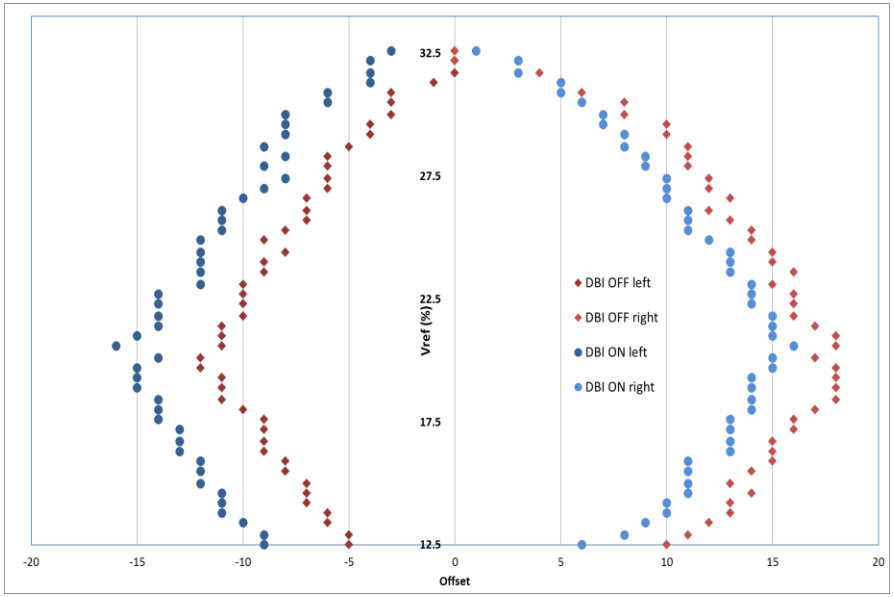
- **Optimal test pattern size**
  - READ : 1MB



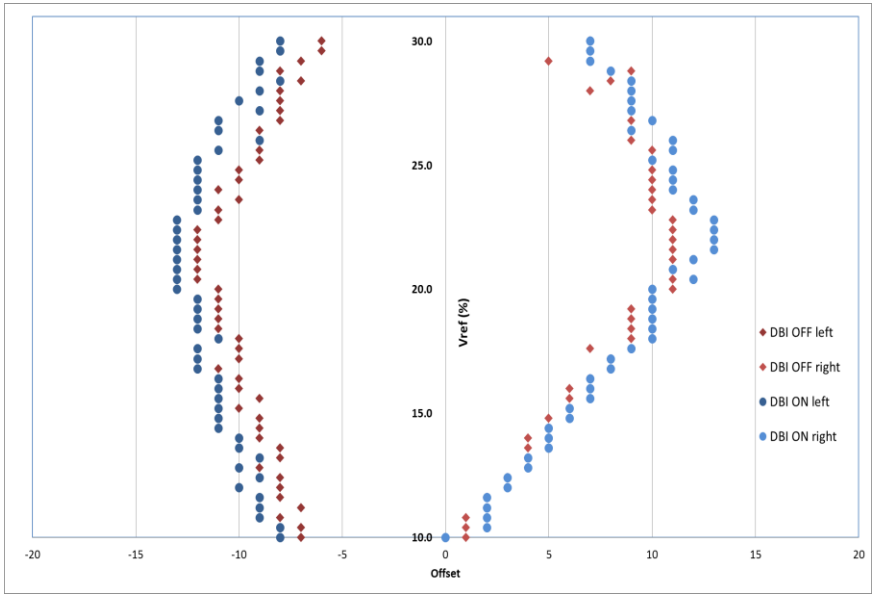
READ

Test Results

- **DBI function affects VWM size and power consumption**



READ



WRITE

Conclusion

- Introduce Valid Window Margin
- Proposed performance improvement IO design technique
- DQS Cleaning Method
- Various VWM test results
- 4420Mbps@0.9V LPDDR4 interface using 10nm FinFET process

Thank you!

QUESTIONS?