Capturing (LP)DDR4 Interface PSIJ and RJ Performance

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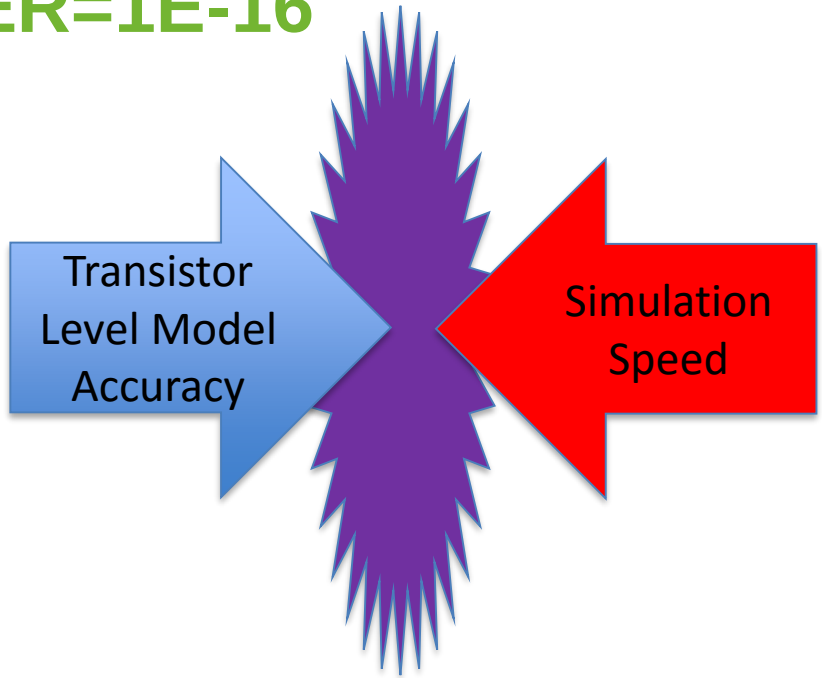
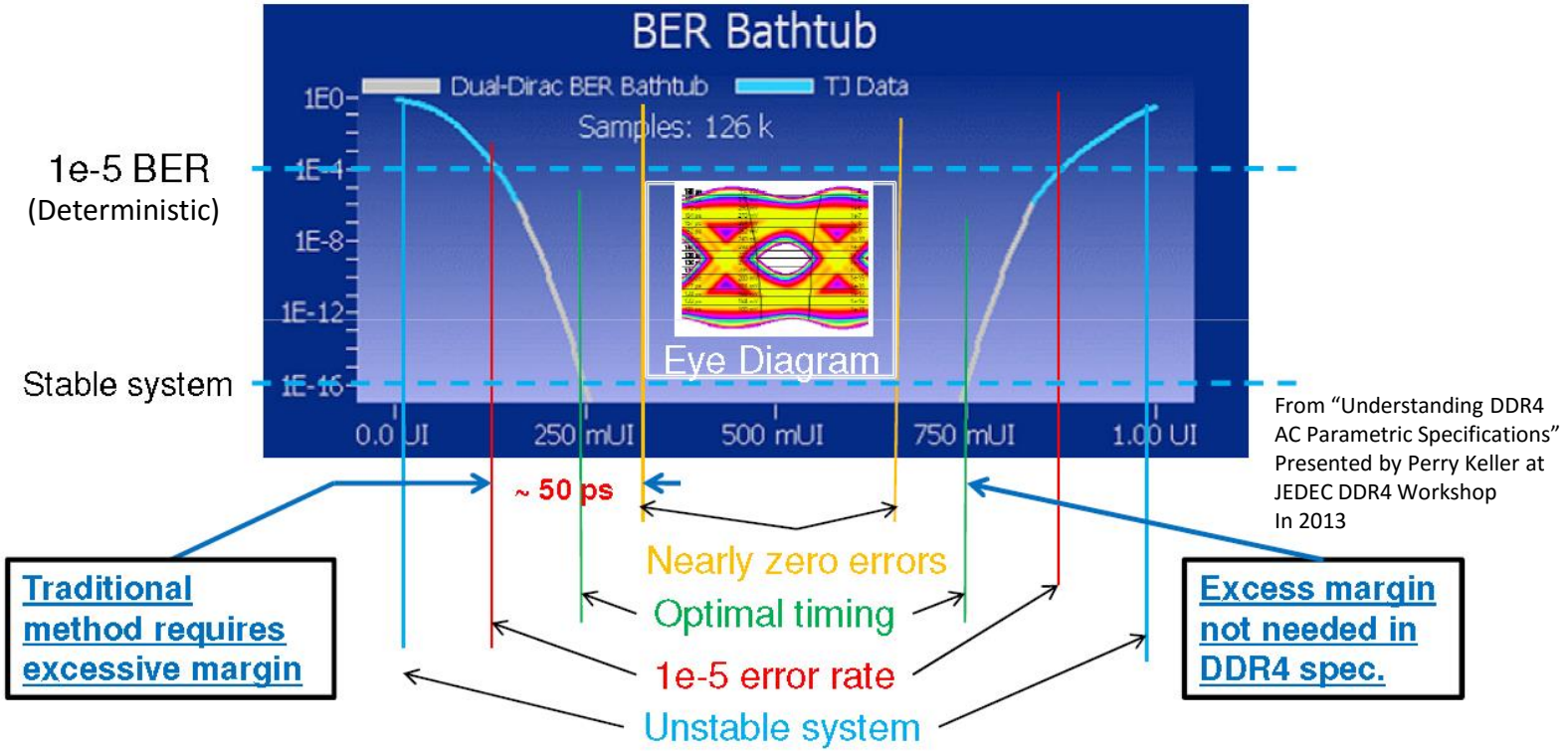
Challenge:
Simulate SSO Effects at BER=1E-16

- **DDR4 and LPDDR4 now have explicit BER requirements.**
- **Simulating $1x10^{16}$ Bits Requires:**
  - Lots of time in a SPICE Simulator…
  - Or
  - A Linear Time Invariant environment in a statistical simulator
- **Capturing SSO Effects *Accurately* Requires:**
  - Transistor Level models (Slow)
  - SSO Effects are non-Linear



Mutually Exclusive?

Prior to DDR4, Padding was Added to DRAM Specs



From "Understanding DDR4 AC Parametric Specifications" Presented by Perry Keller at JEDEC DDR4 Workshop In 2013

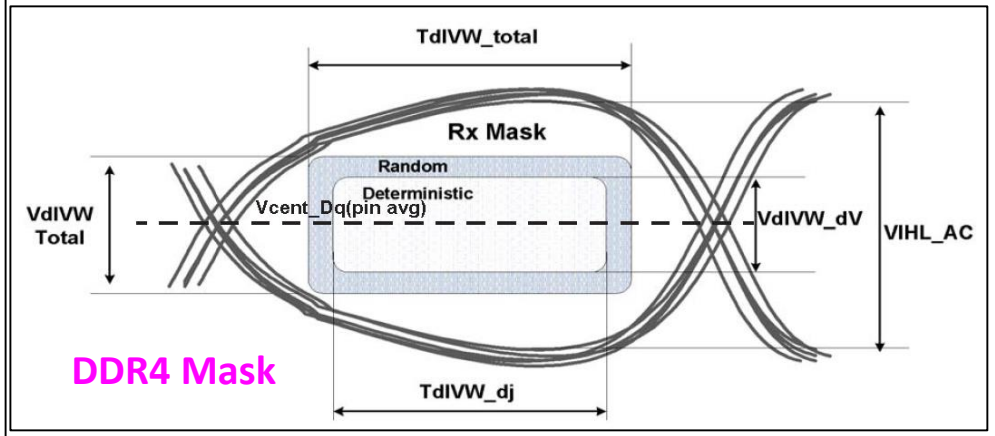
DDR4/LPDDR4 Eye with RJ Requirement

- The DDR4/LPDDR4 mask reports a total that includes a fixed deterministic jitter requirement plus a random jitter requirement.

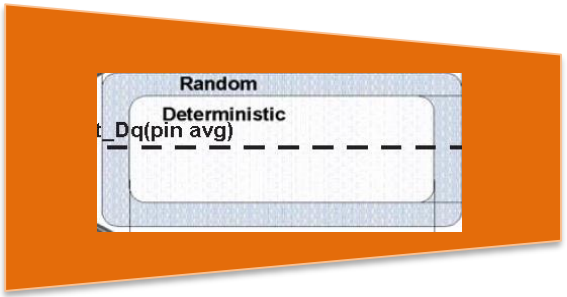
- The RJ requirement is still TBD, but BER of 1E-16 is the anticipated spec.

- If the RMS jitter value is known, the spec window can be varied to reflect the desired BER performance

- The mask assumes time and voltage training, unlike DDR3.

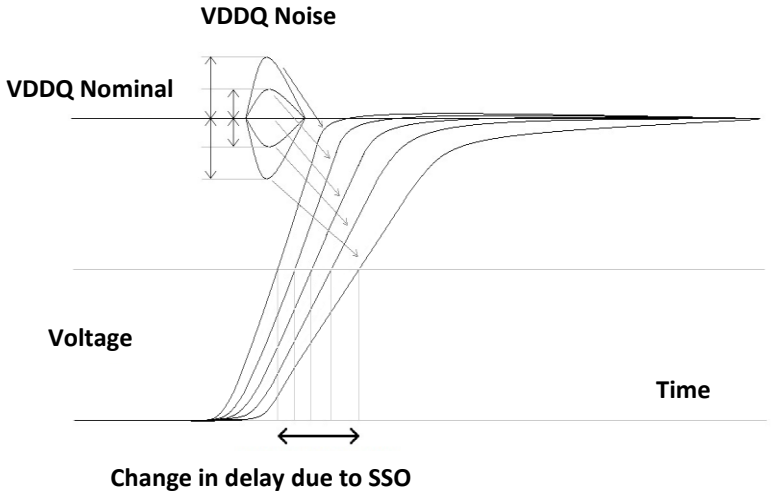


Compare DDR3 to DDR4 Mask

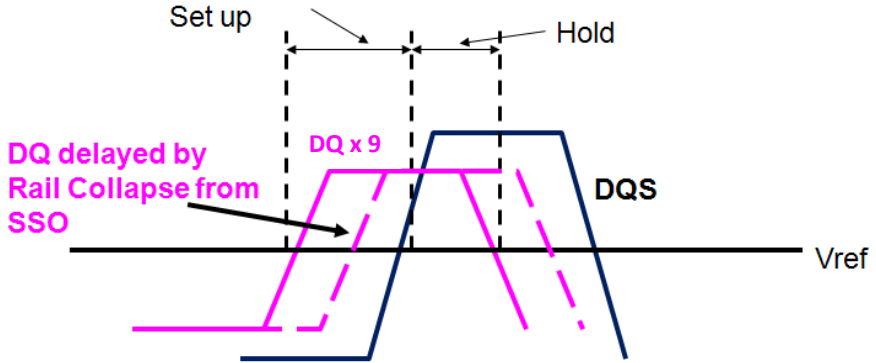


DDR Timing is Dominated by Rail Collapse from Simultaneously Switching Outputs

- Rail noise will delay or speed up edges.
- Droop increases delay through circuits.
- The IO response to rail noise is non-linear



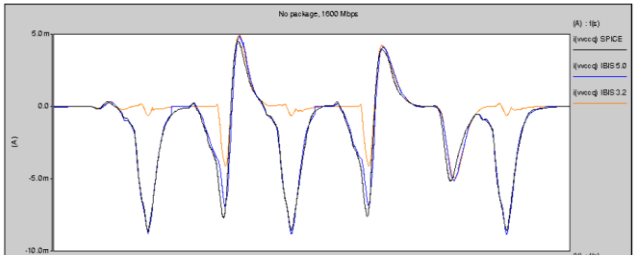
- DQ7:0, DM switch 90° out of phase with DQS.
- Pushout from rail droop erodes Set Up



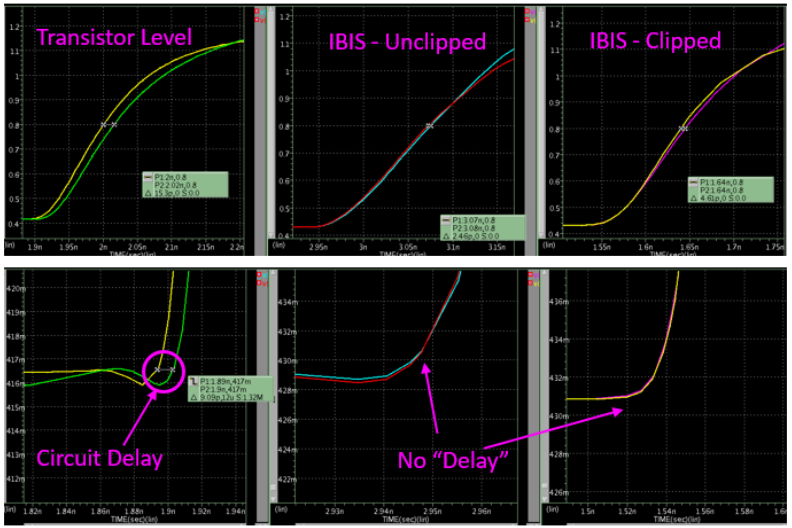
Is IBIS an Option?

- Power Aware IBIS does a good job of matching the currents generated by the SPICE model, especially when compared to older IBIS buffer models.
- IBIS does not do as good a job capturing the PSIJ created by the currents.
- The key difference is the absence of increased delay through the circuitry.
- Power Aware IBIS may have a role in modeling aggressor currents with a SPICE model as the victim.

Currents from SPICE v. IBIS 5.1 and 3.2
Good Match with 5.1



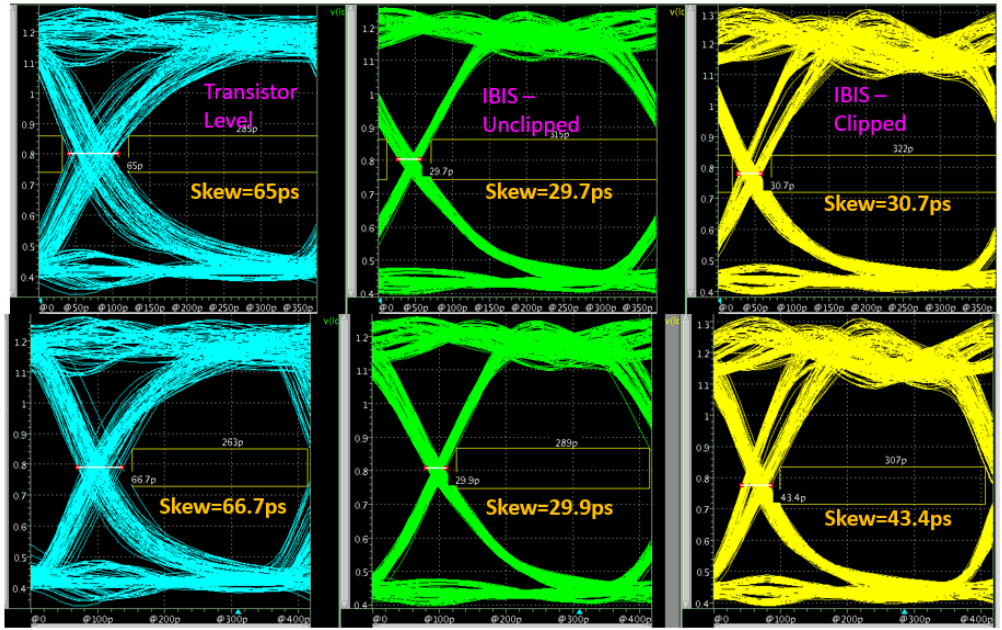
Pushout from Power Rail Collapse



IBIS v. Spice Models

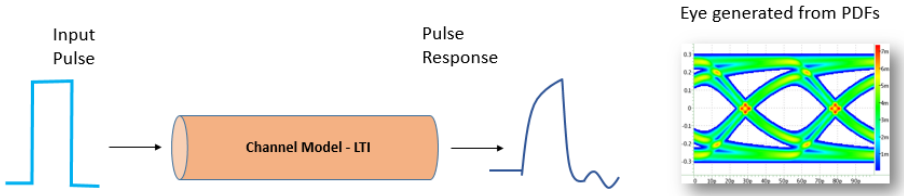
Ideal UI Trigger

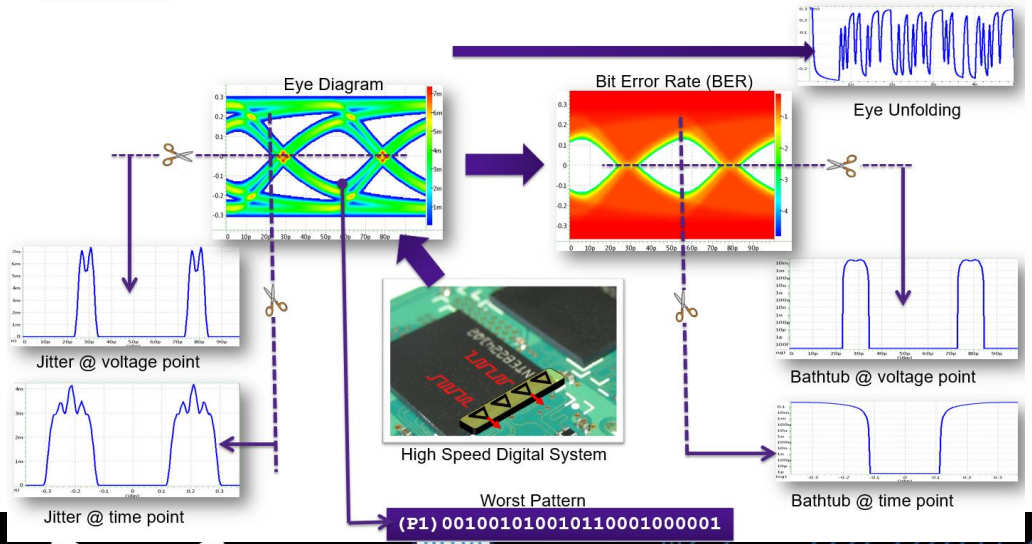
DQS/DQS# Trigger



Leveraging HSPICE® STATEYE Functionality to Capture SSO effects.

In its simplest form STATEYE captures the Pulse response from an LTI system…



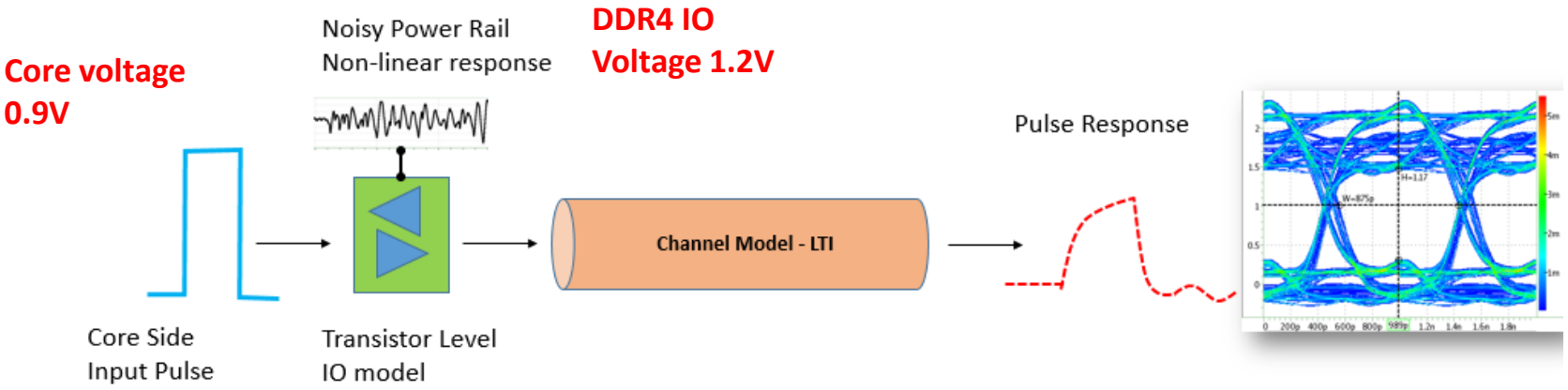


From this, BER information and bathtub curves can be generated to characterize the DDR interface

The STATEYE functionality can also support non-linear effects.

Can we capture SSO performance adequately?

Including the IO Model in the STATEYE Simulation



- The IO becomes part of the channel with the stimulus port applied to the core voltage domain.
- The pulse response is on the IO voltage domain.

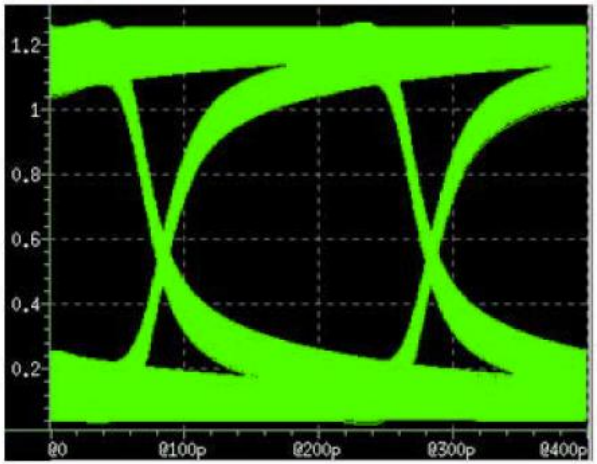
- Current for the IO is drawn from a non-ideal supply path
- The resulting power rail noise creates a non-linear response with the output signal distorted by the SSO noise.

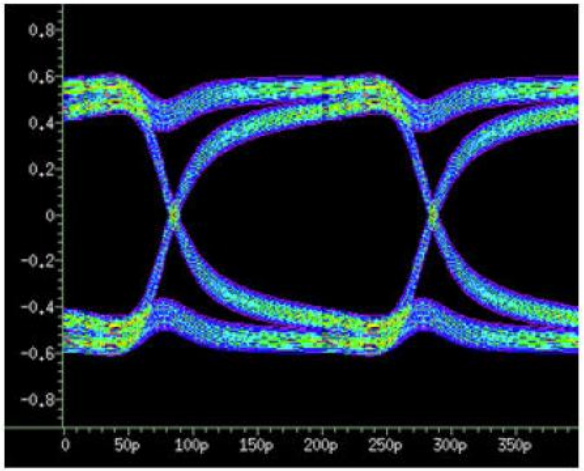
Capturing Non-Linear Response with “Multi-Edge” Mode and “Full Transient” Mode.

- SPICE response on left shows a simple non-linearity with a falling edge faster than the rising edge.
- The standard STATEYE pulse response on the right does not capture this.
- HSPICE implementation of STATEYE includes a edge response methodologies to capture these effects…

SPICE Analysis shows differing edge responses for rise and fall.

Crosspoint concerns

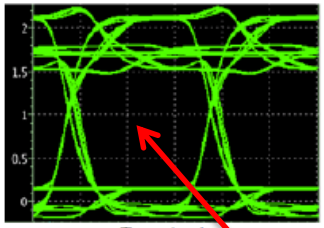




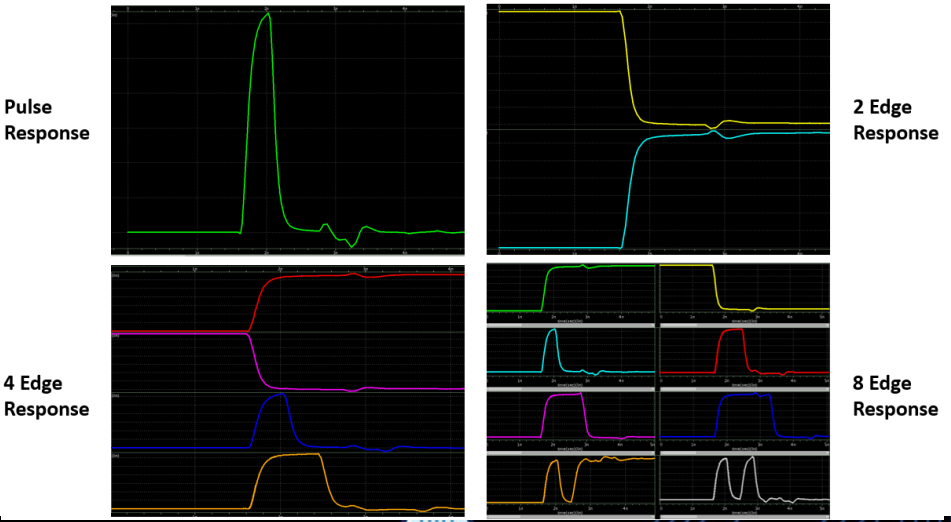
STATEYE standard pulse response does not capture these effects.

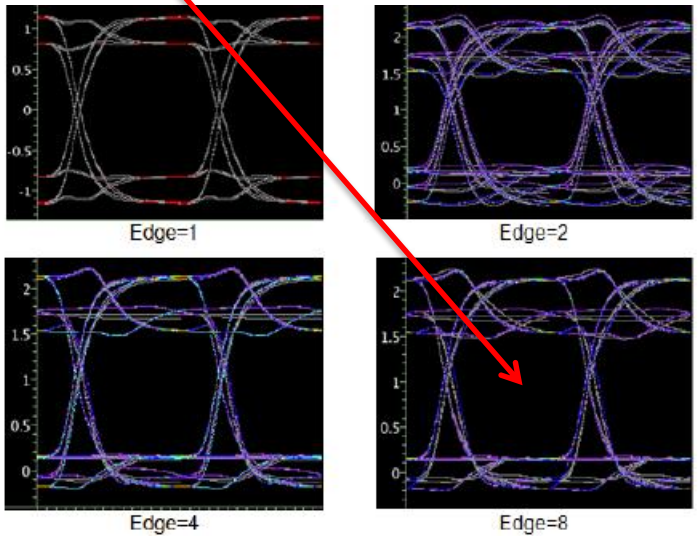
Multiple Edge Response

- One simulation must be run for each edge response. 8 edge= 8x runtime of pulse response.
- Responses can be saved to greatly shorten future runtimes.



- As edges are added, the STATEYE eyes begin to match more features with the SPICE response.

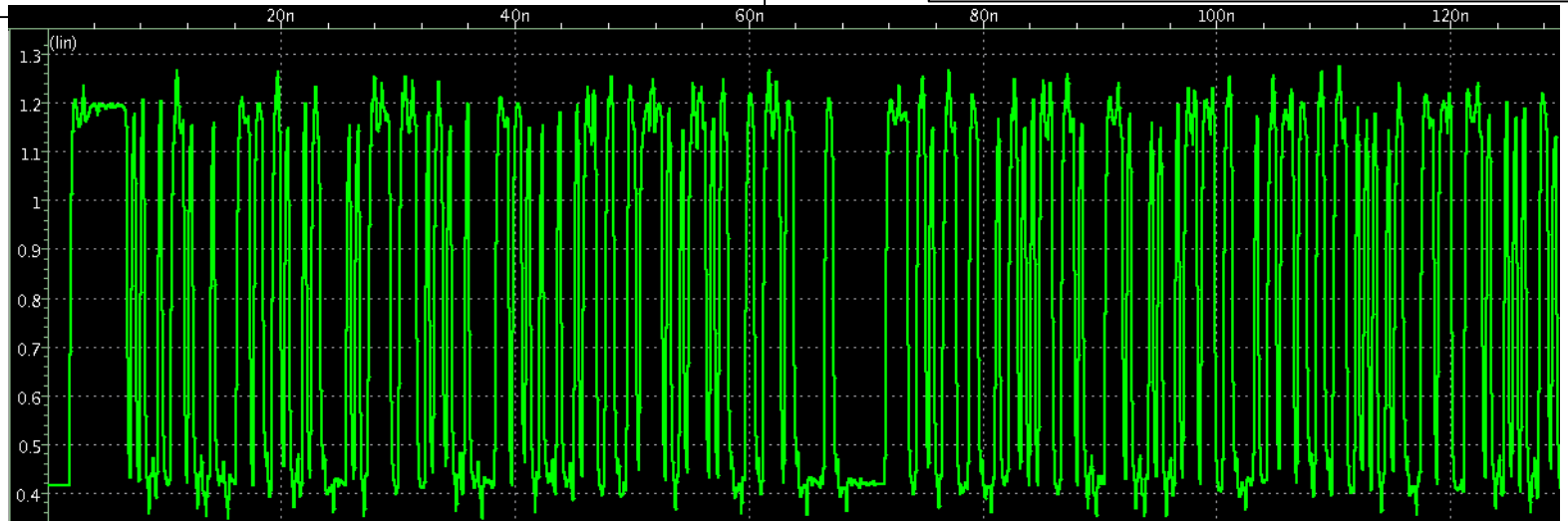




Full Transient Response

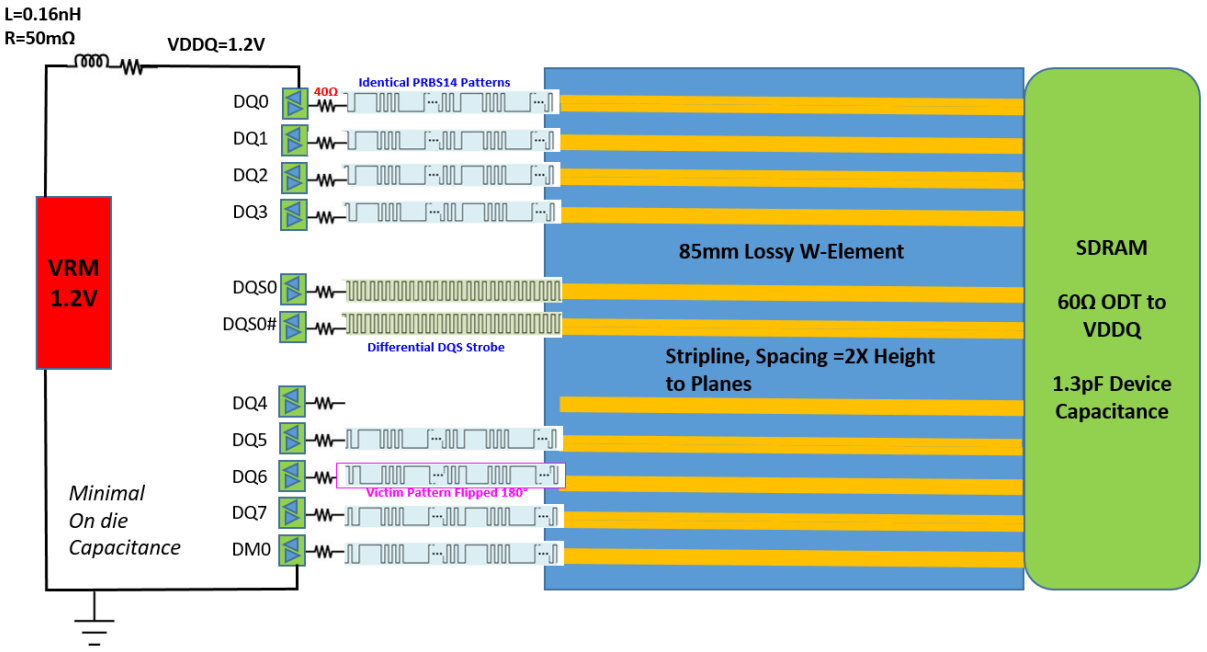
- Generates the probability density function based upon an arbitrary bit stream.
- Responses CANNOT be saved must rerun transient for each case.

- This should provide more accuracy
- Run this mode first to judge accuracy of potential solution. Then look at multi-edge mode for increased flexibility and speed.



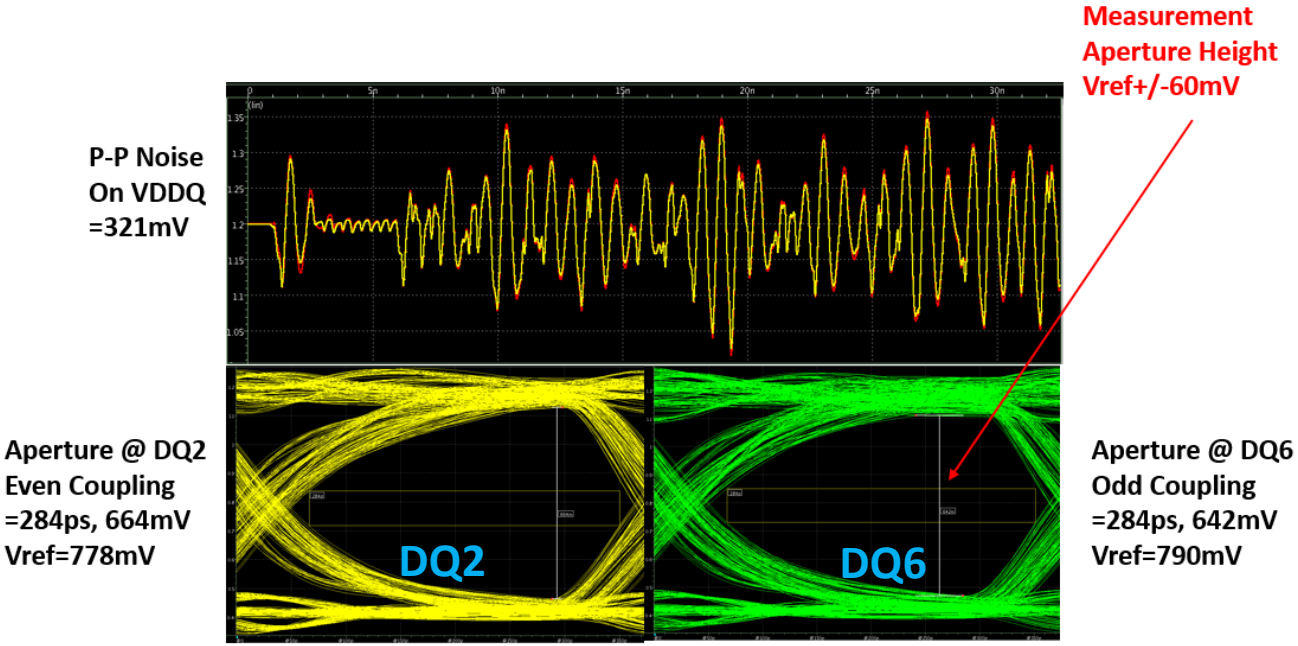
Simulation Environment

- Simulate a single byte lane during a Write operation.
-
- Identical PRBS patterns to excite SSO effects. Then flip one bit to excite Odd mode coupling on one of the bits. 2667Mbps
- Minimal Decoupling included.
- 85mm of 51Ω stripline
- 60Ω ODT to VDDQ



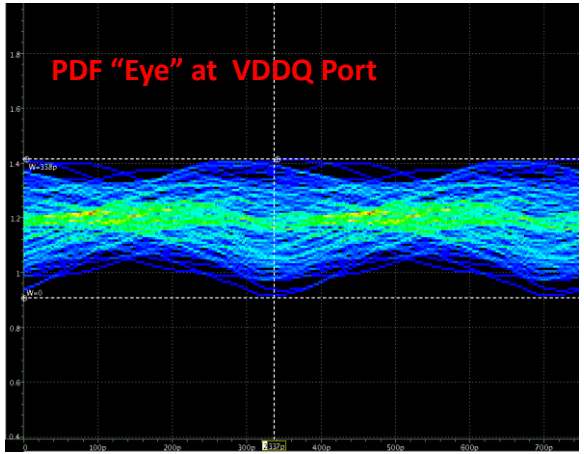
Initial SPICE Transient Results

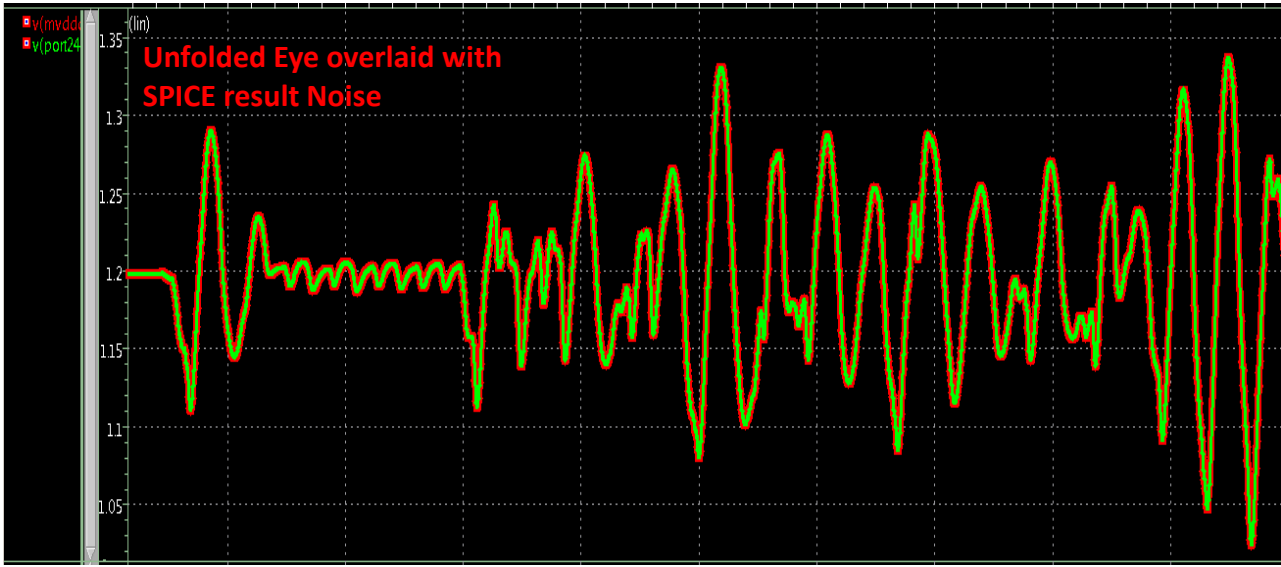
- Baseline for Comparison
  - Assumes the SPICE results are “correct”.
- Significant amount of Rail noise on VDDQ, +/-13%
- DQ2 ~ Even Mode Coupling
- DQ6 ~ Odd Mode Coupling.



Overlay of STATEYE(FT) Noise vs. SPICE

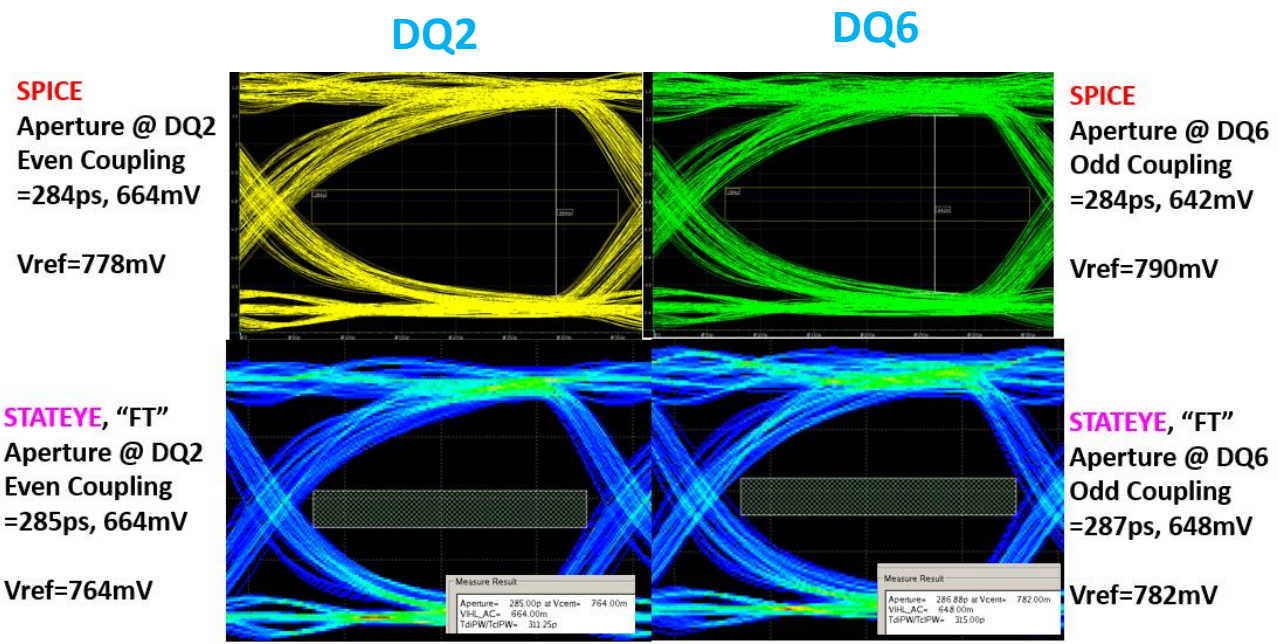
- As expected, the “Full Transient” Mode of STATEYE matches the SPICE results well in terms of capturing the Rail Noise.
- This is important to confirm since the rail noise will be the primary source of non-linearity.





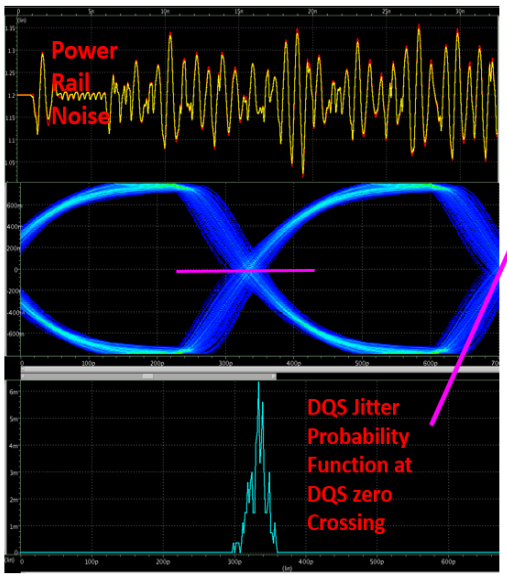
Comparing STATEYE(FT) Eyes to SPICE

- Overall Good Agreement in horizontal and vertical opening.
  - VREF somewhat shifted.
- Eyes are triggered by and ideal Unit Interval.
- DDR is source synchronous, so the Eyes triggered by the DQS must be compared.
  - Include DQS Jitter
  - Jitter tracking effects

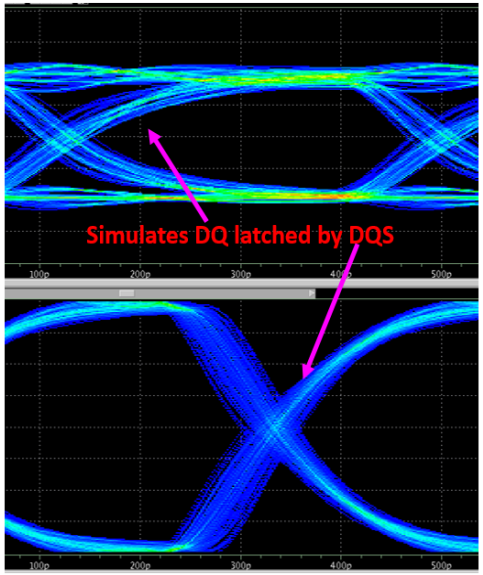


“Triggering” the DQ Eye in STATEYE

- There is no triggering capability, but a DQS jitter function can be applied to the received DQ signal.
- Drawback:
  - Two FT STATEYE simulations are now required.
    - 1 to generate the jitter function and 1 to simulate with the function applied.
- For Further Study:
  - Should this jitter function be applied to the stimulus or at the probe port?



time	probability
-2.362E-11	0.000E+00
-2.175E-11	0.000E+00
-1.987E-11	0.000E+00
-1.800E-11	1.116E-03
-1.612E-11	1.488E-03
-1.425E-11	1.116E-03
-1.237E-11	1.860E-03
-1.050E-11	2.604E-03
-8.624E-12	1.116E-03
-6.749E-12	1.116E-03
-4.874E-12	2.604E-03
-2.999E-12	2.976E-03
-1.124E-12	1.488E-03
2.513E-13	4.836E-03
2.626E-12	1.860E-03
4.501E-12	2.976E-03
6.376E-12	4.092E-03
8.251E-12	1.488E-03
1.013E-11	1.860E-03
1.200E-11	2.232E-03
1.388E-11	2.604E-03
1.575E-11	2.232E-03
1.763E-11	2.976E-03
1.950E-11	3.348E-03
2.138E-11	1.860E-03
2.325E-11	2.604E-03
2.513E-11	1.488E-03
2.700E-11	3.720E-04
2.888E-11	1.116E-03
3.075E-11	1.116E-03
3.263E-11	1.860E-03
3.450E-11	2.232E-03
3.638E-11	1.116E-03
3.825E-11	3.720E-04
4.013E-11	3.720E-04
4.200E-11	0.000E+00
4.388E-11	3.720E-04
4.575E-11	0.000E+00



Comparing STATEYE(FT) Triggered Eyes to SPICE

This is a reasonable Match.

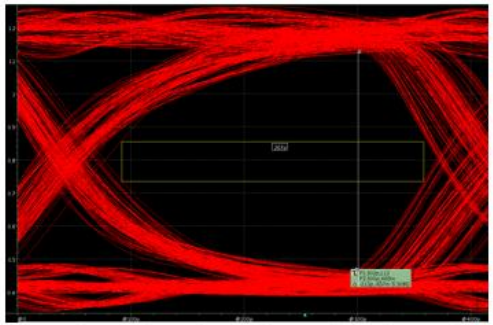
This is one data point.

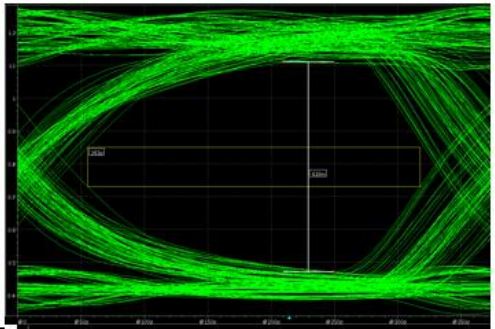
DQ2

DQ6

SPICE
Aperture @ DQ2
Even Coupling
=267ps, 657mV

Vref=795mV



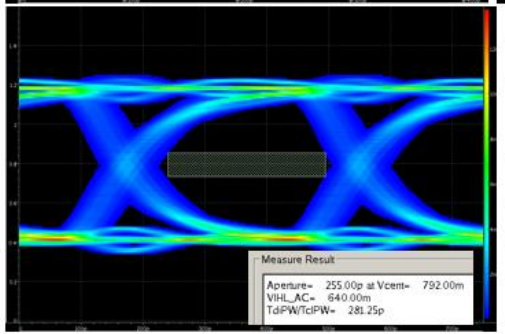


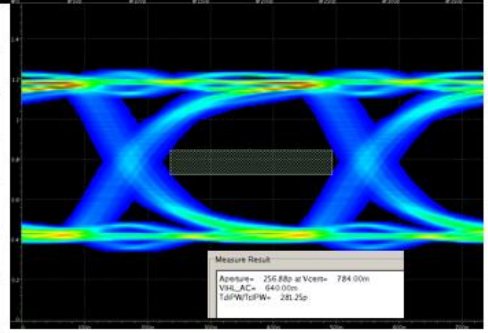
SPICE
Aperture @ DQ6
Odd Coupling
=263ps, 639mV

Vref=790mV

STATEYE, "FT"
Aperture @ DQ2
Even Coupling
=255ps, 640mV

Vref=792mV





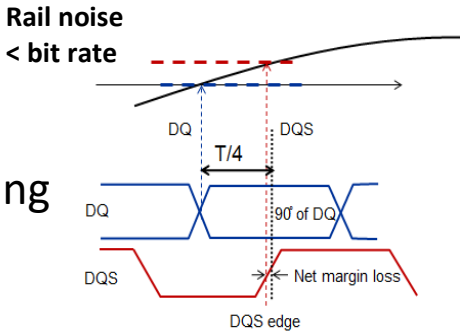
STATEYE, "FT"
Aperture @ DQ6
Odd Coupling
=257ps, 640mV

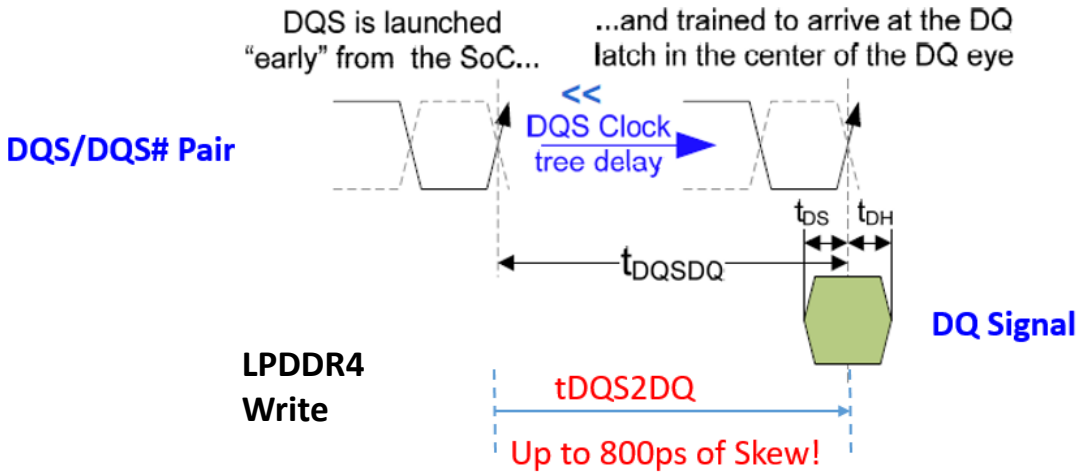
Vref=784mV

A Note on LPDDR4 Write Timing

- Timing closure of DDR interfaces benefits from PSIJ tracking between data and strobe.
- LPDDR4 Write signaling has 200ps to 800ps of skew between the DQ and DQS by design for power savings.
  - > 2UI skew at 3200Mbps
- This reduction of jitter tracking requires tightening the noise specs to control PSIJ effects in the budget

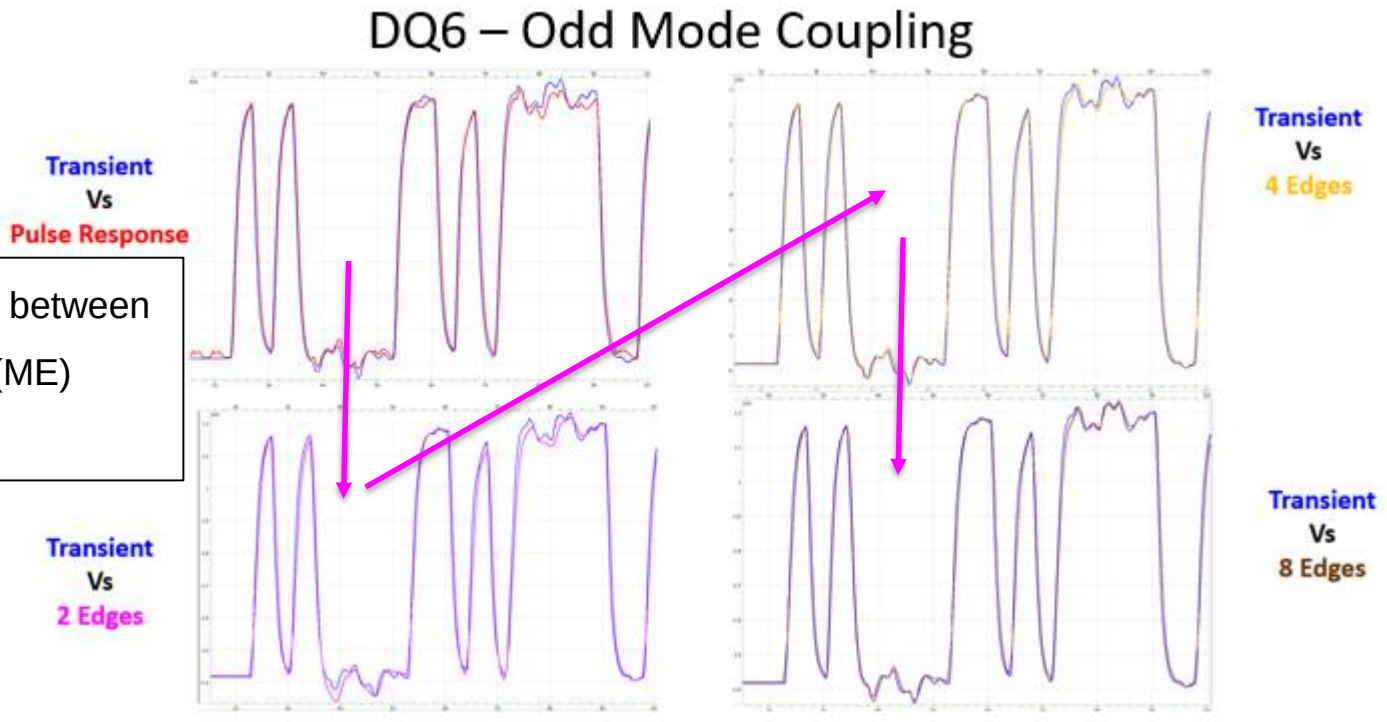
How PSIJ impacts Timing





Multi-Edge Mode – Data Stream Comparison

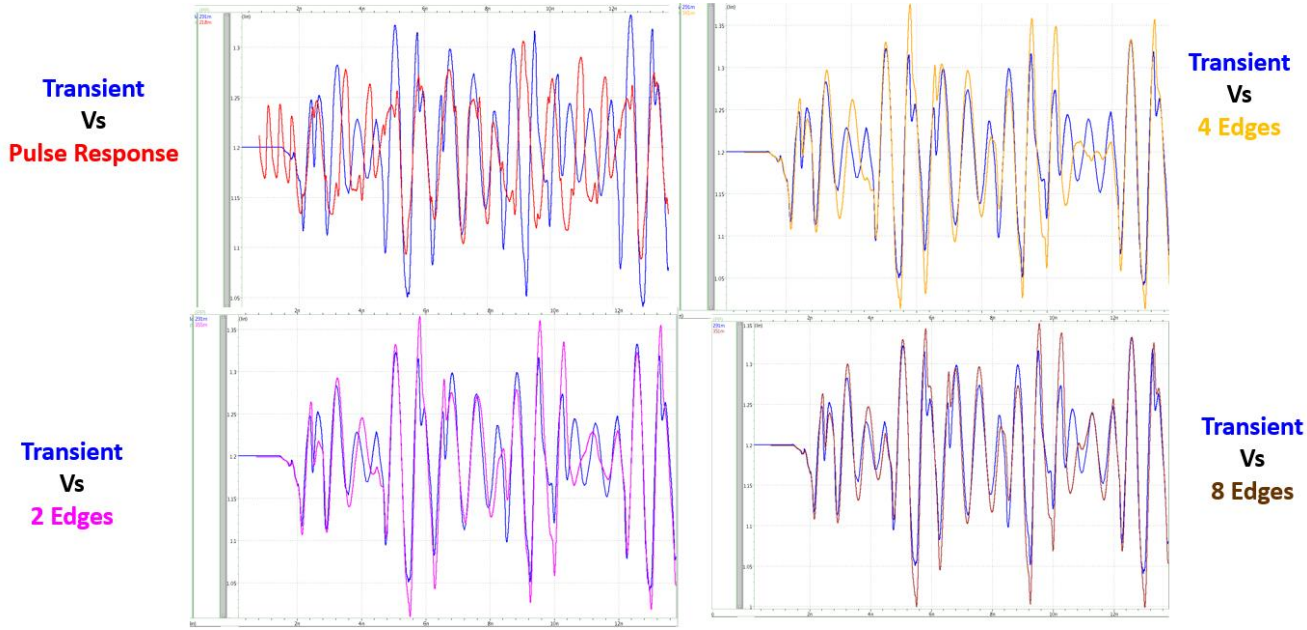
- Reasonable matching between the unfolded STATEYE (ME) result and the SPICE



Multi-Edge Mode – Power Rail Comparison

- Not a great match. With 8 edges the result is getting closer, but still exaggerates peaks.

- The Reusability of edge responses makes ME mode worth pursuing.



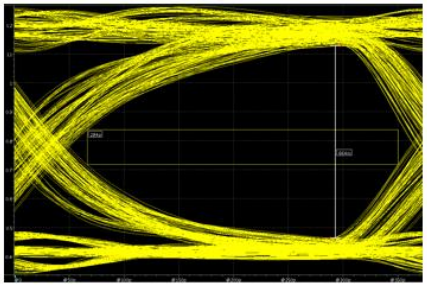
Comparing STATEYE(ME – 8 Edge) Eyes to SPICE

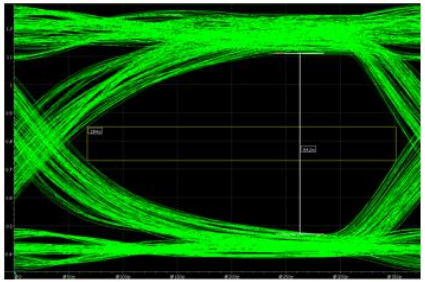
- **Big Miss.**
- STATEYE results seem to be missing the jitter effects from the power rail.
- DQ6 looks closer, but that reflects the odd mode crosstalk on the board more than PSIJ.

DQ2 DQ6

SPICE
Aperture @ DQ2
Even Coupling
=284ps, 664mV

Vref=778mV



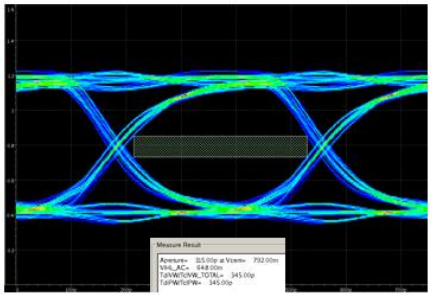


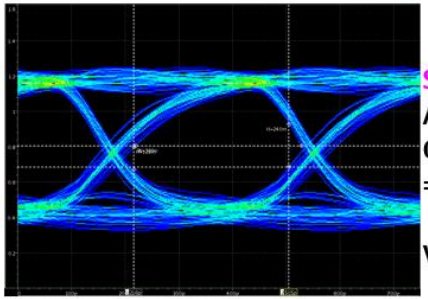
SPICE
Aperture @ DQ6
Odd Coupling
=284ps, 642mV

Vref=790mV

STATEYE, "ME8"
Aperture @ DQ2
Even Coupling
=315ps, 648mV

Vref=792mV





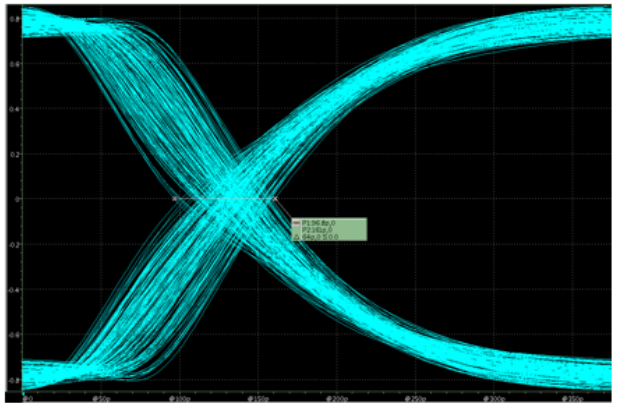
STATEYE, "ME8"
Aperture @ DQ6
Odd Coupling
=289ps, 670mV

Vref=742mV

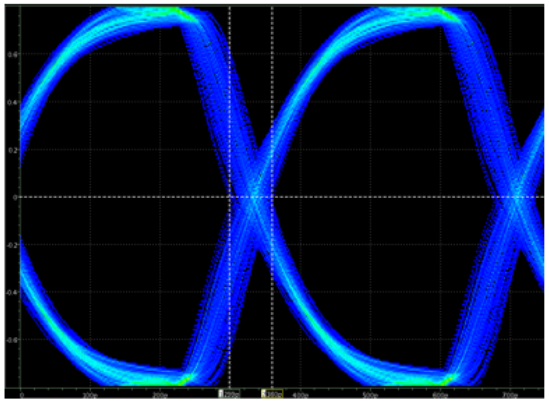
Multi-Edge Mode Misses the Time Shift Component

- Compare the differential DQS SPICE simulation to the Full Transient and Multi-Edge STATEYE Simulations
  - Eliminates any ISI effects and most of the Crosstalk.
- The superposition of edge responses does not capture the delay element of the non-linear response.
- Jitter must be added.

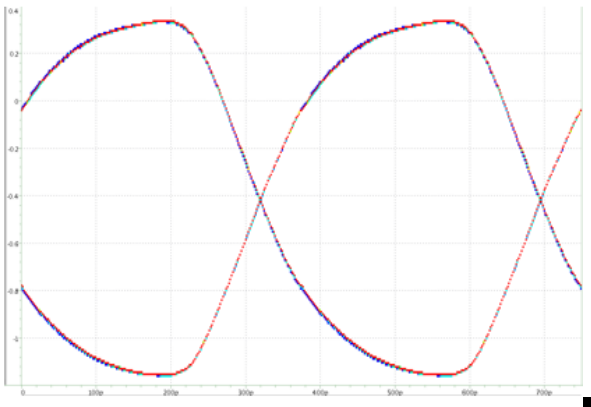
DQS jitter for SPICE=64ps



for STATEYE "FT" =61ps

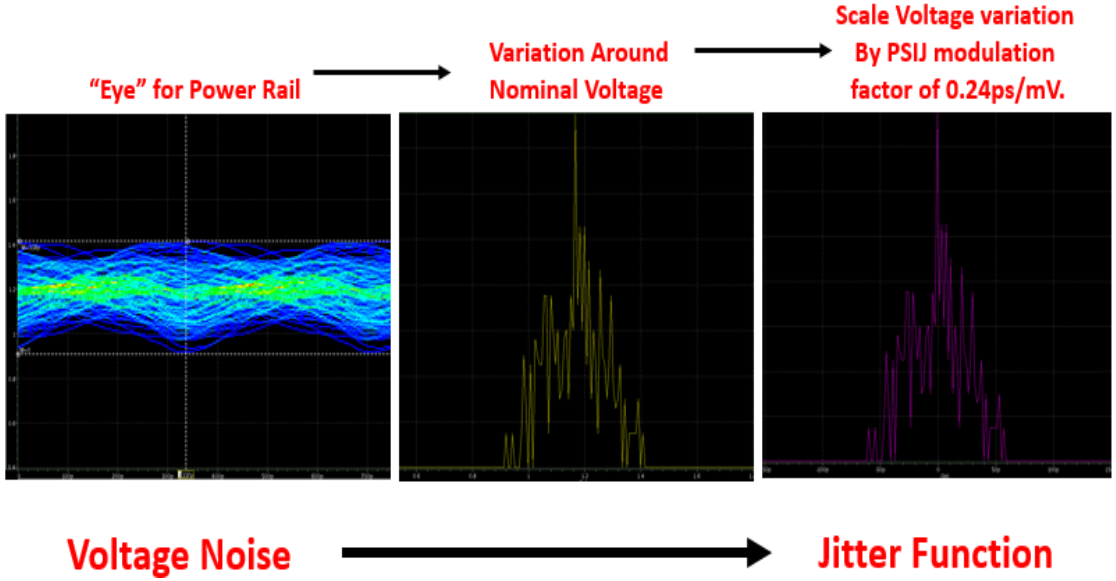


for STATEYE "ME" =~0ps



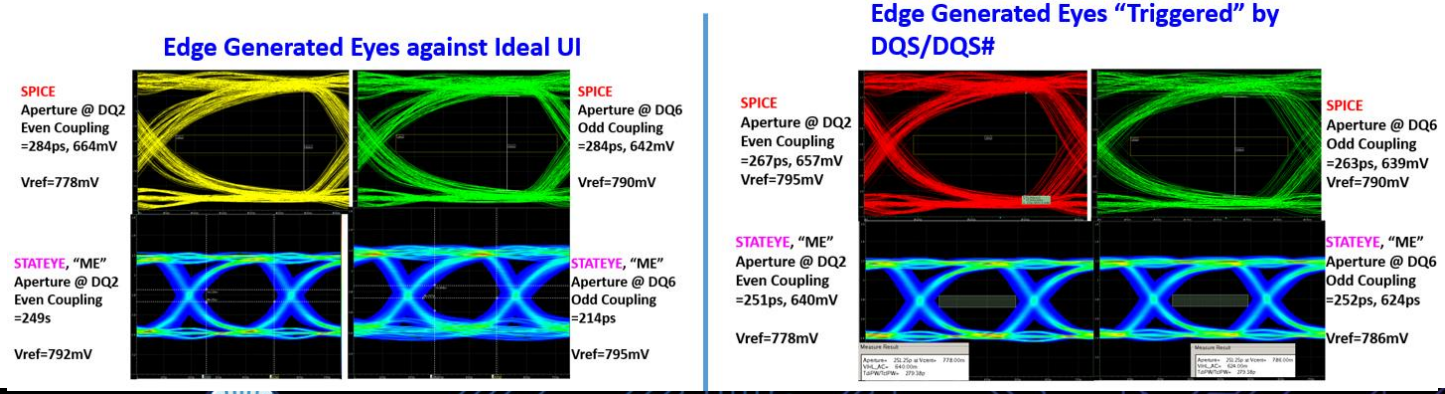
Capturing the Jitter from the Power Supply for ME8

- Similar to generating the DQS jitter function.
  - Cross-section through the power rail response
  - Create a PDF of the voltage noise around nominal.
  - Convert to jitter with ps/mV modulation factor
- Drawback:
  - Additional ME STATEYE simulations are now required.
- For Further Study:
  - Selection of Cross-Section
  - Should this jitter function be applied to the stimulus or at the probe port?



ME-8 Edge with Jitter

- STATEYE Results show significantly more closure than transient against ideal UI.
  - Indicates poor capture of supply noise, wrong cross-section point selected, or a combination of both
- Results are closer when the DQS “trigger” is applied.
- The potential benefit of reusing the edge responses of the Multi-Edge method makes this method worth pursuing despite the current less than impressive results.
  - Capturing the supply noise from a full transient method than applying to ME is worth exploring.
  - This will be the subject of a future paper.

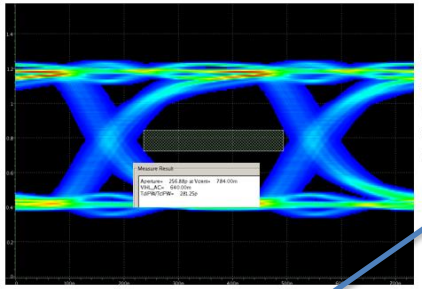


STATEYE Results into the Write Timing Budget

PHY and SDRAM timing contributions for DDR4 Write operation at 2667Mbps			
Skew and Jitter Components		Description	Worst Case Uncertainty Contributions (ps)
	Parameter Name		
PHY Transmit Contributions	PLL Clock Source Jitter	18ps of Jitter from the PLL at BER=1E-16. This is mostly RJ. RMS Jitter =1.095ps-RMS. Treat as Random Jitter.	18
	PowerSupply Induced Jitter	PSIJ from noise on the core power rail. Noise is predominantly at package resonance of 200MHz. Treat as Periodic Jitter.	52
	I/O Rise/Fall Skew	Duty Cycle Distortion that closes the pulse width. Treat the 12 ps as ~1.6% duty cycle distorion at 2667Mbps.	12
	Training Errors	Delay Line Granularity, Step size non-linearity effects and VT drift impact on timing. For simplicity, treat as a static contributor to total uncertainty	30
		Total Transmitter (PHY) Uncertainty	112
SDRAM Receive Contributions	Input Eye Mask	SDRAM Receiver Window Requirements - 0.22UI at 2667Mbps	82
		Total Contributions for End to End Timing	194
		Total Available Window at 2667Mbps	375

Known Quantities:

- **PHY Budget**
- **DRAM Mask Requirement**



STATEYE, "FT"
Aperture @ DQ6
Odd Coupling
=257ps
Vref=784mV

Interconnect XT, ISI, SSO

An aperture of 257ps corresponds to a timing uncertainty of 375ps-257ps=118ps

Strictly linear summation
PHY + DRAM +Channel=
112ps + 82ps+118ps=312ps
Margin=375ps-312ps=63ps

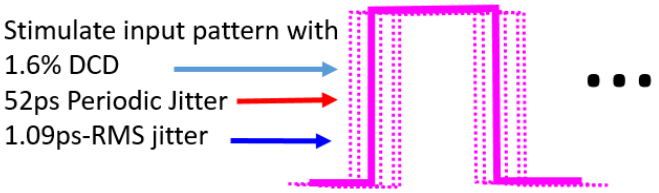
Using STATEYE to Remove Pessimism

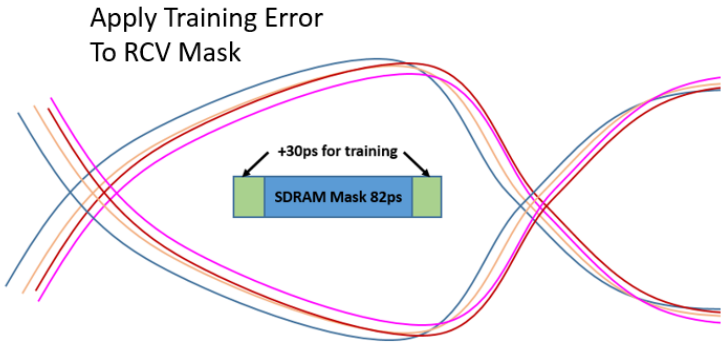
At the input stimulus, Apply jitter functions

- **1.6% Duty Cycle Distortion**
- **52ps Periodic Jitter (200MHz)**
- **1.095ps-rms Random Jitter**

For the Receive mask

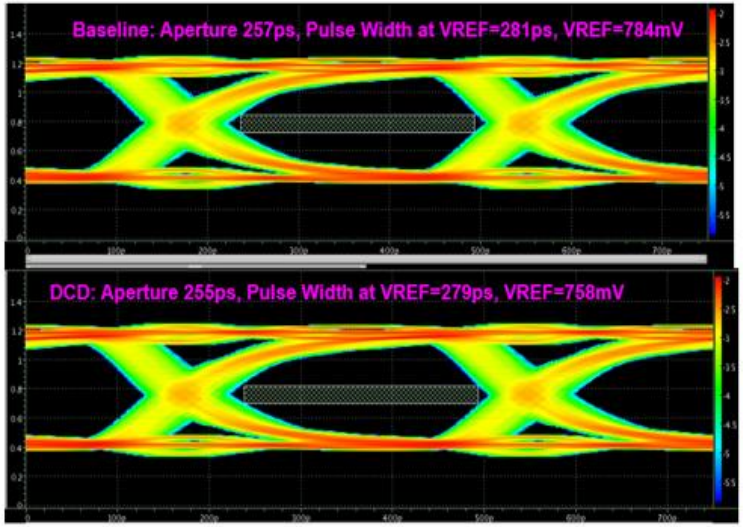
- **DRAM requirement of 82ps**
- **Add the static training error to this window.**
- **Total requirement of 112ps**





Including Duty Cycle Distortion

- DDR4/LPDDR4 interfaces train to the optimum VREF placement.
- Although DCD adds 12ps of uncertainty at the same VREF level, the training will find the widest part of the eye, reducing the effective uncertainty to only 2ps.

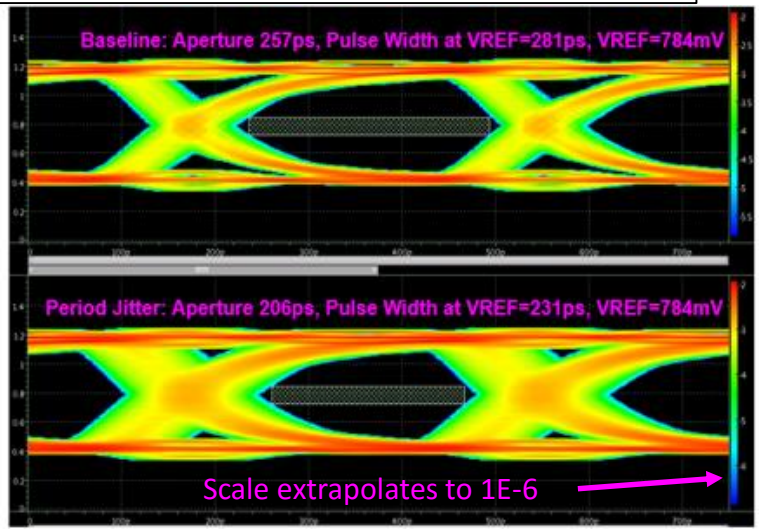


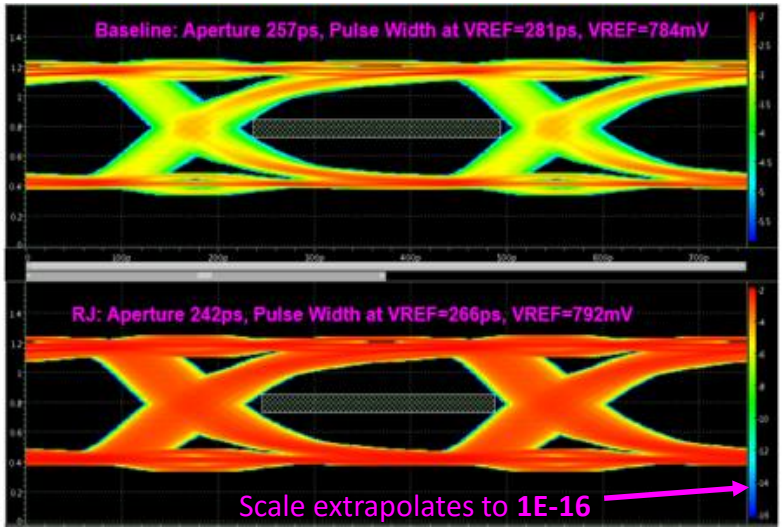
Measured
At Same VREF Level:
12ps reduction

Including Period Jitter and Random Jitter

- The Periodic Jitter reduces the eye by about 51ps.
- Fairly linear impact on result with no shift in ideal VREF.

- Applying RMS jitter of 1.095ps-rms reduces eye by 15ps.
- 1.095 x16.444 (Q-factor) =18ps
- Difference is shift in ideal VREF

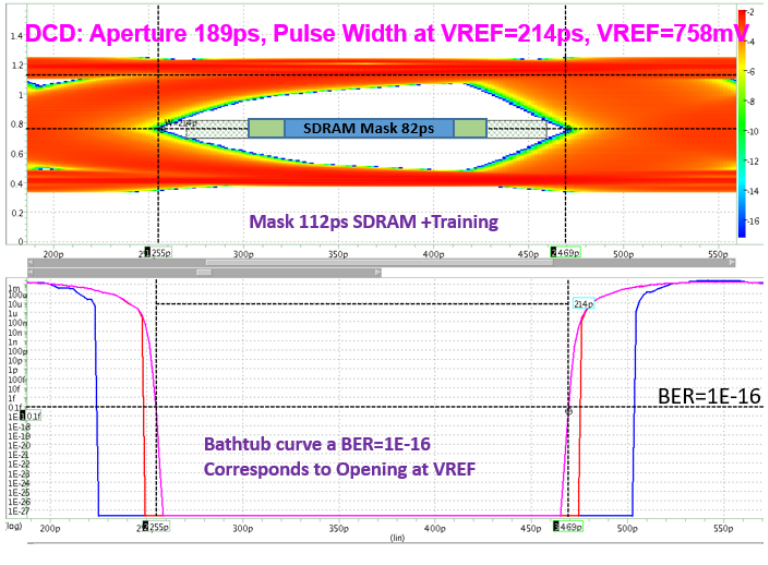




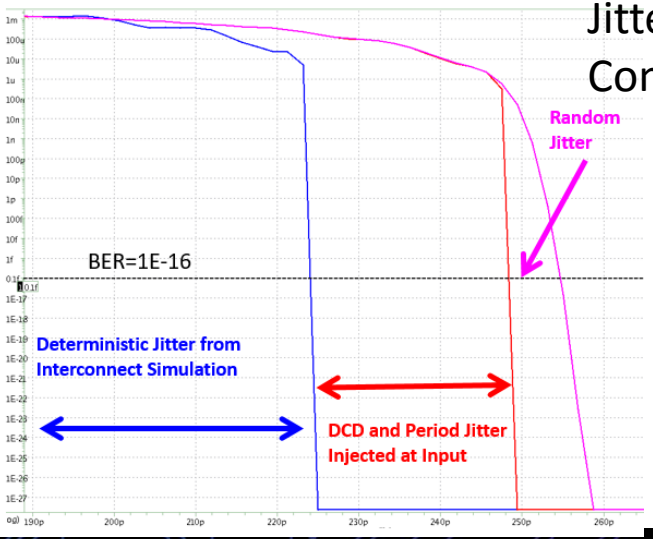
Combine All Input Jitter Sources with Channel Sim

- Total performance margin of interface =189ps-112ps mask = 77ps
- 14ps of pessimism was removed from the linear budget with this method, 3.7% of a UI
- Fairly linear impact on result with no shift in ideal VREF.

Eye plus Bathtub



Jitter Contributions



In Summary

Comparing StatEye Results with Standard HSPICE® Transient Results			
StatEye Mode	**Pros**	**Cons**	**Path Forward**
STATEYE (Full Transient)	Good Match to Transient for Eye and Power Rail	Long Initial Transient No Save and Reload Capabiliites	Expand to Read Operations. More Complex Interfaces (Multi-DIMM)
		Need 2 simulations. 1st to determine DQS jitter Function	
STATEYE (Multi-Edge Mode)	Reasonable Match to Eye Amplitude.	Poor Match to Supply Noise and Jitter.	Refinement of Jitter Function Application. Explore Combining Full Transient Mode with Edge Mode.
	Flexible. Reloading edge responses allows for quick simulation.	Only vertical superposition of Edges	
Topics for Further Exploration			
Applying jitter functions for Budget Purposes	Location of Application Port: Input, Load or Intermediate port after the level shifter but bere the channel?		
	Creating Rail Noise plots in FT mode to be included with ME mode.		
	Selecting Time Slice Location for Voltage Noise Curve.		
	Edge Mode: When combining PSIJ and DQS Jitter functions, are some of the effects being double counted?		
	Is Periodic Jitter the best representation of the PHY power supply induced jitter function?		
Other Interfaces	Read Operations. Accuracy for non Point to Point Applications		
Jitter Amplification	When must if be Considered for DDR and how should it be implemented?		
StatEye Functionality	Limited save and Reload of Full Transient Mode Response. Greater than 8 edges. Jitter Amplification		

Thank you!

QUESTIONS?